2021

Sistema de procesado independiente de audio

Trabajo de Fin de Grado. Universidad de La Laguna

Grado en Ingeniería Electrónica Industrial y Automática

Autor:

José Antonio Montañez Pérez

Tutor:

Francisco Javier Llopis Cánovas

ÍNDICE

1. Agradecimientos.

Alcanzar la finalización de mis estudios como Ingeniero Técnico Industrial no hubiera sido posible sin el apoyo y la ayuda de varias personas. Por ello, doy gracias:

A mi mujer Alba por estar presente en las largas noches de estudios, siempre ayudándome en lo que necesitara y brindándome la tranquilidad que precisaba en los momentos más difíciles.

A mi madre Taty y mi abuela Teresa, las cuales me han permitido hacer realidad este sueño de llegar a ser ingeniero.

A mis suegros, Jesica y Fran, los cuales siempre han estado ahí para lo que necesitara, brindándome consejos y ayuda en cualquier cosa.

A mi grupo de amigos, Miguel, Isaac, Guillermo, Asbel, Alex, Alexis…, por esas largas tardes de estudio en las que afianzábamos conceptos en grupo y nos apoyábamos unos a otros.

A mi tutor de TFG, Francisco Javier Llopis Cánovas, por siempre estar disponible para cualquier consulta y ayudarme en todo momento a encaminar el trabajo.

A Delfín Darias, del Personal de Administración y Servicios del Departamento de Ingeniería Industrial, por facilitarme los medios necesarios para hacer el trabajo y siempre estar disponible para lo que necesitara.

Y por último y no menos importante, a todos los profesores que, de una manera u otra, me han enseñado todo lo necesario para finalizar mis estudios.

2. Abstract – Resumen.

This work deals with the implementation of an audio equalizer as the core block of a system with additional features. These include the signal power amplification by means of an output stage, the division of the signal produced by a microphone or a phantom power supply. On the other hand, the system includes a block devised to ensure the compliance with hearing regulations (within the framework of application of the European Union). Finally, it should be noted that the design relies exclusively on analog functional blocks.

En este trabajo se trata la implementación de un ecualizador de audio como bloque central de un sistema con características adicionales. Estas incluyen la amplificación de potencia de la señal mediante una etapa de salida, la división de la señal producida por un micrófono o una fuente de alimentación *phantom*. Por otro lado, el sistema incluye un bloque concebido para asegurar el cumplimiento de la normativa auditiva (en el marco de aplicación de la Unión Europea). Por último, cabe señalar que el diseño se basa exclusivamente en bloques funcionales analógicos.

3. Keywords – Palabras clave.

Ecualizador – Equalizer;Filtros analógicos – Analog Filters;Conectores - Plugs;Micrófono – Microphone;Butterworth response- respuesta de tipo Butterworth.

4. Introducción.

El prototipo que se detalla en el presente trabajo de fin de grado se fundamenta en un sistema que capta una señal de audio proveniente de un micrófono para procesarla mediante una etapa de amplificación desbalanceada y una etapa de ecualización.

Por otra parte, también se conecta una segunda entrada de audio, la cual, tras ser desbalanceada, se suma con la señal proveniente de la etapa de ecualización. La señal obtenida se transfiere a una etapa de potencia para su transmisión a unos auriculares.

Además de lo especificado anteriormente, el sistema incluirá (figura 1.1):

- Un circuito de conexión *phantom* para poder conectar tanto micrófonos dinámicos como de condensador, y así aumentar la versatilidad del sistema. Además, este circuito permite la alimentación del micrófono sin perturbar otros bloques con la corriente DC.
- Un divisor de audio para aprovechar una "imagen" original del audio del micrófono, por si es necesario procesarla de forma externa para otras utilidades.
- Una fuente de alimentación para suministrar la energía al *phantom* y a la alimentación de todos los circuitos del dispositivo.
- Un circuito que controlará el nivel pico de salida y dejará la carga e circuito abierto para proteger al usuario de niveles sonoros dañinos, en cumplimiento de la normativa europea actual.

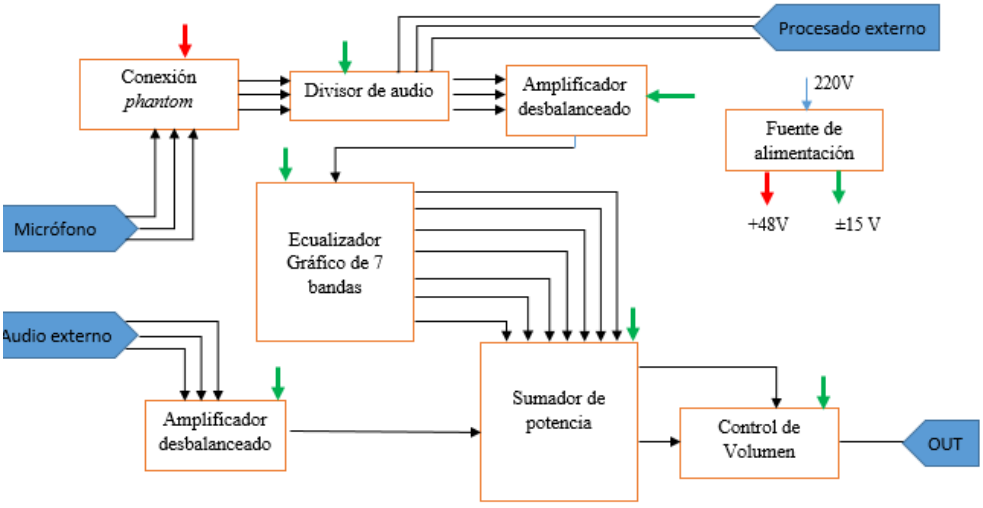


Figura 1.1: Esquema genérico del sistema de procesado independiente de audio [28].

5. Revisión de aspectos básicos.

Una vez introducido el esquema genérico del sistema y antes de analizar cada uno de los bloques funcionales que lo componen, es preciso revisar conceptos relacionados con la base teórica del presente documento. Se abordarán conceptos relacionados con el procesamiento de señales y la acústica.

5.1 Procesamiento de señales.

5.1.1 Filtros.

Los filtros son circuitos que permiten realizar cribados de señales en función de la banda de frecuencia en la que permiten la transmisión de señal. Atendiendo a los componentes del diseño, se clasifican en:

- **Filtros pasivos:** implementados con resistencias, inductores y condensadores (figura 1.2). No precisan de alimentación. No permiten la amplificación de la señal de entrada [1].

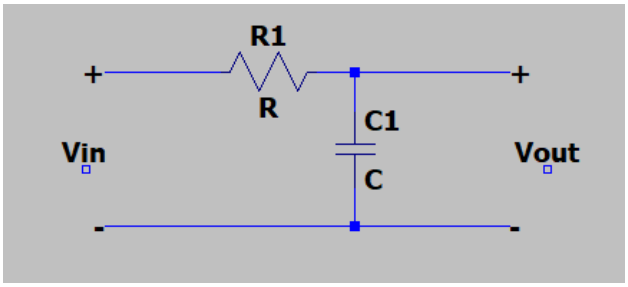


Figura 1.2: Filtro pasivo pasa-alta [28].

- **Filtros activos:** basados en la combinación de elementos pasivos y amplificadores operacionales (en su momento transistores). Se evita el uso de inductores por sus grandes dimensiones, altos costes y su resistencia parásita. Precisan de una etapa de alimentación y permiten la amplificación de señales [1].

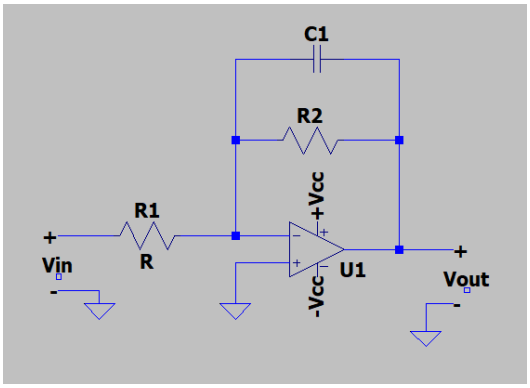


Figura 1.3: Filtro activo pasa-bajas [28].

Además de la clasificación anterior, cabe destacar que los filtros se caracterizan por los siguientes parámetros [3] [1]:

- **Frecuencia de corte:** a la frecuencia de corte a 3 dB, la ganancia del sistema es 3 dB inferior al valor máximo. Este hecho puede variar en función del orden del filtro, como en el caso de los filtros de 4º orden en los que en la frecuencia de corte la atenuación es de 6 dB.
- **Banda de paso:** intervalo de frecuencias, captadas por el filtro, acotado por la frecuencia de corte, en el caso de los filtros pasa-bajas y el filtro pasa-altas. En el caso del filtro pasa-banda, el intervalo estará comprendido entre dos frecuencias de corte.
- **Banda atenuada:** intervalo de frecuencias, rechazadas por el filtro, acotado de manera complementaria al intervalo de frecuencias de la banda de paso.
- **Orden del filtro:** es el grado del polinomio del denominador de la función de transferencia. Determina la pendiente de la curva de respuesta en la zona de transición entre las bandas de paso y atenuada.
- **Factor de calidad (Q):** En los filtros pasa-banda, es el cociente entre la frecuencia resonante y el ancho de banda. Es una medida de la selectividad del filtro. Un valor elevado de Q indica que el filtro selecciona una banda de frecuencias más reducidas, es decir, el filtro es más selectivo.

Atendiendo a la función que desempeña el filtro, también podemos clasificarlos en:

- **Pasa-bajas:** permite el paso de frecuencias inferiores a la frecuencia de corte del filtro.
- **Pasa -altas:** permite el paso de frecuencias superiores a la frecuencia de corte del filtro.
- **Pasa-banda:** permite el paso de la banda de frecuencias comprendidas entre una frecuencia superior y otra inferior, situadas en torno a la frecuencia de resonancia del circuito.
- **Rechazo de banda:** anula el paso de la banda de frecuencias comprendidas entre una frecuencia superior y otra inferior, situadas en torno a la frecuencia de resonancia del circuito.
- **Pasa-todo:** permite el paso de todas las frecuencias, pero modifica la fase de la señal.

Teniendo en cuenta el método de aproximación a la respuesta al modelo ideal, existen diversas variantes entre las que se destacan:

- **Filtro Butterworth:** permite la obtención de una respuesta plana en la banda pasante. Es muy utilizado en los filtros *anti-aliasing* y en aplicaciones de conversión de datos para conseguir una buena precisión de medida en la banda de paso. Cabe destacar que mientras más alto sea el orden del filtro, más pronunciada será la pendiente de atenuación situada en la frecuencia de corte, por lo tanto, la función del filtro se asemejará más al comportamiento de un filtro ideal. En la figura 1.4 se muestra el comportamiento del filtro, en función del orden del mismo [9].

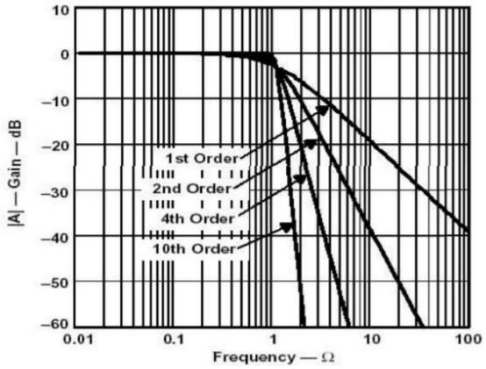


Figura 1.4: Curva de respuesta del filtro Butterworth para varios órdenes [9].

- **Filtro Tschebyscheff:** permite obtener una pendiente más pronunciada que en el caso del Butterworth en la región de transición. En contraposición, su respuesta en la banda de pasante no es plana, sino que se presenta rizados a razón de la siguiente fórmula.

$$N\ de\ rizados = n/2;$$ Siendo n el orden del filtro.

De la fórmula anterior se puede deducir que el orden del filtro es directamente proporcional al número de rizados y al incremento de la pendiente de atenuación, es decir que, mientras más alto sea el orden del filtro, más pronunciada será la pendiente de atenuación, pero a su vez aumentará el rizado en la banda pasante.
Su utilización se restringe únicamente a aquellos casos en el que el contenido de frecuencias es más importante que la magnitud. En la figura 1.5 se muestra el comportamiento del filtro, en función del orden del mismo [9].

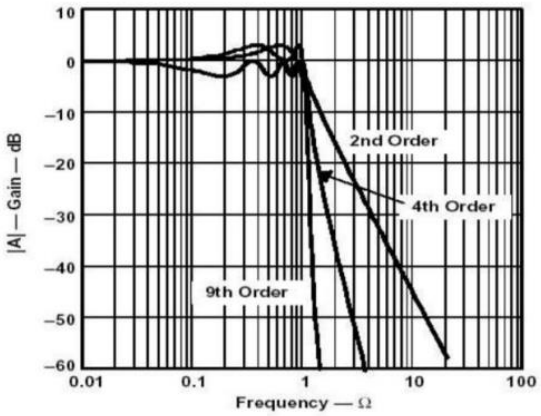


Figura 1.5: Curva de respuesta del filtro Tschebyscheff para varios órdenes [9].

- **Filtro Bessel:** posee la pendiente de atenuación menos pronunciada en la región de transición (figura 1.6). Ofrece una respuesta plana en la banda pasante. Tiene una respuesta lineal con respecto a la fase, lo cual resulta en un retardo constante en todo el ancho de banda deseado [9].

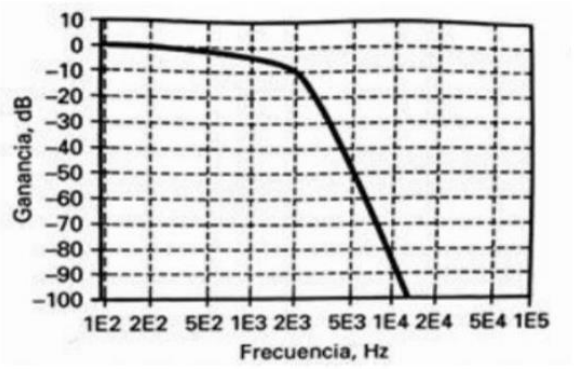


Figura 1.6: Curva de respuesta del filtro Bessel para varios órdenes [9].

Por otra parte, y atendiendo al orden del filtro, podemos diseñar filtros de primer orden (figura 1.7) y de segundo orden (figura 1.8). Para diseñar filtros de orden superior, solo es necesario combinar filtros de primer y segundo orden en cascada (figura 1.9) [30].

En cuanto a la tipología de diseño, cabe destacar la estructura Sallen-Key (figura 1.10). Dicha estructura es muy usada en la construcción de filtros debido a su excelente rendimiento. Es fácil de implementar y se puede variar fácilmente el valor de Q al cambiar la ganancia del sistema o la selección de componentes en la etapa de diseño [8].

Además de esta estructura, también existen otras como, por ejemplo: Cauer, Variable de estado, Biquad, Twin-Tee, Viena y Fliege [8].

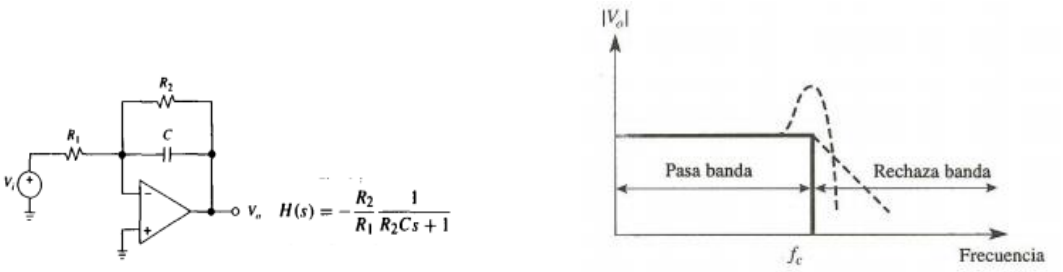


Figura 1.7: Filtro pasa-baja de 1º orden [22]

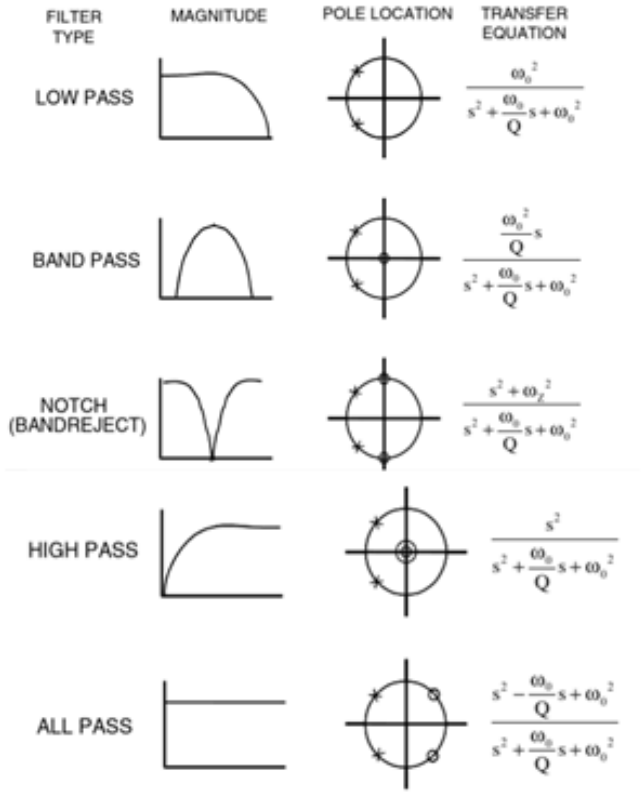


Figura 1.8: Funciones de transferencia de filtros de 2º orden [6]

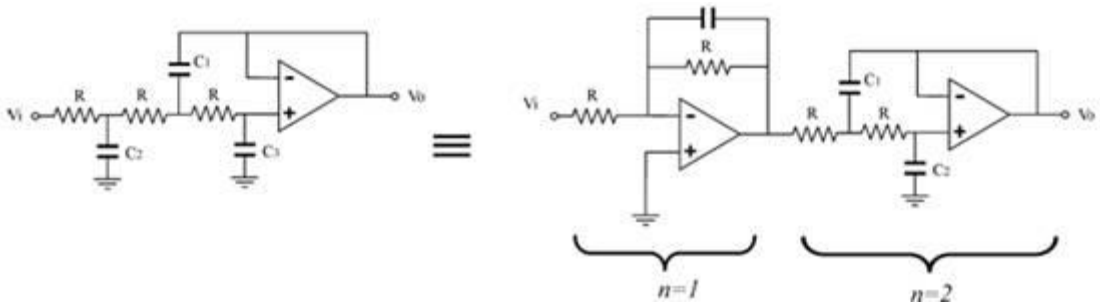


Figura 1.9: Ejemplo de implementación de un filtro de orden 3 [31].

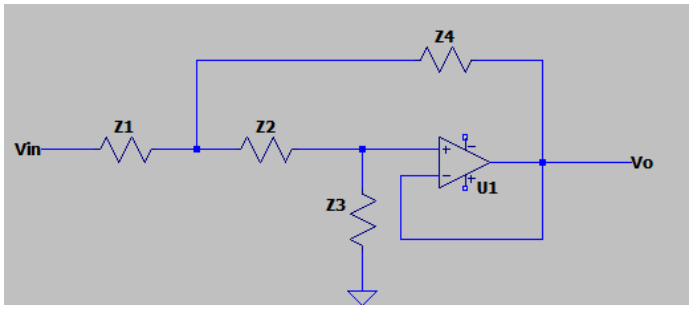


Figura 1.10: Estructura genérica de la tipología Sallen-Key para filtros de 2º orden [28].

El desarrollo matemático para obtener la función de transferencia genérica del sistema Sallen-Key, se recoge en el Anexo I. A partir de dicho desarrollo, se obtiene la función de transferencia que se muestra a continuación:

$$\frac{\text{Vout}}{Vin} = \frac{Z_3 * Z_4}{Z_1 * (Z_2 + Z_4) + Z_4 * (Z_3 + Z_2)}$$

Una vez obtenida la función de transferencia, se puede obtener fácilmente un filtro pasa-bajas o pasa-altas. Solo es necesario variar el tipo del componente de la impedancia como se muestra a continuación:

- Filtro Pasa-baja: Z1= R1 ; Z2= R2 ; Z3= 1/jwC2 ; Z4= 1/jwC1 [22].

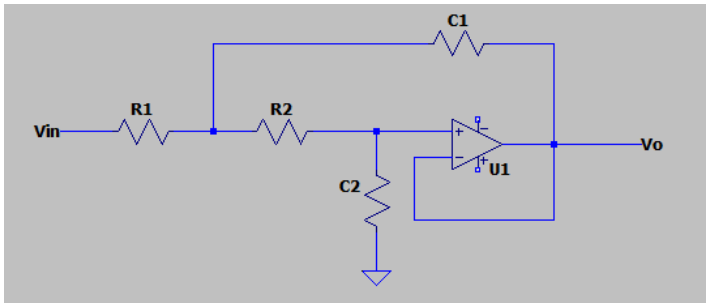


Figura 1.11: Estructura Sallen-Key filtro pasa-baja [28].

- Filtro Pasa-alta: Z1= 1/jwC1 ; Z2= 1/jwC2 ; Z3= R2 ; Z4= R1. [22].

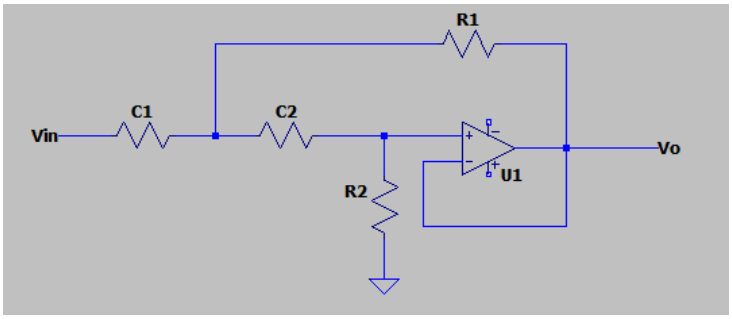


Figura 1.12: Estructura Sallen-Key filtro pasa-alta [28].

5.1.2 Ecualizadores.

La ecualización es un recurso de gran utilidad en el campo del procesamiento del audio ya que permite solventar la falta de respuesta plana de los equipos, potenciando o atenuando ciertas frecuencias.

- **El Ecualizador Gráfico:** es el más frecuente que podemos encontrar en el mercado. Podemos encontrarlo tanto el formato de *faders* deslizantes (figura 1.13), mediante el cual podemos ver y dibujar la curva de ecualización, como el modelo de perillas rotativas (figura 1.14) [10].

Figura 1.13: Ecualizador gráfico con *faders* deslizantes [32].

Figura 1.14: Ecualizador gráfico con perillas rotativas [33].

Ambos modelos tienen el mismo funcionamiento. El control de cada mecanismo afecta a diferentes frecuencias, llamadas "bandas". Cuantas más bandas tenga un ecualizador gráfico, más preciso será, ya que se podrá actuar sobre más frecuencias de manera específica [10].

- **El Ecualizador Semi-Paramétrico:** es más versátil que el ecualizador gráfico, puesto que, en lugar de un solo control por banda, dispone de dos. Uno selecciona la frecuencia a modificar y el otro modifica el volumen de la banda seleccionada (figura 1.15) [10].

Figura 1.15: Ecualizador semi-paramétrico [34]

- **El Ecualizador Paramétrico:** funciona de la misma forma que un semi-paramétrico, con la mejora de que contiene un control más llamado "Q" o factor de calidad. Este nuevo control permite ajustar el rango de frecuencias que contiene la banda, permitiendo así ser más o menos selectivo a la hora del procesado de audio [10].

A continuación, se detalla un ejemplo del funcionamiento:

Supongamos que seleccionamos la frecuencia de 100 Hz, y decidimos atenuarla. En un ecualizador semi-paramétrico, resultará afectada no solo la frecuencia exacta de 100 Hz, sino las adyacentes, como los 90 o 110 Hz. Pero en el caso de un ecualizador paramétrico, podemos controlar el factor "Q" para que solo sea afectada la frecuencia de 100 Hz [10].

5.1.3 Etapas de salida.

Partiendo de que existen diferentes clases de etapas de salida, vamos a focalizar en la explicación de las etapas en clase A, B y AB.

- **Clase A.**

Se polariza un único transistor en la zona de respuesta lineal. Además, tiene capacidad de responder a señales de cualquier polaridad. Funciona como un amplificador lineal convencional, pero disipa gran cantidad de potencia incluso cuando la señal de entrada es nula. [37]

Aunque esta clase de amplificadores de potencia son reemplazados por mejores diseños, dado su bajo rendimiento, son populares en el ámbito de la electrónica básica orientada al uso no profesional (figura 1.16) (figura 1.17) [38].

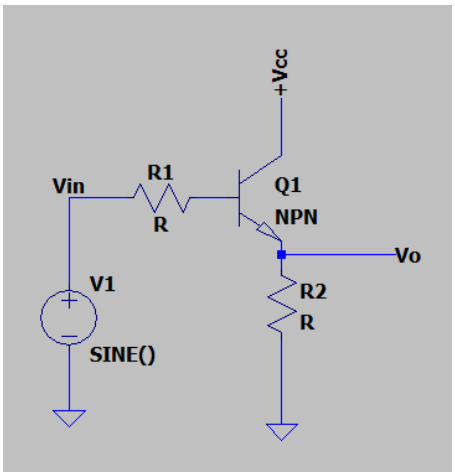


Figura 1.16: Etapa de salida clase A [28].

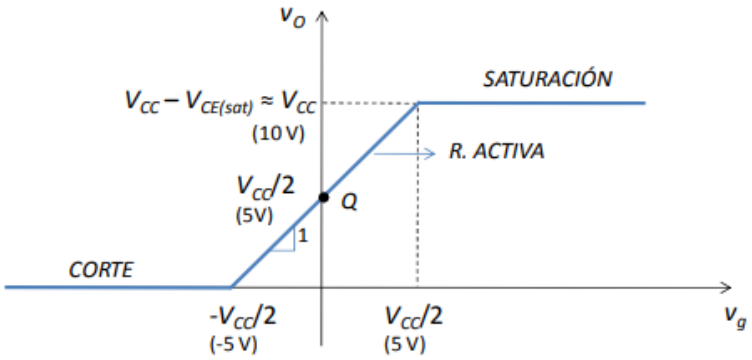


Figura 1.17: Gráfica VTC de la etapa de salida clase A [37].

- **Clase B.**

Diseñados para mejorar la eficiencia y los problemas de calentamiento de la etapa en clase A, los amplificadores de potencia de clase B constan de dos transistores complementarios. Un transistor amplifica la mitad positiva de la señal de entrada y el otro amplifica la mitad negativa (figura 1.18) (figura 1.19). [37]

Es posible alcanzar una eficiencia teórica de aproximadamente del 75%, pero debido a la superposición de dos mitades de la señal de entrada, existe una pequeña distorsión en la región de cruce [37].

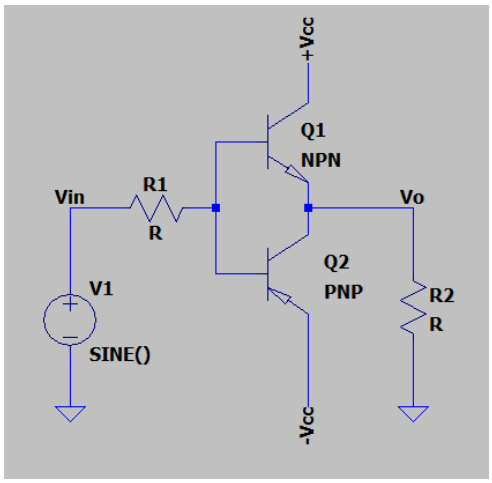


Figura 1.18: Amplificador de potencia en clase B [28].

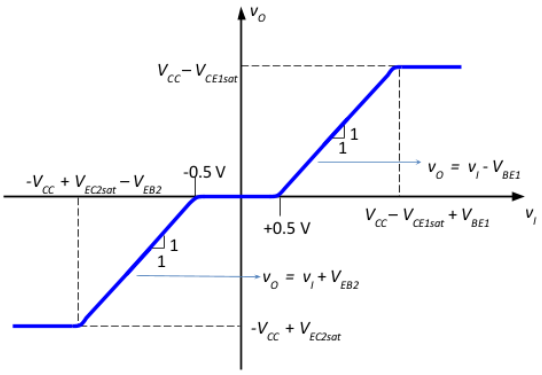


Figura 1.19: Gráfica VTC de la etapa de salida en clase B [37].

- **Clase AB.**

Diseñados para reducir el problema de eficiencia de los amplificadores de clase A y la distorsión de cruce en los amplificadores de clase B, los amplificadores en clase AB usan una combinación de diodos y resistencias para proporcionar una pequeña tensión de polarización que reduce la distorsión cerca de la región de cruce (figura 1.20) (figura 1.21) [37]

La mejora en la región de cruce acarrea una disminución de la eficiencia, pero esto se puede solventar mediante el empleo de un operacional en configuración de seguidor de tensión entre la entrada y la salida [37].

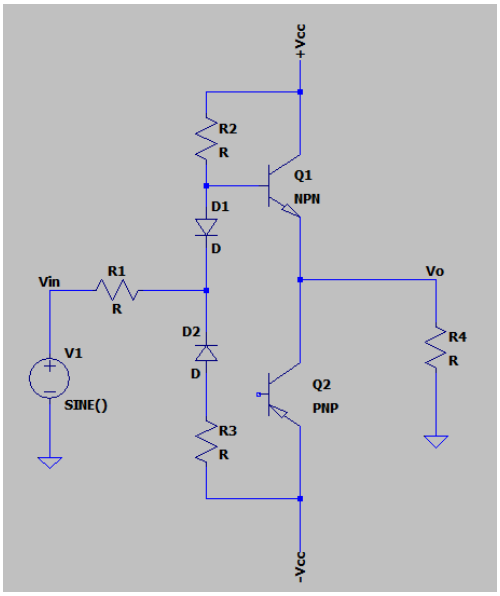


Figura 1.20: Amplificador de potencia en clase AB [28].

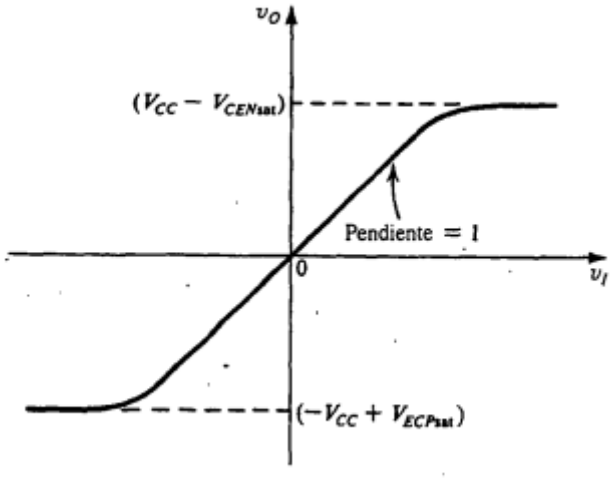


Figura 1.21: Gráfica VTC de la etapa de salida en clase AB [37].

5.2 Conceptos de acústica y elementos de audio

La Acústica es la rama de la Física que estudia el sonido, el cual se define como la variación de presión producida en un medio por un elemento vibrante y que el oído humano puede percibir. Por otra parte, el ruido se define como un conjunto de sonidos no armónicos o descompasados, siendo molesto y desagradable para el receptor. [13]

Cabe destacar que los parámetros del ruido y del sonido son equivalentes a la hora de proceder a su reducción o eliminación. [13]

5.2.1 Parámetros del sonido.

La variación de presión de sonido más simple, es la correspondiente a una onda sinusoidal pura. Teniendo en cuenta esto, pasamos a especificar los parámetros que caracterizan a dicha onda [13]:

- **Velocidad del sonido (c):** En el aire al nivel del mar a 20 ºC es aproximadamente de 340 m/s.
- **Longitud de onda (λ):** Hace referencia a la distancia entre crestas sucesivas en una onda sinusoidal. Se relaciona con la frecuencia mediante la expresión: λ= c/f.
- **Periodo (P):** Es el tiempo transcurrido entre dos picos sucesivos. Se relaciona con la frecuencia mediante la expresión: P= 1/f
- **Amplitud (A):** Mide las variaciones de presión. Dado que las variaciones de presión audibles se encuentran entre 20 μNw/m^2 y 108 μNw/m^2, se adoptó para su medición una unidad logarítmica llamada decibelio (dB) en la que interviene una magnitud de referencia, que es precisamente la mínima presión audible o presión de umbral.

$$\mathrm{dB} = 20\log_{10}\left(\frac{\mathrm{P}}{\mathrm{Po}}\right)\mathrm{dB} = 10\log_{10}\left(\frac{\mathrm{W}}{\mathrm{Wo}}\right)\mathrm{dB}$$

$$\mathrm{Po} = \frac{20\mu\mathrm{N}}{\mathrm{m}^2} = 20\mu\mathrm{Pa}\,;\ \mathrm{Wo} = 10^{-12}\mathrm{vatios}$$

Figura 1.22: Cálculo de dB.

- **Nivel de presión sonora (Lp):** parámetro que permite clasificar los niveles sonoros. Su cálculo viene asociado a la siguiente ecuación:

$$Lp = 20\log_{10}\left(\frac{P}{Po}\right)dB$$

Fuente	Presión de sonido (Pa)	Nivel de presión sonora (dB)
Susurro de hojas	0,0000632	10
Conversación normal	0,01	54
Televisor en casa	0,02	60
Automóvil de pasajeros como se escucha desde el borde de la carretera	0,1	74
Martillo de gato	2.0	100
Motor a reacción escuchado desde 100 yardas	100	134
Banda de rock extremadamente ruidosa	200	140
Motor a reacción como se escucha desde 1 yarda	630	150

Figura 1.23: Ejemplos de conversión de presión acústica a Lp [14].

- **Frecuencia (f):** Es el número de variaciones de presión por unidad de tiempo, se expresa en ciclos por segundo o Hercios (Hz).

5.2.2 Percepción del oído.

El sistema auditivo humano está capacitado para oír sonidos de frecuencias comprendidas entre los 20 Hz y los 20.000 Hz. Teniendo en cuenta esto, la siguiente figura muestra los efectos del sonido en el oído, atendiendo al nivel de presión sonora [41].

Niveles Sonoros y Respuesta Humana		
Sonidos característicos	**Nivel de presión sonora [dB]**	**Efecto**
Zona de lanzamiento de cohetes (sin protección auditiva)	180	Pérdida auditiva irreversible
Operación en pista de jets Sirena antiaérea	140	Dolorosamente fuerte
Trueno	130	
Despegue de jets (60 m) Bocina de auto (1 m)	120	Maximo esfuerzo vocal
Martillo neumático Concierto de Rock	110	Extremadamente fuerte
Camión recolector Petardos	100	Muy fuerte
Camión pesado (15 m) Tránsito urbano	90	Muy molesto Daño auditivo (8 Hrs)
Reloj Despertador (0,5 m) Secador de cabello	80	Molesto
Restaurante ruidoso Tránsito por autopista Oficina de negocios	70	Difícil uso del teléfono
Aire acondicionado Conversación normal	60	Intrusivo
Tránsito de vehículos livianos (30 m)	50	Silencio
Líving Dormitorio Oficina tranquila	40	
Biblioteca Susurro a 5 m	30	Muy silencioso
Estudio de radiodifusión	20	
	10	Apenas audible
	0	Umbral auditivo

Figura 1.24: Tabla de efectos del sonido en el oído humano [15].

Tras visualizar la figura anterior, se denota la importancia de controlar los niveles de presión sonora, dado que en caso de exponer al sistema auditivo a niveles de Lp altos y durante periodos de tiempo no controlados, se pueden originar problemas en la audición, que en algunos casos pueden llegar a ser irreversibles [41].

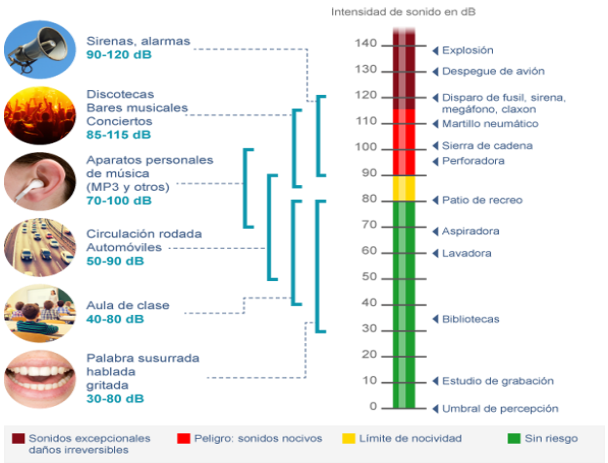


Figura 1.25: Peligrosidad de los niveles de presión sonora [41].

5.2.3 Sensibilidad del oído.

El sistema auditivo contiene dos parámetros de regulación, el volumen del sonido recibido y la agrupación de dos sonidos que pueden distanciarse mediante un tiempo de retardo [13].

- **Volumen.**

El oído humano no percibe todas las frecuencias con la misma intensidad. Su comportamiento viene especificado en la siguiente tabla [13].

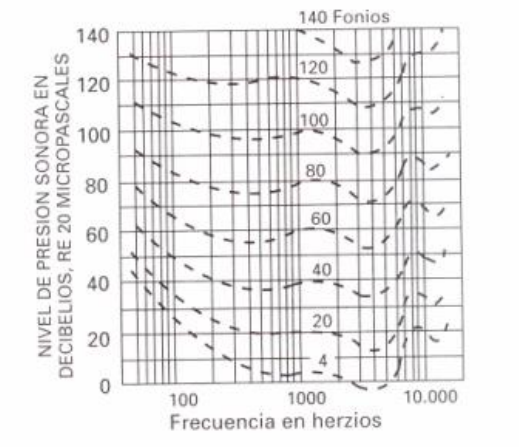


Figura 1.26: Curvas de audición del oído humano [13].

En la figura 1.26, se comprueba que el oído es más sensible en la banda comprendida entre los 500 y 6.000 Hz, y que carece de sensibilidad para captar sonidos graves agudos con bajo volumen.

Cabe destacar que la banda de frecuencias en la que fluctúa la voz humana está comprendida entre los 500 y los 2.000 Hz y que para percibir un sonido el doble de intenso, este debe incrementarse 10 dB [42].

- ***Delay*.**

Todos los sonidos que llegan al oído con un retardo igual o inferior a 60 ms, son agrupados y percibidos como un único sonido a mayor intensidad. Este fenómeno psicoacústico recibe el nombre de reverberación, y tiene una gran importancia en el ámbito de la música ya que, existen dispositivos específicos para añadir *delay* y de esa manera conseguir efectos de personalización de la señal de audio (figura 1.27) [43].

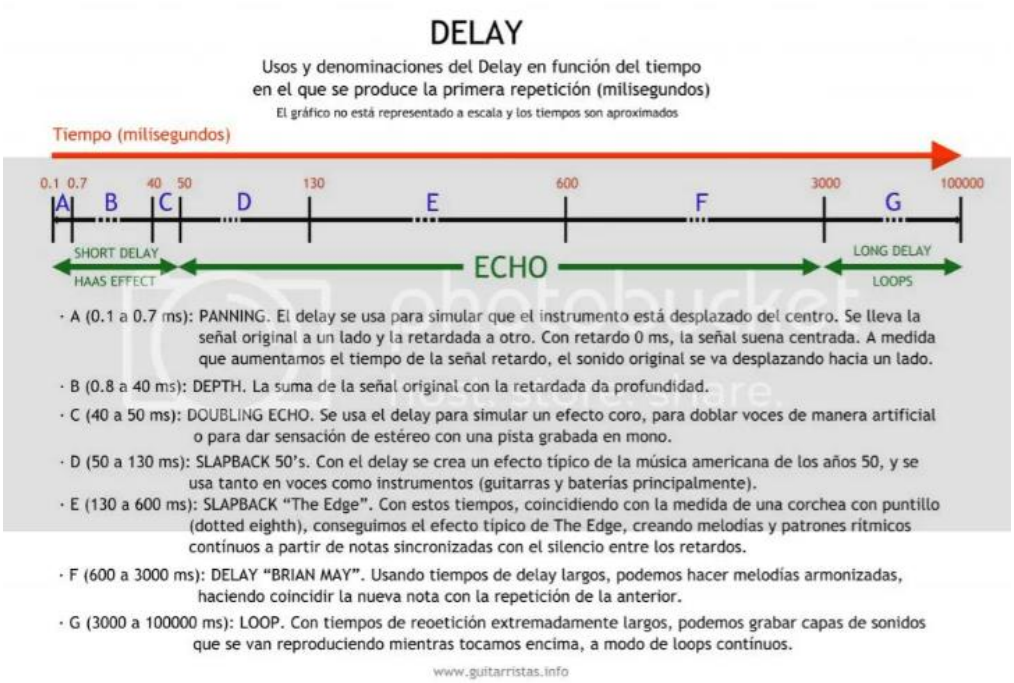


Figura 1.27: Efectos producidos mediante el uso del *delay* [44].

5.2.4 Dispositivos de entrada.

Se entiende por dispositivo de entrada al elemento encargado de generar la señal eléctrica asociada a la vibración de las ondas sonoras.

En el campo del sonido se emplean micrófonos para captar las señales acústicas transmitidas por el aire desde el foco de emisión y transformarlas en señales eléctricas para su posterior procesado [45] [46].

- **El micrófono:** transductor acústico que transforma la presión sonora recibida en una señal eléctrica que reproduce el equipo al que se encuentra conectado. A continuación, se detalla la clasificación atendiendo al tipo de transducción: [45] [46]
  - **Dinámicos:** se utilizan para cualquier tipo de transmisión, pero son más utilizados para captar sonidos en directo. No precisan de alimentación externa y suelen ser más baratos en comparación a otros tipos de micrófonos. En contraposición, son menos sensibles que otros tipos de micrófonos y no se recomienda para captar altas frecuencias.

Figura 1.28: Modelo comercial de micrófono dinámico. [47]

- **De condensador:** Son más sensibles que los micrófonos dinámicos y tienen una respuesta más plana en las frecuencias altas. Se utilizan habitualmente en los estudios de grabación. Un inconveniente es que debido a su alta sensibilidad no solo recoge el sonido que tienes más cerca, sino que, si no grabamos en un entorno adaptado se pueden introducir sonidos no deseados.

Figura 1.29: Modelo comercial de micrófono de condensador. [47]

- **De cinta:** en su mayoría son bidireccionales, aunque existen algunos modelos unidireccionales. Son micrófonos grandes y delicados, y su respuesta en frecuencia es de tonalidad cálida, ya que su respuesta en frecuencias agudas, suele ser bastante pobre. Todos los micrófonos de cinta incorporan un pequeño transformador para elevar la baja tensión de salida que son capaces de dar y para adaptar la baja impedancia de salida.

Figura 1.30: Modelo comercial de micrófono de cinta.[47]

- **Electret:** Son micrófonos pequeños, se usan normalmente como accesorio para colocar en la camisa y hacer pequeñas grabaciones o para captar sonidos de instrumentos al colocarlos directamente sobre ellos.

Figura 1.31: Modelo comercial de micrófono electret [47].

5.2.5 Dispositivos de salida.

Se entiende por dispositivo de salida al encargado de emitir las señales procesadas en las etapas anteriores.

Los altavoces y los auriculares se emplean en el campo del audio para satisfacer esta misión. Son los encargados de desempeñar el trabajo inverso a los dispositivos de entrada. Transforman las señales eléctricas, que ya han pasado por las diversas etapas de procesado, en señales acústicas que se propagaran por el aire.

Usualmente la impedancia de los auriculares y los altavoces oscila entre 16 y 600 ohmios, este dato lo podemos corroborar al realizar un estudio de mercado.

Los auriculares precisan de señales de audio de menor energía, contrariamente a los altavoces, para reproducir sonidos de alto volumen.

Figura 1.32: Modelo comercial de altavoz [47].

Figura 1.33: Modelo comercial de auriculares [47].

5.2.6 Dispositivos de transmisión y conexión.

- **Cables:** Elementos de conducción de señales eléctricas, usualmente fabricados en cobre, utilizados en varios campos industriales y comerciales. Desde el punto de vista del sonido, la clasificación primaria de los cables es: [48]
    - **Cables no balanceados:** son más sensibles a la adición de ruido a la señal transmitida mediante el proceso de transporte. Su construcción se basa en un cable conductor y un cable de toma de tierra.
    - **Cables balanceados:** están diseñados para anular toda interferencia introducida en el canal de transmisión. Esto se consigue mediante la adición de un cable interno adicional en la estructura del cable no balanceado. Por un cable se transmite la señal sin desfase y por el otro se transmite desfasada 180º, por lo que, tras invertir la señal desfasada, al sumarse se cancelaran los ruidos originados por el medio de transmisión.

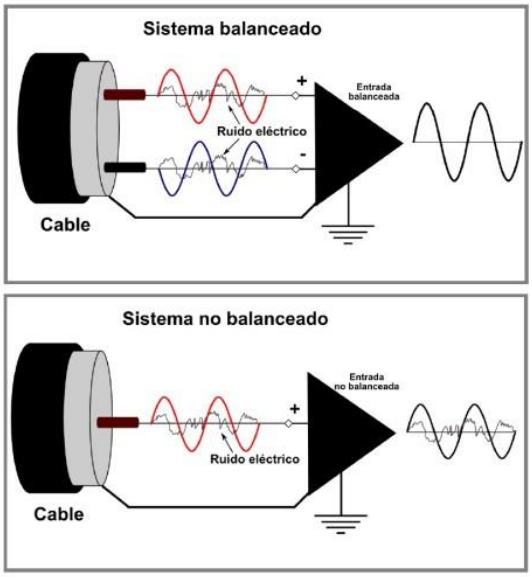


Figura 1.34: Resumen de los tipos de cables en clasificación primaria [48].

Una vez comprendida la clasificación primaria de los cables, podemos clasificarlos en función del conector empleado:

- **Cables analógicos:**

    - **Cables XLR:** son siempre balanceados. Tienen un mecanismo de enclavamiento que evita la desconexión involuntaria. Pueden ser de gran longitud y no tener interferencia de ruido.

Figura 1.35: Disposición de pines del cable XLR [49][50].

- **Cables TRS (Tip-Ring-Sleeve)**: son balanceados y contienen conectores de tres cables en el interior (dos conductores y una toma de tierra). Son fáciles de identificar gracias a los dos anillos de goma en el conector.

PHASE	Termination Point
POSITIVE (+)	TIP
NEGATIVE (-)	RING
SIGNAL GROUND	SLEEVE

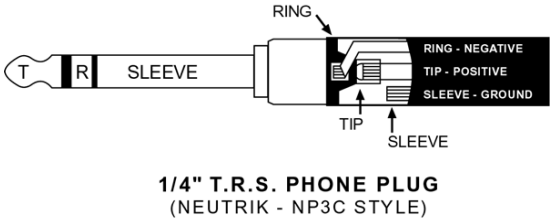


Figura 1.36: Disposición de pines del cable TRS [51].

- **Cables TS (Tip-Sleeve):** son no balanceados ya que, contienen dos cables internos: un conductor y una toma de tierra. Tienen un anillo de goma en el conector.

PHASE	Termination Point
POSITIVE (+)	TIP
NEGATIVE (-)	SLEEVE
SIGNAL GROUND	SLEEVE

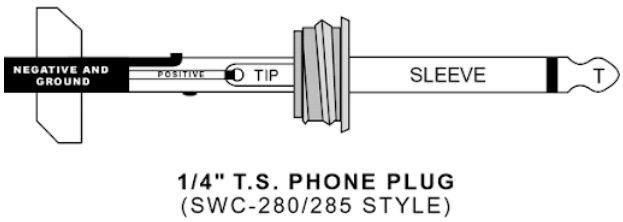


Figura 1.37: Disposición de pines del cable TS [52].

- **Cables digitales:**
  - **Cables MIDI:** se usan para sincronizar y comunicar instrucciones entre dispositivos.

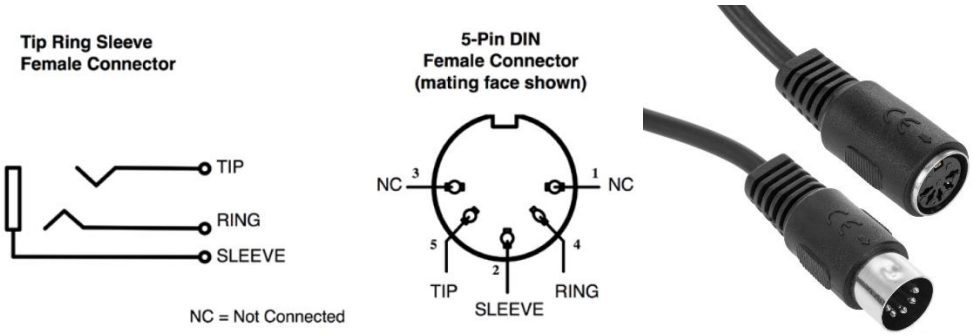


Figura 1.38: Disposición de pines del cable MIDI [53][54].

- **Cables USB**: muy usados en la producción de audio. Se incorporan en interfaces de audio, sintetizadores modernos y cajas de ritmos. Cabe destacar que transmiten información MIDI.

5.2.7 Alimentación phantom.

La alimentación *phantom* es una fuente de alimentación de 48 V en corriente continua que se emplea para suministrar energía a los micrófonos de condensador y a las cajas de inyección. La tensión puede ser de 12, 24 y 48 V, y se conecta directamente a los cables que trasmiten la señal de audio. Este hecho no modifica la señal de audio en el medio de transmisión ya que se debe emplear un circuito específico para eliminar la componente de continua a la entrada del siguiente dispositivo [55]. En cables balanceados se debe conectar la tensión a los pines 2 y 3, en el caso de conectores XLR.

Cabe destacar que un micrófono dinámico balanceado correctamente funcionará con o sin la alimentación *phantom* conectada, pero en el caso de los micrófonos de cinta se recomienda desconectar la alimentación *phantom* [55].

El método correcto de desconectar un dispositivo de la alimentación *phantom* es el siguiente: primero se deberá apagar el canal del dispositivo conectado y luego se desconecta. En caso contrario se producirá un chasquido muy sonoro producido por la alimentación *phantom* [55].

5.2.8 Limitaciones normativas.

A parte de focalizar el trabajo en realizar un correcto diseño del dispositivo explicado en el presente documento, es de gran importancia informarse sobre la normativa actual asociada a las emisiones de sonido tanto en auriculares como en reproductores de música. Por ello y tras realizar un análisis de la normativa actual se debe cumplir lo siguiente:

Tal y como establece en la directiva 2001/95/CE: “Los reproductores de música personales irán acompañados de advertencias adecuadas relativas a los riesgos que presenta el uso del aparato y las formas para evitar estos riesgos, así como de información para los usuarios sobre los casos en que la exposición supone un riesgo de lesión auditiva. Se limitará el tiempo de exposición sonora a fin de evitar las lesiones auditivas.”

Por otra parte, el Comité Europeo de Normalización Electrotécnica ha emitido la norma UNE-EN IEC 62368-1:2020 para regularizar el mercado de audio y video en materia de seguridad. En dicha norma se informa de lo siguiente: “El límite estándar de sonido será de 80dB(A). Aunque se permitirá la posibilidad de incrementar a 100dB(A) con aviso sobre los riesgos de su uso por encima de los niveles de seguridad cada 20h de escucha”.
El cumplimiento de esta norma ya se ha empezado a implementar en los dispositivos de telefonía móvil. Para ello se emplea una reducción del volumen y un mensaje emergente avisando del volumen excesivo al usar auriculares.

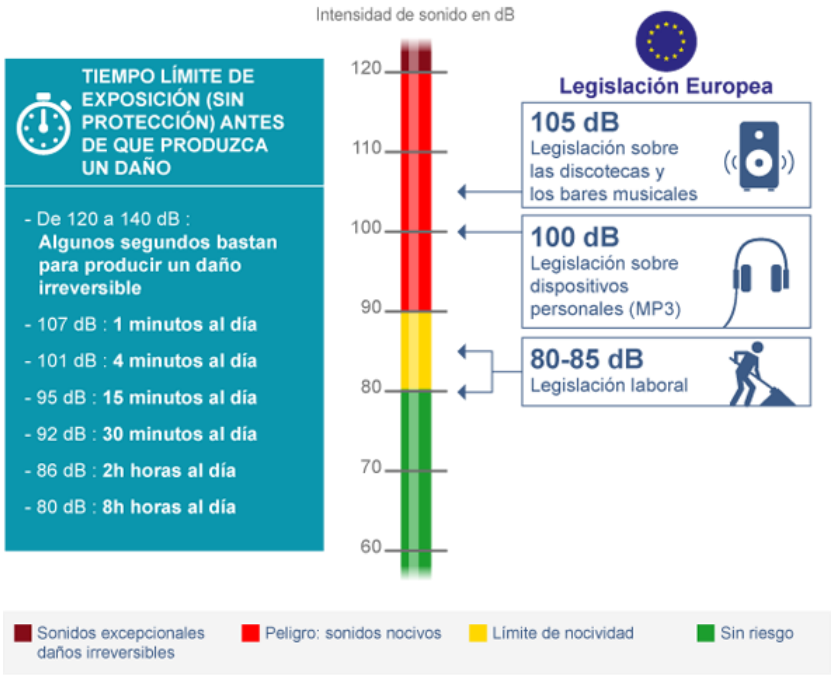


Figura 1.39: Resumen de la normativa acústica de la UE [41].

6. Diseño, simulaciones y experimentación.

Partiendo de los antecedentes que enmarcan el origen del diseño y del preámbulo teórico que determina la base sobre la que se fundamenta este trabajo de fin de grado, se retoma la figura mostrada en la introducción asociada al esquema del sistema de procesado independiente de audio.

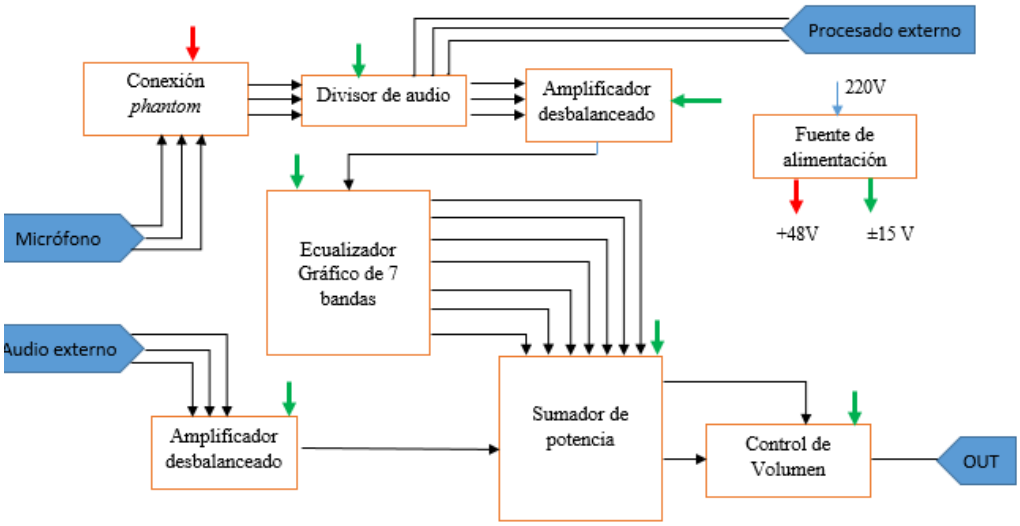


Figura 1.40: Esquema genérico del sistema de procesado independiente de audio [28].

En la figura anterior se puede ver un esquema de bloques funcionales que en conjunto forman un sistema orientado al procesado de dos señales de audio entrantes, volcando en la salida una señal personalizada fruto de la combinación y mezcla de ambas señales de entrada.

Los bloques funcionales se resumen a continuación:

1. **Circuito de conexión para alimentación *phantom*:** este circuito permite alimentar dispositivos de entrada que precisan de una alimentación en DC para captar señales acústicas y transformarlas en señales eléctricas. Gracias a este bloque funcional podemos emplear tanto micrófonos dinámicos como micrófonos de condensador, ampliando así la versatilidad del dispositivo final al habilitar una entrada universal de información desde cualquier dispositivo.
2. **Divisor de audio:** mediante este bloque funcional se toma una "imagen" de la señal de entrada 1, permitiendo así redirigir la señal original hacia otros dispositivos de procesado de señal.
3. **Preamplificador desbalanceado 1:** permite adecuar la señal de entrada 1, proveniente del micrófono, elevando el voltaje antes de entrar en el siguiente bloque funcional, la etapa de ecualización. Esto evita la adición de ruidos de bajo voltaje en la señal de entrada. Cumple la función de controlar el volumen primario de la entrada 1.
4. **Ecualizador gráfico de 7 bandas:** partiendo del diseño de Rod Elliott se ha diseñado un ecualizador gráfico con 7 bandas. Este bloque funcional permite la personalización del tono de la señal de entrada 1 en cada una de las 7 bandas, creando así una señal personalizada bajo las especificaciones del usuario.
5. **Preamplificador desbalanceado 2:** permite armonizar la señal de entrada 2 al eliminar los ruidos originados por el medio de transmisión hasta nuestro dispositivo. A diferencia del preamplificador de la entrada 1, este preamplificador no precisa de una ganancia variable por lo que el diseño será más simplificado.

6. **Sumador de potencia:** habilita la suma de la señal de entrada 1, modificada en las etapas anteriores, con la señal de entrada 2. Además, es el circuito que soportará la carga de potencia solicitada por el dispositivo de salida que se conecte a nuestro dispositivo. Contiene los controles de volumen generales para el canal 1 y el canal 2, asociados a las entradas 1 y 2, respectivamente.
7. **Control de volumen:** este bloque es uno de los más importantes del dispositivo ya que permite proteger al usuario de subidas del nivel de presión sonora, por encima de 100 dB SPL, en la salida del dispositivo. En definitiva, permite cumplir la normativa vigente de la Unión Europea en materia de protección y seguridad auditiva.
8. **Fuente de Alimentación:** permite dar la energía necesaria a todo el circuito mediante la aportación de las tensiones de alimentación y la alimentación *phantom*, a partir de la conversión de una entrada de tensión doméstica de 220 V.

6.1 Circuito de conexión para alimentación phantom.

- **Descripción:**

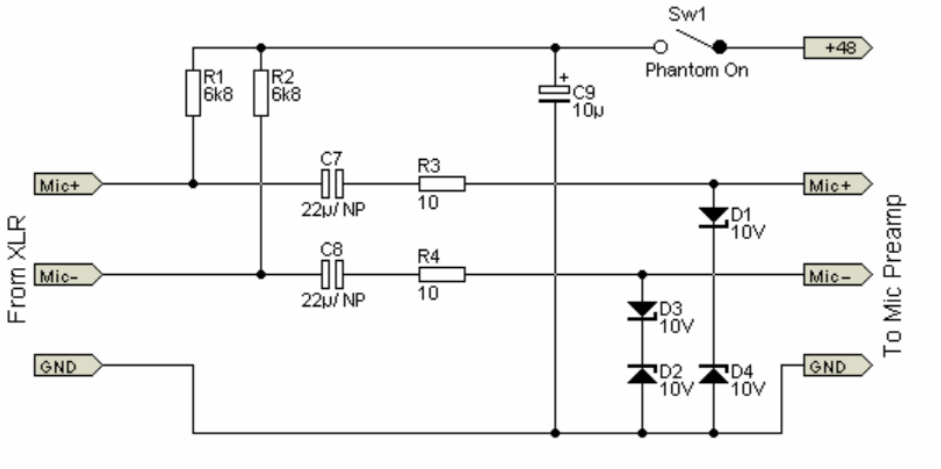


Figura 1.41: Diseño de la conexión phantom de Rod Elliott © 2002 [11].

Con el fin de transmitir la alimentación *phantom* de +48V en DC, a los dispositivos de entrada, de una manera eficiente y evitando el paso de dicha alimentación a los demás bloques funcionales, se ha optado por diseño creado por Rod Elliott mostrado en la figura 1.41.

En dicho diseño el autor propone el uso de resistencias de 6800 Ω para conectar la alimentación de 48 V DC a los pines 2 y 3 de la conexión balanceada XLR. Se destaca que los valores de las resistencias deben ser lo más cercanos posibles para para facilitar el funcionamiento óptimo del circuito. [11]

Por otra parte, se emplean condensadores de 22 uF que permiten obtener una respuesta plana a 20Hz. Se aconseja que estos condensadores sean de poliéster para evitar distorsión, aunque se permite el uso de electrolíticos teniendo siempre precaución con la orientación de las patillas. [11]

Además, se usan diodos Zener para limitar el voltaje máximo aplicado al siguiente bloque funcional. Deben ser de 10V y 1W para que soporten las descargas repentinas que influyan en el circuito. La corriente de sobretensión máxima para los zeners de 1W 10V es típicamente 450 mA. Dicho valor no se alcanza en micrófonos. [11]

Las resistencias de 10 Ω tienen poca influencia en el cometido del circuito, pero sirven como apoyo a los zeners para limitar su corriente pico. [11]

El interruptor de corte de la alimentación de 48 V DC debe ser de corte silencioso para evitar el chasquido característico de la desconexión de la alimentación *phantom*. [11]

Por último, se emplea un condensador electrolítico de 10 uF para depurar posibles armónicos presentes en la alimentación de +48 V y así solo usar la componente de continua. [11]

- **Simulación:**

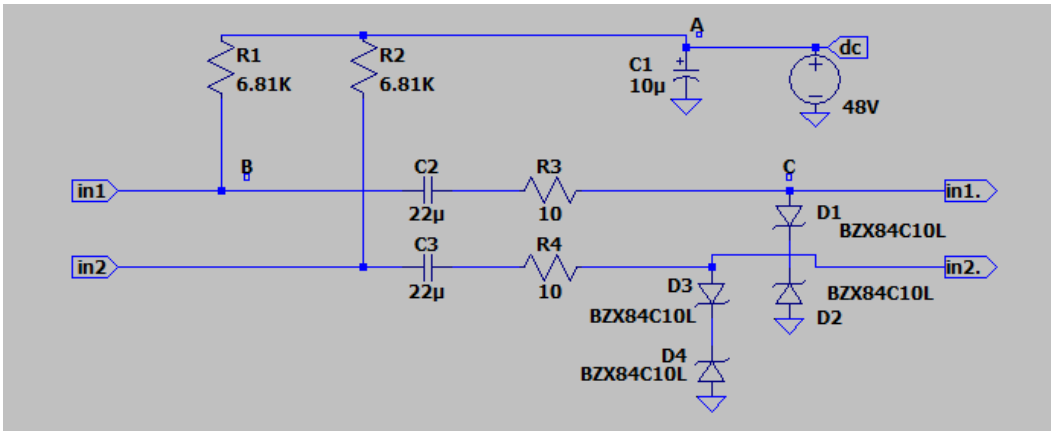


Figura 1.42: Implementación del diseño en LTSpice [28].

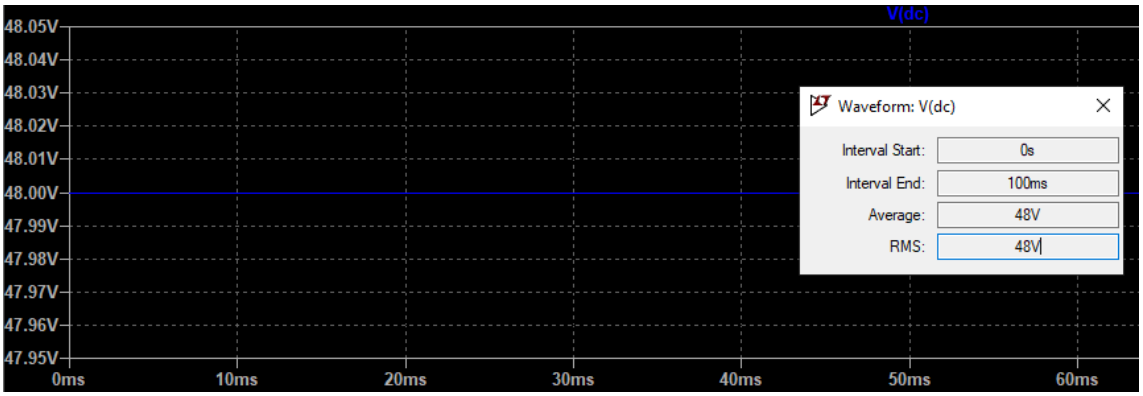


Figura 1.43: Comprobación de tensión en el punto A. (tiempo-voltaje) [28]

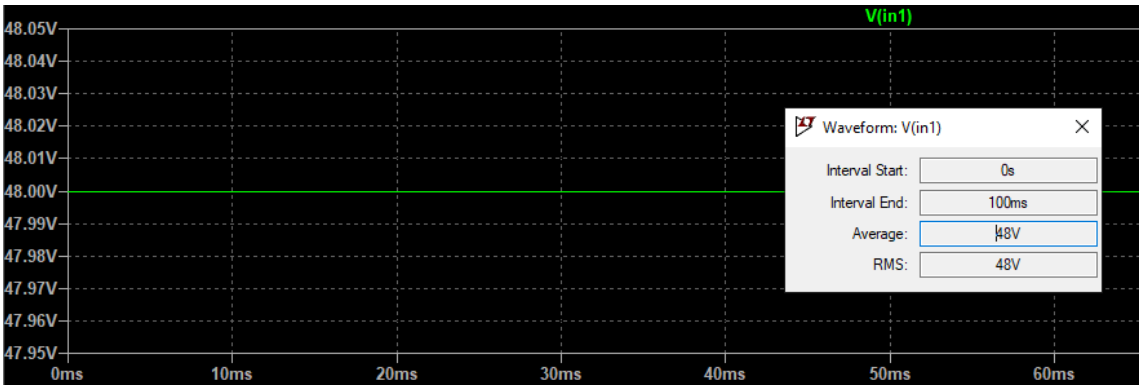


Figura 1.44: Comprobación de tensión en el punto B. (tiempo-voltaje) [28]

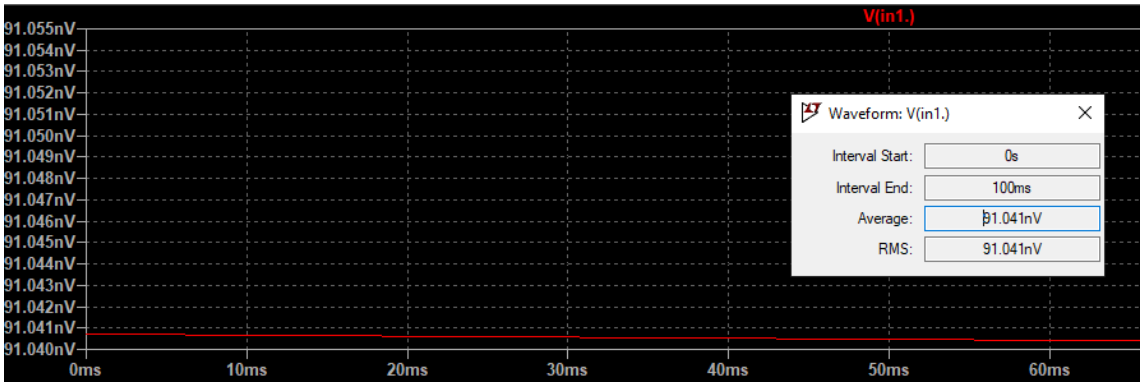


Figura 1.45: Comprobación de tensión en el punto C. (tiempo-voltaje) [28]

Tras realizar el proceso de simulación del circuito comprobamos el correcto funcionamiento del mismo dado que, al realizar las mediciones en los puntos A y B el voltaje medido es el esperado, 48 V. Además, en el punto C se verifica la no presencia de la tensión de 48 V al medir un valor de 91.041 nV, valor aproximable a 0V.

6.2 Divisor de audio.

- **Descripción:**

Siendo uno de los bloques funcionales más sencillos, aporta al dispositivo una función muy importante, permitiendo tomar una imagen o copia de la señal original introducida por la entrada 1, para personalizarla al gusto del usuario y a la vez habilitando una personalización externa de la misma señal en otros dispositivos, como mesas de sonido.

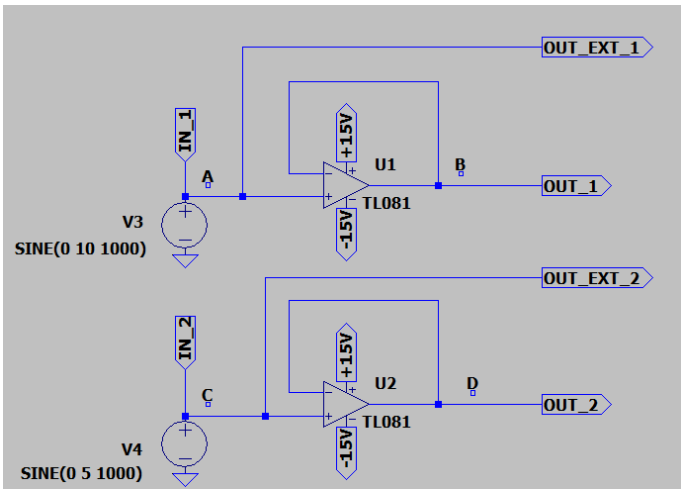


Figura 1.46: Diseño del divisor de audio [28].

Como se puede ver en la figura 1.46, el diseño se centra en la implementación de dos seguidores de tensión que toman la señal de cada uno de los cables del conector XLR asociado a la entrada 1. Otra ventaja de este bloque funcional es que eliminamos la posibilidad de fallos ocasionados por la corriente de la señal de entrada, ya que, gracias al funcionamiento de los seguidores de tensión se aísla la corriente entrante.

- **Simulación:**

Después de realizar la configuración de las fuentes de tensión de entrada, con una señal de 10 V a 1 kHz y una señal de 5 V a 1 kHz, para probar el circuito. Se han obtenido los siguientes resultados al medir en los puntos de prueba:

Cabe destacar que se emplea un modelo Spice del operacional TL081, obtenido de la página oficial de Texas Instruments, alimentado a +15 V y -15 V en sus pines de alimentación.

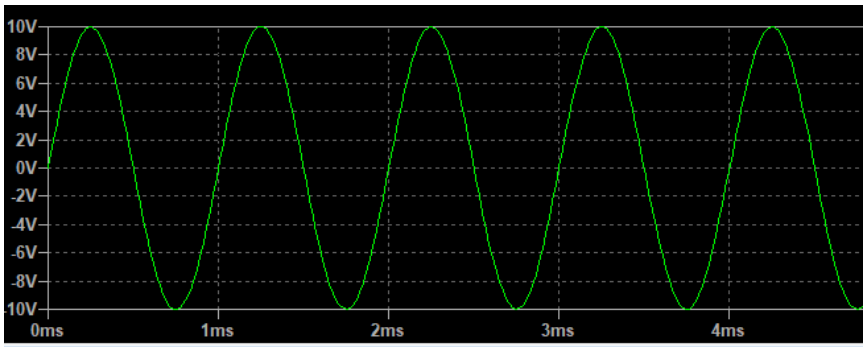


Figura 1.47: Comprobación de tensión en el punto A. (tiempo-voltaje) [28]

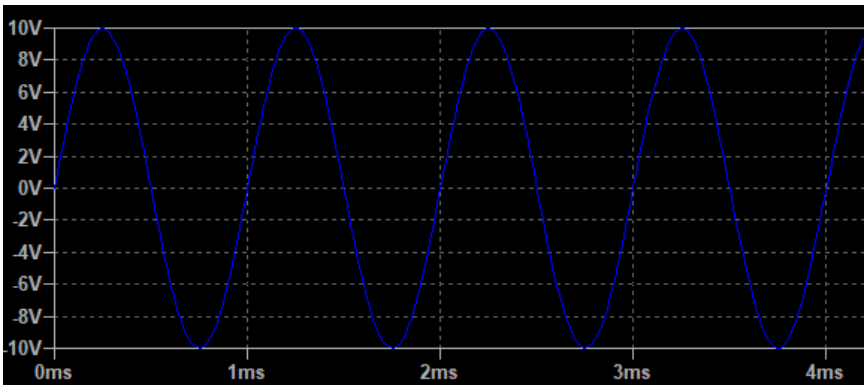


Figura 1.48: Comprobación de tensión en el punto B. (tiempo-voltaje) [28]

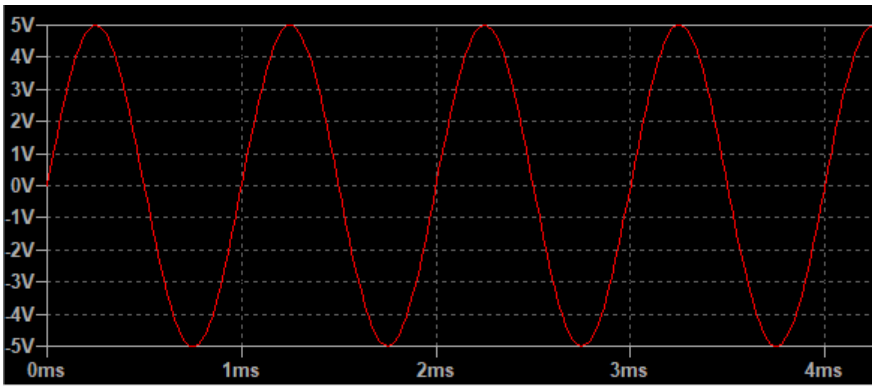


Figura 1.49: Comprobación de tensión en el punto C. (tiempo-voltaje) [28]

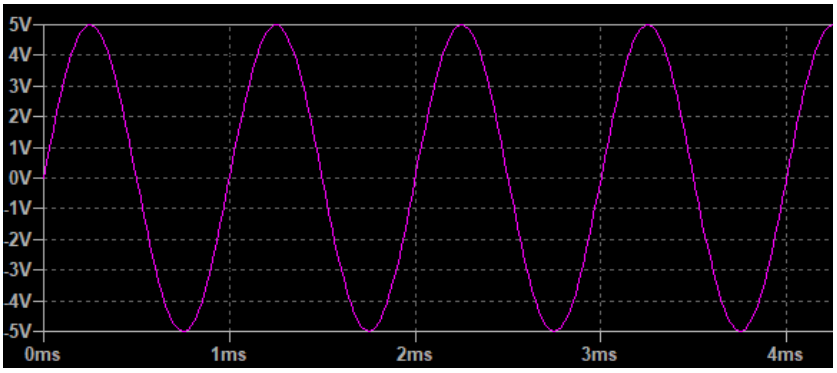


Figura 1.50: Comprobación de tensión en el punto D. (tiempo-voltaje) [28]

Una vez finalizado el proceso de comprobación y visualizando los resultados obtenidos, se comprueba el correcto funcionamiento del circuito en la etapa de simulación dado que se obtiene el mismo voltaje en la entrada y la salida, tanto en el canal 1 como en el canal 2.

6.3 Preamplificador desbalanceado 1.

- **Descripción:**

El preamplificador, como su propio nombre indica, permite amplificar la señal de entrada y así adecuarla para que, en las etapas siguientes de procesado, asociadas a los bloques funcionales contiguos, no sea tan latente el ruido de baja amplitud que se suele adicionar en los circuitos.

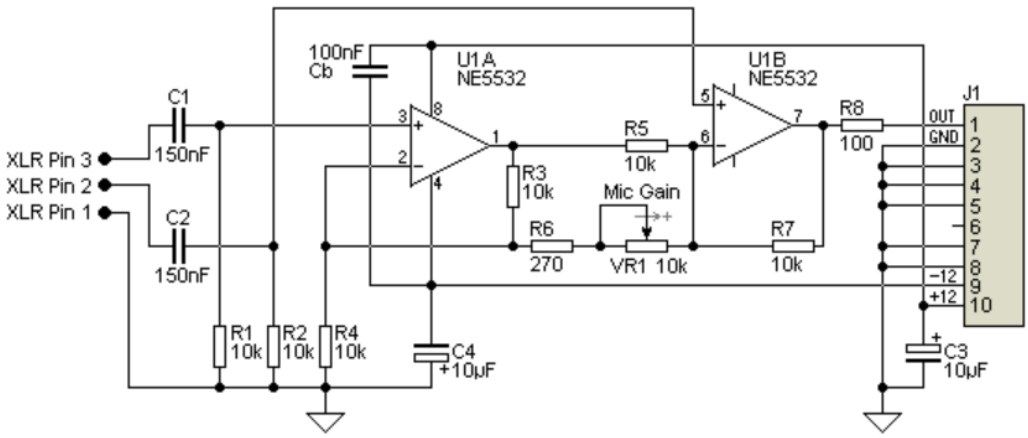


Figura 1.51: Diseño del preamplificador desbalanceador de Rod Elliott © 2008. [12]

En el diseño mostrado en la figura 1.51, el integrado J1 no será de utilidad para el desarrollo de nuestro bloque funcional. Las alimentaciones serán por conexión directa a los operacionales con un valor de +15 y -15 V.

Al igual que en el caso de la conexión *phantom*, el autor Rod Elliott propone un circuito que permite captar una señal proveniente de un conector XLR, que en nuestro caso vendrá desde el divisor de audio. Dicha señal será desbalanceada mediante el proceso de invertir la señal del pin3 y sumarla a la señal del pin2. Como ya se explicó en apartados anteriores, este proceso permite quitar el ruido que contenía la señal originado por el medio de transmisión. Además de esta funcionalidad, el diseño de Rod Elliott nos permite amplificar con una ganancia variable, modificable mediante el control del potenciómetro VR1, desde 4, valor mínimo, hasta 78, valor máximo. [12]

Los condensadores de entrada dan una caída de baja frecuencia de -3dB a aproximadamente 104Hz. [12]

- **Simulación:**

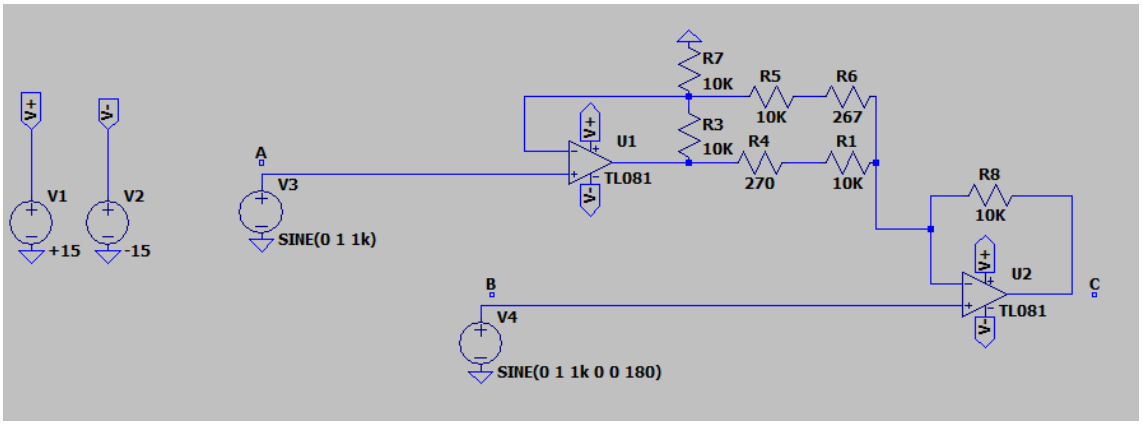


Figura 1.52: Implementación del preamplificador desbalanceado 1 [28].

Primeramente, configuramos las fuentes de entrada con una señal de 1 V a 1kHz, para la entrada 1 (V3), y una señal similar a la anterior pero desfasada 180º, para la entrada 2 (V4).

Seguidamente, alimentamos los TL081 con una tensión de alimentación de +15 y -15 V.

Una vez configurada la simulación procedemos a probar al circuito con el potenciómetro en un valor de 10 kΩ (R1).

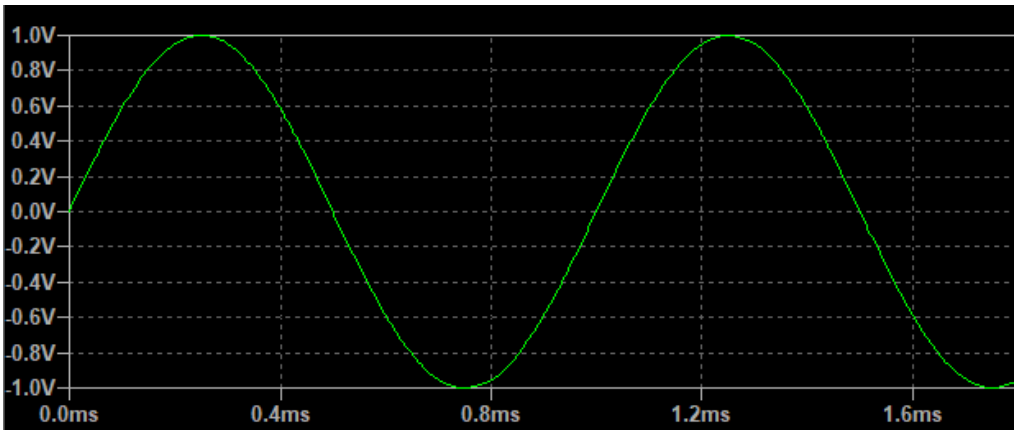


Figura 1.53: Comprobación de tensión en el punto A. (tiempo-voltaje) [28]

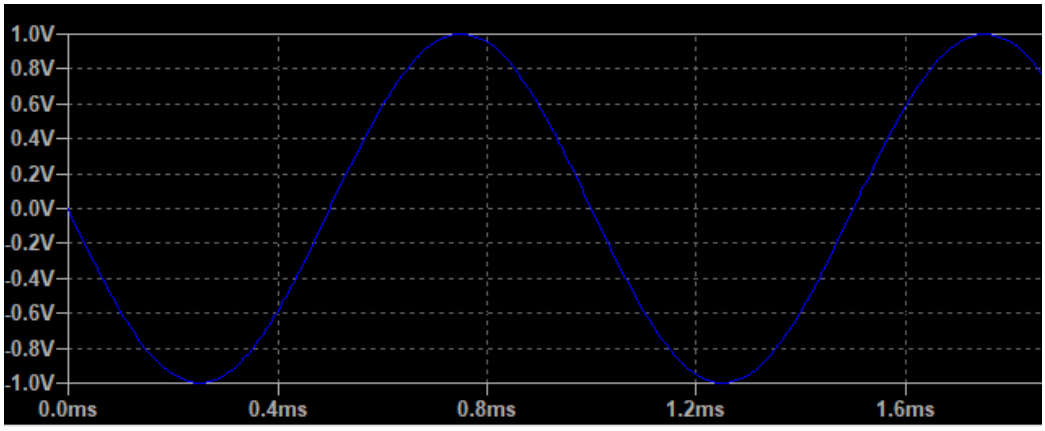


Figura 1.54: Comprobación de tensión en el punto B. (tiempo-voltaje) [28]

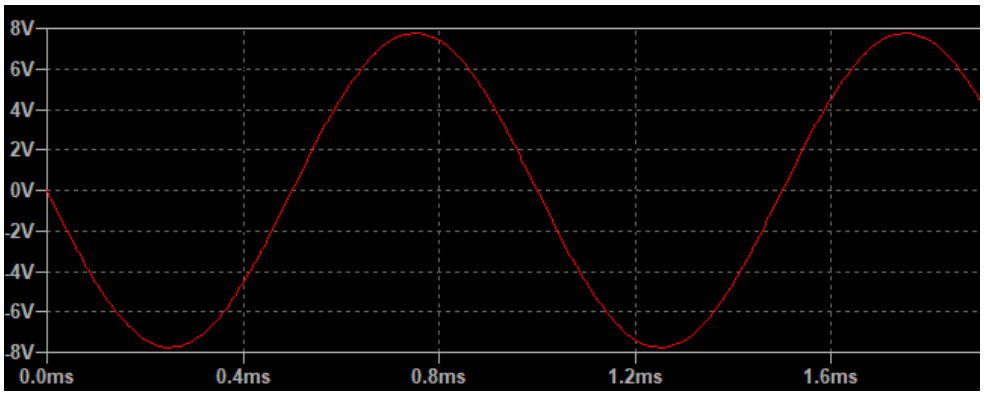


Figura 1.55: Comprobación de tensión en el punto C. (tiempo-voltaje) [28]

Tal y como se comprueba al visualizar los resultados obtenidos, el circuito devuelve resultados razonables, dado que, al introducirle una señal de 1 V (punto A) y una señal de 1 V desfasada 180º (punto B), se obtiene a la salida (punto C) un valor de 8 V, correspondiente a la aplicación de la ganancia con valor 4, que se esperaba al configurar el potenciómetro en el máximo valor.

Por otra parte, cuando se configura el potenciómetro en su valor más bajo, actuando prácticamente el valor de 270 Ω, el resultado obtenido es una señal cuadrada entre los valores de alimentación,(figura 1.56). Es lo esperado dado que, al aplicarse la ganancia máxima de 78, el operacional satura a sus valores de alimentación.

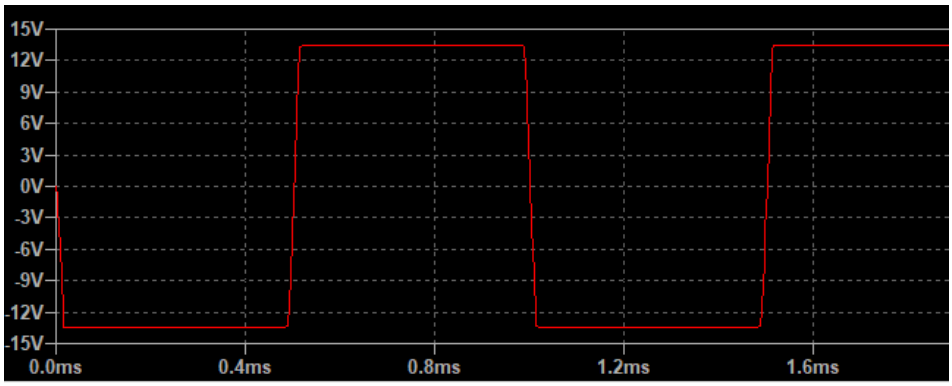


Figura 1.56: Comprobación de tensión en el punto C con ganancia máxima. (tiempo-voltaje) [28]

Una forma de comprobar que el circuito amplifica adecuadamente es ubicar el potenciómetro en su posición media con un valor de 5 kΩ y ver que amplifica la señal. Esto se comprueba en la figura 1.57.

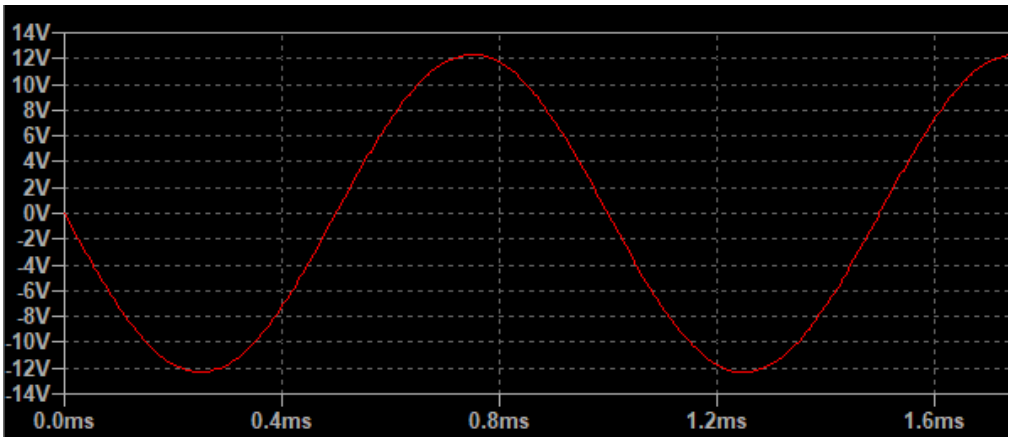


Figura 1.57: Comprobación de tensión en el punto C con ganancia media. (tiempo-voltaje) [28]

6.4 Ecualizador gráfico de 7 bandas.

- **Descripción:**

Partiendo de la idea de crear un ecualizador de 7 bandas (<16 Hz, 63 Hz -250 Hz, 250 Hz -1 kHz, 1 kHz -4 kHz, 4 kHz -16 kHz, >16 kHz) que conservara la señal de entrada en la salida en caso de no realizar modificaciones en las bandas de frecuencia, el diseño de combinación de filtros de 2º y 4º orden, del autor Linkiwtz Lab, orientado a la creación de un ecualizador de 4 bandas con una topología de implementación específica, marcó el comienzo del diseño del ecualizador de 7 bandas.

Primeramente, se deben usar filtros activos de 4º orden empleando la tipología sallen-key (implementando dos filtros de 2º orden en serie), esto permite que la pendiente en la frecuencia de corte sea más pronunciada (-24 dB/octava), favoreciendo así el corte de frecuencias no deseadas. [16]

Para el diseño se usan 2 filtros de 4º orden para las frecuencias de 16 y 16 kHz, pasa-baja y pasa-alta, respectivamente. Además, se usan combinaciones de filtros pasa-baja y pasa-alta, de 4º orden, para ir confeccionando las demás bandas de frecuencia. [16]

La tipología empleada es la especificada por Linkiwtz Lab en la que se emplea primero un pasa-baja, seguido de un pasa-alta en serie y continuado de otro pasa-baja para completar las primeras 2 banda. La explicación es más intuitiva si nos fijamos en la figura 1.58. [16]

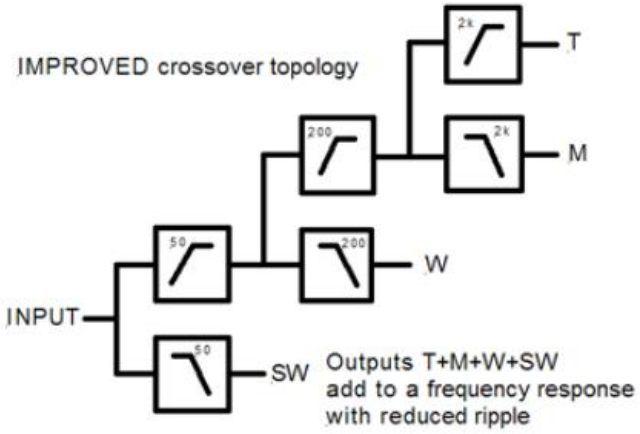


Figura 1.58: Topología de diseño de Linkiwtz Lab © 1998-2019 [16]

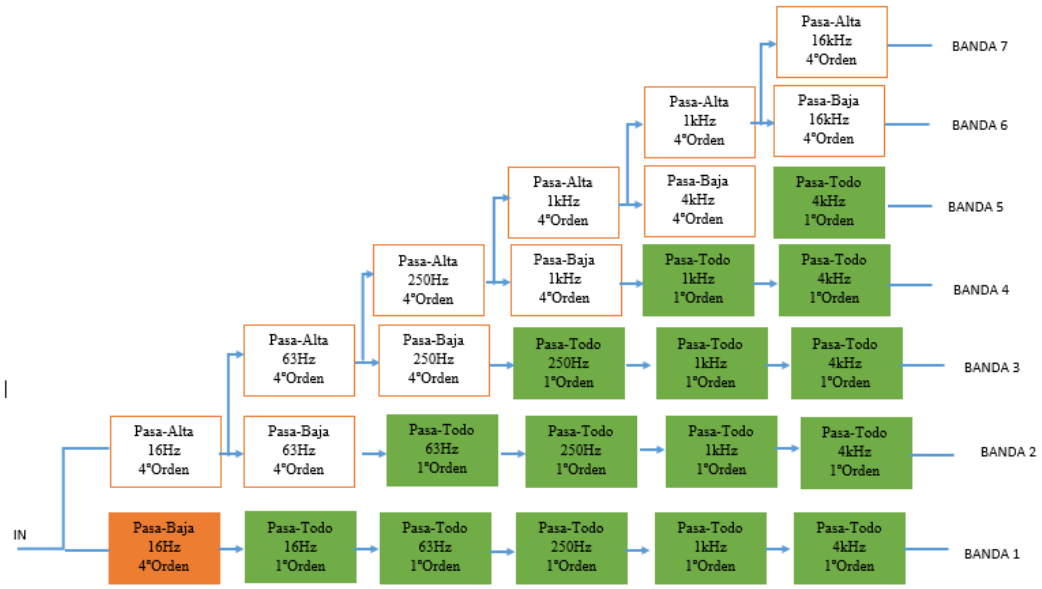


Figura 1.59: Topología de diseño del ecualizador de 7 bandas [28].

A la tipología de Linkiwtz Lab se le deben añadir unos filtros pasa-todo de 1ºorden para compensar el desfase acumulado. De esta forma obtendremos una respuesta plana en el cruce de las bandas. En definitiva, si introducimos una señal de 16 Hz, la señal pasará por el pasa-baja de 16 Hz y por el pasa-alta de 16 Hz en serie con el pasa alta de 63 Hz, en este segundo camino la señal se retrasa 41º (valor obtenido mediante la simulación del circuito) por lo que se debe retrasar la señal que tomo el camino 1 para que al sumarlas de una respuesta plana en el cruce.

Después de trazar el diseño del ecualizador, hay que dimensionar el circuito mediante el procedimiento adecuado en función del filtro a dimensionar. Los procedimientos de cálculo para hallar los componentes de cada filtro se detallan a continuación;

- **Pasa Baja:**
  1. Tomamos los siguientes parámetros: m*=1, R*= 10 kΩ-100 kΩ, Q = 0,71.
  2. Resolvemos las siguientes ecuaciones para obtener C1,C2,R2,R1:

$$C^* = \frac{1}{\sqrt{m*n}*2\pi*f_o*R^*} \quad (1)$$

$$n^* = 4 * Q^2 \quad (2)$$

$$\sqrt{m * n^*} = Q * (m^* + 1) \quad (3)$$

$$C2 \approx C^* \quad (4)$$

$$C1 \approx C^* * n^* \quad (5)$$

Hallar valores comerciales de C1 y C2. (6)

$$n = \frac{C2}{C1} \quad (7)$$

$$k = \frac{n}{Q^2} - 2 \quad (8)$$

$$m = \frac{k + \sqrt{k^2 - 4}}{2} \quad (9)$$

$$R2 = \frac{1}{\sqrt{m*n}*2\pi*f_o*C2} \quad (10)$$

$$R1 = R2 * m \quad (11)$$

Los resultados obtenidos tras realizar los procedimientos anteriores en el dimensionado de los filtros pasa-baja, se muestran en el Anexo II.

- **Pasa Alta:**
  1. Tomamos los siguientes parámetros: n*=1, R*= 1 kΩ -1 MΩ s, Q = 0,71.
  2. Resolvemos las siguientes ecuaciones para obtener C1,C2,R2,R1:

$$C^* = \frac{1}{\sqrt{m*n}*2\pi*f_o*R^*} \quad (1)$$

$$m = 4 * Q^2 \quad (2)$$

$$\sqrt{m*n} = Q * (n^* + 1) \quad (3)$$

$$C2 \approx C^* \quad (4)$$

$$C1 \approx C^* \quad (5)$$

Hallar valores comerciales de C1 y C2. (6)

$$R1 = \frac{1}{\sqrt{m*n}*2\pi*f_o*C1} \quad (7)$$

$$R2 = R1 * m \quad (8)$$

Los resultados obtenidos tras realizar los procedimientos anteriores en el dimensionado del ecualizador se muestran en el Anexo III.

- Simulación:

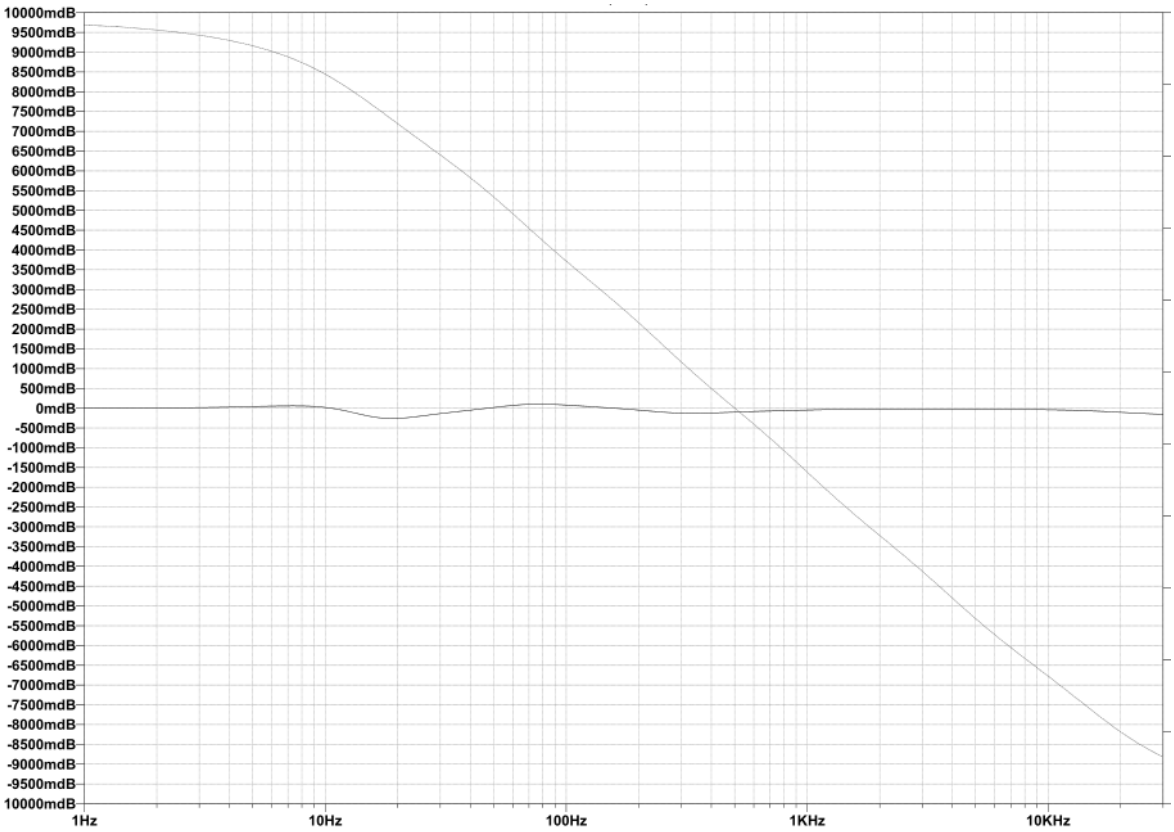


Figura 1.60: Barrido en frecuencia del ecualizador de 7 bandas. (frecuencia-dB) [28].

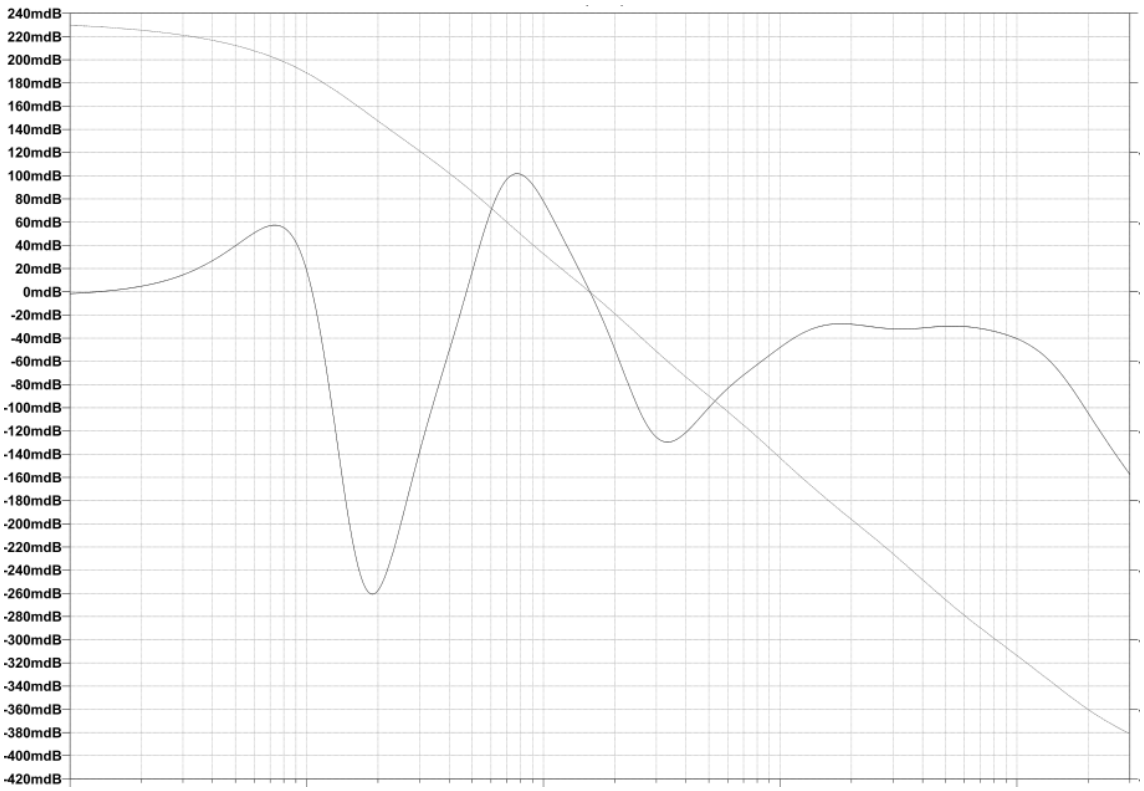


Figura 1.61: Barrido en frecuencia, en detalle, del ecualizador de 7 bandas. (frecuencia-dB) [28].

Tras realizar un barrido en frecuencia, logarítmico, de la suma de las 7 bandas, provenientes de la salida del ecualizador, podemos ver en la figura 1.60 que en primera instancia la señal tiene una respuesta plana, pero si detallamos en un rango entre +240 mdB y -420 mdB, podemos comprobar (figura 1.61) que el filtro no reproduce una respuesta totalmente plana. Esto se debe a las tolerancias de los componentes, al no ser exactamente los valores que marcan las ecuaciones teóricas, la respuesta cambia debido a esas pequeñas imperfecciones de fabricación.

Aunque podamos pensar que unas variaciones dentro del rango especificado en la figura 1.61, pueden tomarse como despreciables, los cálculos nos demuestran que si hay grandes incidencias en el audio final.

Si tomamos una entrada de 200 mVp y un auricular con 20 Ω de impedancia y 115 dB SPL/mW de sensibilidad:

- Calculamos el voltaje de salida tomando una ganancia en el ecualizador de -260 mV:

$$20\log_{10}\left(\frac{Vout}{100mV}\right) = -260mV$$

- Despejando de la ecuación anterior, obtenemos que el voltaje de salida será de 194 mVp. Con el valor del voltaje de salida, hallamos la potencia en la carga de 20 Ω.

$$P_{out} = \frac{Vp\ out^2}{2 * R} = \frac{0.194^2}{2 * 20\Omega} = 0.94\ mW$$

- Con el valor de la potencia y la sensibilidad se calcula el nivel de presión sonora que generara el auricular.

$$dB\ SPL = Sensibilidad * Pout = 115\frac{dB\ SPL}{mW} * 0.94mW = 108.1\ dB\ SPL$$

- Si realizamos el mismo procedimiento, pero suponiendo que la respuesta es plana y, por lo tanto, el voltaje de entrada y salida es el mismo, obtenemos un nivel de presión sonora de 115 dB SPL.

Tras realizar esta comprobación, podemos ver que la ausencia de respuesta plana, genera en este ejemplo una diferencia de 7 dB SPL entre el caso ideal y el real.

En el anexo V se adjuntan los barridos en frecuencia de cada banda de frecuencias. Con dichos barridos, se comprueba el buen funcionamiento de los filtros dado que, se verifica que la frecuencia de corte se encuentra a -6 dB. Se muestra un ejemplo a continuación:

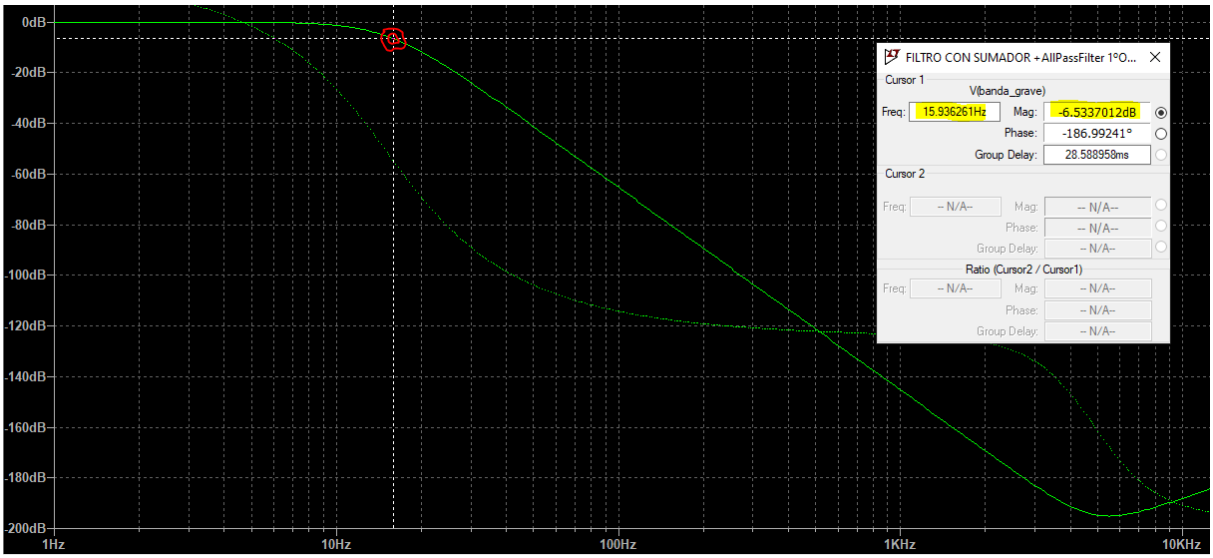


Figura 1.62: Barrido en frecuencia del filtro pasa bajas de 16 Hz. (frecuencia-dB) [28].

- Fase experimental:

Tras realizar un análisis mediante simiulaciones, se procedío a montar el diseño del ecualizador en una placa protoboard. Los operacionales empleados en el diseño físico fueron los modelos TL081, TL082 y TL084. Se decidió emplear dichos moldelos para compactar el diseño aorivechando que los modelos TL0XX vienen diseñados con 1, 2 o 4 operacionales en su interior.

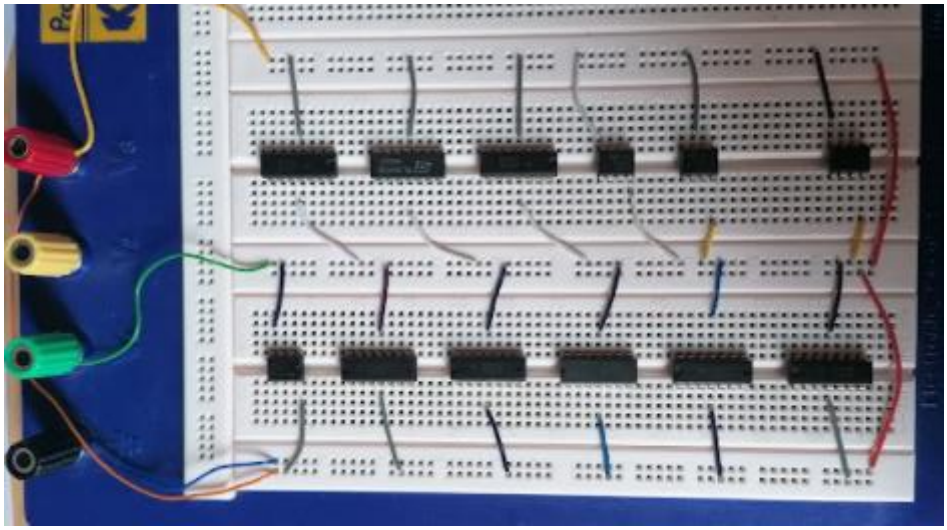


Figura 1.63: Disposición de operacionales en la protoboard [28].

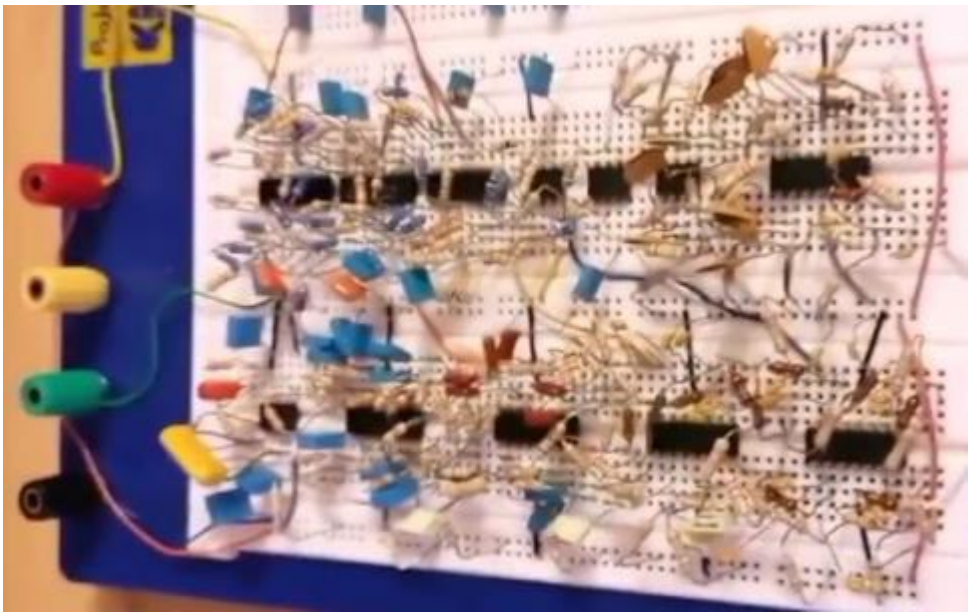


Figura 1.64: Disposición final de todos los componentes [28].

En el Anexo VI se recogen los barridos en frecuencia realizados al circuito mediante el programa LabView. En ellos se ve comprueba el correcto funcionamiento de todas las bandas del circuito.

Cabe destacar que al sumar las bandas y realizar un barrido en frecuencia, la respuesta no es totalmente plana debido a las variaciones entre componentes. En la figura 1.65, se observa el barrido nombrado anteriormente y es importante mencionar que la ausencia de la banda localizada entre los 10 y 100 Hz, la cual aparece cancelada en la figura, se puede deber a un error de procesado de señales del LabView. En la figura 1.66, se puede verificar, mediante el uso del osciloscopio, que la señal que aparece cancelada en el LabView, está presente.

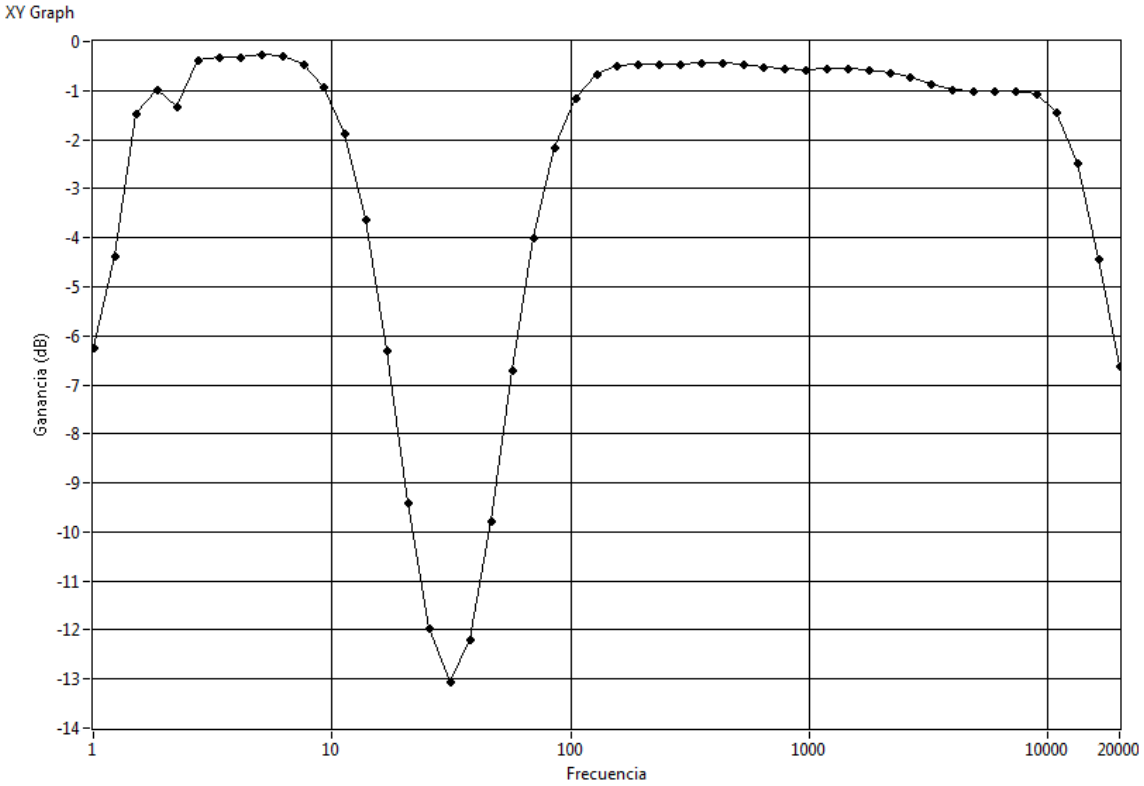


Figura 1.65: Barrido en frecuencia de la suma de las 7 bandas del ecualizador con LabView [28].

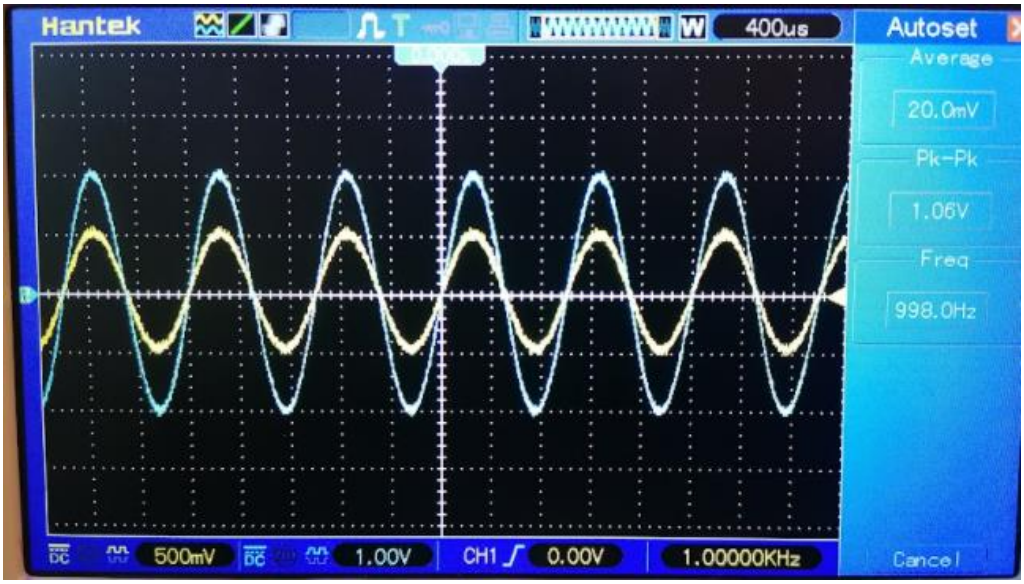


Figura 1.66: Comprobación de la banda cancelada en la figura 1.65 [28].

6.5 Preamplificador desbalanceado 2.

- **Descripción:**

A diferencia del circuito planteado para la implementación del preamplificador desbalanceado 1, el circuito del preamplificador desbalanceado 2 es un diseño más sencillo basado en un restador con ganancia unitaria. De ese modo se suma la señal de entrada 1 con la otra señal que está desfasada 180º, previamente invertida, y se obtiene una señal libre de ruidos y con el doble de amplitud.

No es necesario llevar a cabo un control del volumen regulado como en el caso de la señal de entrada 1, dado que, este canal se ha diseñado para que se conecte un dispositivo externo que ya tenga regulación de volumen propia.

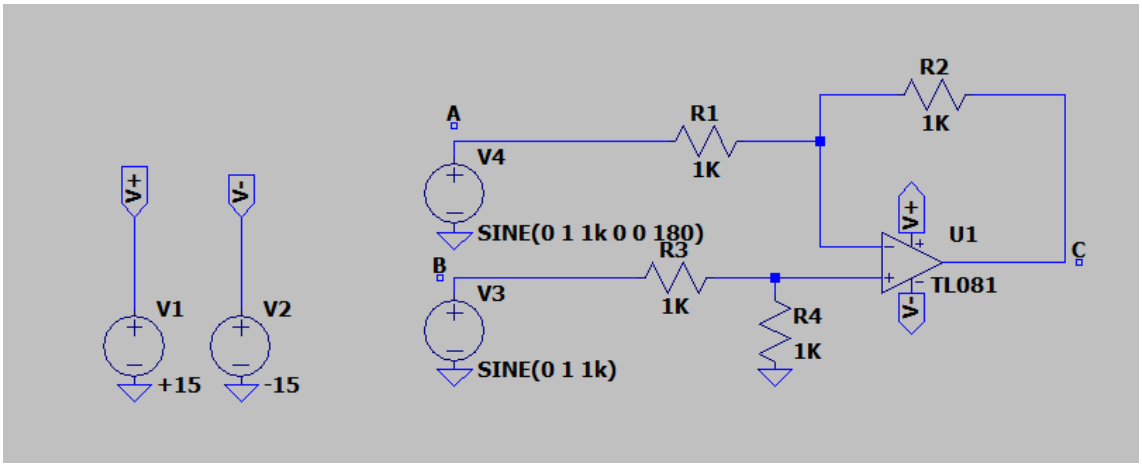


Figura 1.67: Implementación del circuito del preamplificador desbalanceado 2 [28].

- **Simulación:**

Una vez configuradas las fuentes de entrada con señales de 1 V a 1 kHz. Se procede a medir el voltaje en los puntos A, B y C.

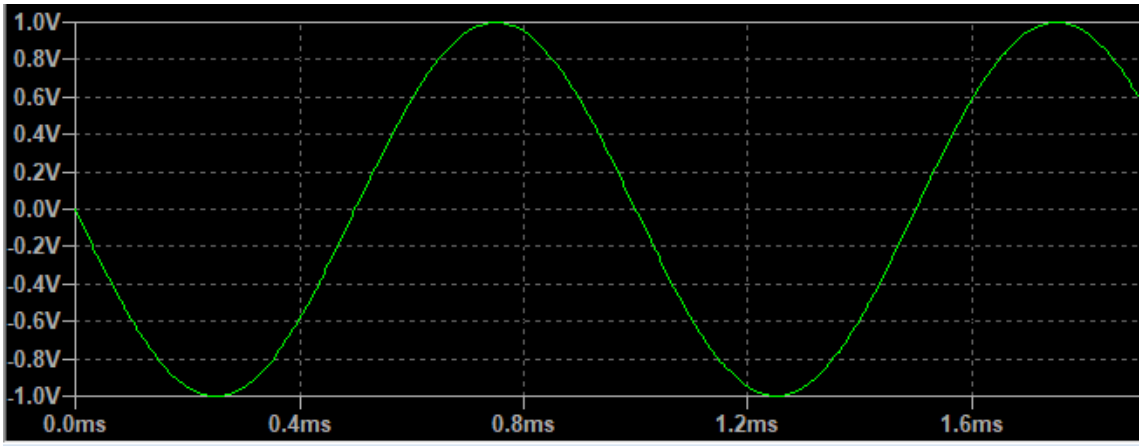


Figura 1.68: Comprobación de tensión en el punto A. (tiempo-voltaje) [28]

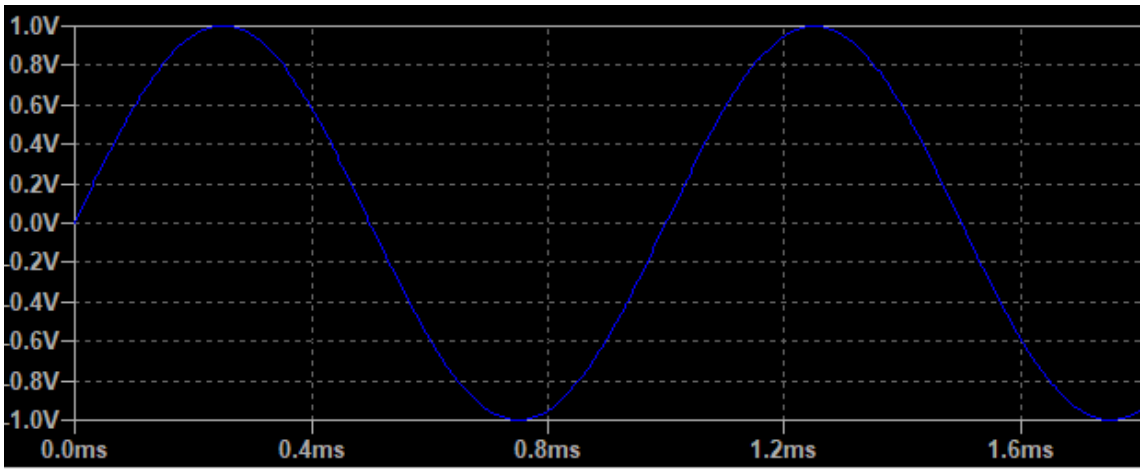


Figura 1.69: Comprobación de tensión en el punto B. (tiempo-voltaje) [28]

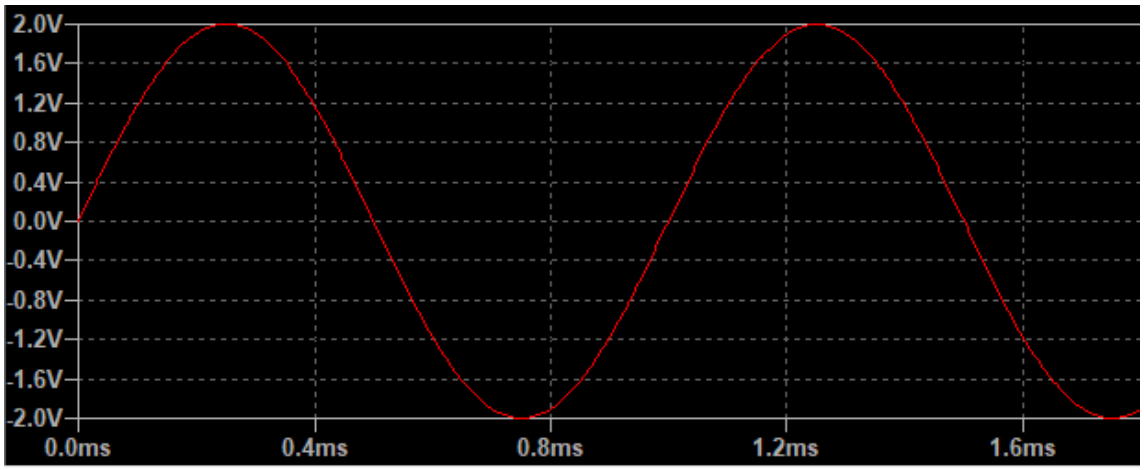


Figura 1.70: Comprobación de tensión en el punto C. (tiempo-voltaje) [28]

Una vez tomadas las medidas en los puntos del circuito, se comprueba el correcto funcionamiento del mismo porque en el punto C se mide el doble del voltaje de entrada.

6.6 Sumador de potencia.

- **Descripción:**

Este bloque funcional es el encargado de sumar la señal procesada, origen de la entrada 1, y la señal asociada a la entrada 2.

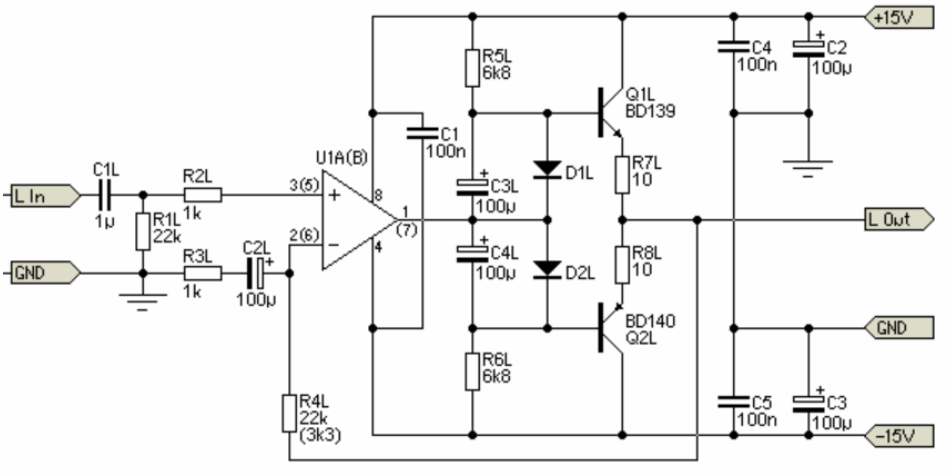


Figura 1.71: Diseño del amplificador de auriculares de Rod Elliott © 2005. [18]

Como se puede ver en la figura 1.71, el circuito una atapa AB realimentada en la que se emplea una ganancia en el lazo de realimentación. A partir del diseño de Rod Elliott, se ha optado por añadir una sumador en la entrada y modificar la ganancia para que sea unitaria. De este modo es podrán sumar las señales provenientes de la entrada 1 y 2, y además se podrán suministrar la corriente que precise la carga sin temer por dañar todos los bloques anteriores, ya que, será este bloque funcional el encargado de soportar las solicitaciones de carga.

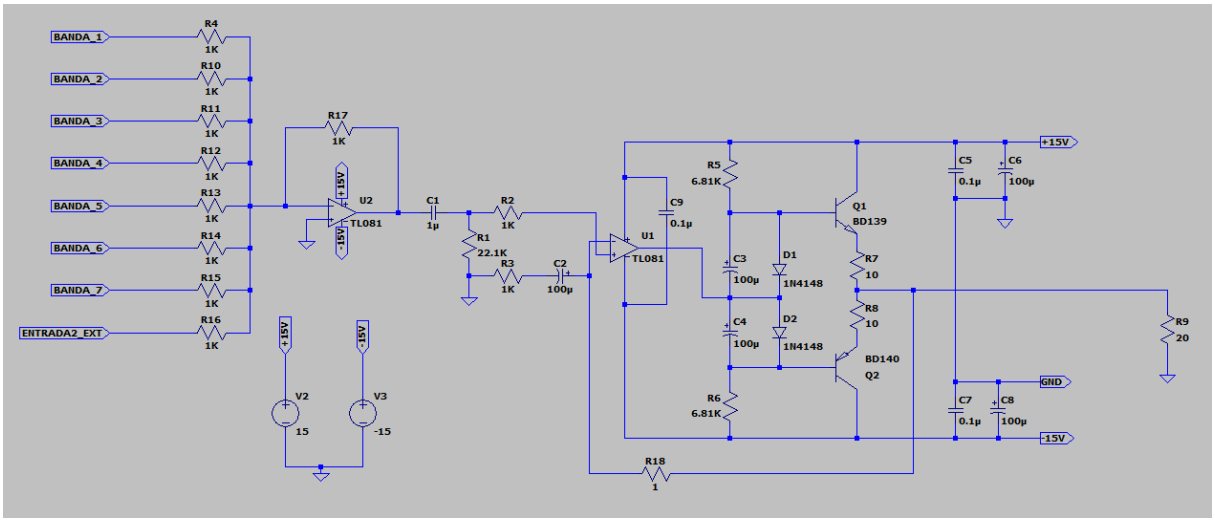


Figura 1.72: Diseño del sumador de potencia [28].

En el Anexo VII se muestra el cálculo de la función de transferencia del lazo de realimentación de la figura 1.72.

6.7 Control de volumen:

Este bloque funcional, se centra en habilitar un sistema de corte de emergencia que entrará en servicio en caso de que se superen los 100 dB SPL en la salida del sistema. La estrucutura del circuito se detalla a continuación:

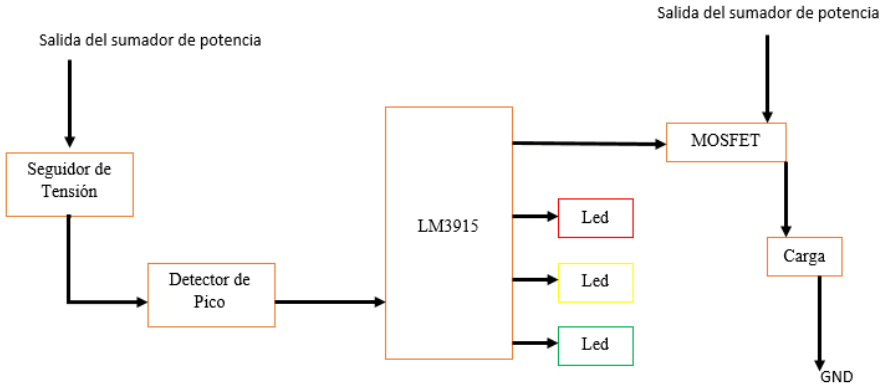


Figura 73: Estructura del circuito de control de volumen [28].

Para controlar el nivel sonoro se ha optado por la implementación de un detector de pico, diseñado por Rod Elliott, para registrar el voltaje máximo de la señal, utilizando un seguidor de tensión para tomar una muestra de la señal de salida antes de la conexión a la carga. Mediante el uso del integrado LM3915 podemos comparar el valor máximo con un valor de amplitud de referencia generado por el propio integrado. El LM3915 habilitará varias salidas en las que se colocarán leds de colores (verde, amarillo y rojo) para avisar al usuario de que se está alcanzando el nivel sonoro crítico, especificado por la normativa europea. Cuando se alcance el voltaje máximo asociado con la emisión de los 100 dB SPL, un MOSFET de canal N y conmutación rápida, entrará en la región de corte para evitar una exposición a niveles sonoros altos. El MOSFET se colocará entre el sumador de potencia y la conexión de la carga a la salida del sistema.

Una desventaja de este bloque funcional es la dependencia a un dispositivo de salida fijo, dado que una vez se diseñe el circuito y se ajuste un valor de referencia en el LM3915, no se podrá variar la impedancia de la carga a conectar dado que, en ese caso, el voltaje de referencia ajustado en el LM3915 deberá ser otro para realizar el corte de suministro de señal a los 100 dB SPL.

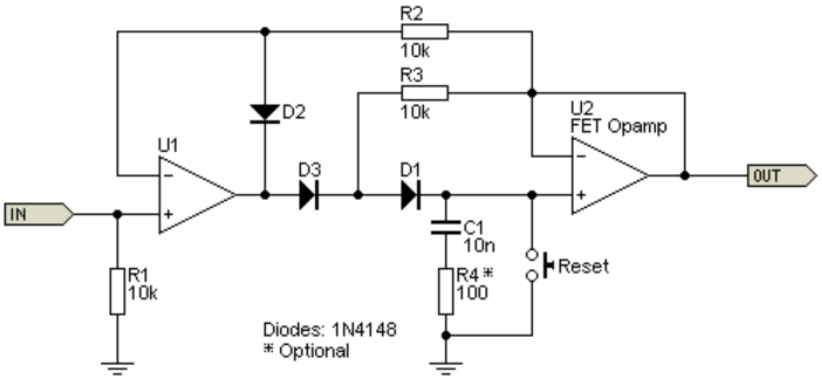


Figura 1.74: Diseño del detector de pico de Rod Elliott © 2017. [17]

Según Rodd Elliott: “El diodo (D2) asegura que la salida del operacional no pueda oscilar por debajo del voltaje de entrada negativo, lo que mejora la velocidad del detector y minimiza el voltaje a través del diodo de detección de pico (D1). Esto ayuda a reducir la corriente de fuga inversa. Durante el período de retención, existe el mismo voltaje en ambos extremos del D1. En esa condición, no puede haber fugas a través del diodo y un 1N4148 funcionará perfectamente incluso con varios segundos de retención. La combinación que se muestra de 10 nF y 100 Ω permite capturar con precisión un pulso de 5 µs o más, pero esto depende de los amplificadores operacionales utilizados y debe optimizarse para satisfacer sus necesidades. No se espera de este circuito una alta precisión con altas frecuencias, a no ser que se utilicen operacionales rápidos.” [17]

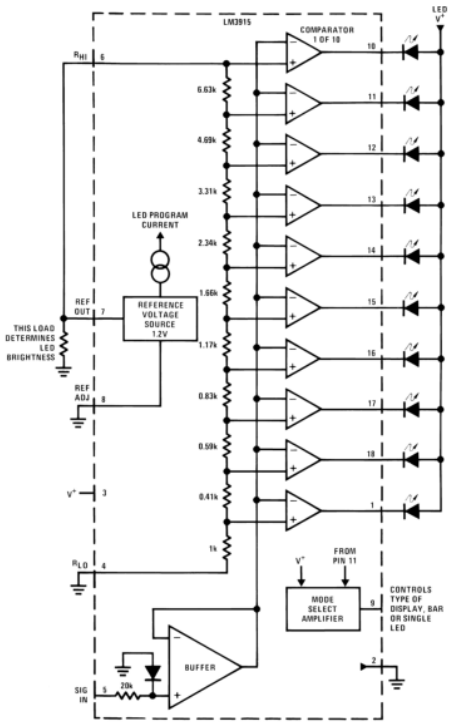


Figura 1.75: Esquema interno del integrado LM3915. [19]

Para el ajuste del voltaje de referencia se tomará como dispositivo de salida a conectar, unos auriculares con una impedancia de 20 Ω y una sensibilidad de 115 dB SPL/mW. Teniendo esto en cuenta, el voltaje asociado a la emisión de 100 dB SPL se asocia a un voltaje de 186.5 mV.

Tras revisar los métodos de cálculo del voltaje de referencia incluidos en el *datasheet* del LM3915, procedemos a realizar el cálculo.

Partiendo de la idea de conectar un led a cada comparador, el *datasheet* dice que la corriente entregada por cada comparador será del orden de 10 veces la Iref del integrado. Teniendo esto en cuenta y sabiendo que el voltaje de referencia debe ser 186.5 mV, y que se quiere diseñar el sistema para exista un corriente de salida de 10 mA en la salida del operacional, se debe seguir la siguiente disposición:

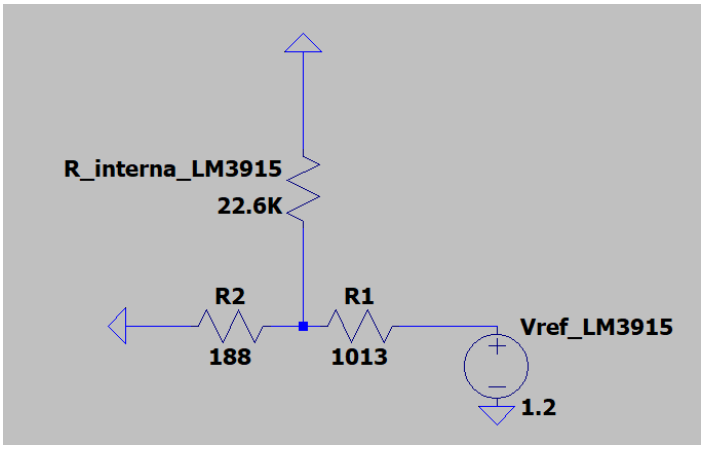


Figura 1.76: Diseño del voltaje de referencia del LM3915. [19]

Por otra parte, el integrado consta de dos modos de funcionamiento configurables en el pin 9. El modo punto, en el que solo un led se enciende en cada vez (pin 9 al aire) y el modo barra en el que los leds se irán encendiendo manteniendo los anteriores encendidos (pin 9 conectado a la alimentación). De los dos modos de funcionamiento se debe configurar el modo barra.

7. Implementación en PCB.

- **Ecualizador de 7 bandas con sumador:**

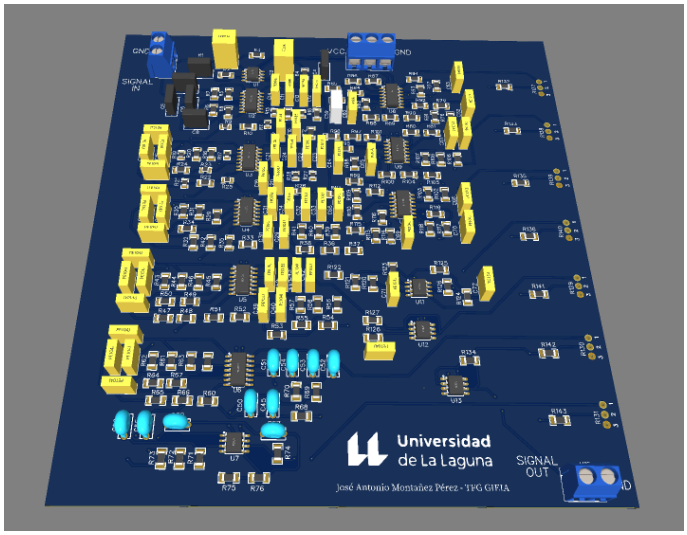


Figura 1.77: PCB del ecualizador de 7 bandas con un sumador [28]

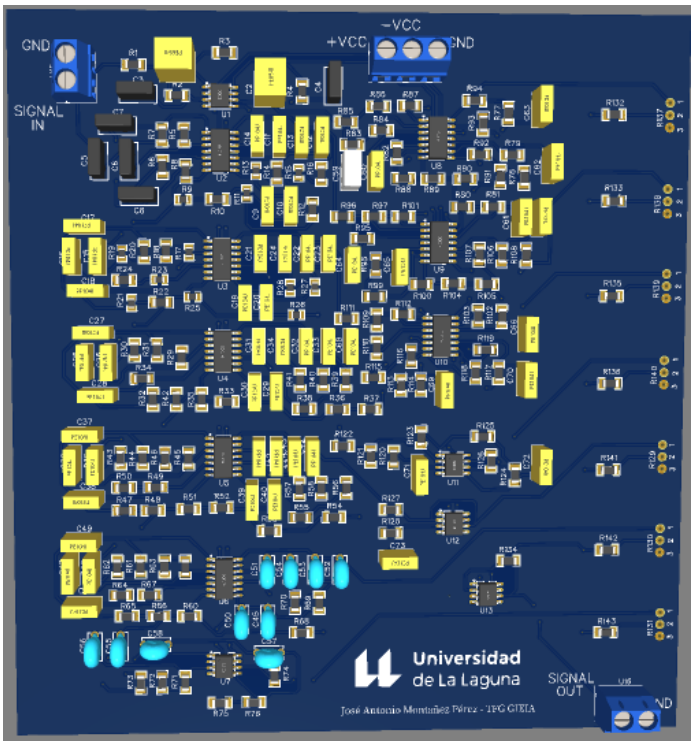


Figura 1.78: PCB del ecualizador de 7 bandas con un sumador [28]

8. Conclusion- Conclusión.

Approaching a design from an analog point of view, without employing any digital input, represents a very involved job. It has been shown that in the field of audio processing a slight variation of the tolerances in the components, in the design of the PCB itself or breadboards, or simply, a component made of another material, can make the design of the device very difficult.

From the point of view of the efficiency, some functional blocks could be implemented digitally.

On the other hand, in the equalizer block, the dependence between analog electronics and large systems was clearly seen. Even using components with SMD technology, the size of the designed PCB is too large compared to other digital designs.

It is also important to emphasize the importance of knowing and mastering the diagnosis of PCBs or breadboards. A bad contact can take hours of work to find the solution.

Last but not least, the regulatory limitations established by law must always be taken into account, both in the marketing phases and in the design phases.

Abordar un diseño desde un punto de vista analógico, sin emplear ninguna entrada digital, representa un trabajo muy complicado. Se ha demostrado que en el campo del procesamiento de audio una ligera variación de las tolerancias en los componentes, en el diseño de la propia PCB o protoboards, o simplemente, un componente fabricado en otro material, puede dificultar mucho el diseño del dispositivo.

Desde el punto de vista de la eficiencia, algunos bloques funcionales podrían implementarse digitalmente.

Por otro lado, en el bloque del ecualizador, se vio claramente la dependencia entre la electrónica analógica y los grandes sistemas. Incluso utilizando componentes con tecnología SMD, el tamaño de la PCB diseñada es demasiado grande en comparación con otros diseños digitales.

También es importante enfatizar la importancia de conocer y dominar el diagnóstico de PCB o protoboards. Un mal contacto puede llevar horas de trabajo para encontrar la solución.

Por último, pero no menos importante, siempre se deben tener en cuenta las limitaciones normativas que establece la ley, tanto en las fases de marketing como en las fases de diseño.

9. Bibliografía.

[1] Tecnológico Nacional de México Campus Laguna, "Filtros activos", Ingeniería de Sistemas. [En línea]. Disponible en: http://www.itlalaguna.edu.mx/2014/Oferta%20Educativa/Ingenierias/Sistemas/Plan%201997-2004/Ecabas/ecabaspdf/FILTROS%20ACTIVOS.pdf

[2] A.R. Hambley, *Electrónica,* 2º Edición, 2001.

[3] Universitas Miguel Hernández, "Diseño de filtros analógicos", Circuitos electrónicos analógicos. [En línea]. Disponible en:https://sites.google.com/a/goumh.umh.es/circuitos-electronicos-analogicos/transparencias/tema-2#TOC-Introducci-n

[4] Universidad de Burgos, "Filtrado", Instrumentación electrónica, Área de tecnología electrónica. [En línea]. Disponibles en: https://www3.ubu.es/ingelec/tecelec/inaki/Instelec/docsinstrum/Apuntes/06-FILTRADO_%20v5-8PW.pdf

[5] Texas Instrumens, "Analysis of the sallen-key architecture", Application report. [En línea]. Disponible en: http://www.ti.com/lit/an/sloa024b/sloa024b.pdf

[6] W.G. Jung, *Op Amp applications handbook,* Elsevier, 2005.

[7] ResearchGate, "Gráfica de respuesta de un filtro pasa-alta". [En línea]. Disponible en: https://www.researchgate.net/figure/Frequency-response-of-an-all-pass-filter-configuration_fig4_308266042

[8] R. Elliot, "Active Filters - Characteristics, Topologies and Examples", *Elliott Sound Products,* [En línea]. Disponible en: https://sound-au.com/articles/active-filters.htm#s1

[9] P. Rosero Montalvo, "Diseño de filtros 2", Circuitos Analógicos Digitales. [En línea]. Disponible en: http://www.paulrosero-montalvo.com/gallery/dise%C3%B1o%20de%20filtros%202.pdf

[10] Aula Actual, "El ecualizador – qué es y cómo funciona", [En línea]. Disponible en:https://www.aulaactual.com/el-ecualizador-que-es-y-como-funciona/

[11] R. Elliot, "48V Phantom Feed Supply for Microphones", *Elliott Sound Products,* [En línea]. Disponible en: https://sound-au.com/project96.htm

[12] R. Elliot, "Ultra-Simple Microphone Preamplifier", *Elliott Sound Products,* [En línea]. Disponible en: https://sound-au.com/project122.htm

[13] Universidad de Granada, "Medidas del ruido". [En línea]. Disponible en:https://www.ugr.es/~ramosr/CAMINOS/conceptos_ruido.pdf

[14] ThermaXX Jackets, "Sound Pressure Math Made Easy", Niveles sonoros y conversiones de presión. [En línea]. Disponible en: https://www.thermaxxjackets.com/sound-pressure-math/

[15] Universidad Nacional de Rosario,"Niveles Sonoros" Facultad de ciencias exactas, ingeniería y agrimensura. [En línea]. Disponible en: https://www.fceia.unr.edu.ar/acustica/comite/niveles.htm

[16] Linkiwtz Lab, "Issues in loudspeaker design – 5", Crossover topology issues. [En línea]. Disponible en: https://www.linkwitzlab.com/frontiers_5.htm#V

[17] R. Elliot, "Peak Detection Circuits", *Elliott Sound Products,* [En línea]. Disponible en: https://sound-au.com/appnotes/an014.htm

18] R. Elliot, "Headphone Amplifier", *Elliott Sound Products,* [En línea]. Disponible en: https://sound-au.com/project113.htm

[19] Mouser, "Datasheet LM3915", Texas Instruments, [En línea]. Disponible en: https://www.mouser.com/datasheet/2/405/lm3915-443929.pdf

[20] Wikipedia, "Filtro paso-alto", [En línea]. Disponible en: https://es.wikipedia.org/wiki/Filtro_paso_alto

[21] Electrónica en general, "Instrumentación: filtros activos", [En línea]. Disponible en: https://electronicaengeneral.wordpress.com/2015/04/12/instrumentacion-filtros-activos/]

[22] S. Franco, "*Design with operational amplifiers and analog integrated circuits*", 3º Edición, 2012.

[23] Wikipedia, "Filtro paso-todo", [En línea]. Disponible en:https://en.wikipedia.org/wiki/All-pass_filter

[25] Universidad de Valladolid, "Análisis, diseño y caracterización de filtros activos implementados mediante el circuito integrado UAF42", Trabajo de Fin de Grado. [En línea]. Disponible en: https://www.google.com/url?sa=i&url=https%3A%2F%2Fuvadoc.uva.es%2Fbitstream%2F10324%2F33055%2F1%2FTFG-G3428.pdf&psig=AOvVaw32xoNgVqYxLWHsotRHLHnB&ust=1631448159198000&source=images&cd=vfe&ved=0CA0Q3YkBahcKEwiwp7Gi8PbyAhUAAAAAHQAAAAAQAw

[26] Electrónica, "Efecto del tipo de condensador en un circuito de filtro activo", [En línea]. Disponible en: https://electronica.guru/questions/44801/efecto-del-tipo-de-condensador-en-un-circuito-de-filtro-acti

[27] Universidad de las Palmas de Gran Canaria, "Filtros activos", [En línea]. Disponible en: https://www2.ulpgc.es/hege/almacen/download/29/29861/filtros.pdf

[28] Material de elaboración propia.

[29] Wilaeba Electronica, "Filtro Rechaza banda Activo de 2do Orden RC", [En línea]. Disponible en: https://wilaebaelectronica.blogspot.com/2017/11/filtro-rechaza-banda-activo-de-2do-orden-rc.html

[30] Universidad de las Palmas de Gran Canaria, "Filtros activos", [En línea]. Disponible en: https://www2.ulpgc.es/hege/almacen/download/29/29861/filtros.pdf

[31] Universitas Miguel Hernández, "Diseño de filtros por el método de la aproximación.", Análisis de Circuitos y Sistemas Lineales. [En línea]. Disponible en:

https://repositorio.innovacionumh.es/Proyectos/P_19/Tema_5/UMH_06.htm

[32] Thomann, "Imagen del MA Ligh-ting grandMA3 onPC Fader Wing", [En línea]. Disponible en: https://www.thomann.de/es/ma_lighting_grandma3_onpc_fader_wing.htm?glp=1&gclid=Cj0KCQjw4eaJBhDMARIsANhrQABFvHqs0trIrsu3ShMuGpjRmcntmh-4lfQKvp5u2cJAmZO5JaZ_AMYaAm6xEALw_wcB

[33] Thomann, "Golden Age Pro-ject EQ-81 MKIII", [En línea]. Disponible en https://www.thomann.de/es/golden_age_project_eq_81_mkiii.htm?glp=1&gclid=Cj0KCQjw4eaJBhDMARIsANhrQAAwPSkMihJdwxjU0edovqPRJP78DRs8UUyfHLjEpBceJoLbs8UuS8EaAoH8EALw_wcB

[34] Google Sites, "Ecualizador semiparametrico", [En línea]. Disponible en: https://sites.google.com/site/megafoniaysonorizacionronald/t05-equipos-de-tratamiento-de-la-senal-de-audio/5-2-ecualizadores/5-2-4-ecualizador-semiparametrico

[35] Universidad de Cantabria, "Amplificadores de Potencia", [En línea]. Disponible en: https://www.ctr.unican.es/asignaturas/instrumentacion_5_IT/IEC_5.pdf

[36] J. Pleite Guerra, "*Electrónica para Ingenieros*", McGraw-Hill, 2009.

[37] A.S.Sedra, "*Circuitos Microelectrónicos*", Oxford, 2000.

[38] Electrónica Lugo, "Amplificador de Potencia", [En línea]. Disponible en: https://electronicalugo.com/que-es-un-amplificador-de-potencia-tipos-clases-y-aplicaciones/

[39] Electrónica Lugo, "Amplificador de Potencia", [En línea]. Disponible en: https://electronicalugo.com/que-es-un-amplificador-de-potencia-tipos-clases-y-aplicaciones/

[40] Alfredo de Río Vazquez, "Amplificadores de Potencia", [En línea]. Disponible en: http://ario.webs.uvigo.es/docencia/eangrado/EAN_GRADO_P5.pdf

[41] Neuroreille, "Viaje al mundo de la audición", [En línea]. Disponible en: http://www.cochlea.org/es/ruido

[42] Universidad Politécnica de Madrid,"Duplicar la intensidad del sonido", Grupo de investigación en instrumentación y acústica aplicada [En línea]. Disponible en: http://www.i2a2.upm.es/faq-items/duplicar-la-intensidad-de-un-sonido/

[43] J. M. Merino, "La percepción acústica: Tono y timbre", [En línea]. Disponible en: https://dialnet.unirioja.es/descarga/articulo/4458407.pdf

[44] ISP music and producer, "Delay: Controlando los milisegundos", [En línea]. Disponible en: https://www.ispmusica.com/foros-ispmusica/didactica-guitarra/2295-delay-controlando-los-milisegundos.html

[45] Musicopolix, "Tipos de micrófonos", [En línea]. Disponible en:

https://musicopolix.com/blog/2015/04/16/que-microfono-comprar-4-tipos-de-microfonos/

[46] Musicopolix, "Tipos de micrófonos", [En línea]. Disponible en:

https://musicopolix.com/blog/2015/04/16/que-microfono-comprar-4-tipos-de-microfonos/

[47] Thomann, “Materiales de audio”, imágenes de catálogo, [En línea]. Disponible en: https://www.thomann.de/es/index.html

[48]Blog LANDR, “Cables de Audio”, [En línea]. Disponible en: https://blog.landr.com/es/cables-de-audio-todo-lo-que-necesitas-saber-sobre-los-tipos-de-cables-de-audio-infografia/

[49] Wikipedia, “XLR-3”, [En línea]. Disponible en: https://es.wikipedia.org/wiki/XLR-3

[50]Sonido Madrid, “Conecto XLR”, [En línea]. Disponible en: https://www.alquilersonidomadrid.net/conector-xlr

[51] Foro Auriculares.org, “Cables artesanales. Pruebas y experiencias”, [En línea]. Disponible en: https://www.auriculares.org/foro/index.php?topic=7990.375

[52] Clark WireAndCable, “1/4" Phone - 2 Circuits/TS”, [En línea]. Disponible en: http://www.clarkwire.com/PinOut14TwoCircuit.htm

[53] Hispasonic, “El MIDI sobre jack TRS por fin se hace estándar”, [En línea]. Disponible en: https://www.hispasonic.com/noticias/midi-jack-trs-estandar/43930

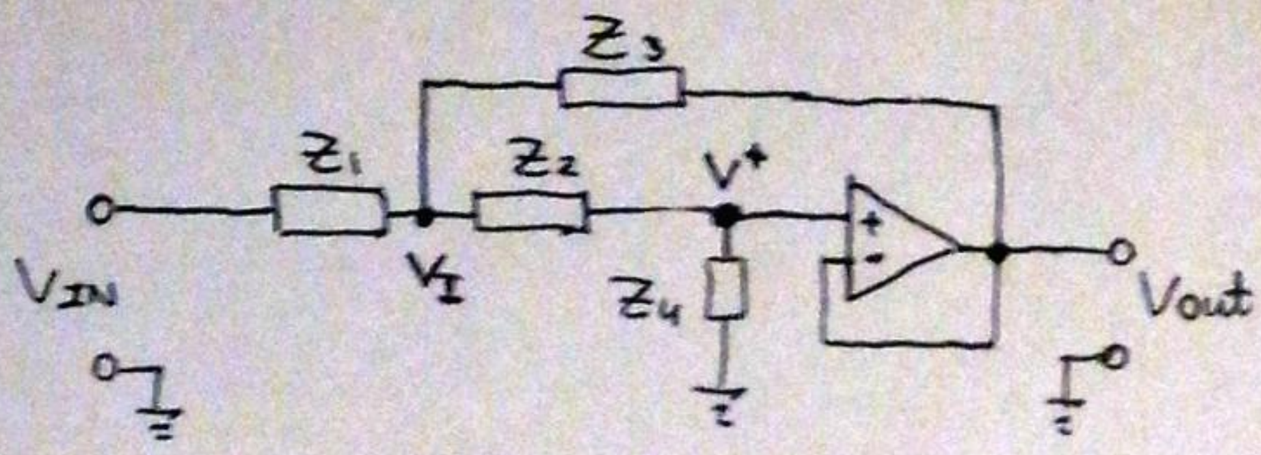
[54]CableMatic, “Cable midi de 5 pines”, [En línea]. Disponible en: https://cablematic.com/es/productos/cable-midi-de-5-pines-macho-a-hembra-1-m-MI112/

[55]Producciones El Sótano, “La Alimentación Phantom”, [En línea]. Disponible en: https://www.produccioneselsotano.com/la-alimentacion-phantom/#:~:text=Podr%C3%ADamos%20definir%20la%20alimentaci%C3%B3n%20phantom,transportan%20las%20se%C3%B1ales%20de%20audio.

10. Anexos.

- Anexo I. Función de transferencia genérica de la tipología Sallen Key.
- Anexo II. Resultados de los componentes para los filtros pasa-bajas del ecualizador
- Anexo III. Resultados de los componentes para los filtros pasa-altas del ecualizador.
- Anexo IV. Resultados de los componentes para los filtros pasa-todo del ecualizador.
- Anexo V. Barridos en frecuencia en etapa de simulación.
- Anexo VI. Barridos en frecuencia en etapa de experimentación.
- Anexo VII. Función de transferencia del lazo de realimentación del sumador de potencia.
- Anexo VIII. Función de transferencia del filtro pasa-todo.
- Anexo IX. *Datasheet* del TL081.
- Anexo X. *Datasheet* del TL082.
- Anexo XI. *Datasheet* del TL084.
- Anexo XII. *Datasheet* del LM3915.

Anexo I.
Función de transferencia genérica de la tipología sallen key.



$$\frac{V_{IN}-V_I}{Z_1}=\frac{V_I-V_{out}}{Z_3}+\frac{V_I-V^+}{Z_2}\ (1) \quad \Big| \quad \frac{V_I-V^+}{Z_2}=\frac{V^+}{Z_4}\ (2) \quad \Big| \quad V^+=V^-=V_{out}\ (3)$$

(2) (3) $\quad \frac{V_I-V_{out}}{Z_2}=\frac{V_{out}}{Z_4} \rightarrow V_I=V_{out}\left(\frac{Z_2}{Z_4}+1\right)$ (4)

(1) (4) $\quad \frac{V_{IN}-\frac{V_{out}Z_2}{Z_4}-V_{out}}{Z_1}=\frac{\frac{V_{out}Z_2}{Z_4}}{Z_3}+\frac{\frac{V_{out}Z_2}{Z_4}}{Z_2}$

$$V_{IN}=Z_1\left(V_{out}\frac{Z_2}{Z_4Z_3}+V_{out}\frac{Z_2}{Z_4Z_2}\right)+V_{out}+V_{out}\frac{Z_2}{Z_4}$$

$$V_{IN}=V_{out}\left(\frac{Z_1Z_2}{Z_4Z_3}+\frac{Z_1}{Z_4}+1+\frac{Z_2}{Z_4}\right)$$

$$V_{IN}=V_{out}\cdot\left(\frac{Z_1Z_2+Z_1Z_3+Z_4Z_3+Z_2Z_3}{Z_4Z_3}\right)$$

$$\boxed{G(S)=\frac{V_{out}}{V_{IN}}=\frac{Z_4Z_3}{Z_1(Z_2+Z_3)+Z_3(Z_4+Z_2)}}$$

Filtro Pasa-Bajas

$Z_1=R_1$

$Z_2=R_2$

$Z_3=\frac{1}{j\omega C_1}$

$Z_4=\frac{1}{j\omega C_2}$

Filtro Pasa - Altas

$Z_1=\frac{1}{j\omega C_1}$

$Z_2=\frac{1}{j\omega C_2}$

$Z_3=R_1$

$Z_4=R_2$

Anexo II.
Resultados de los componentes para los filtros pasa-bajas del ecualizador

10K-100K

frecuencia (Hz)	m*	R* (Ω)	Q	C*	n*	C2(COMERCIAL) (F)	C1* (F)
16	1	22000	0,71	3,18412E-07	2	3,30E-07	6,60E-07
63	1	27000	0,71	6,58912E-08	2	6,80E-08	1,36E-07
250	1	27000	0,71	1,66046E-08	2	1,80E-08	3,60E-08
1000	1	33000	0,71	3,39639E-09	2	3,30E-09	6,60E-09
4000	1	27000	0,71	1,03779E-09	2	1,00E-09	2,00E-09
16000	1	51000	0,71	1,37354E-10	2	1,20E-10	2,40E-10

PASO BAJO							
C1(COMERCIAL) (F)	n	k	m	R2 (Ω)	R1 (Ω)	R1(COMERCIAL) (Ω)	R2(COMERCIAL) (Ω)
6,80E-07	2,00	1,967466772	1	21314,31	21314,3067	22000	22000
1,36E-07	2,00	1,967466772	1	26269,7338	26269,7338	25900	25900
3,60E-08	2,00	1,967466772	1	25008,7866	25008,7866	25020	25020
6,60E-09	2,00	1,967466772	1	34102,8908	34102,8908	34100	34100
2,00E-09	2,00	1,967466772	1	28134,8849	28134,8849	28100	28100
2,40E-10	2,00	1,967466772	1	58614,3435	58614,3435	59000	59000

Anexo III.
Resultados de los componentes para los filtros pasa-altas del ecualizador

1k-1M C1=C2

PASO ALTO							
frecuencia (Hz)	n	R* (Ω)	Q	C* (F)	m	C1(COMERCIAL) (F)	R1 (Ω)
16	1	22000	0,71	3,18412E-07	2	3,30E-07	21314,31
63	1	27000	0,71	6,58912E-08	2	6,80E-08	26269,73378
250	1	27000	0,71	1,66046E-08	2	3,30E-08	13641,16
1000	1	33000	0,71	3,39639E-09	2	3,30E-09	34102,89
4000	1	27000	0,71	1,03779E-09	2	1,00E-09	28134,88
16000	1	51000	0,71	1,37354E-10	2	1,20E-10	58614,34

R1(COMERCIAL) (Ω)	R2 (Ω)	R2(COMERCIAL) (Ω	C (LAB) (F)
22000	42628,6135	42900	390n
25900	52539,4676	52600	100n
13800	27282,3126	27000	27n
34100	68205,7815	68220	6,8n
28100	56269,7698	56220	1,5n
59000	117228,687	118000	0,39n

Anexo IV.
Resultados de los componentes para los filtros pasa-todo del ecualizador.

	1ºorden				
	fc (Hz)	R (Ω)	R1 (Ω)	C1 (F)	C1 (COMERCIAL) (F)
1	42,18	1000	17200	2,1938E-07	2,20E-07
2	168,95	1000	34800	2,70697E-08	2,70E-08
3	668,89	1000	23800	9,99743E-09	1,00E-08
4	2674,85	1000	39680	1,49951E-09	1,50E-09
5	10711,77	1000	10000	1,4858E-09	1,50E-09

fc del Ecualizador(Hz)	desfase (º)
15,77	41
63,17	41
250,09	41
1000,08	41
4004,97	41

5% para R

desfase (rad)	fo (Hz)
0,715584993	42,17878096
0,715584993	168,9496359
0,715584993	668,8903807
0,715584993	2674,84823
0,715584993	10711,76766

Anexo V.
Barridos en frecuencia en etapa de simulación.

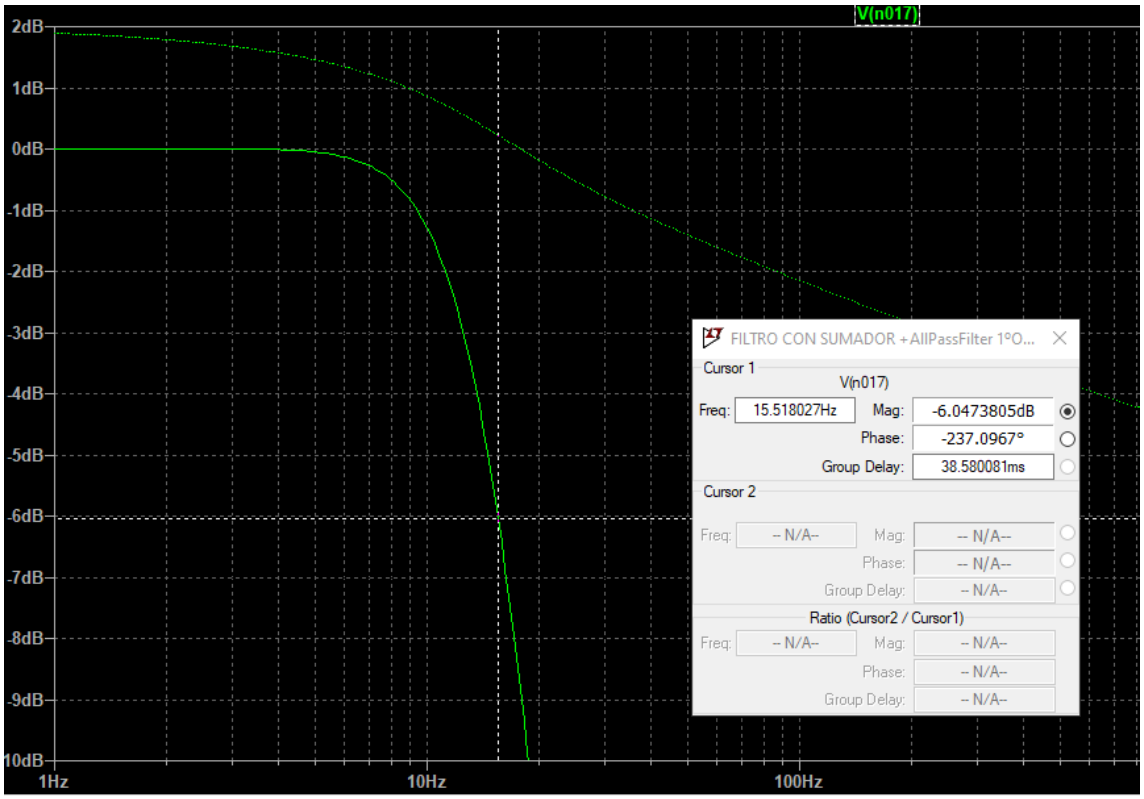


Figura 79: Barriendo en frecuencia de la banda 1 del ecualizador. [28]

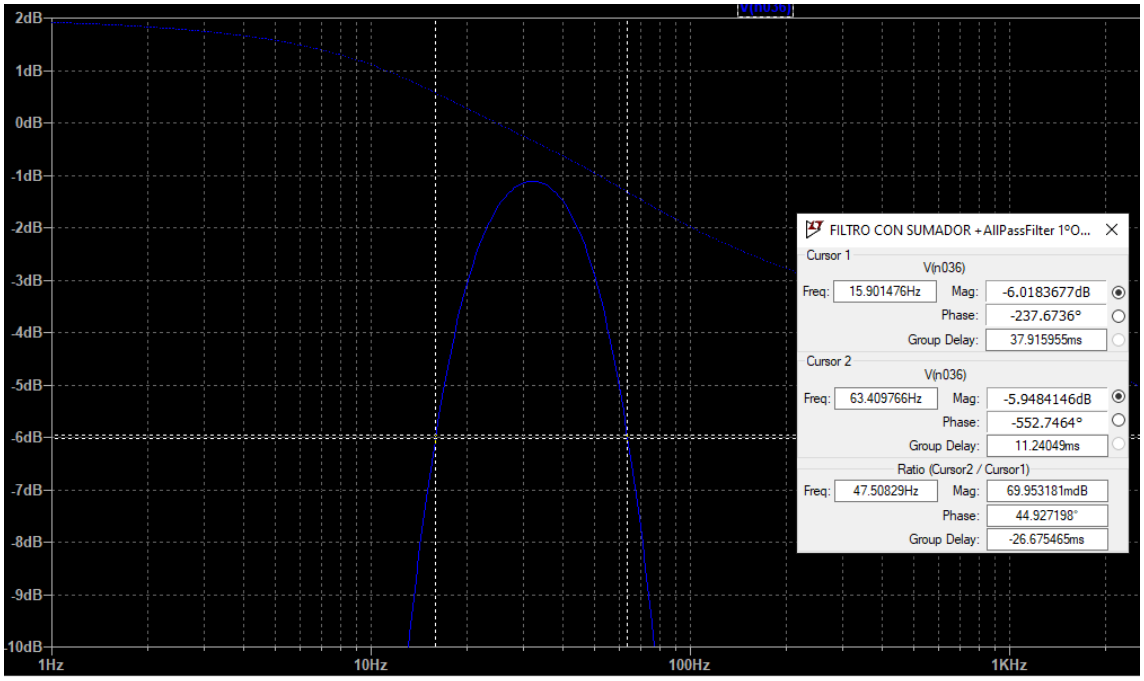


Figura 80: Barriendo en frecuencia de la banda 1 del ecualizador. [28]

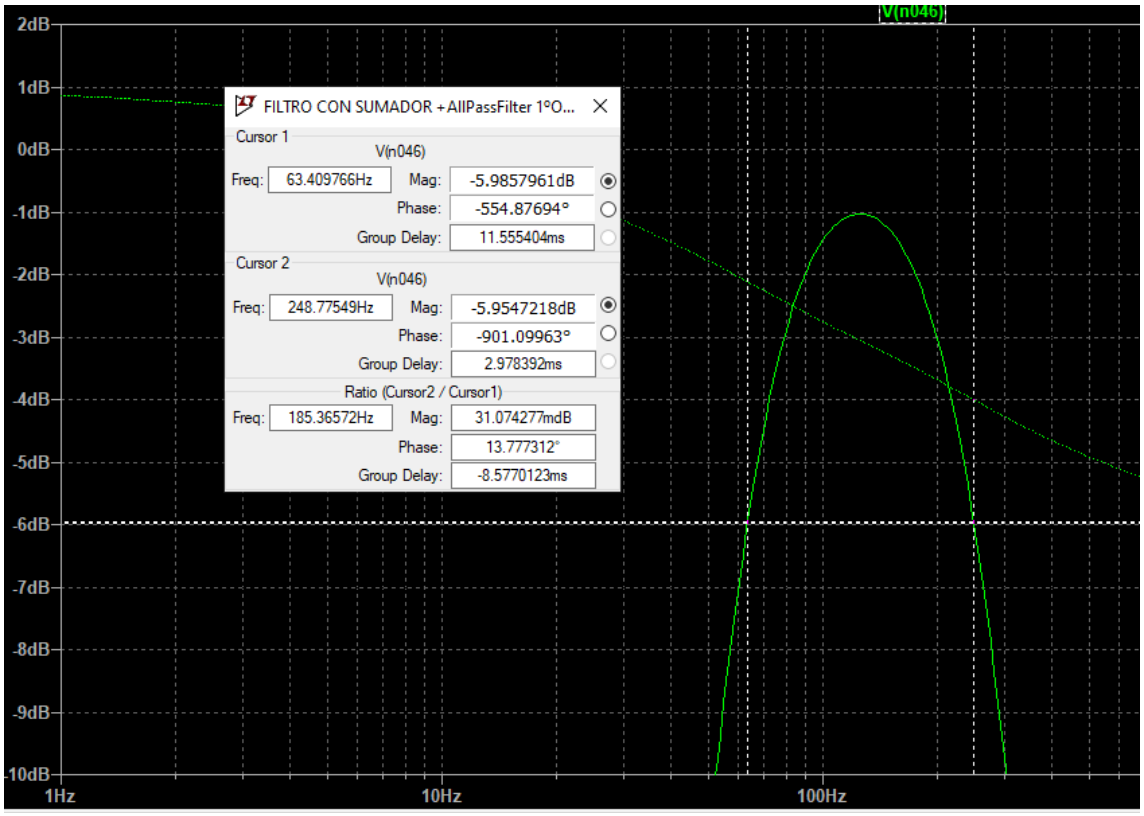


Figura 81: Barriendo en frecuencia de la banda 1 del ecualizador. [28]

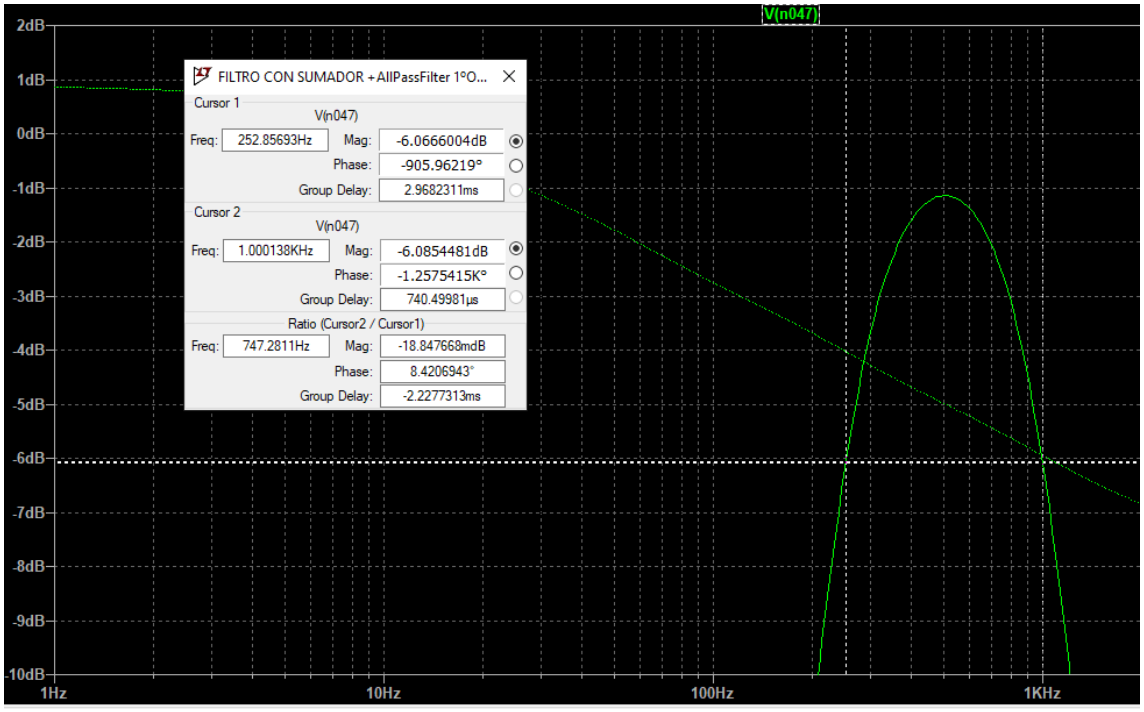


Figura 82: Barriendo en frecuencia de la banda 1 del ecualizador. [28]

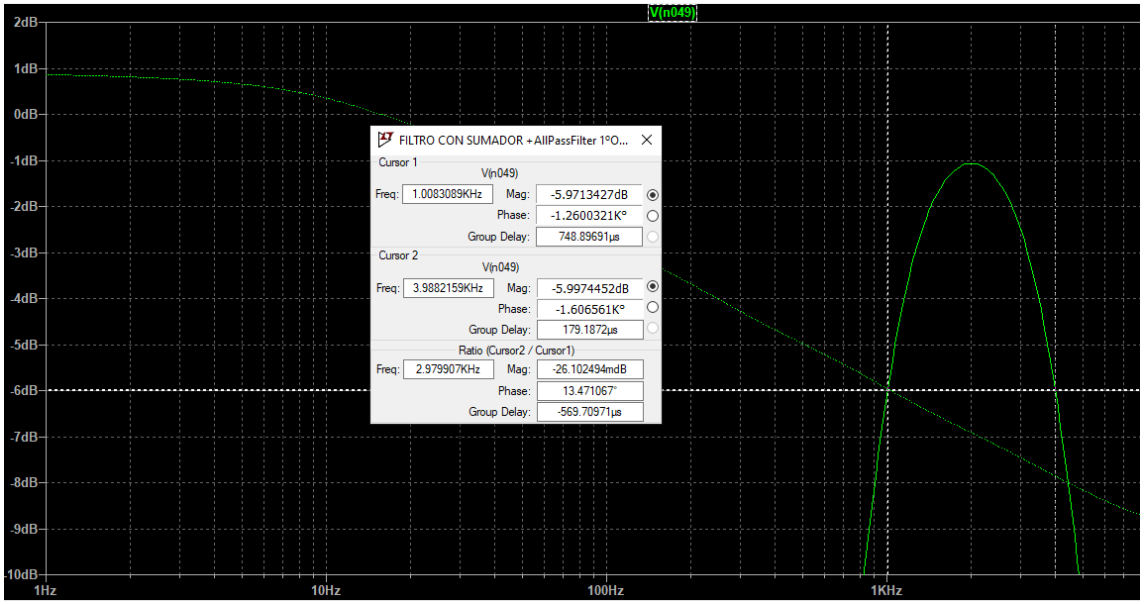


Figura 83: Barriendo en frecuencia de la banda 1 del ecualizador. [28]

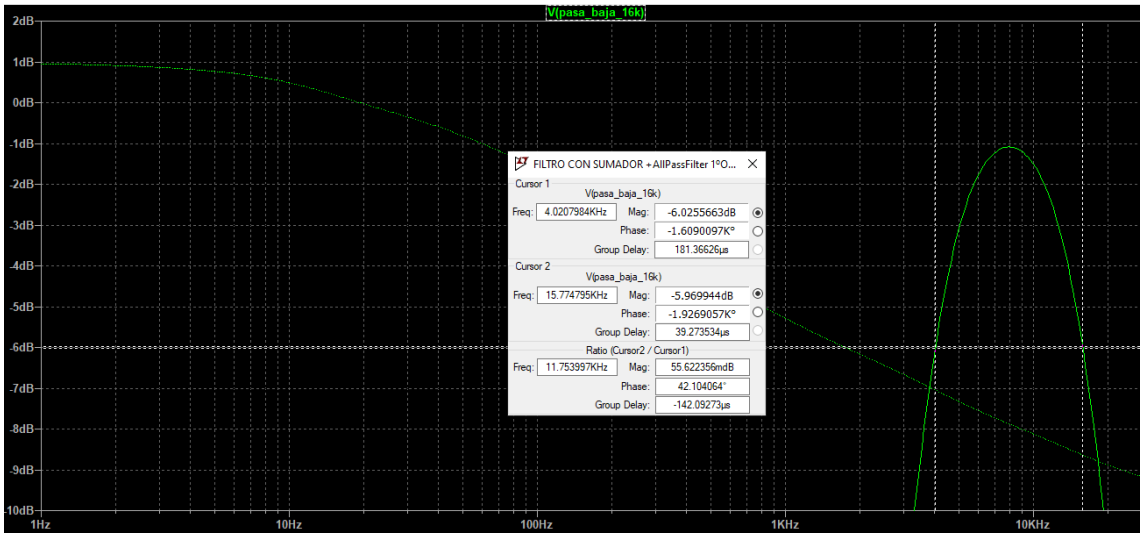


Figura 84: Barriendo en frecuencia de la banda 1 del ecualizador. [28]

Anexo VI.
Barridos en frecuencia en etapa de experimentación.

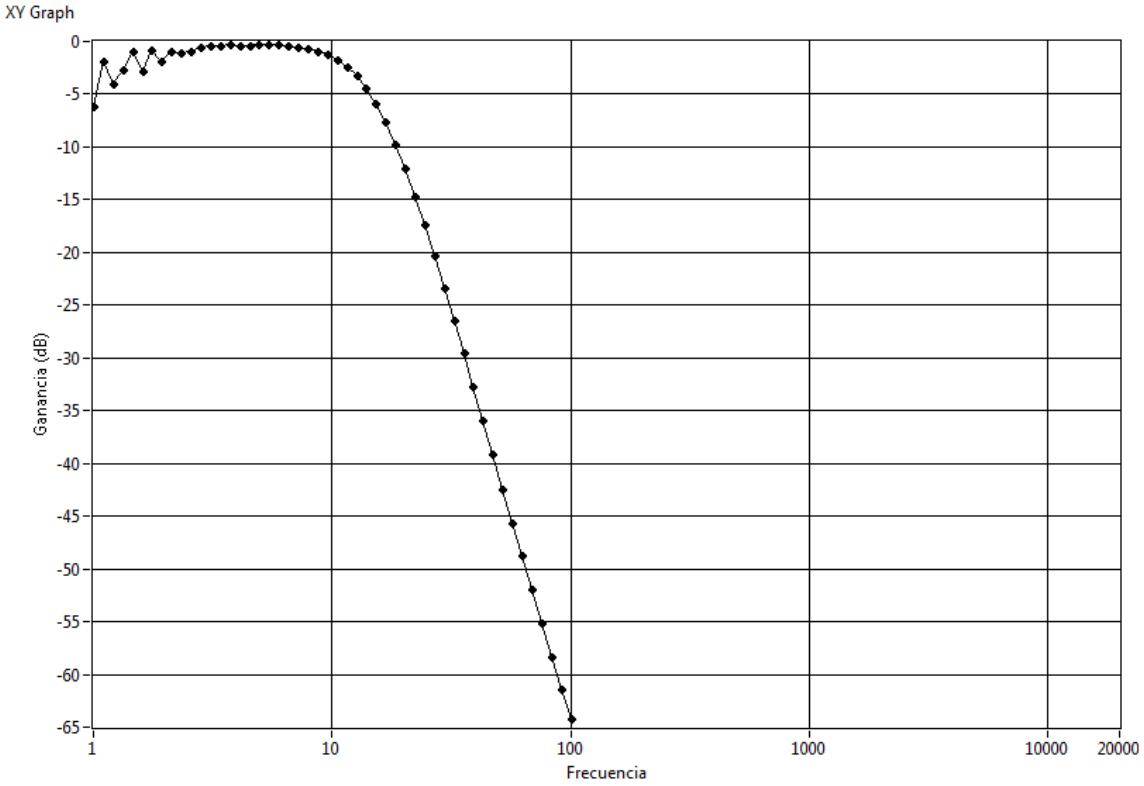


Figura 85: Barriendo en frecuencia de la banda 1 del ecualizador. [28]

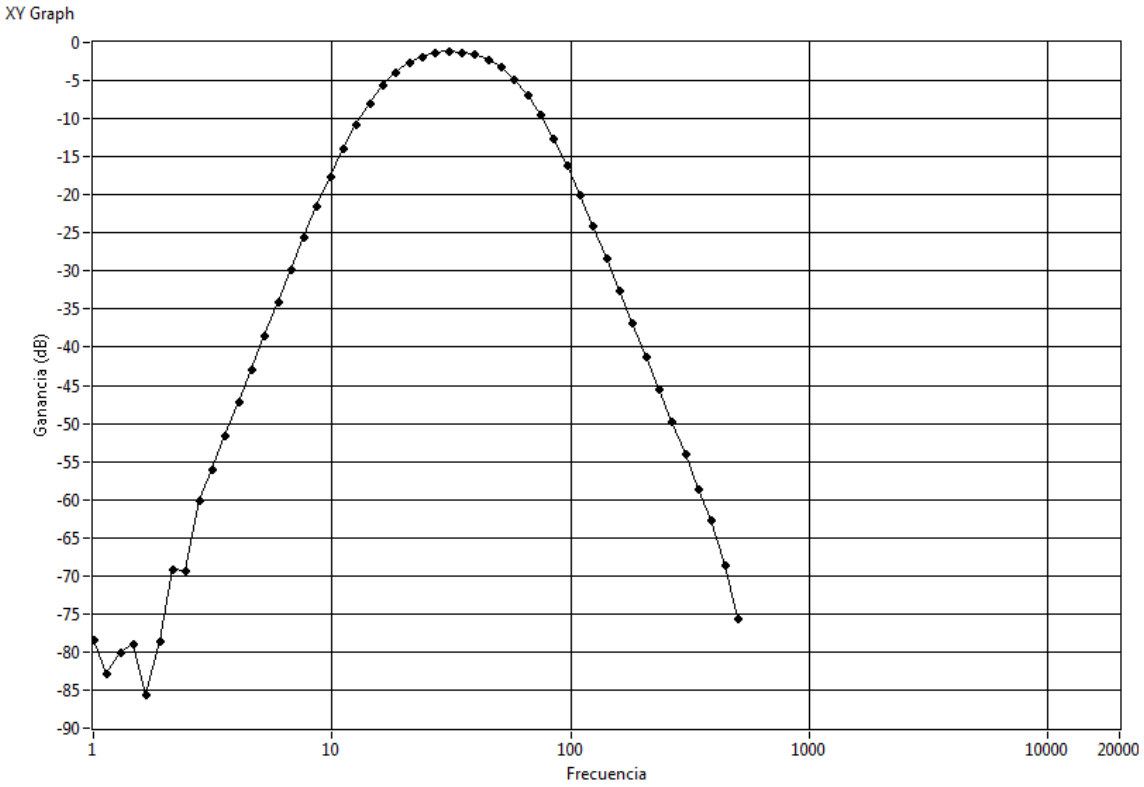


Figura 86: Barriendo en frecuencia de la banda 2 del ecualizador. [28]

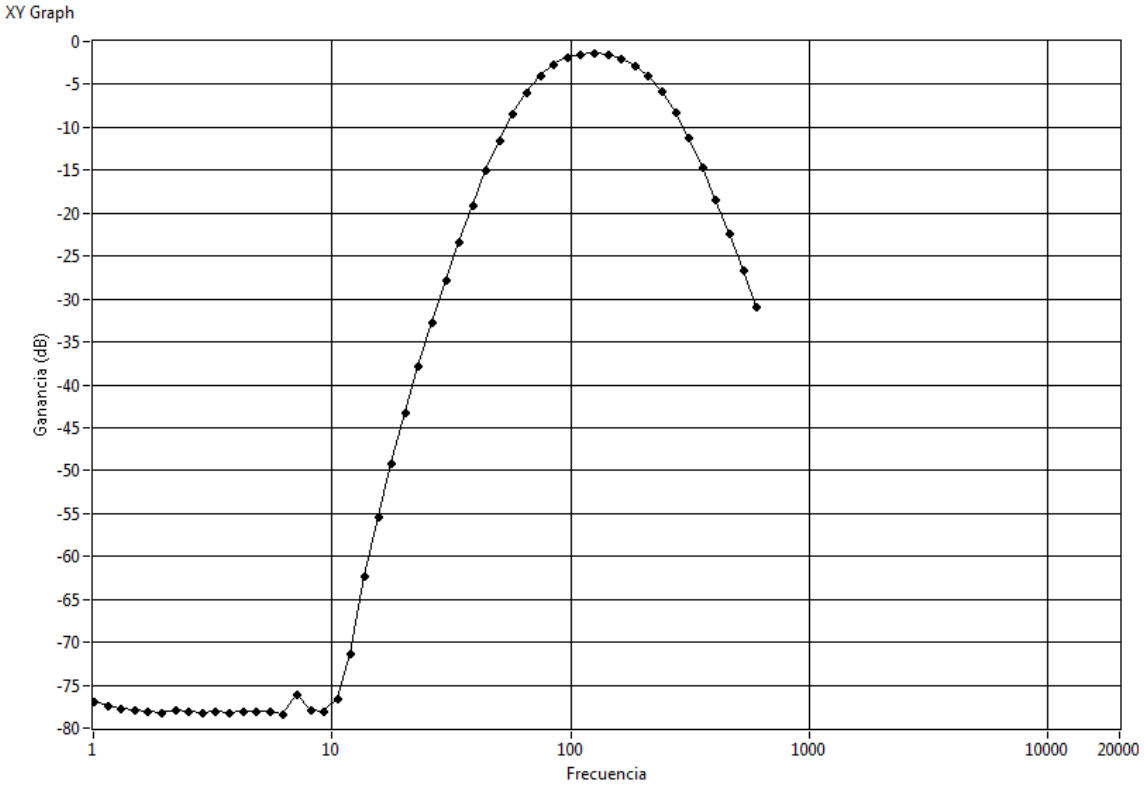


Figura 87: Barriendo en frecuencia de la banda 3 del ecualizador. [28]

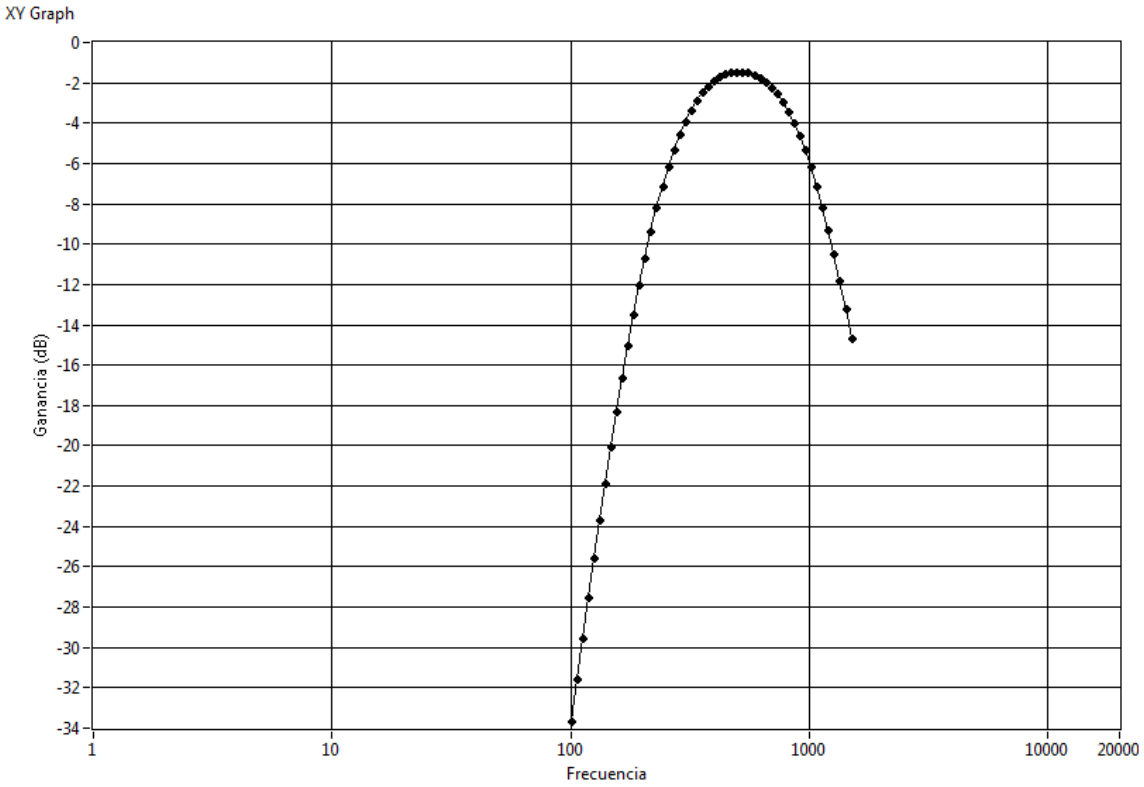


Figura 88: Barriendo en frecuencia de la banda 4 del ecualizador. [28]

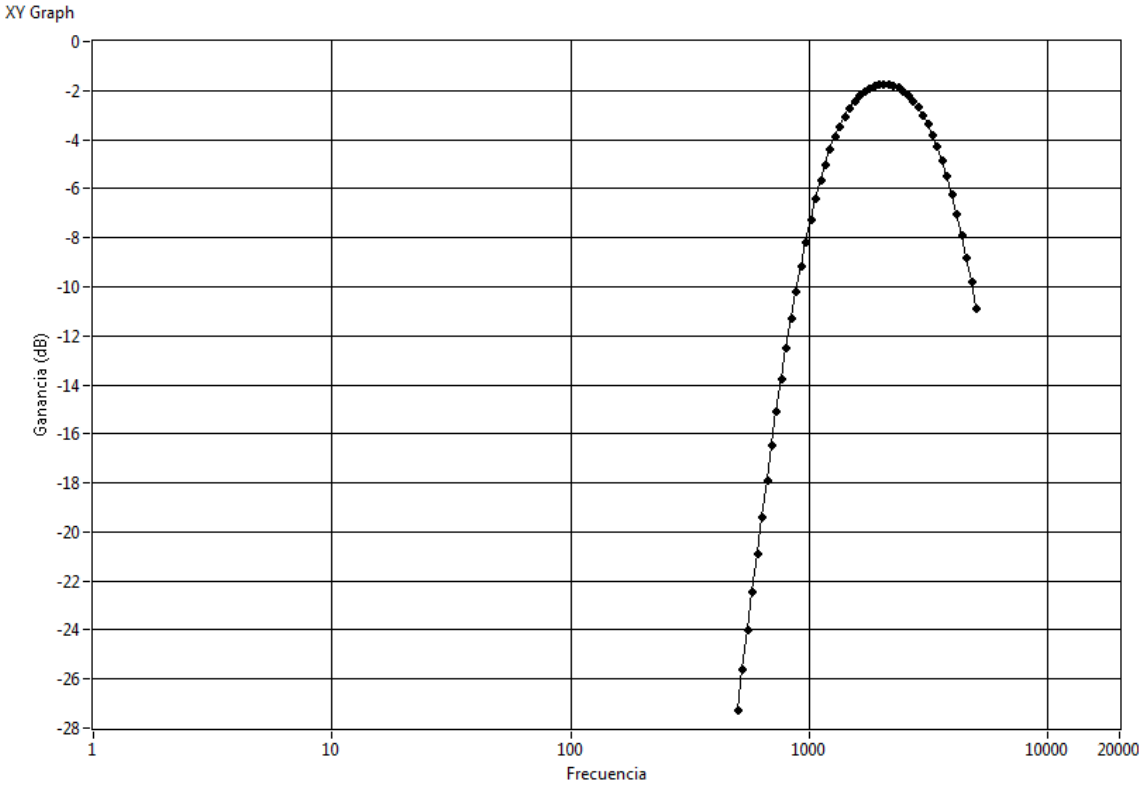


Figura 89: Barriendo en frecuencia de la banda 5 del ecualizador. [28]

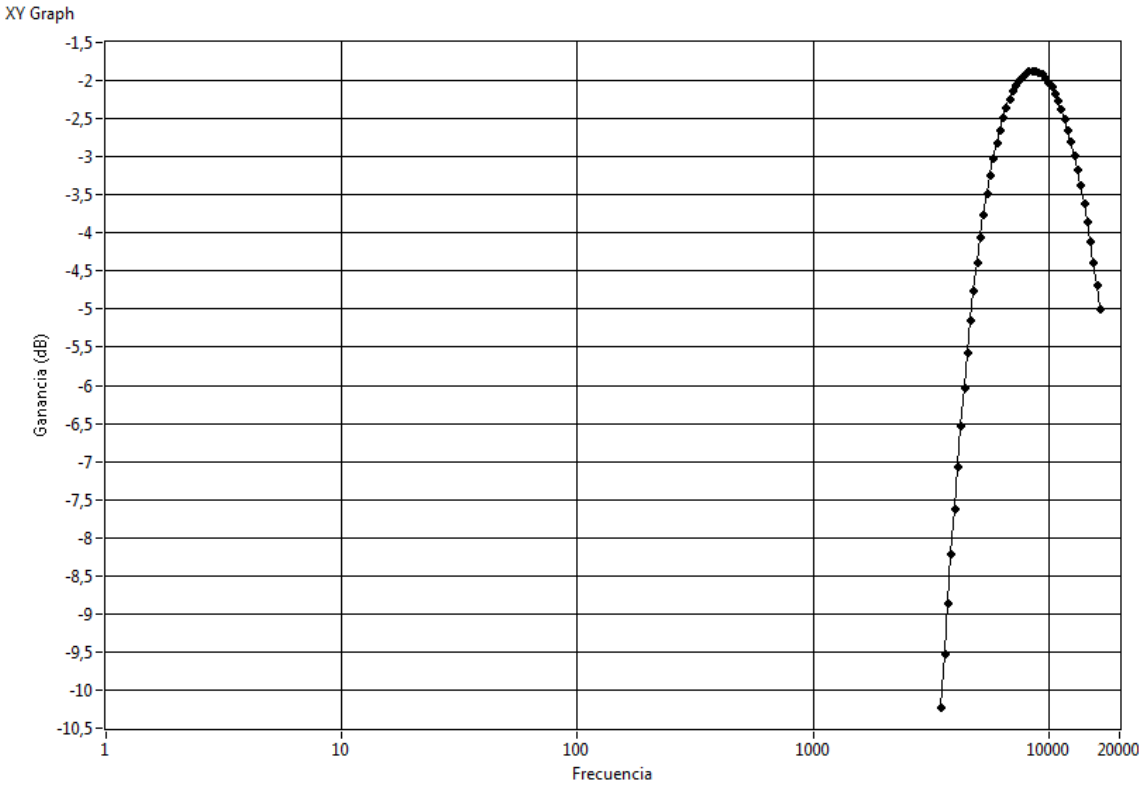
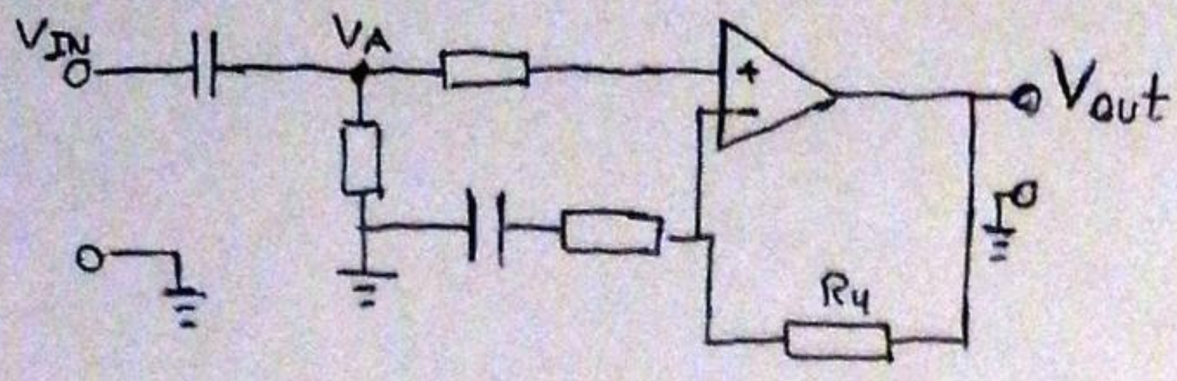


Figura 90: Barriendo en frecuencia de la banda 6 del ecualizador. [28]

Anexo VII.
Función de transferencia del lazo de realimentación del sumador de potencia.



$$\frac{V_{IN}-V_A}{Z_{C_1}} = \frac{V_A}{R_1} \longrightarrow V_{IN}R_1 = V_A(Z_{C_1}+R_1) \rightarrow \boxed{V_A = V_{IN}\cdot\left(\frac{R_1}{R_1+Z_{C_1}}\right)} \quad (1)$$

$$\frac{V_{out}}{R_4+R_3+Z_{C_2}} = \frac{V_{out}-V_A}{R_4} \rightarrow V_{out}(R_3+Z_{C_2}) = V_A(R_4+R_3+Z_{C_2})$$

$$\boxed{V_{out} = V_A\cdot\left(\frac{R_4+R_3+Z_{C_2}}{R_3+Z_{C_2}}\right)} \quad (2)$$

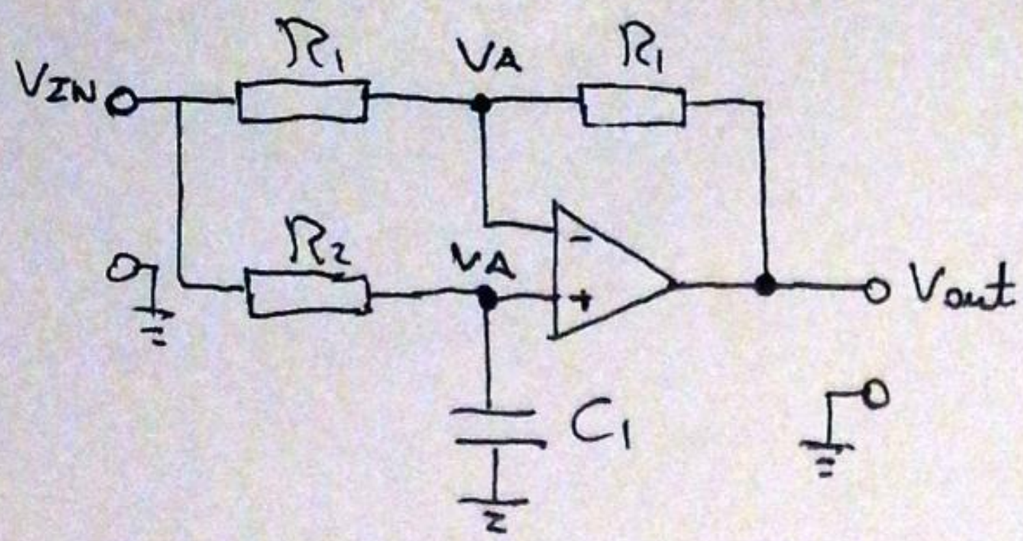
$$\left.\begin{matrix}(1)\\(2)\end{matrix}\right\} \quad \frac{V_{out}}{V_{IN}} = \frac{R_1(R_4+R_3+Z_{C_2})}{Z_{C_1}R_3+Z_{C_1}Z_{C_2}+R_1Z_{C_2}+R_1R_3} =$$

$$= \frac{R_1\left(R_4+R_3+\frac{1}{sC_2}\right)}{\frac{R_3}{sC_1}+\frac{1}{s^2C_1C_2}+\frac{R_1}{sC_2}+R_1R_3} = \frac{R_1\left(R_4+R_3+\frac{1}{sC_2}\right)\cdot s^2C_1C_2}{R_3sC_2+1+R_1sC_1+R_1R_3s^2C_1C_2} =$$

$$= \frac{R_1s^2C_1C_2(R_4+R_3)+sR_1C_1}{R_3sC_2+1+R_1sC_1+R_1R_3s^2C_1C_2} = \frac{s^2R_1C_1C_2(R_4+R_3)+sR_1C_1}{s^2(R_1R_3C_1C_2)+s(R_1C_1+R_3C_2)+1}$$

$$\boxed{G(s) = \frac{R_4+R_3}{R_3}\cdot\frac{s^2+\frac{s}{C_2(R_4+R_3)}}{s^2+s\left(\frac{R_1C_1+R_3C_2}{R_1R_3C_1C_2}\right)+\frac{1}{R_1R_3C_1C_2}}}$$

Anexo VIII.
Función de transferencia del filtro pasa-todo.



$$\left.\begin{aligned}\frac{V_{IN}-V_A}{R_1} &= \frac{V_A-V_{out}}{R_1} \quad (1)\\ \frac{V_{IN}-V_A}{R_2} &= \frac{V_A}{Z_{C_1}} \quad (2)\end{aligned}\right\} \quad V_A = \frac{V_{IN}+V_{out}}{2}$$

$$\frac{V_{IN}}{R_2} - \left(\frac{V_{IN}+V_{out}}{2R_2}\right) = \frac{V_{IN}+V_{out}}{2Z_{C_1}} \Rightarrow \frac{V_{IN}}{R_2} - \frac{V_{IN}}{2R_2} - \frac{V_{out}}{2R_2} = \frac{V_{IN}}{2Z_{C_1}} + \frac{V_{out}}{2Z_{C_1}}$$

$$V_{IN}\left(\frac{1}{R_2} - \frac{1}{2R_2} - \frac{1}{2Z_{C_1}}\right) = V_{out}\left(\frac{1}{2Z_{C_1}} + \frac{1}{2R_2}\right)$$

$$\frac{V_o}{V_{IN}} = \frac{2Z_{C_1} - Z_{C_1} - R_2}{R_2 + Z_{C_1}} = \frac{Z_{C_1} - R_2}{Z_{C_1} + R_2}$$

$$G(s) = \frac{-s + \frac{1}{R_2C_1}}{s + \frac{1}{R_2C_1}}$$

$$f_o = \frac{1}{2\pi R_2 C_1}$$

$$\phi = -2\tan^{-1}\left(\frac{\omega}{\omega_o}\right)$$

Anexo IX.
Datasheet del TL081.

TL081

General purpose JFET single operational amplifiers

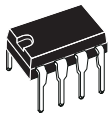
Features

- Wide common-mode (up to V_{CC}^+) and differential voltage range
- Low input bias and offset current
- Output short-circuit protection
- High input impedance JFET input stage
- Internal frequency compensation
- Latch-up free operation
- High slew rate: 16 V/µs (typ)

Description

The TL081, TL081A and TL081B are high-speed JFET input single operational amplifiers incorporating well matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

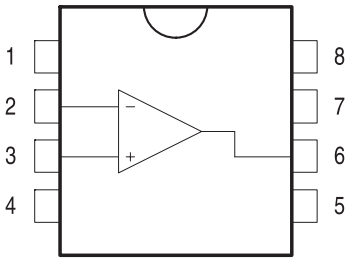
The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.



N
DIP8
(Plastic package)

D
SO-8
(Plastic micropackage)

Pin connections
(top view)



1 - Offset null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

1 Schematic diagram

Figure 1. Schematic diagram

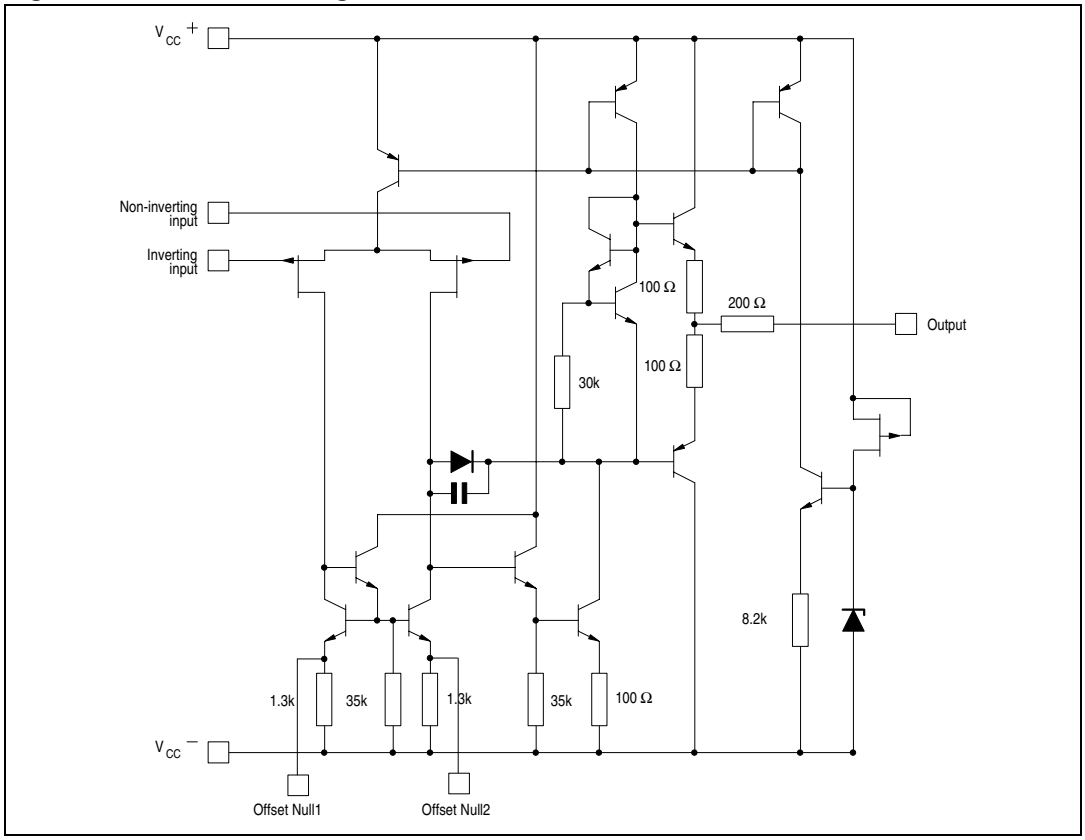
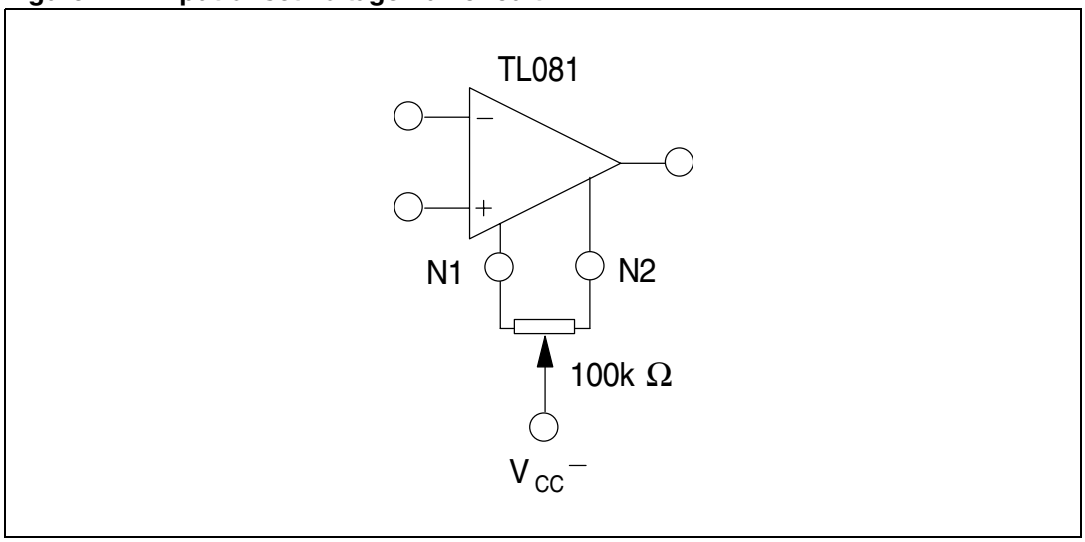


Figure 2. Input offset voltage null circuit



2 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	TL081I, AI, BI	TL081C, AC, BC	Unit
V_{CC}	Supply voltage (1)	±18		V
V_{in}	Input voltage (2)	±15		V
V_{id}	Differential input voltage (3)	±30		V
P_{tot}	Power dissipation	680		mW
	Output short-circuit duration (4)	Infinite		
T_{stg}	Storage temperature range	-65 to +150		°C
R_{thja}	Thermal resistance junction to ambient(5) (6) SO-8 DIP8	 125 85		°C/W
R_{thjc}	Thermal resistance junction to case(5) (6) SO-8 DIP8	 40 41		°C/W
ESD	HBM: human body model(7)	500		V
	MM: machine model(8)	200		V
	CDM: charged device model(9)	1.5		kV

1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^{+} and V_{CC}^{-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
3. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. Rth are typical values.
7. Human body model: 100 pF discharged through a 1.5kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
9. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 2. Operating conditions

Symbol	Parameter	TL081I, AI, BI	TL081C, AC, BC	Unit
V_{CC}	Supply voltage range	6 to 36		V
T_{oper}	Operating free-air temperature range	-40 to +105	0 to +70	°C

3 Electrical characteristics

Table 3. V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	TL081I, AC, AI, BC, BI			TL081C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input offset voltage (R_s = 50Ω) T_{amb} = +25°C TL081 TL081A TL081B $T_{min} \le T_{amb} \le T_{max}$ TL081 TL081A TL081B		 3 3 1	 10 6 3 13 7 5		3	10 13	mV
DV_{io}	Input offset voltage drift		10			10		µV/°C
I_{io}	Input offset current (1) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		5	100 4		5	100 10	pA nA
I_{ib}	Input bias current (1) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		20	200 20		20	400 20	nA
A_{vd}	Large signal voltage gain (R_L = 2kΩ, V_o = ±10V) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	50 25	200		25 15	200		V/mV
SVR	Supply voltage rejection ratio (R_S = 50Ω) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	80 80	86		70 70	86		dB
I_{CC}	Supply current, no load T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		1.4	2.5 2.5		1.4	2.5 2.5	mA
V_{icm}	Input common mode voltage range	±11	+15 -12		±11	+15 -12		V
CMR	Common mode rejection ratio (R_S = 50Ω) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	80 80	86		70 70	86		dB
I_{os}	Output short-circuit current T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	10 10	40	60 60	10 10	40	60 60	mA
$\pm V_{opp}$	Output voltage swing T_{amb} = +25°C R_L = 2kΩ R_L = 10kΩ $T_{min} \le T_{amb} \le T_{max}$ R_L = 2kΩ R_L = 10kΩ	10 12 10 12	12 13.5		10 12 10 12	12 13.5		V
SR	Slew rate (T_{amb} = +25°C) V_{in} = 10V, R_L = 2kΩ, C_L = 100pF, unity gain	8	16		8	16		V/µs

Table 3. V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified) (continued)

Symbol	Parameter	TL081I, AC, AI, BC, BI			TL081C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_r	Rise time (T_{amb} = +25°C) V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, unity gain		0.1			0.1		µs
K_{ov}	Overshoot (T_{amb} = +25°C) V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, unity gain		10			10		%
GBP	Gain bandwidth product (T_{amb} = +25°C) V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF, F= 100kHz	2.5	4		2.5	4		MHz
R_i	Input resistance		10^{12}			10^{12}		Ω
THD	Total harmonic distortion (T_{amb} = +25°C), F= 1kHz, R_L = 2kΩ,C_L = 100pF, A_v = 20dB, V_o = $2V_{pp}$		0.01			0.01		%
e_n	Equivalent input noise voltage R_S = 100Ω, F= 1kHz		15			15		$\frac{nV}{\sqrt{Hz}}$
∅m	Phase margin		45			45		degrees

1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

Figure 3. Maximum peak-to-peak output voltage versus frequency

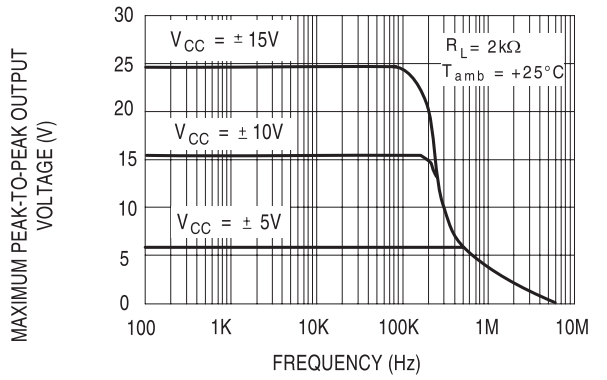


Figure 4. Maximum peak-to-peak output voltage versus frequency

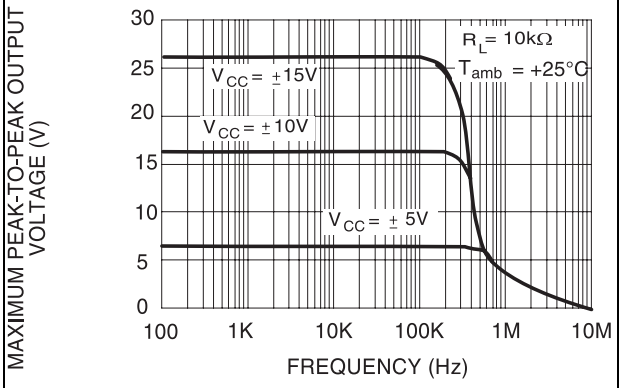


Figure 5. Maximum peak-to-peak output voltage versus frequency

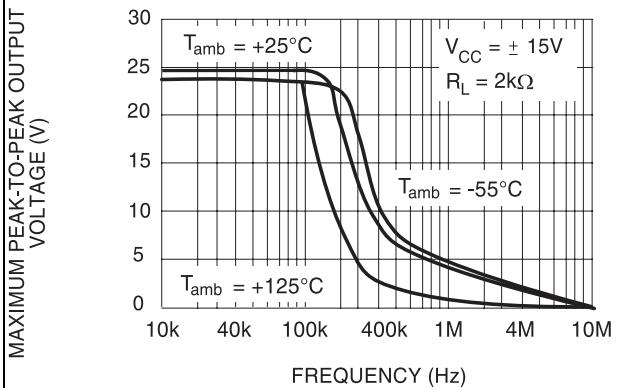


Figure 6. Maximum peak-to-peak output voltage versus free air temperature

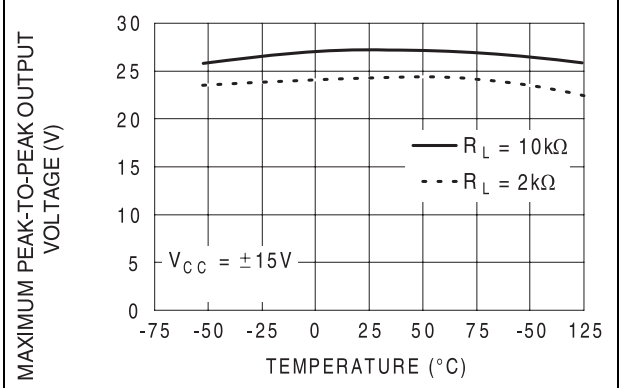


Figure 7. Maximum peak-to-peak output voltage versus load resistance

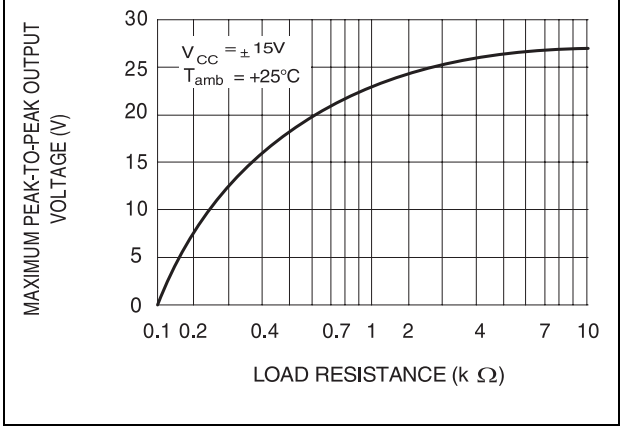


Figure 8. Maximum peak-to-peak output voltage versus supply voltage

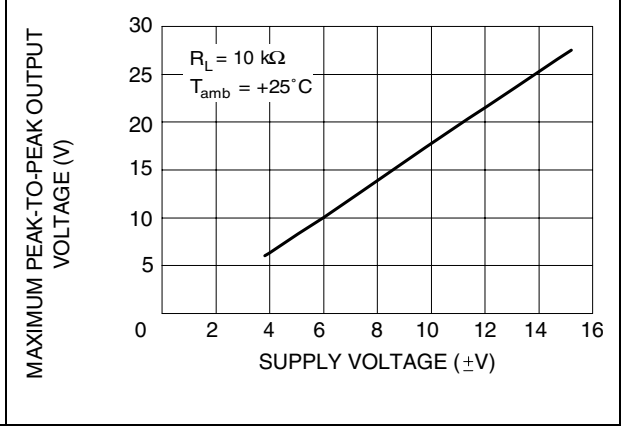


Figure 9. Input bias current versus free air temperature

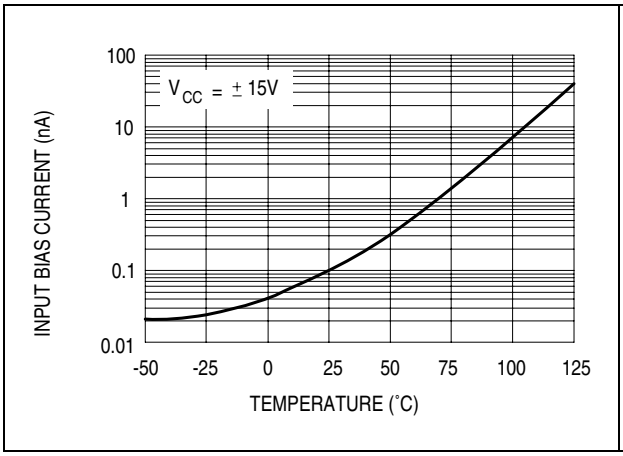


Figure 10. Large signal differential voltage amplification versus free air temp

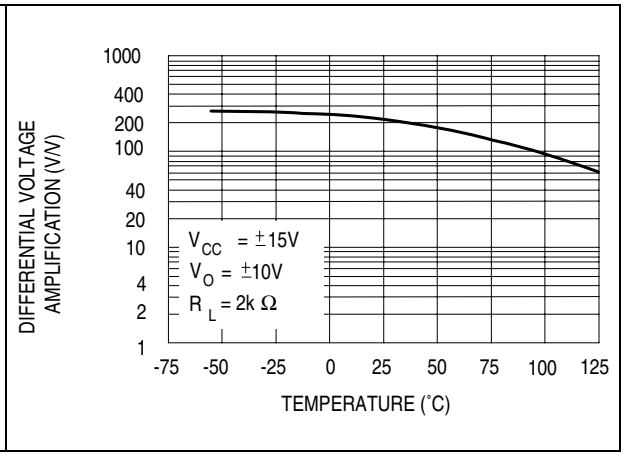


Figure 11. Large signal differential voltage amplification and phase shift versus frequency

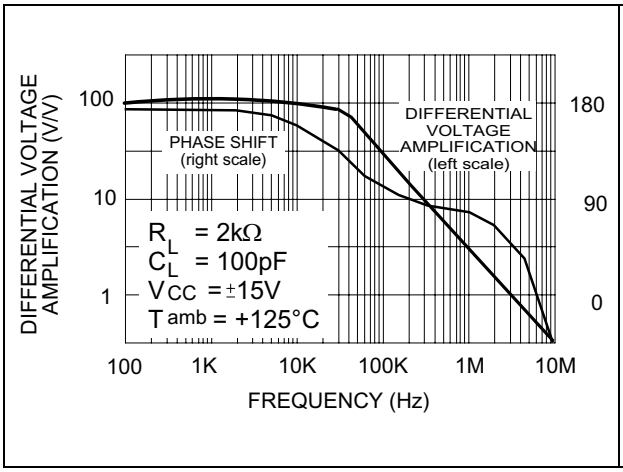


Figure 12. Total power dissipation versus free air temperature

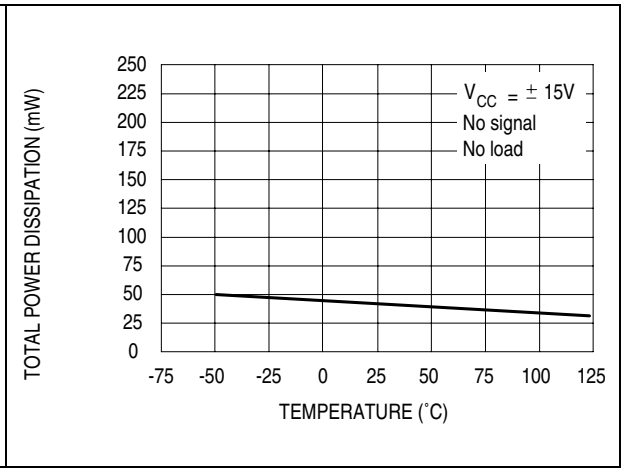


Figure 13. Supply current per amplifier versus free air temperature

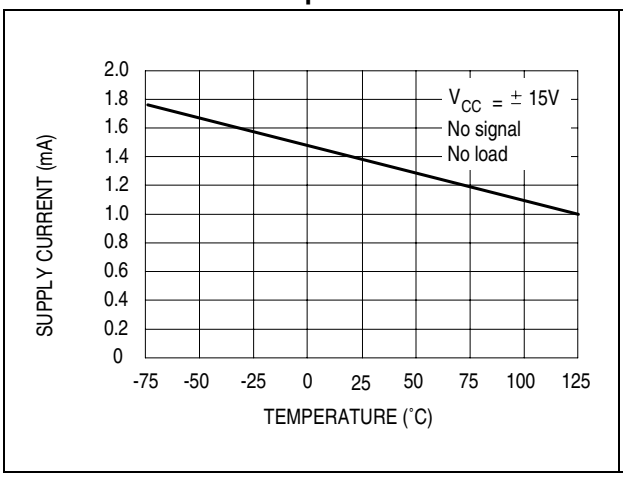


Figure 14. Supply current per amplifier versus supply voltage

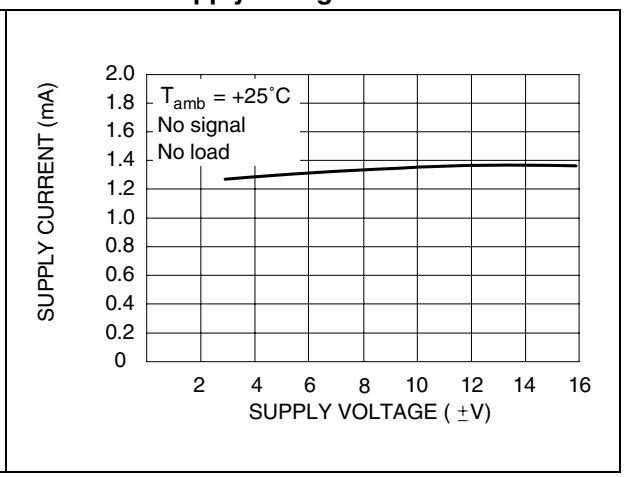


Figure 15. Common mode rejection ratio versus free air temperature

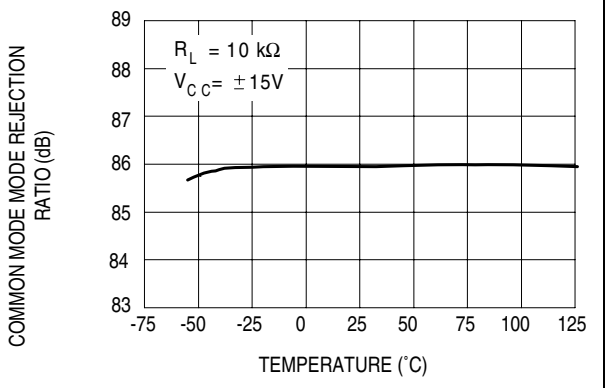


Figure 16. Equivalent input noise voltage versus frequency

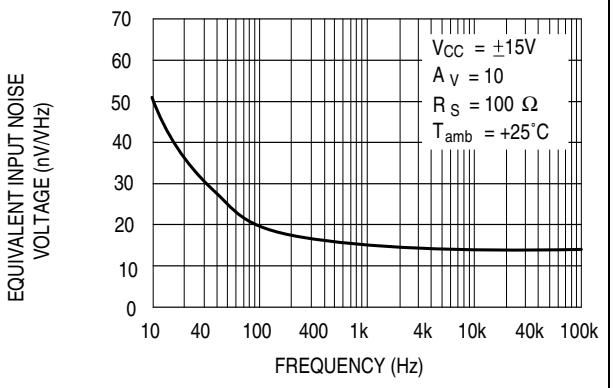


Figure 17. Output voltage versus elapsed time

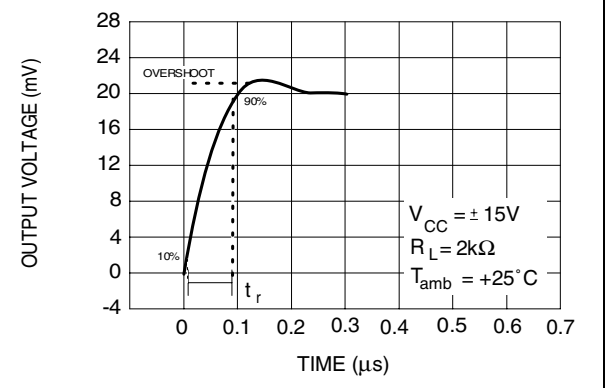


Figure 18. Total harmonic distortion versus frequency

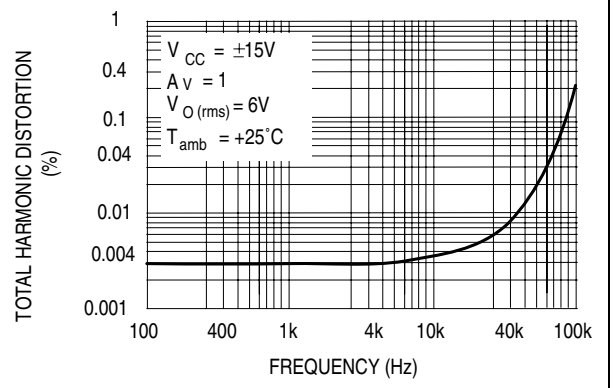
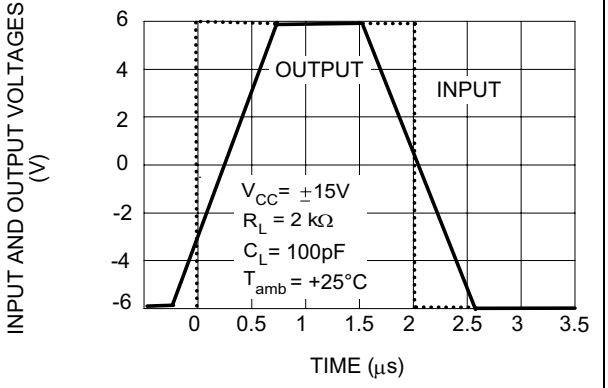


Figure 19. Voltage follower large signal pulse response



4 Parameter measurement information

Figure 20. Voltage follower

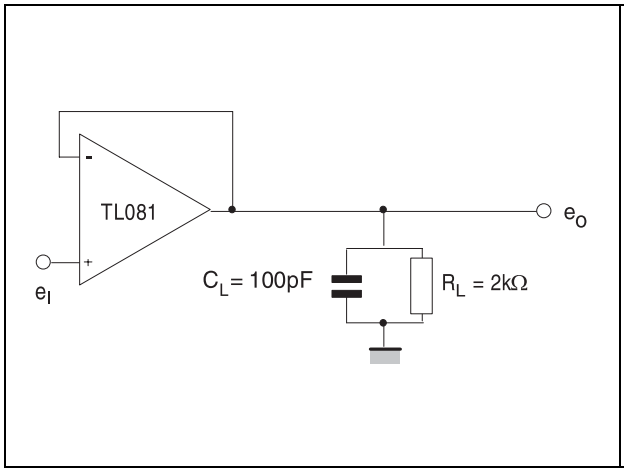
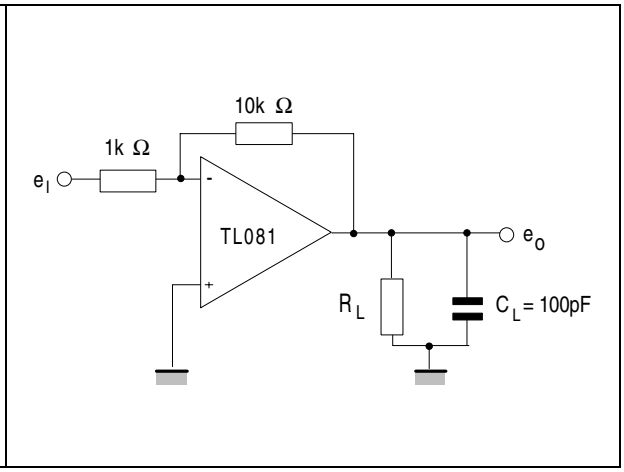


Figure 21. Gain-of-10 inverting amplifier



5 Typical applications

Figure 22. 0.5 Hz square wave oscillator

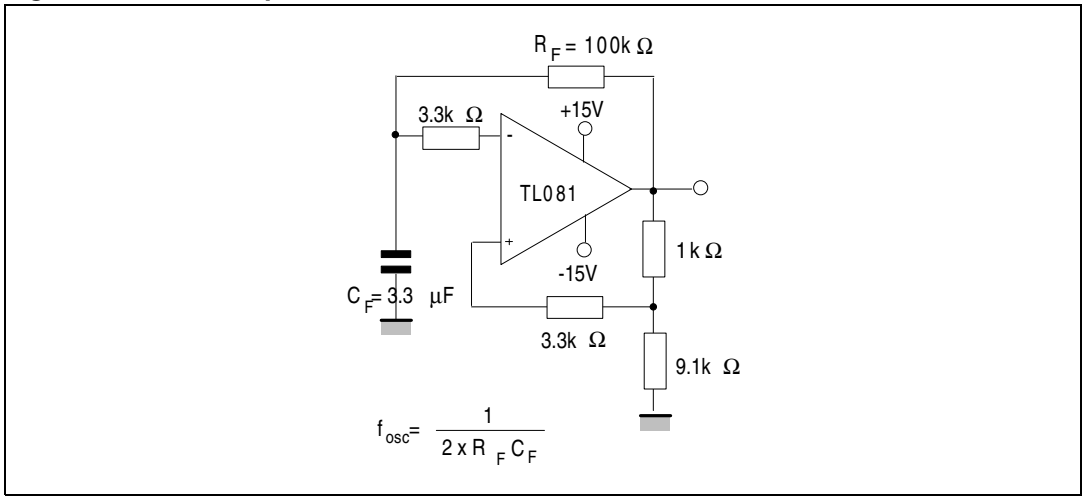
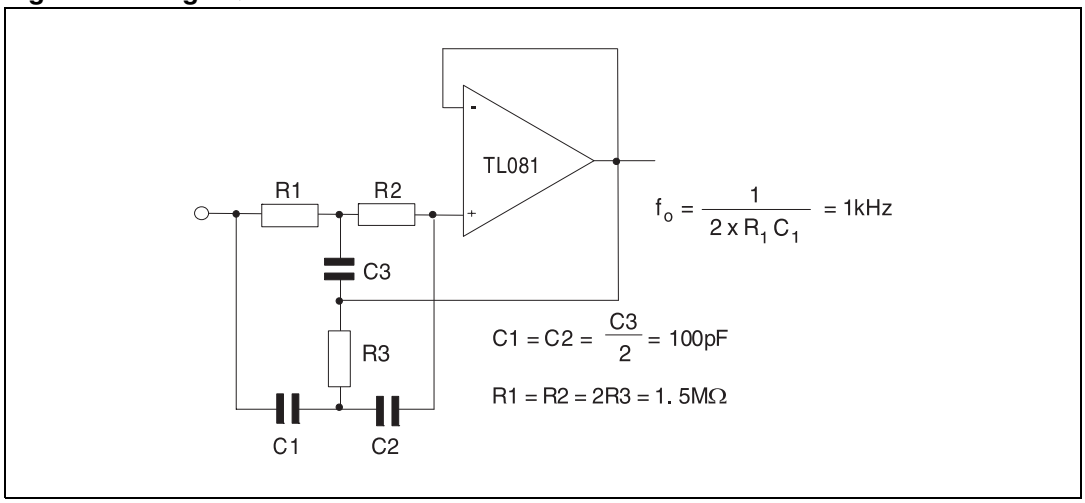


Figure 23. High Q notch filter



6 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

6.1 DIP 8 package information

Figure 24. DIP8 package mechanical drawing

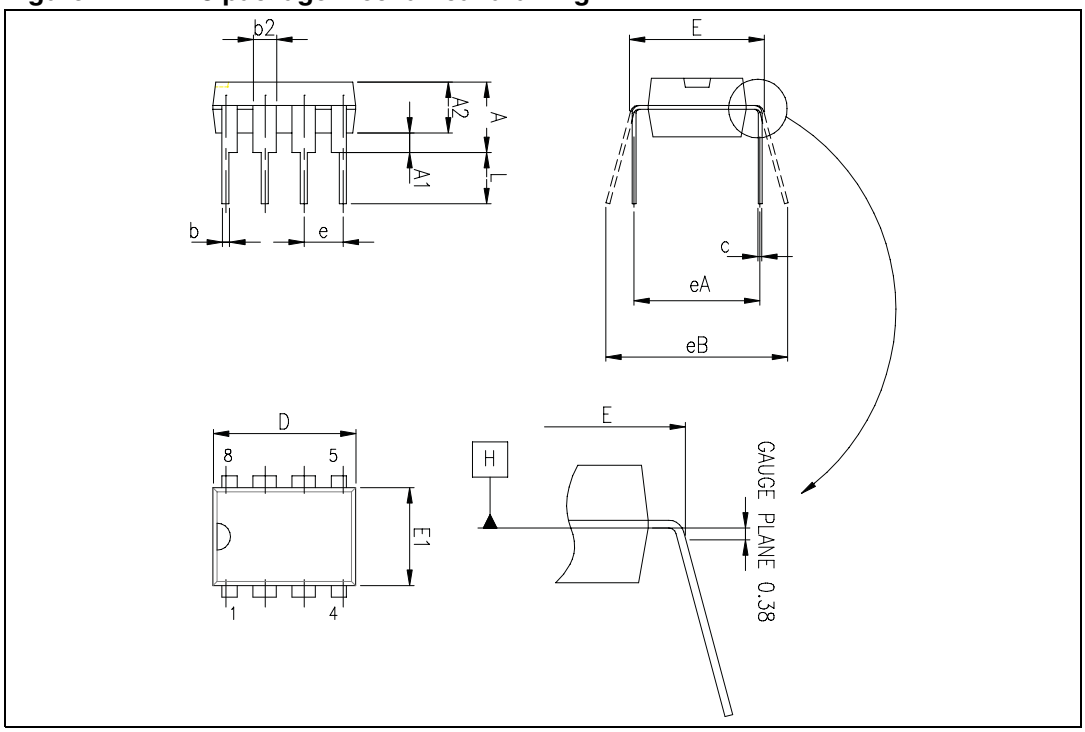


Table 4. DIP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

6.2 SO-8 package information

Figure 25. SO-8 package mechanical drawing

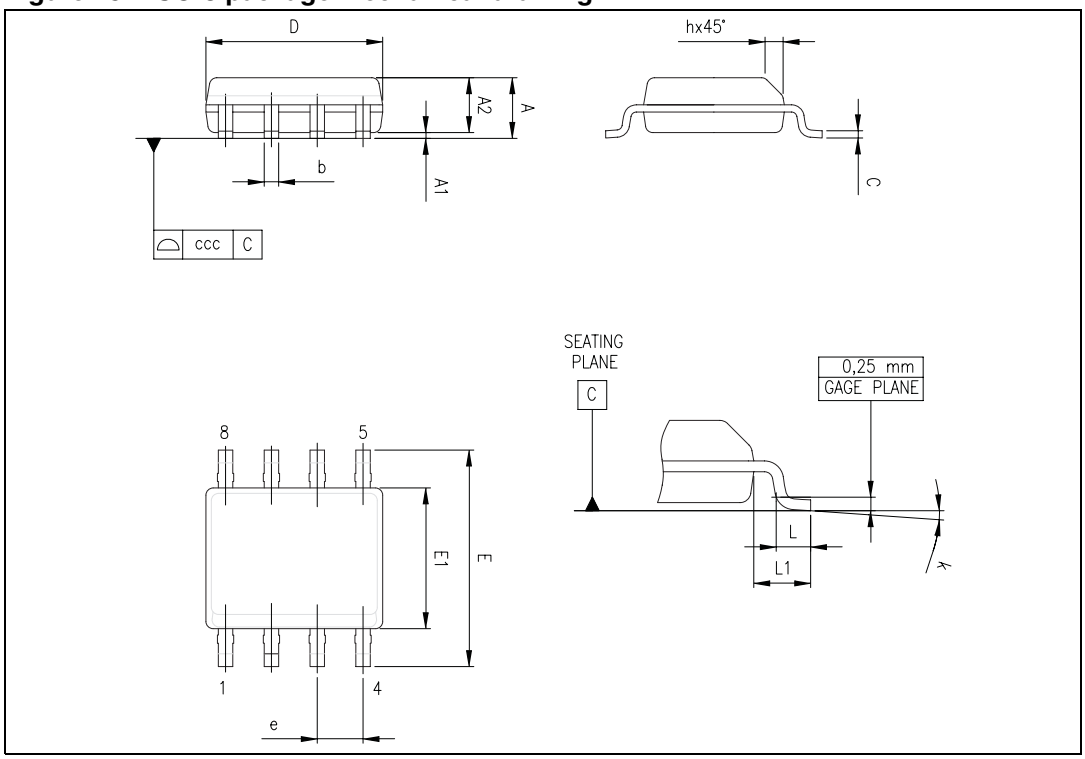


Table 5. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004

7 Ordering information

Table 6. Order codes

Order code	Temperature range	Package	Packing	Marking
TL081IN TL081AIN TL081BIN	-40°C, +105°C	DIP8	Tube	TL081IN TL081AIN TL081BIN
TL081ID/IDT TL081AID/AIDT TL081BID/BIDT		SO-8	Tube or tape & reel	081I 081AI 081BI
TL081IYD/DT(1) TL081AIYD/DT(1) TL081BIYD/DT(1)		SO-8 (Automotive grade)	Tube or tape & reel	081IY 081AIY 081BIY
TL081CN TL081ACN TL081BCN	0°C, +70°C	DIP8	Tube	TL081CN TL081ACN TL081BCN
TL081CD/CDT TL081ACD/ACDT TL081BCD/BCDT		SO-8	Tube or tape & reel	081C 081AC 081BC

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are on-going.

8 Revision history

Table 7. Document revision history

Date	Revision	Changes
30-Apr-2001	1	Initial release.
27-Jul-2007	2	Added values for R_{thja} and R_{thjc} in *Table 1: Absolute maximum ratings*. Added *Table 2: Operating conditions*. Added automotive grade part numbers in *Table 6: Order codes*. Format update.
27-Jun-2008	3	Removed information concerning military temperature range (TL081Mx, TL081AMx, TL081BMx). Added missing order codes for automotive grade products and updated footnote in *Table 6: Order codes*.

Anexo X.
Datasheet del TL082.

TL082 Wide Bandwidth Dual JFET Input Operational Amplifier

Check for Samples: TL082-N

FEATURES

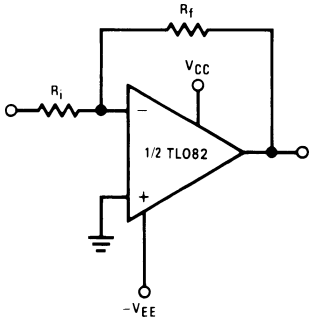
- **Internally Trimmed Offset Voltage: 15 mV**
- **Low Input Bias Current: 50 pA**
- **Low Input Noise Voltage: 16nV/√Hz**
- **Low Input Noise Current: 0.01 pA/√Hz**
- **Wide Gain Bandwidth: 4 MHz**
- **High Slew Rate: 13 V/µs**
- **Low Supply Current: 3.6 mA**
- **High Input Impedance: $10^{12}\Omega$**
- **Low Total Harmonic Distortion: ≤0.02%**
- **Low 1/f Noise Corner: 50 Hz**
- **Fast Settling Time to 0.01%: 2 µs**

DESCRIPTION

These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Typical Connection



Connection Diagram

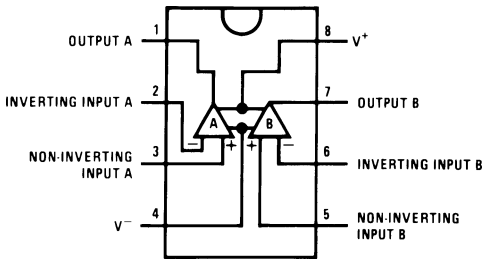
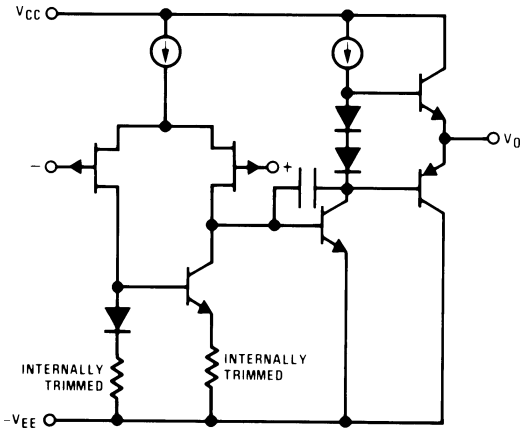


Figure 1. PDIP/SOIC Package (Top View)
See Package Number D0008A or P0008E

Simplified Schematic



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage	±18V
Power Dissipation(3)	(4)
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	150°C
Differential Input Voltage	±30V
Input Voltage Range (5)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C
ESD rating to be determined.	

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The power dissipation limit, however, cannot be exceeded.
(4) For operating at elevated temperature, the device must be derated based on a thermal resistance of 115°C/W junction to ambient for the P0008E package.
(5) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

DC Electrical Characteristics (1)

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		5	15	mV
		Over Temperature			20	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (1) (2)		25	200	pA
		T_j ≤ 70°C			4	nA
I_B	Input Bias Current	T_j = 25°C, (1) (2)		50	400	pA
		T_j ≤ 70°C			8	nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C, V_O = ±10V, R_L = 2 kΩ	25	100		V/mV
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15		V
				−12		V
CMRR	Common-Mode Rejection Ratio	R_S ≤ 10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(3)	70	100		dB
I_S	Supply Current			3.6	5.6	mA

(1) These specifications apply for V_S = ±15V and 0°C ≤T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.
(2) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
(3) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

AC Electrical Characteristics (1)

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1Hz-20 kHz (Input Referred)		−120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C	8	13		V/µs
GBW	Gain Bandwidth Product	V_S = ±15V, T_A = 25°C		4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		25		nV/√Hz
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01		pA/√Hz
THD	Total Harmonic Distortion	A_V = +10, R_L = 10k, V_O = 20 Vp − p, BW = 20 Hz−20 kHz		<0.02		%

(1) These specifications apply for V_S = ±15V and 0°C ≤T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Typical Performance Characteristics

Input Bias Current

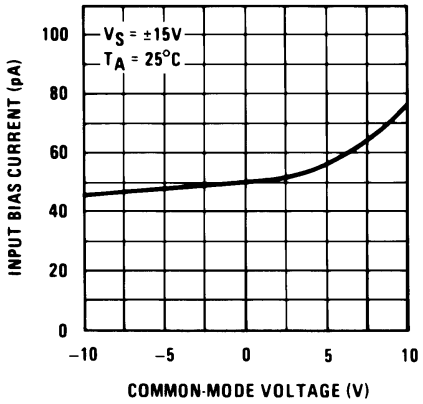


Figure 2.

Input Bias Current

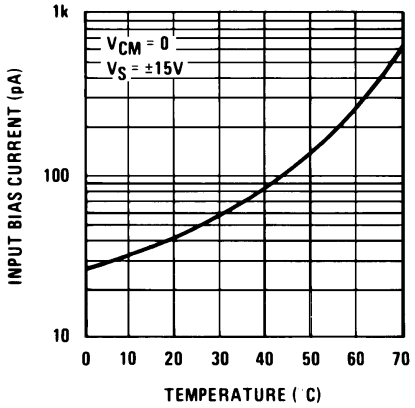


Figure 3.

Supply Current

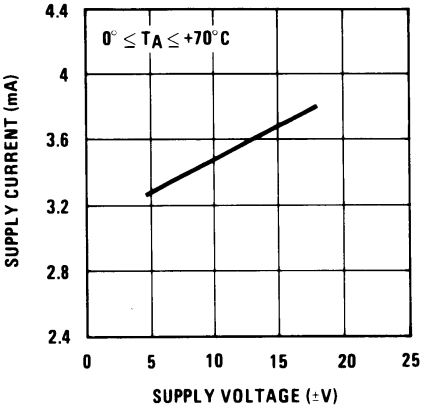


Figure 4.

Positive Common-Mode Input Voltage Limit

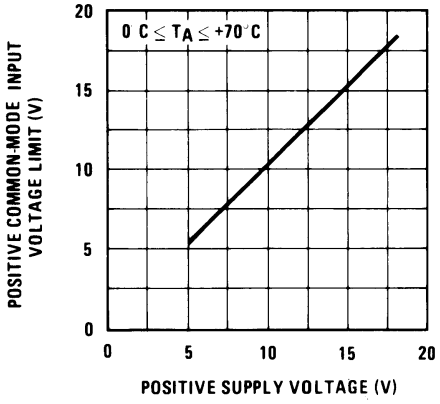


Figure 5.

Negative Common-Mode Input Voltage Limit

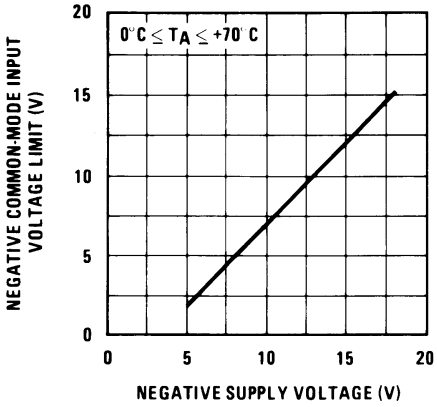


Figure 6.

Positive Current Limit

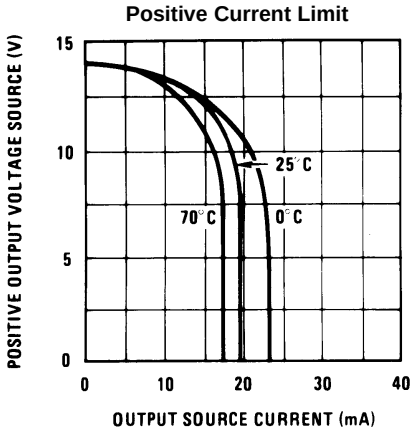


Figure 7.

Typical Performance Characteristics (continued)

Negative Current Limit

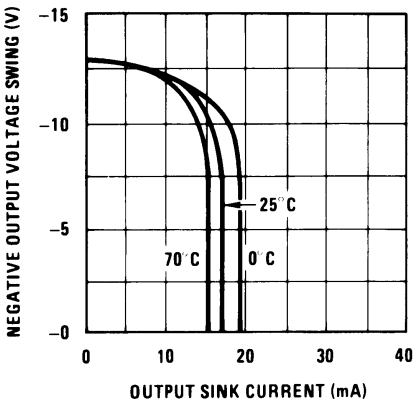


Figure 8.

Voltage Swing

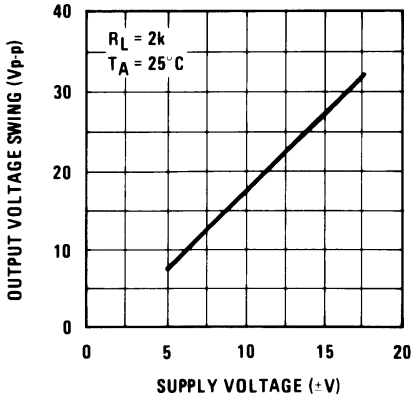


Figure 9.

Output Voltage Swing

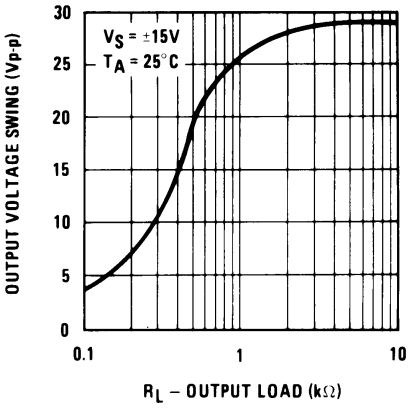


Figure 10.

Gain Bandwidth

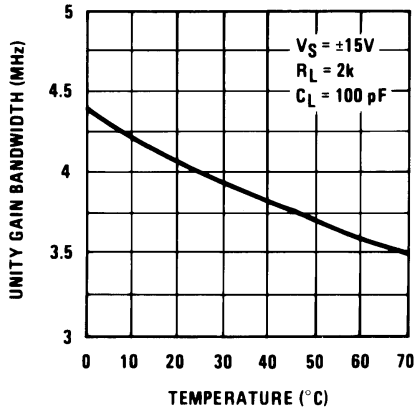


Figure 11.

Bode Plot

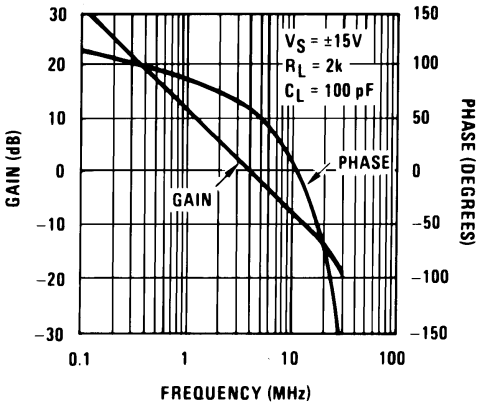


Figure 12.

Slew Rate

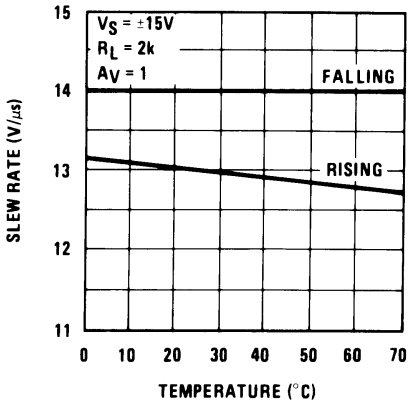


Figure 13.

Typical Performance Characteristics (continued)

Distortion vs Frequency

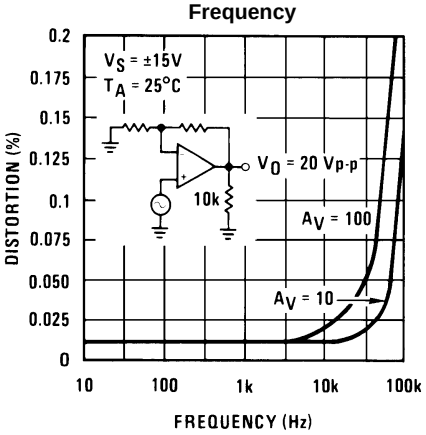


Figure 14.

Undistorted Output Voltage Swing

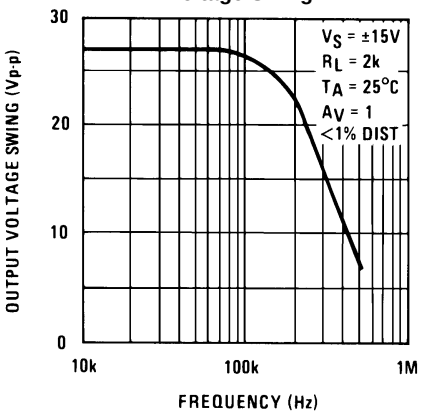


Figure 15.

Open Loop Frequency Response

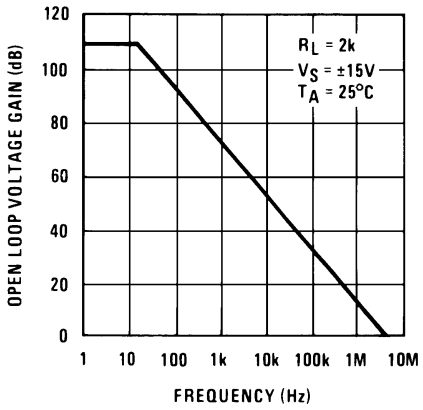


Figure 16.

Common-Mode Rejection Ratio

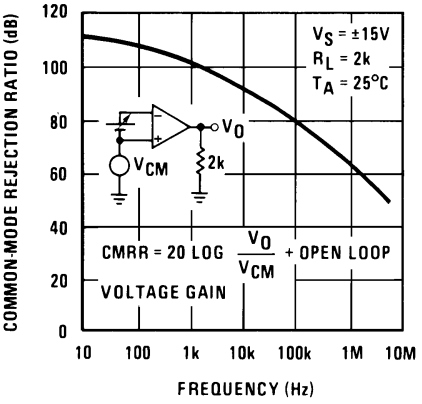


Figure 17.

Power Supply Rejection Ratio

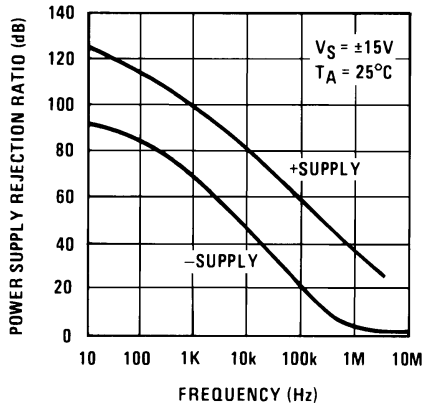


Figure 18.

Equivalent Input Noise Voltage

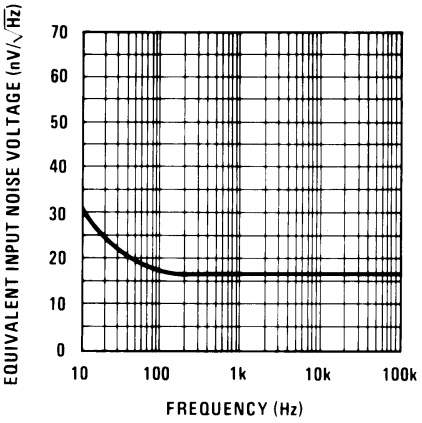


Figure 19.

Typical Performance Characteristics (continued)

Open Loop Voltage Gain (V/V)

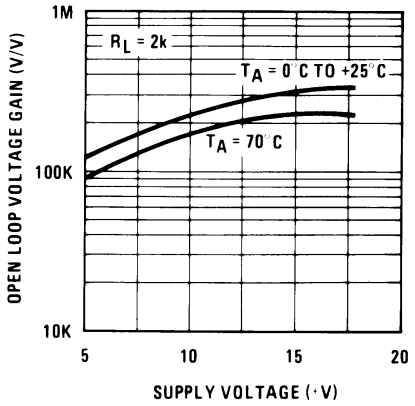


Figure 20.

Output Impedance

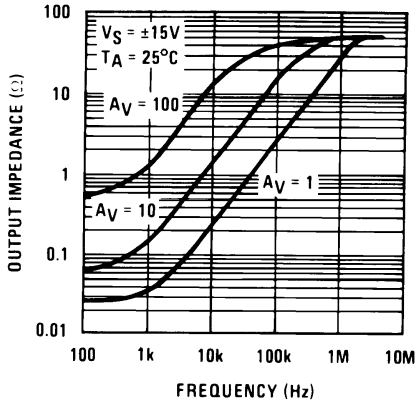


Figure 21.

Inverter Setting Time

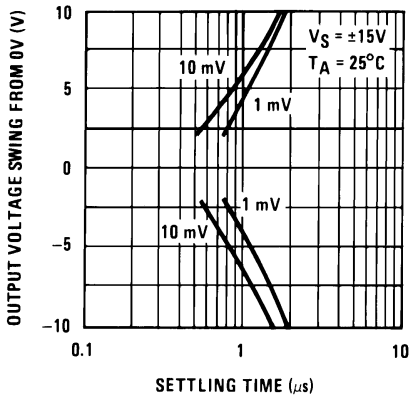


Figure 22.

Pulse Response

Small Signal Inverting

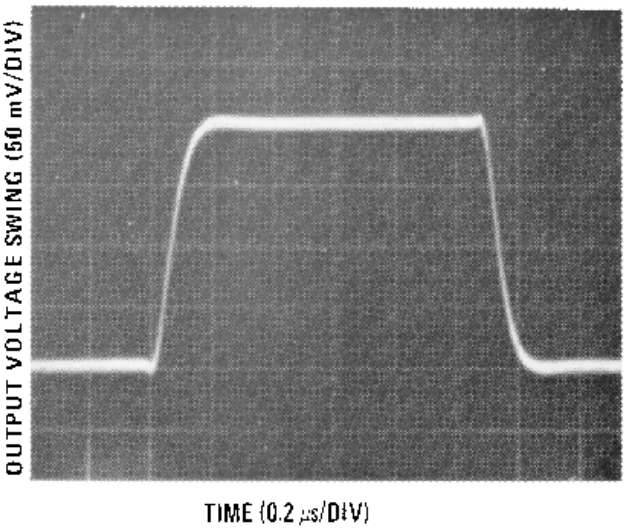


Figure 23.

Large Signal Inverting

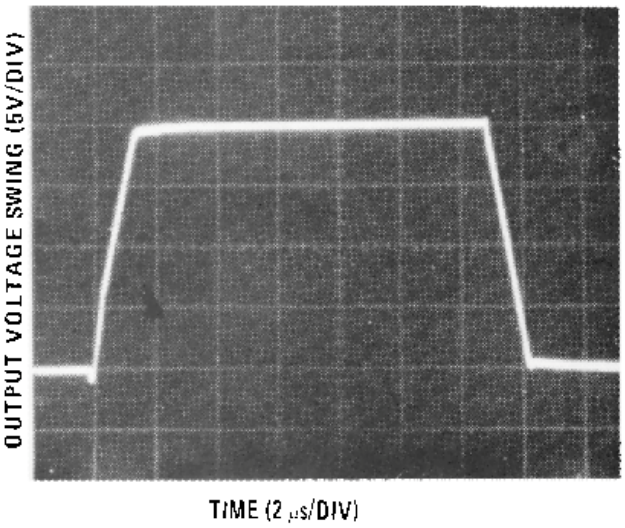


Figure 24.

Small Signal Non-Inverting

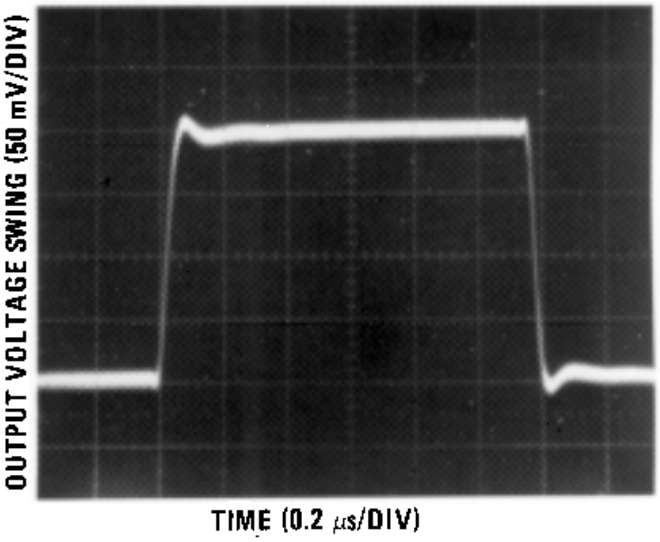


Figure 25.

Large Signal Non-Inverting

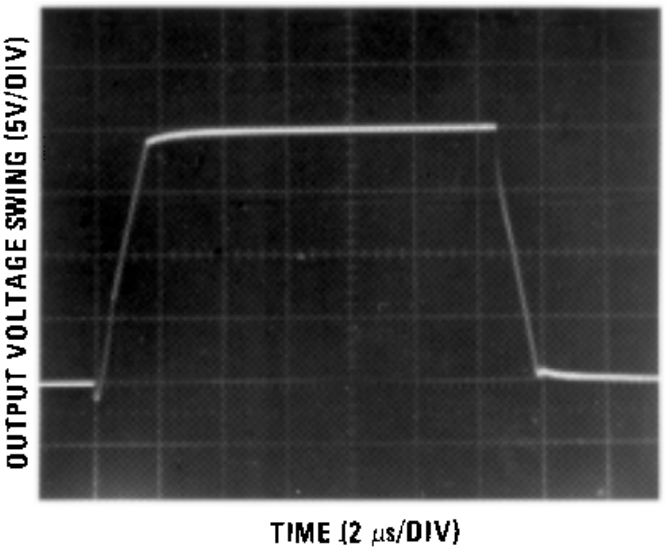


Figure 26.

Pulse Response (continued)

Current Limit (R_L = 100Ω)

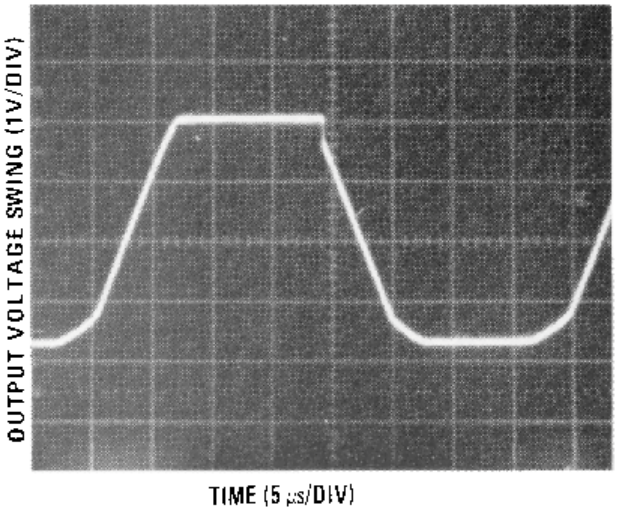


Figure 27.

APPLICATION HINTS

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

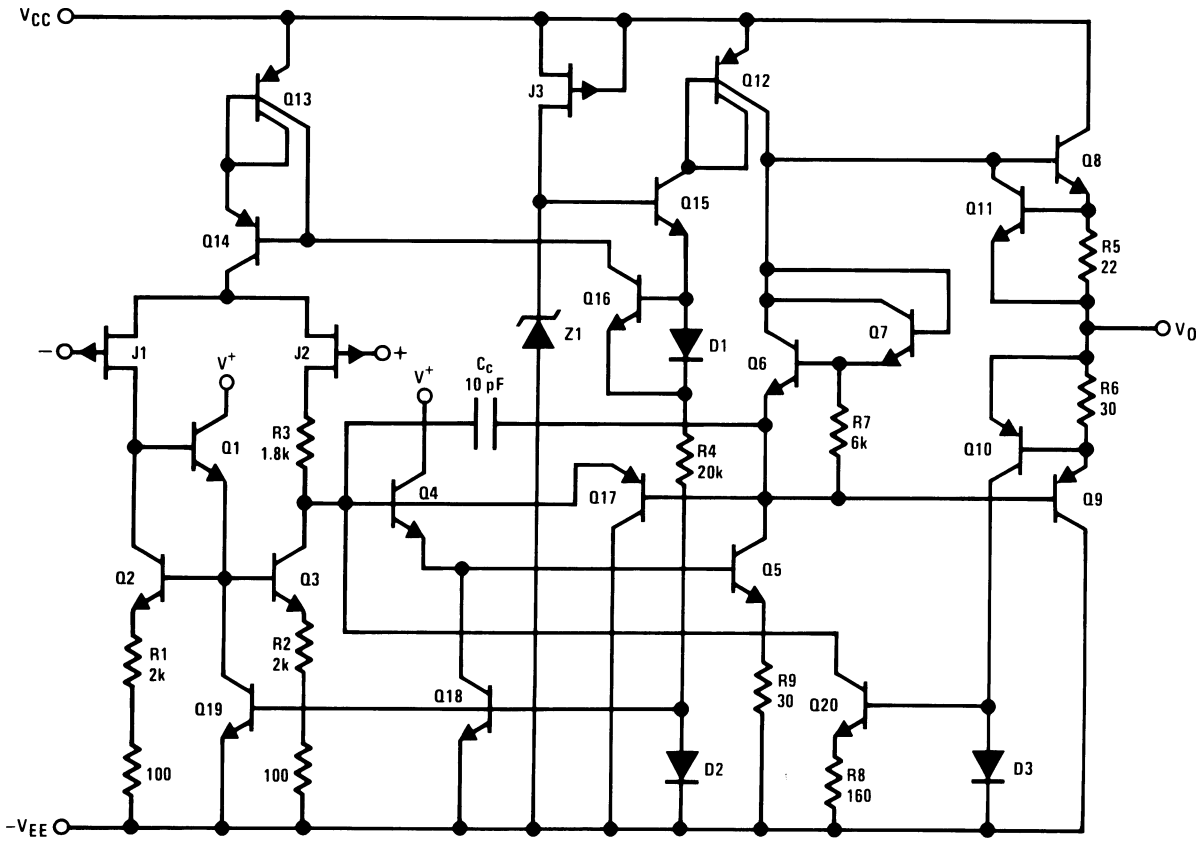
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

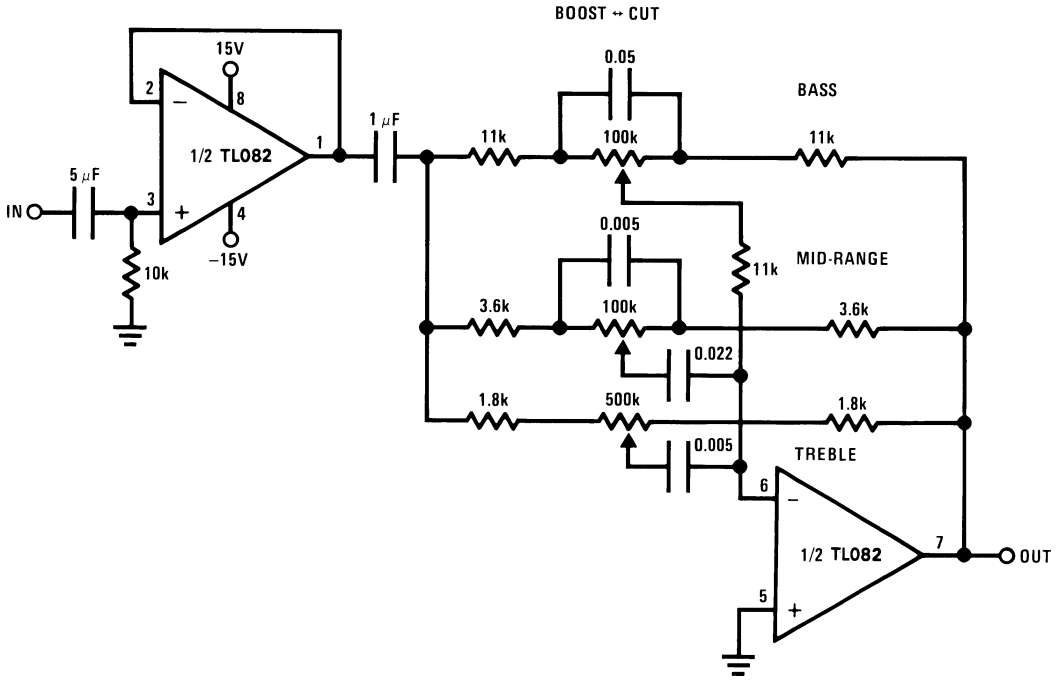
As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



Typical Applications



- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

All controls flat.

Bass and treble boost, mid flat.

Bass and treble cut, mid flat.

Mid boost, bass and treble flat.

Mid cut, bass and treble flat.

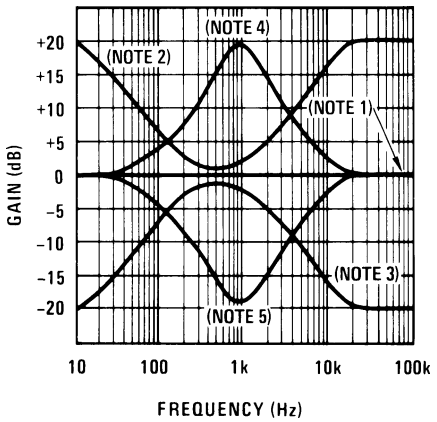
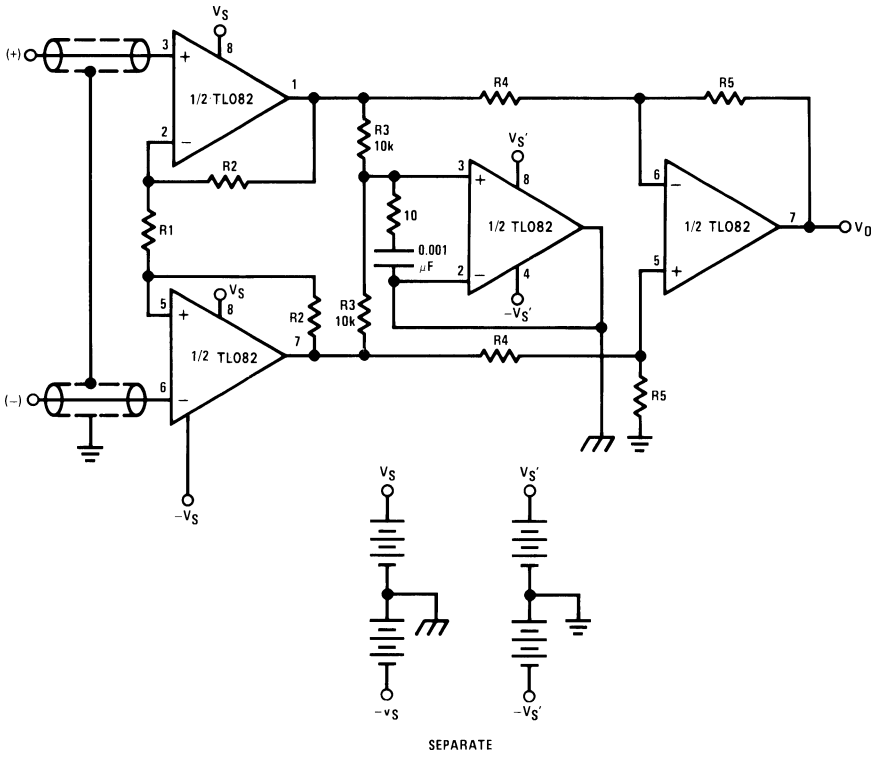


Figure 28. Three-Band Active Tone Control



$$A_V = \left(\frac{2R2}{R1} + 1\right)\frac{R5}{R4}$$

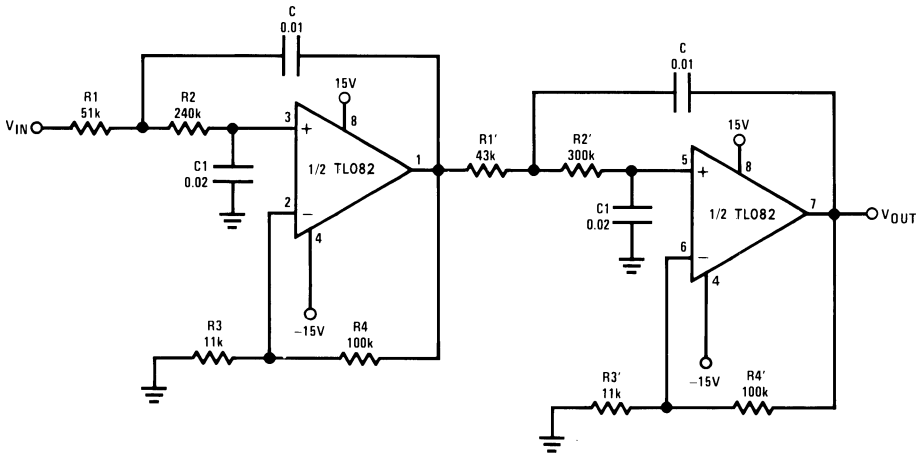
and are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With A_{VT} = 1400, resistor matching = 0.01%: CMRR = 136 dB

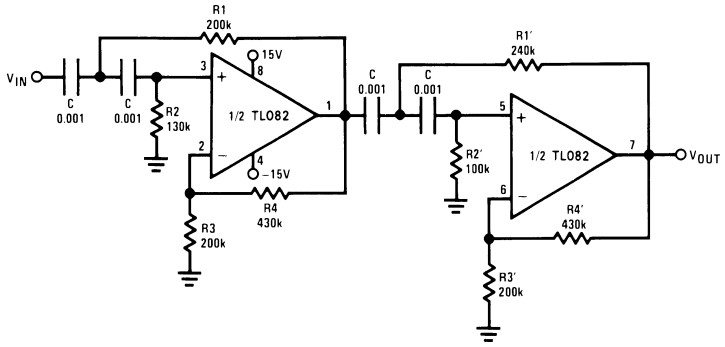
- Very high input impedance
- Super high CMRR

Figure 29. Improved CMRR Instrumentation Amplifier



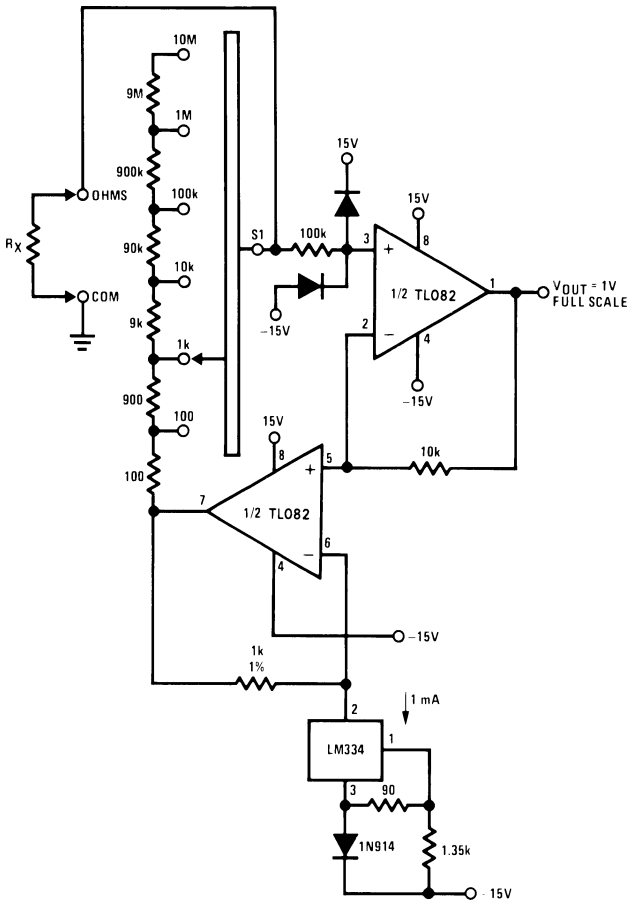
- Corner frequency (f_C) = $\sqrt{\frac{1}{R1R2CC1}} \bullet \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \bullet \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

Figure 30. Fourth Order Low Pass Butterworth Filter



- Corner frequency (f_C) = $\sqrt{\frac{1}{R1R2C^2}} \bullet \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \bullet \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10

Figure 31. Fourth Order High Pass Butterworth Filter



$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 7 of the TL082CP.

Figure 32. Ohms to Volts Converter

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL082CM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	0 to 70	TL 082CM	Samples
TL082CMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	0 to 70	TL 082CM	Samples
TL082CP/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	Call TI | SN	Level-1-NA-UNLIM	0 to 70	TL082 CP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL082-N :

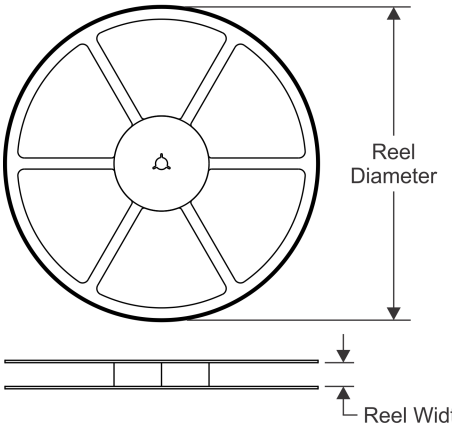
- Automotive: TL082-Q1

NOTE: Qualified Version Definitions:

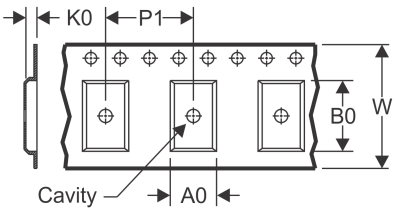
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

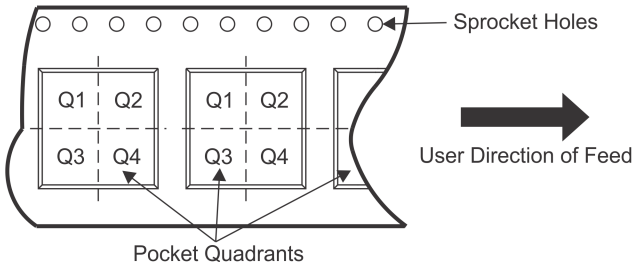


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

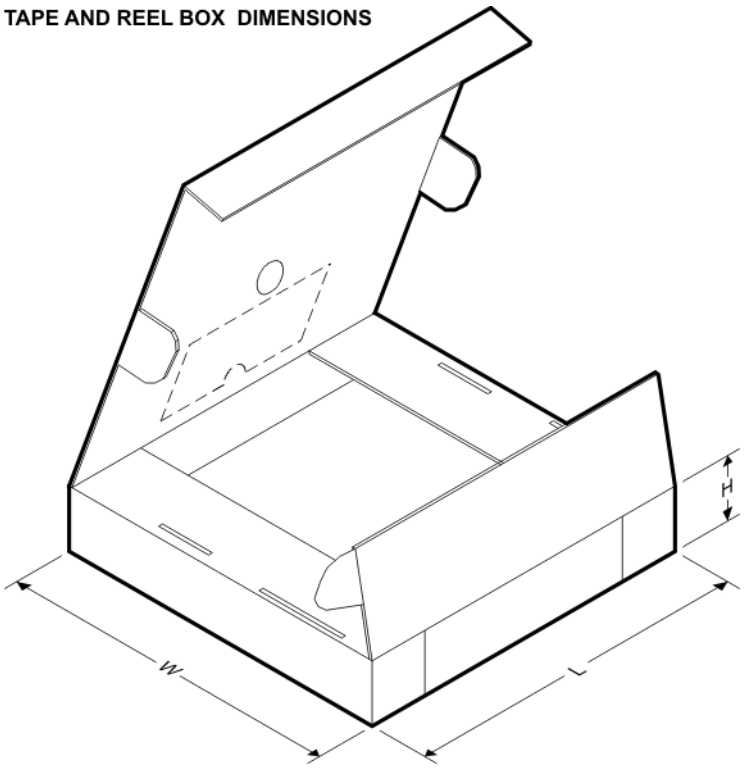
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

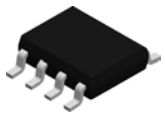
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL082CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL082CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

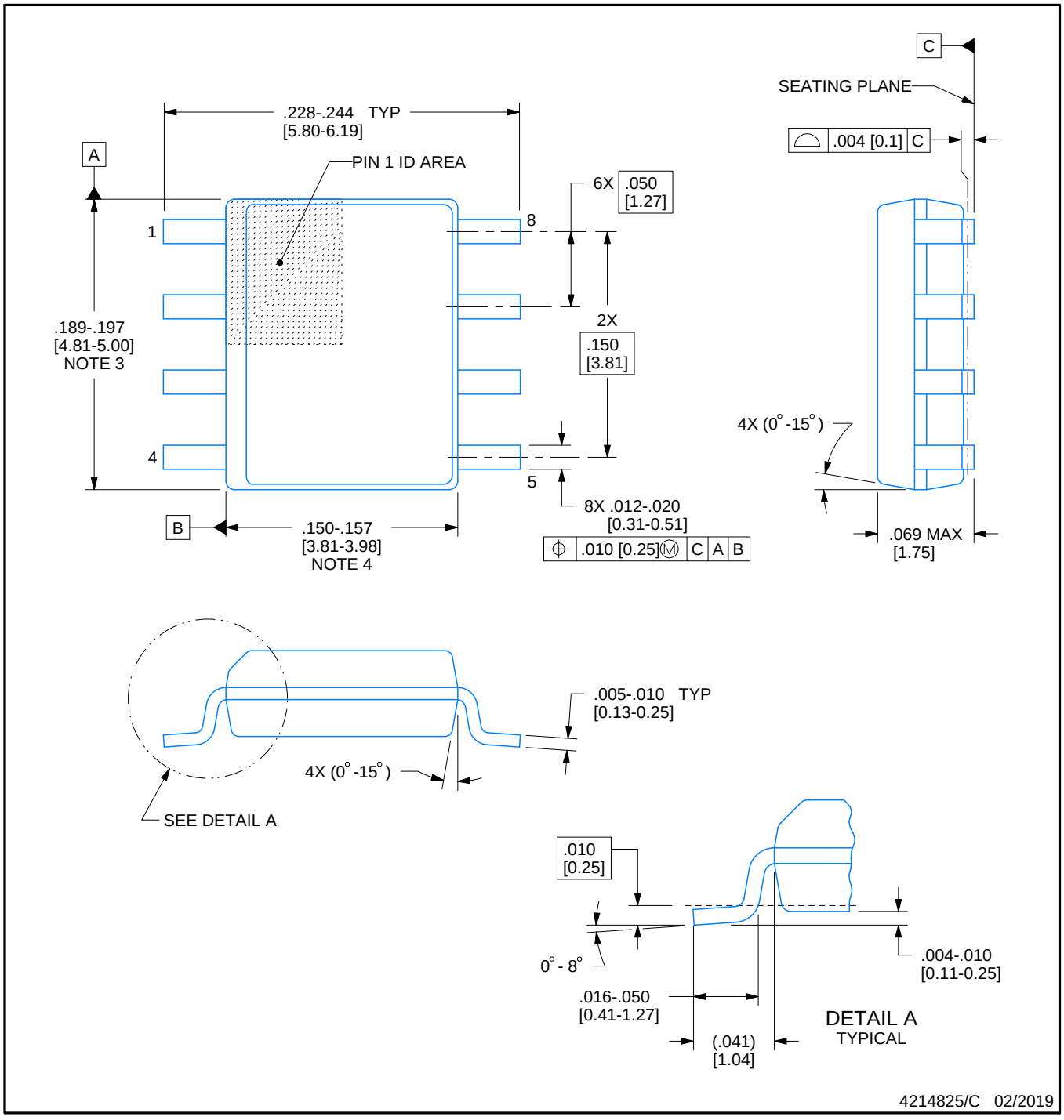


PACKAGE OUTLINE

D0008A

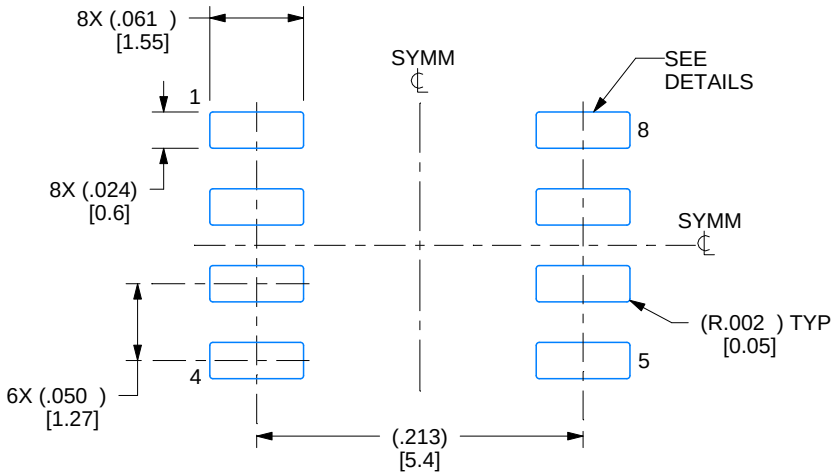
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

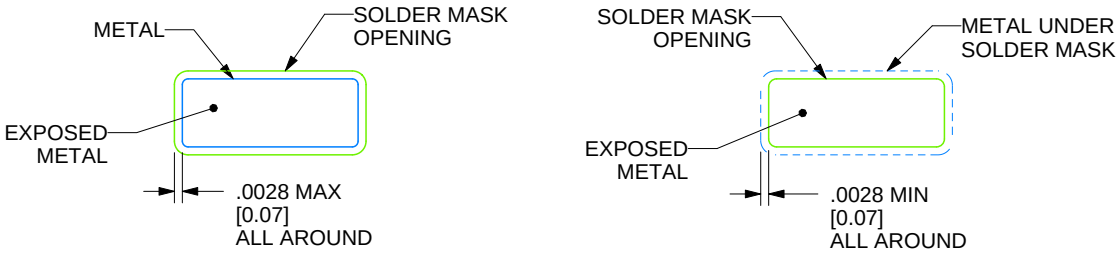


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

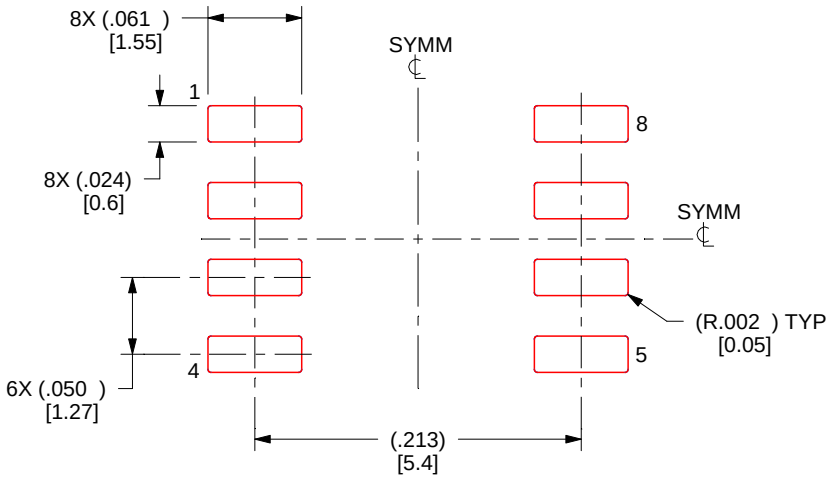
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



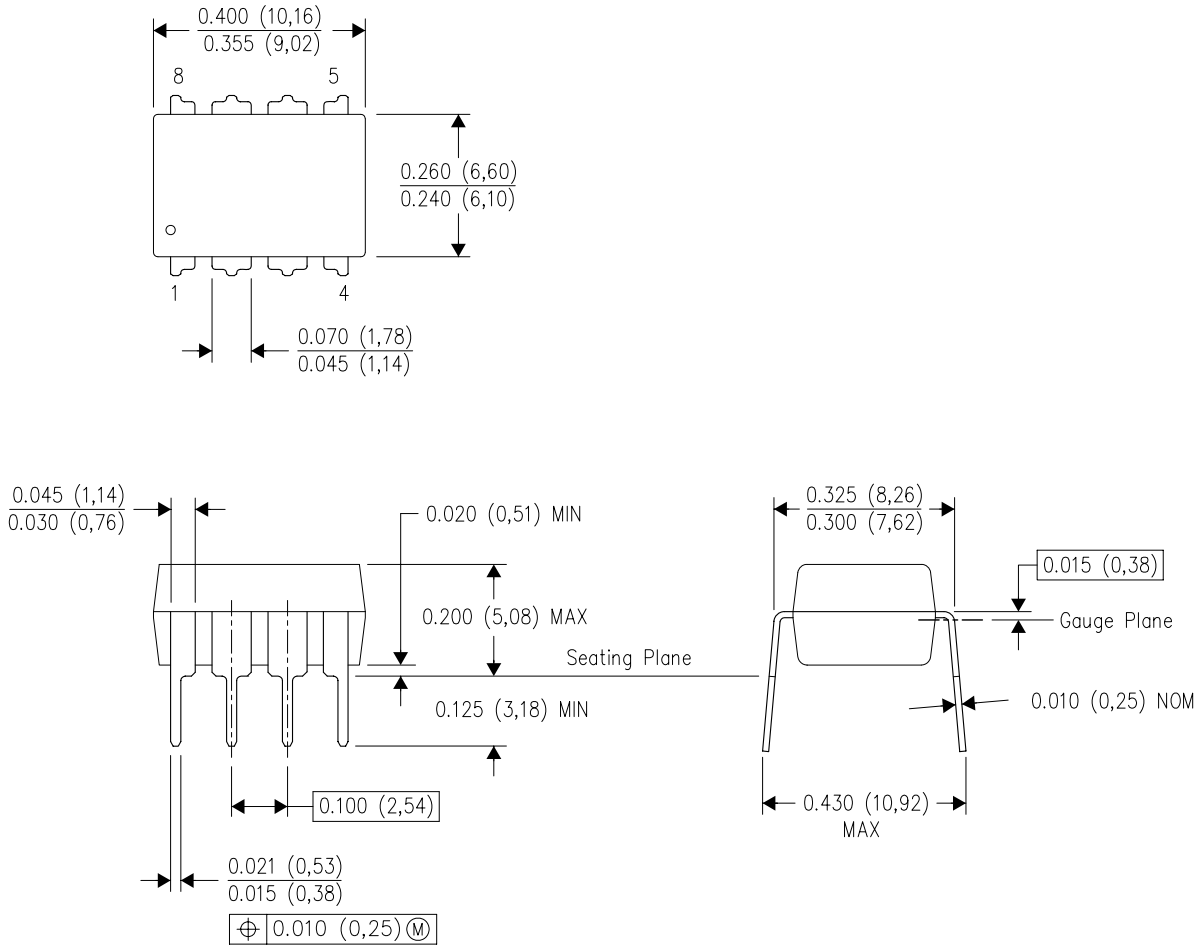
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Anexo XI.
Datasheet del TL084.

TL08xx FET-Input Operational Amplifiers

1 Features

- High slew rate: 20 V/µs (TL08xH, typ)
- Low offset voltage: 1 mV (TL08xH, typ)
- Low offset voltage drift: 2 µV/°C
- Low power consumption: 940 µA/ch (TL08xH, typ)
- Wide common-mode and differential voltage ranges
  - Common-mode input voltage range includes V_{CC+}
- Low input bias and offset currents
- Low noise: V_n = 18 nV/√Hz (typ) at f = 1 kHz
- Output short-circuit protection
- Low total harmonic distortion: 0.003% (typ)
- Wide supply voltage: ±2.25 V to ±20 V, 4.5 V to 40 V

2 Applications

- Solar energy: string and central inverter
- Motor drives: AC and servo drive control and power stage modules
- Single phase online UPS
- Three phase UPS
- Pro audio mixers
- Battery test equipment

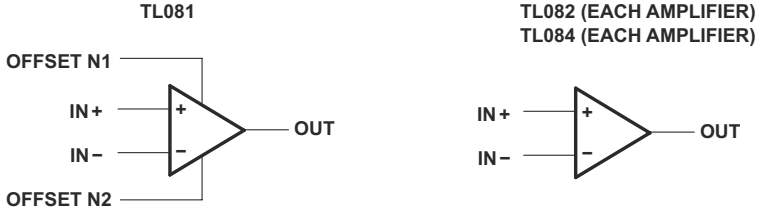
3 Description

The TL08xH (TL081H, TL082H, and TL084H) family of devices are the next-generation versions of the industry-standard TL08x (TL081, TL082, and TL084) devices. These devices provide outstanding value for cost-sensitive applications, with features including low offset (1 mV, typical), high slew rate (20 V/µs), and common-mode input to the positive supply. High ESD (1.5 kV, HBM), integrated EMI and RF filters, and operation across the full –40°C to 125°C enable the TL08xH devices to be used in the most rugged and demanding applications.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TL081x	PDIP (8)	9.59 mm × 6.35 mm
	SC70 (5)	2.00 mm × 1.25 mm
	SO (8)	6.20 mm × 5.30 mm
	SOIC (8)	4.90 mm × 3.90 mm
	SOT-23 (5)	1.60 mm × 1.20 mm
TL082x	PDIP (8)	9.59 mm × 6.35 mm
	SO (8)	6.20 mm × 5.30 mm
	SOIC (8)	4.90 mm × 3.90 mm
	SOT-23 (8)	2.90 mm × 1.60 mm
	TSSOP (8)	4.40 mm × 3.00 mm
	VSSOP (8)	3.00 mm × 3.00 mm
TL082M	CDIP (8)	9.59 mm × 6.67 mm
	LCCC (20)	8.89 mm × 8.89 mm
TL084x	PDIP (14)	19.30 mm × 6.35 mm
	SO (14)	10.30 mm × 5.30 mm
	SOIC (14)	8.65 mm × 3.91 mm
	SOT-23 (14)	4.20 mm × 2.00 mm
	TSSOP (14)	5.00 mm × 4.40 mm
TL084M	CDIP (14)	19.56 mm × 6.92 mm
	LCCC (20)	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Symbols

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

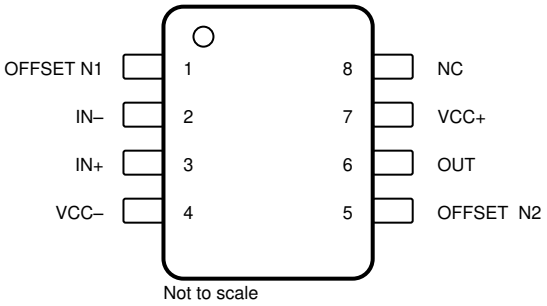
Changes from Revision I (May 2015) to Revision J (November 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added TL08xH devices throughout the data sheet	1
• Added features for TL08xH to the *Features* section	1
• Added link to applications in the *Applications* section	1
• Added TL08xH in the *Description* section	1
• Added TL08xH in the *Device Information* table	1
• Updated pinout diagrams and pinout tables in *Pin Configurations and Functions* section	4
• Added TSSOP, VSSOP and DDF packages to TL082x in *Pin Configuration and Functions* section	4
• Added DYY package to TL084x in *Pin Configuration and Functions* section	4
• Added *Typical Characteristics:TL08xH* section in *Specifications* section	17
• Removed Table of Graphs in *Typical Characteristics: All Other Devices* section	24
• Removed references to obsolete documentation	34

Changes from Revision H (January 2014) to Revision I (May 2015)	Page
• Added *Applications* section, *Device Information* table, Pin Functions table, Thermal Information table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, ESD information, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added *Applications*	1
• Moved *Typical Characteristics* into *Specifications* section.	24

Changes from Revision G (September 2004) to Revision H (January 2014) **Page**

- Deleted *Ordering Information* table....1

5 Pin Configuration and Functions



NC- no internal connection

Figure 5-1. TL081x D, P, and PS Package
8-Pin SOIC, PDIP, and SO
Top View

Table 5-1. Pin Functions: TL081x

PIN		I/O	DESCRIPTION
NAME	NO.		
IN–	2	I	Inverting input
IN+	3	I	Noninverting input
NC	8	—	Do not connect
OFFSET N1	1	—	Input offset adjustment
OFFSET N2	5	—	Input offset adjustment
OUT	6	O	Output
VCC–	4	—	Power supply
VCC+	7	—	Power supply

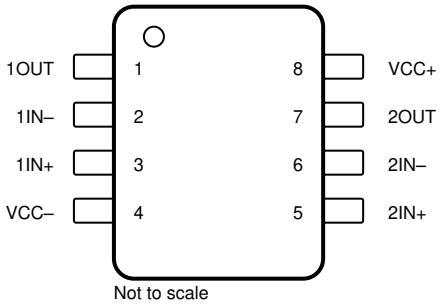
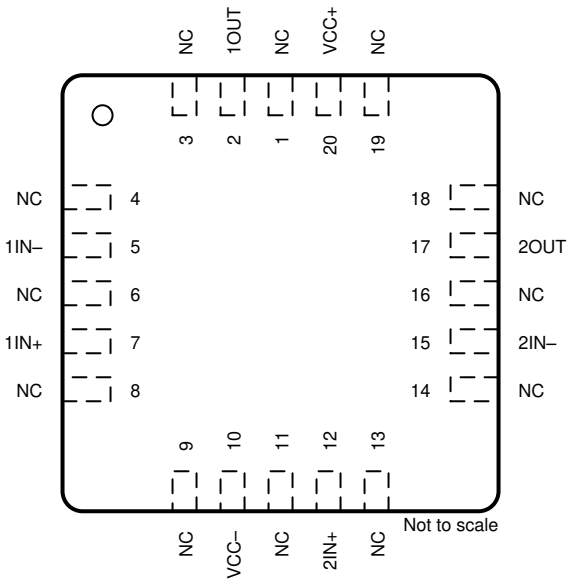


Figure 5-2. TL082x D, DDF, DGK, JG, P, PS, and PW Package 8-Pin SOIC, SOT-23 (8), VSSOP, CDIP, PDIP, SO, and TSSOP Top View

Table 5-2. Pin Functions: TL082x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN–	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
VCC–	4	—	Power supply
VCC+	8	—	Power supply



NC- no internal connection

Figure 5-3. TL082 FK Package
20-Pin LCCC
Top View

Table 5-3. Pin Functions: TL082x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	5	I	Inverting input
1IN+	7	I	Noninverting input
1OUT	2	O	Output
2IN–	15	I	Inverting input
2IN+	12	I	Noninverting input
2OUT	17	O	Output
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	Do not connect
VCC–	10	—	Power supply
VCC+	20	—	Power supply

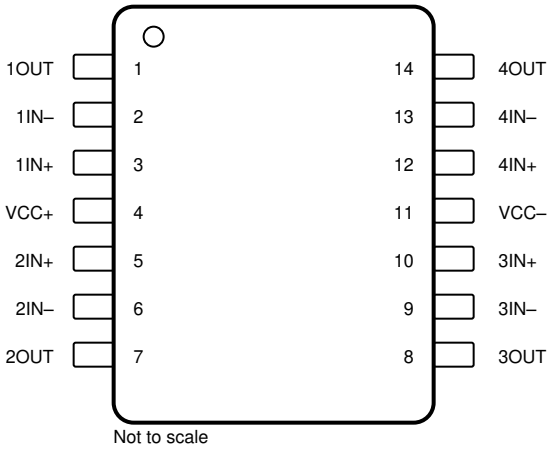
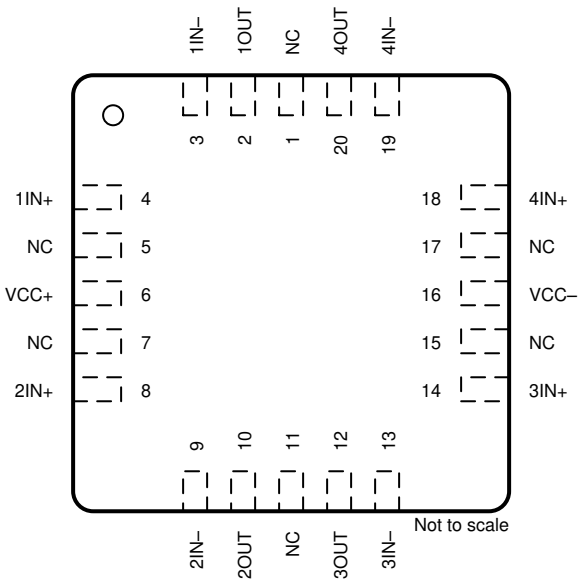


Figure 5-4. TL084x D, N, NS, PW, J, and DYY Packages
14-Pin SOIC, PDIP, SO, TSSOP, CDIP, and SOT-23 (14)
Top View

Table 5-4. Pin Functions: TL084x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN–	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
3IN–	9	I	Inverting input
3IN+	10	I	Noninverting input
3OUT	8	O	Output
4IN–	13	I	Inverting input
4IN+	12	I	Noninverting input
4OUT	14	O	Output
V_{CC-}	11	—	Power supply
V_{CC+}	4	—	Power supply



NC- no internal connection

Figure 5-5. TL084 FK Package
20-Pin LCCC
Top View

Table 5-5. Pin Functions: TL084x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	3	I	Inverting input
1IN+	4	I	Noninverting input
1OUT	2	O	Output
2IN–	9	I	Inverting input
2IN+	8	I	Noninverting input
2OUT	10	O	Output
3IN–	13	I	Inverting input
3IN+	14	I	Noninverting input
3OUT	12	O	Output
4IN–	19	I	Inverting input
4IN+	18	I	Noninverting input
4OUT	20	O	Output
NC	1, 5, 7, 11, 15, 17	—	Do not connect
VCC–	16	—	Power supply
VCC+	6	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings: TL08xH

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, $V_S = (V_{CC+}) - (V_{CC-})$		0	42	V
Signal input pins	Common-mode voltage (3)	$(V_{CC-}) - 0.5$	$(V_{CC+}) + 0.5$	V
	Differential voltage (3)		$V_S + 0.2$	V
	Current (3)	–10	10	mA
Output short-circuit (2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

6.2 Absolute Maximum Ratings: All Other Devices

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage(2)	-18	18	V
V_{ID}	Differential input voltage(3)	-30	+30	V
V_I	Input voltage(2) (4)	-15	+15	V
	Duration of output short circuit(5)	Unlimited		
	Continuous total power dissipation	See *Section 6.15*		
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+, with respect to IN−.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

6.3 ESD Ratings: TL08xH

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 ESD Ratings: All Other Devices

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.5 Recommended Operating Conditions: TL08xH

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, $(V_{CC+}) – (V_{CC–})$	4.5	40	V
V_I	Input voltage range	$(V_{CC–}) + 2$	$(V_{CC+}) + 0.1$	V
T_A	Specified temperature	–40	125	°C

6.6 Recommended Operating Conditions: All Other Devices

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
$V_{CC–}$	Supply voltage		–5	–15	V
V_{CM}	Common-mode voltage		$V_{CC–} + 4$	$V_{CC+} – 4$	V
T_A	Ambient temperature	TL08xM	–55	125	°C
		TL08xQ	–40	125	
		TL08xI	–40	85	
		TL08xC	0	70	

6.7 Thermal Information for Single Channel: TL081H

THERMAL METRIC [1]		TL081H		UNIT
		D [2] (SOIC)	DBV [2] (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) This package option is preview for TL081H.

6.8 Thermal Information for Dual Channel: TL082H

THERMAL METRIC [1]		TL082H			UNIT
		D [2] (SOIC)	DGK [2] (VSSOP)	PW [2] (TSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	TBD	°C/W

THERMAL METRIC (1)		TL082H			UNIT
		D (2) (SOIC)	DGK (2) (VSSOP)	PW (2) (TSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	TBD	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

(2) This package option is preview for TL082H.

6.9 Thermal Information for Quad Channel: TL084H

THERMAL METRIC (1)		TL084H		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.2	134.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.3	62.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.2	77.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28.8	13.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.8	77.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.10 Thermal Information: All Other Devices

THERMAL METRIC(1)		TL08xxx										UNIT
		D (SOIC)		FK (LCCC)	J (CDIP)		N (PDIP)		NS (SO)		PW (TSSOP)	
		8 PIN	14 PIN	20 PIN	8 PIN	14 PIN	8 PIN	14 PIN	8 PIN	14 PIN	8 PIN	14 PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	86				85	80	95	76	150	113	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance			5.61	15.05	14.5							

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.11 Electrical Characteristics: TL08xH

For $V_S = (V_{CC+}) – (V_{CC–}) = 4.5$ V to 40 V (±2.25 V to ±20 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{O\ UT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±1	±4	mV
			T_A = –40°C to 125°C			±5	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±2		µV/°C
PSRR	Input offset voltage versus power supply	V_S = 5 V to 40 V, $V_{CM} = V_S / 2$	T_A = –40°C to 125°C		±1	±10	µV/V
	Channel separation	f = 0 Hz			10		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±1	±120	pA
			T_A = –40°C to 125°C (1)			±5	nA
I_{OS}	Input offset current				±0.5	±120	pA
			T_A = –40°C to 125°C (1)			±5	nA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			9.2		μV_{PP}
					1.4		μV_{RMS}
e_N	Input voltage noise density	f = 1 kHz			37		$nV/\sqrt{Hz}$
		f = 10 kHz			21		
i_N	Input current noise	f = 1 kHz			80		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			$(V_{CC–}) + 1.5$		(V_{CC+})	V
CMRR	Common-mode rejection ratio	V_S = 40 V, $(V_{CC–}) + 2.5$ V < V_{CM} < $(V_{CC+}) – 1.5$ V		100	105		dB
CMRR	Common-mode rejection ratio		T_A = –40°C to 125°C	95			dB
CMRR	Common-mode rejection ratio	V_S = 40 V, $(V_{CC–}) + 2.5$ V < V_{CM} < (V_{CC+})		90	105		dB
CMRR	Common-mode rejection ratio		T_A = –40°C to 125°C	80			dB
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 2		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40 V, $V_{CM} = V_S / 2$, $(V_{CC–}) + 0.3$ V < V_O < $(V_{CC+}) – 0.3$ V	T_A = –40°C to 125°C	118	125		dB
A_{OL}	Open-loop voltage gain	V_S = 40 V, $V_{CM} = V_S / 2$, R_L = 2 kΩ, $(V_{CC–}) + 1.2$ V < V_O < $(V_{CC+}) – 1.2$ V	T_A = –40°C to 125°C	115	120		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				5.25		MHz
SR	Slew rate	V_S = 40 V, G = +1, C_L = 20 pF			20		V/µs

For V_S = (V_{CC+}) – ($V_{CC–}$) = 4.5 V to 40 V (±2.25 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_S	Settling time	To 0.1%, V_S = 40 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			0.63		µs
		To 0.1%, V_S = 40 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			0.56		
		To 0.01%, V_S = 40 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			0.91		
		To 0.01%, V_S = 40 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			0.48		
	Phase margin	G = +1, R_L = 10kΩ, C_L = 20 pF			56		°
	Overload recovery time	V_{IN} × gain > V_S			300		ns
THD+N	Total harmonic distortion + noise	V_S = 40 V, V_O = 6 V_{RMS}, G = +1, f = 1 kHz			0.00012		%
EMIRR	EMI rejection ratio	f = 1 GHz			53		dB
OUTPUT							
	Voltage output swing from rail	Positive rail headroom	V_S = 40 V, R_L = 10 kΩ		115	210	mV
			V_S = 40 V, R_L = 2 kΩ		520	965	
		Negative rail headroom	V_S = 40 V, R_L = 10 kΩ		105	215	
			V_S = 40 V, R_L = 2 kΩ		500	1030	
I_{SC}	Short-circuit current				±26		mA
C_{LOAD}	Capacitive load drive				300		pF
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			125		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			937.5	1125	µA
			T_A = –40°C to 125°C			1130	
	Turn-On Time	At T_A = 25°C, V_S = 40 V, V_S ramp rate > 0.3 V/µs			60		µs

(1) Max I_B and I_{os} data is specified based on characterization results.

6.12 Electrical Characteristics for TL08xC, TL08xxC, and TL08xI

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	TL081C, TL082C, TL084C			TL081AC, TL082AC, TL084AC			TL081BC, TL082BC, TL084BC			TL081I, TL082I, TL084I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	15		3	6		2	3		3	6	mV
			Full range			20			7.5			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18			18			18		μV/°C
I_{IO}	Input offset current(2)	V_O = 0	25°C		5	200		5	100		5	100		5	100	pA
			Full range			2			2			2			10	nA
I_{IB}	Input bias current(2)	V_O = 0	25°C		30	400		30	200		30	200		30	200	pA
			Full range			10			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	–12 to 15		±11	–12 to 15		±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ		±10	±12		±10	±12		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
			Full range	15			15			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	70	86		75	86		75	86		75	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω	25°C	70	86		80	86		80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120			120			120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range for T_A is 0°C to 70°C for TL08_C, TL08_AC, TL08_BC and –40°C to 85°C for TL08_I.

(2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 6-52. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

6.13 Electrical Characteristics for TL08xM and TL084x

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]	T_A	TL081M, TL082M			TL084Q, TL084M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18		µV/°C
I_{IO}	Input offset current[2]	V_O = 0	25°C		5	100		5	100	pA
			125°C			20			20	nA
I_{IB}	Input bias current[2]	V_O = 0	25°C		30	200		30	200	pA
			125°C			50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L ≥ 2 kΩ		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		25	200		V/mV
			Full range	15			15			
B_1	Unity-gain bandwidth		25°C		3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120		dB

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.

(2) Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 6-52. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as possible.

6.14 Switching Characteristics

$V_{CC±}$ = ±15 V, T_A= 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, see Figure 7-1		8[1]	13		V/µs
		V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, T_A = −55°C to 125°C, see Figure 7-1		5[1]			
t_r	Rise-time	V_I = 20 V, R_L = 2 kΩ, C_L = 100 pF, see Figure 7-1			0.05		µs
	overshoot factor				20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		µV
I_n	Equivalent input noise current	R_S = 20 Ω	f = 1 kHz		0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, A_{VD} = 1, R_S ≤ 1 kΩ, R_L ≥ 2 kΩ, f = 1 kHz			0.003%		

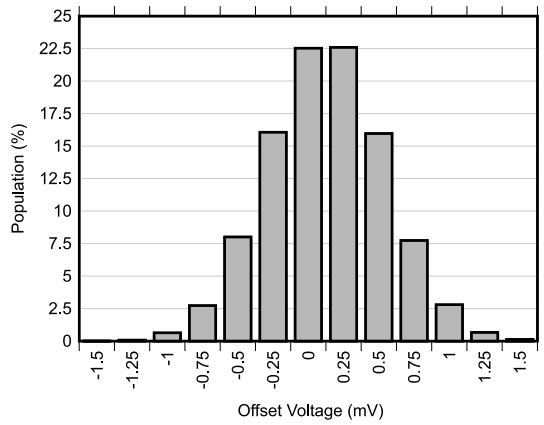
(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.15 Dissipation Rating Table

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 m/W	490 mW	186 mW
FK	680 mW	11.0 mW/°C	88°C	680 m/W	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 m/W	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 m/W	546 mW	210 mW

6.16 Typical Characteristics: TL08xH

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)



T_A = 25°C

Figure 6-1. Offset Voltage Production Distribution

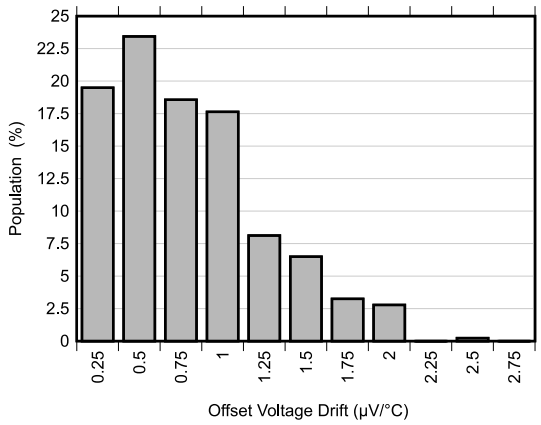
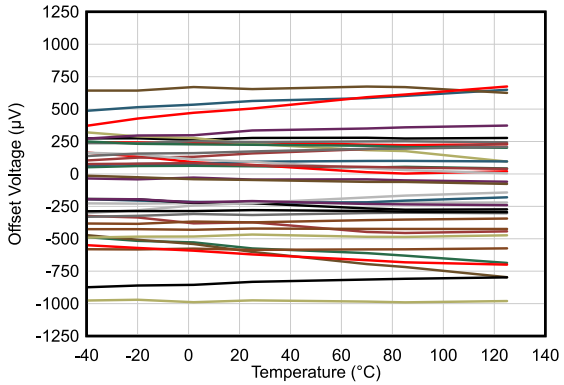
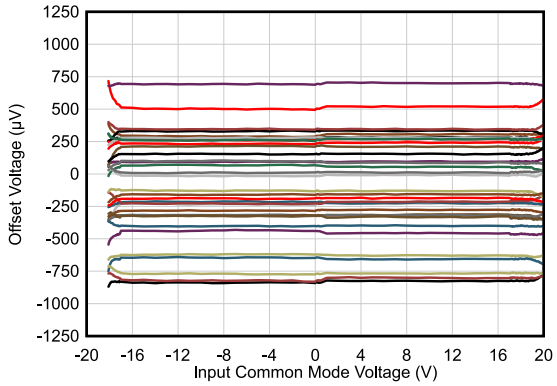


Figure 6-2. Offset Voltage Drift Distribution



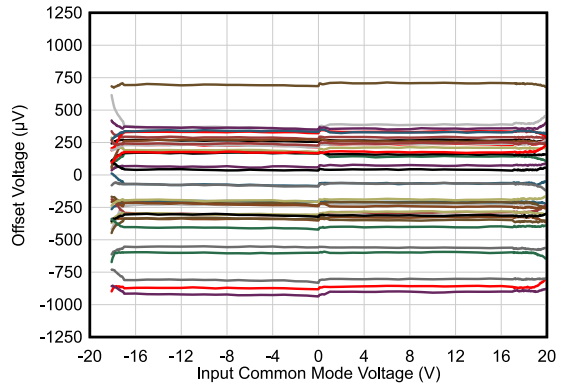
V_{CM} = V_S / 2

Figure 6-3. Offset Voltage vs Temperature



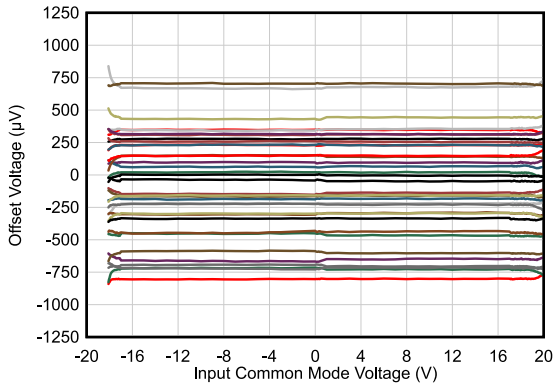
T_A = 25°C

Figure 6-4. Offset Voltage vs Common-Mode Voltage



T_A = 125°C

Figure 6-5. Offset Voltage vs Common-Mode Voltage



T_A = –40°C

Figure 6-6. Offset Voltage vs Common-Mode Voltage

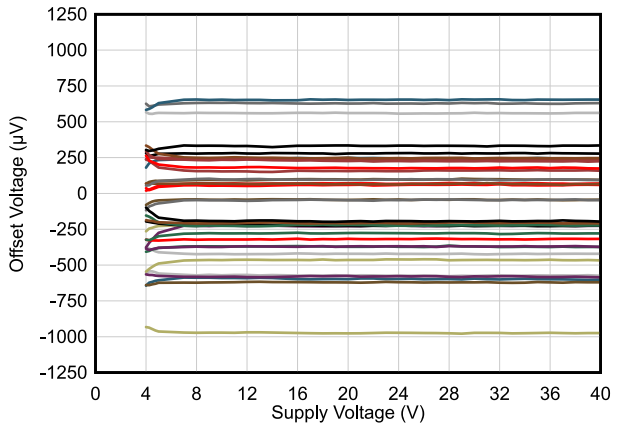


Figure 6-7. Offset Voltage vs Power Supply

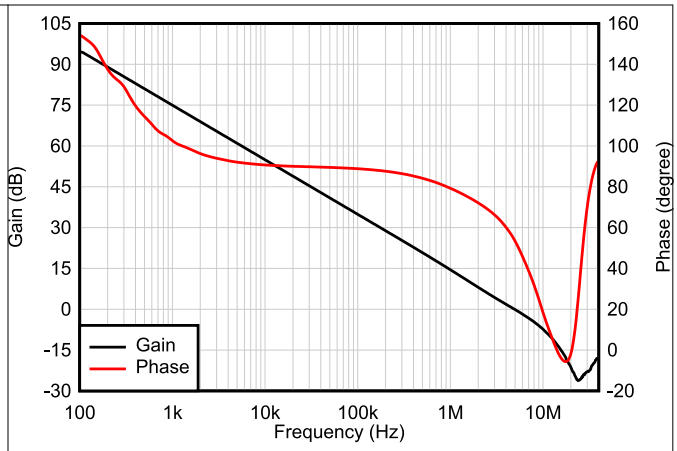


Figure 6-8. Open-Loop Gain and Phase vs Frequency

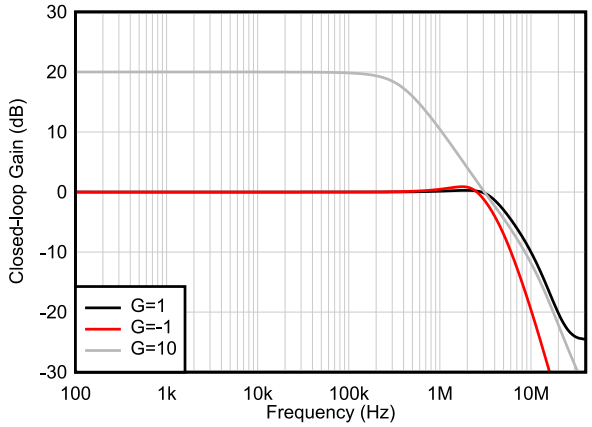


Figure 6-9. Closed-Loop Gain vs Frequency

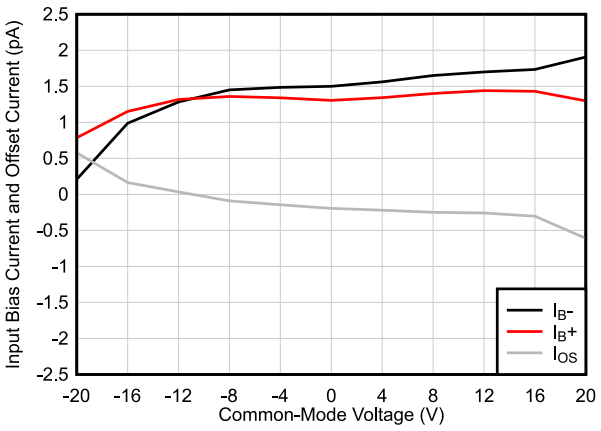


Figure 6-10. Input Bias Current vs Common-Mode Voltage

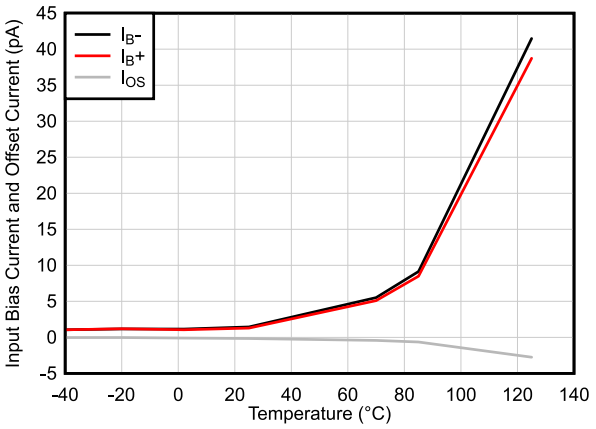


Figure 6-11. Input Bias Current vs Temperature

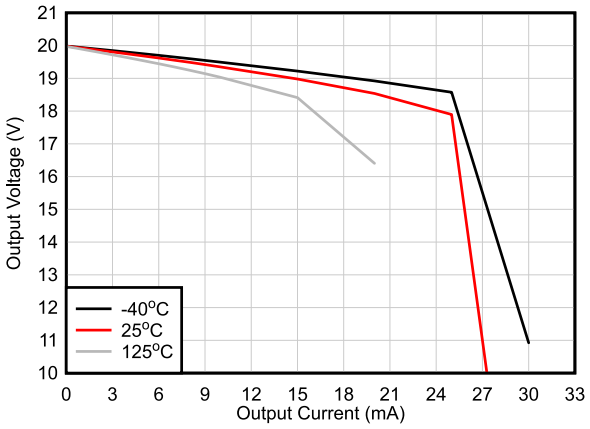


Figure 6-12. Output Voltage Swing vs Output Current (Sourcing)

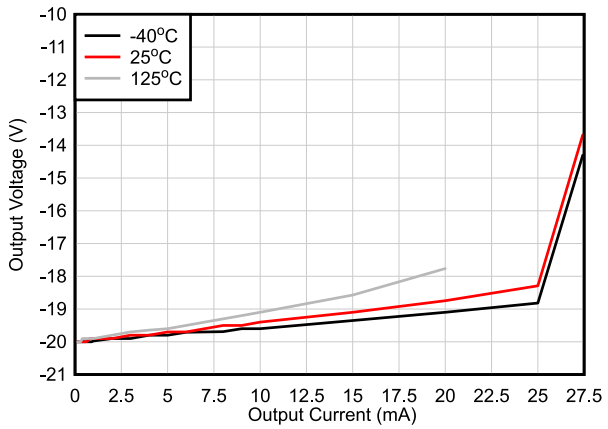


Figure 6-13. Output Voltage Swing vs Output Current (Sinking)

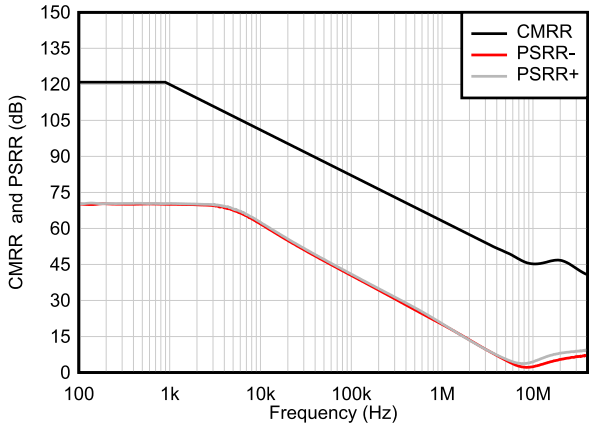
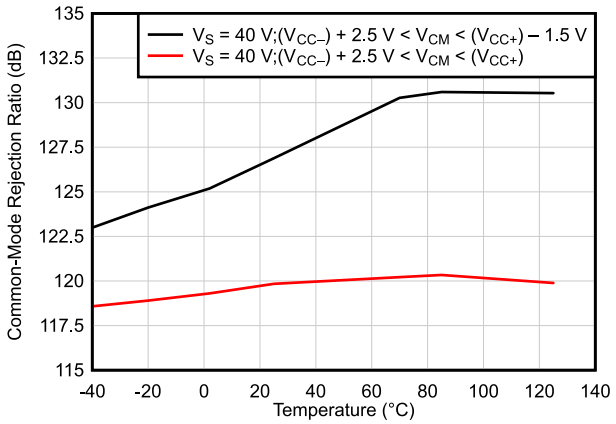
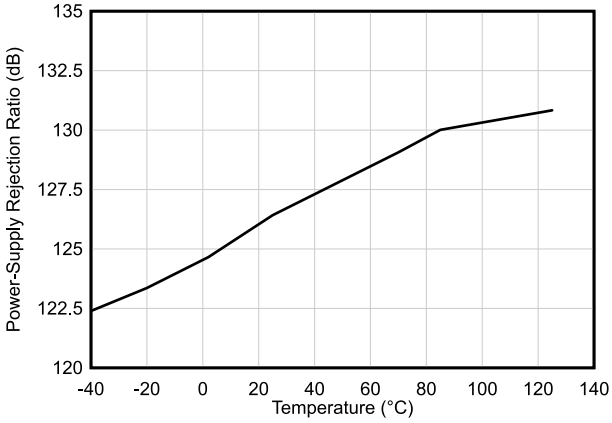


Figure 6-14. CMRR and PSRR vs Frequency



f = 0 Hz

Figure 6-15. CMRR vs Temperature (dB)



f = 0 Hz

Figure 6-16. PSRR vs Temperature (dB)

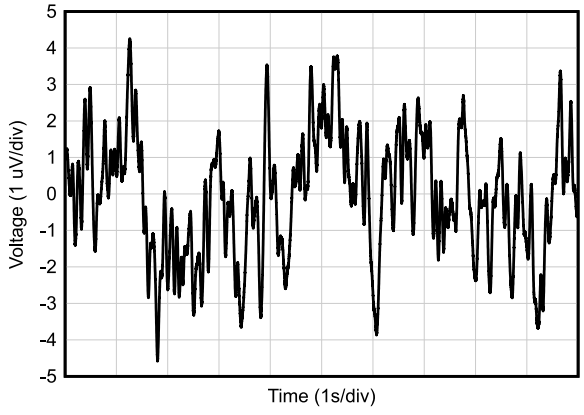


Figure 6-17. 0.1-Hz to 10-Hz Noise

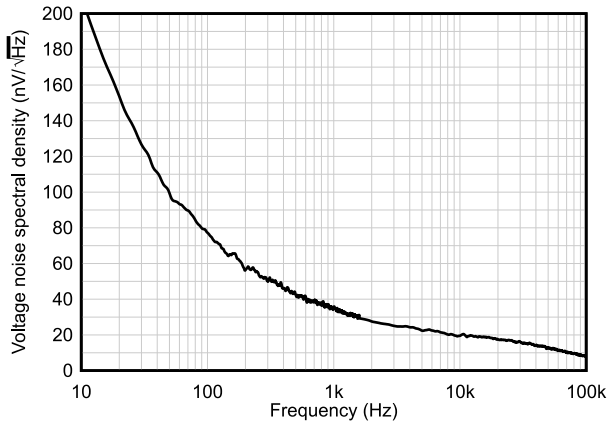
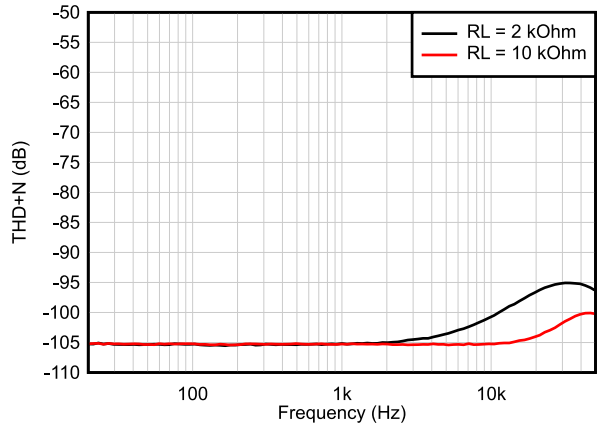
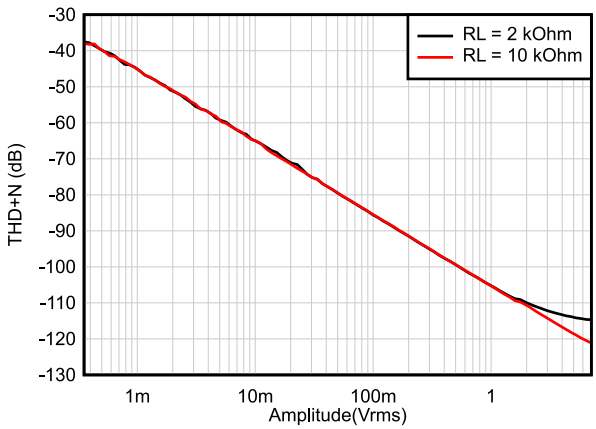


Figure 6-18. Input Voltage Noise Spectral Density vs Frequency



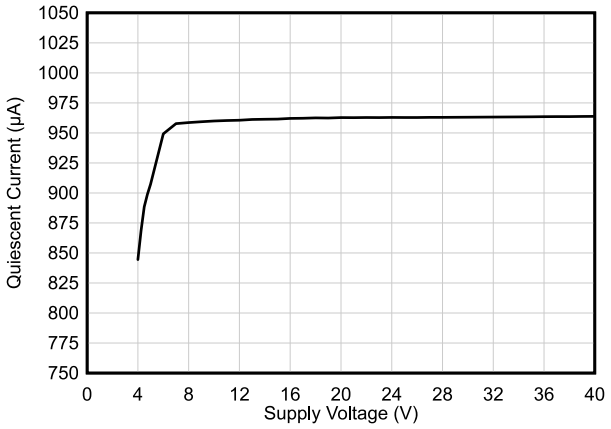
BW = 80 kHz, V_{OUT} = 1 V_{RMS}

Figure 6-19. THD+N Ratio vs Frequency



BW = 80 kHz, f = 1 kHz

Figure 6-20. THD+N vs Output Amplitude



V_{CM} = V_S / 2

Figure 6-21. Quiescent Current vs Supply Voltage

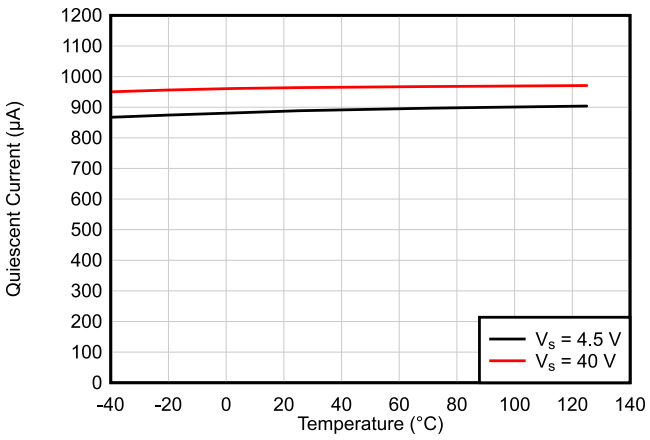


Figure 6-22. Quiescent Current vs Temperature

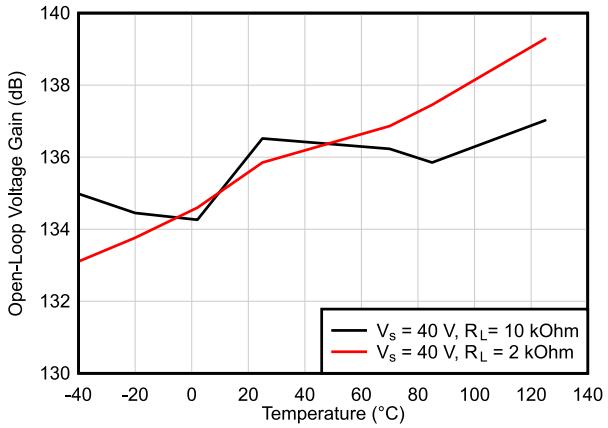


Figure 6-23. Open-Loop Voltage Gain vs Temperature (dB)

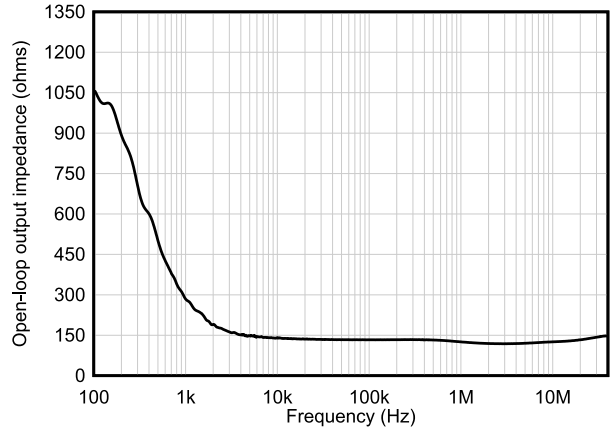
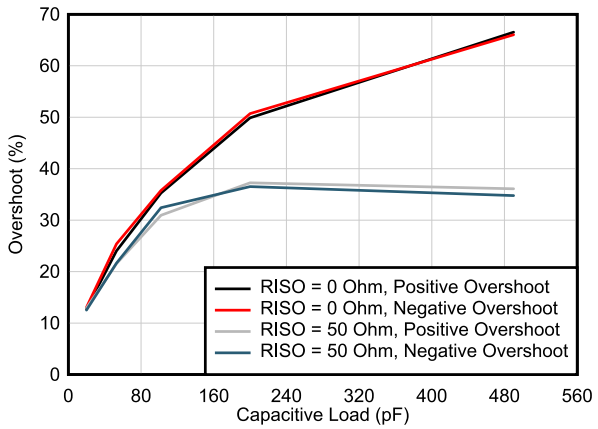
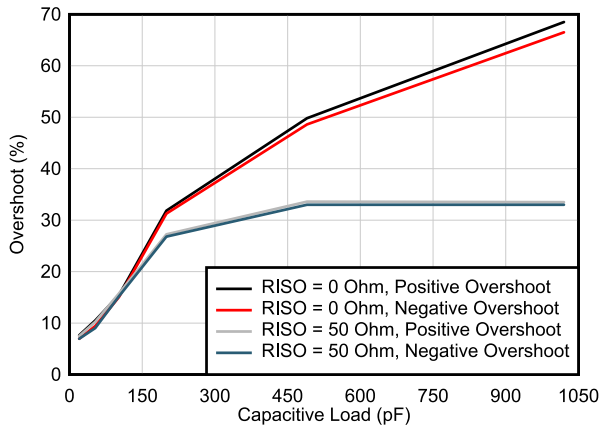


Figure 6-24. Open-Loop Output Impedance vs Frequency



G = –1, 25-mV output step

Figure 6-25. Small-Signal Overshoot vs Capacitive Load



G = 1, 10-mV output step

Figure 6-26. Small-Signal Overshoot vs Capacitive Load

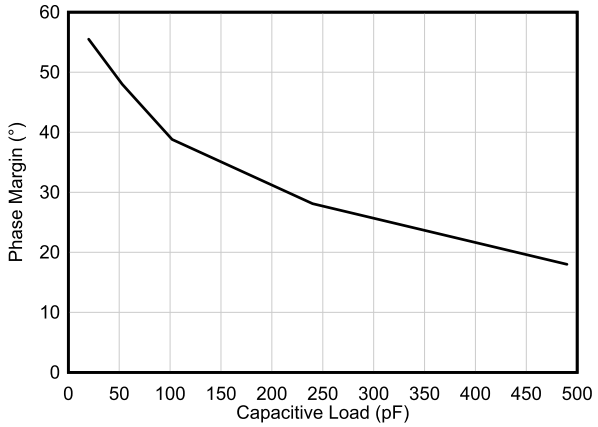
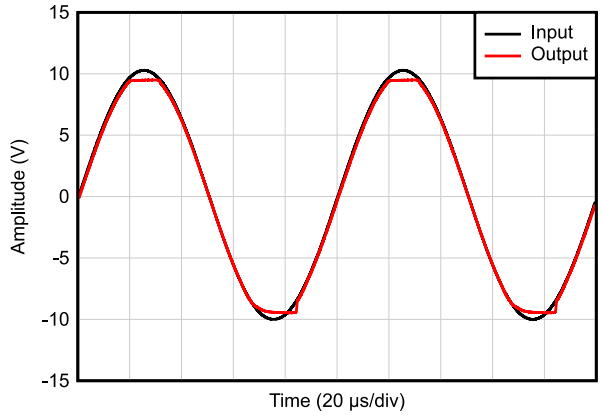
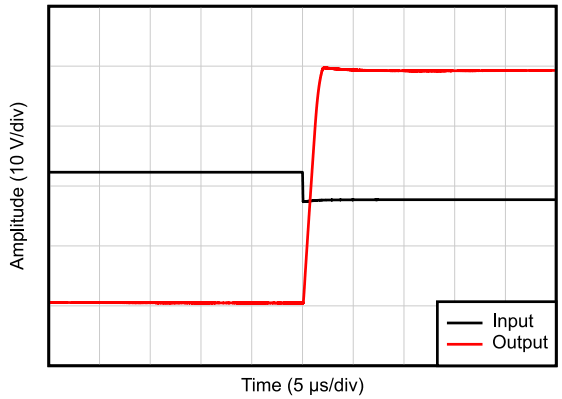


Figure 6-27. Phase Margin vs Capacitive Load



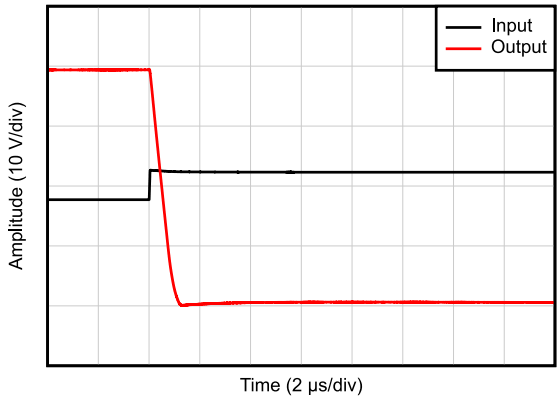
V_S = ±10 V, V_{IN} = V_{OUT}

Figure 6-28. No Phase Reversal



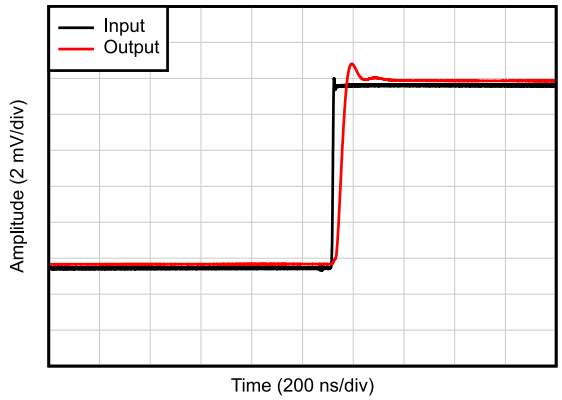
G = –10

Figure 6-29. Positive Overload Recovery



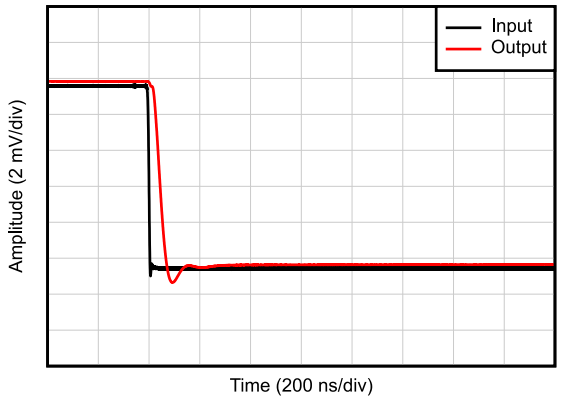
G = –10

Figure 6-30. Negative Overload Recovery



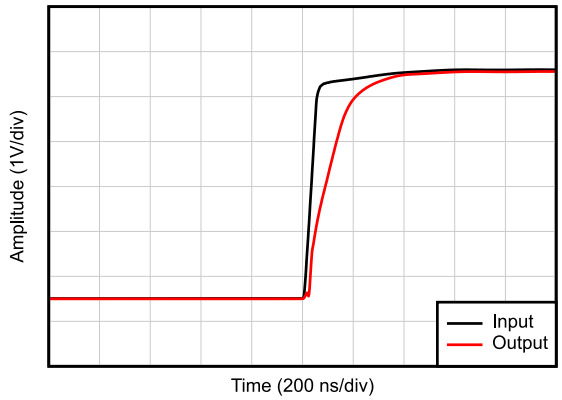
C_L = 20 pF, G = 1, 10-mV step response

Figure 6-31. Small-Signal Step Response, Rising



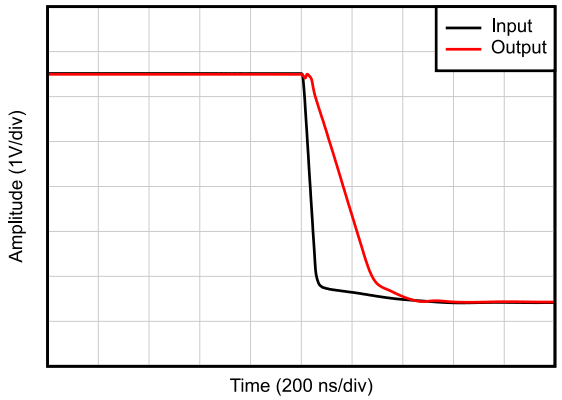
C_L = 20 pF, G = 1, 10-mV step response

Figure 6-32. Small-Signal Step Response, Falling



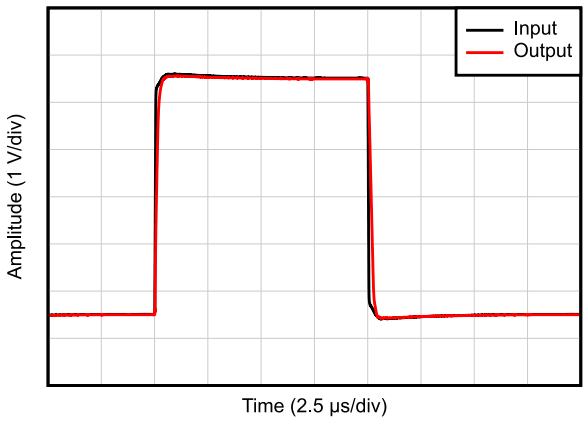
C_L = 20 pF, G = 1

Figure 6-33. Large-Signal Step Response (Rising)



C_L = 20 pF, G = 1

Figure 6-34. Large-Signal Step Response (Falling)



C_L = 20 pF, G = 1

Figure 6-35. Large-Signal Step Response

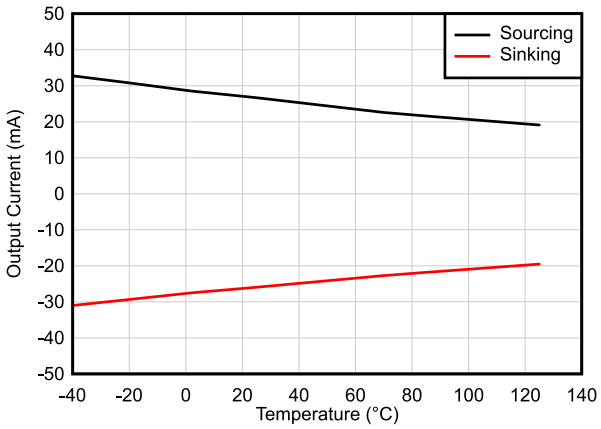


Figure 6-36. Short-Circuit Current vs Temperature

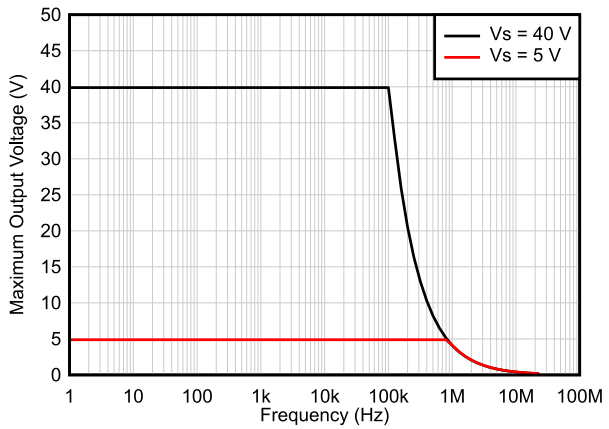


Figure 6-37. Maximum Output Voltage vs Frequency

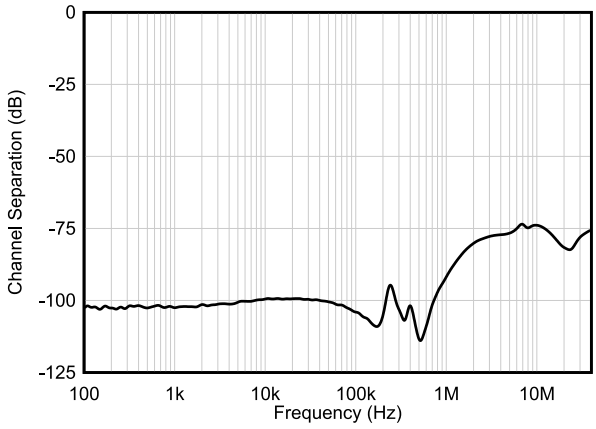


Figure 6-38. Channel Separation vs Frequency

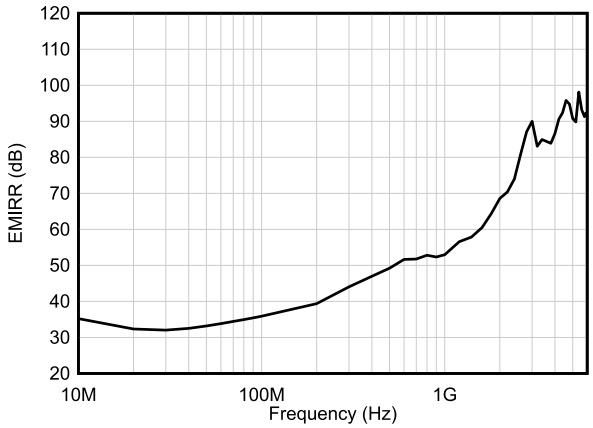


Figure 6-39. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

6.17 Typical Characteristics: All Other Devices

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. The Figure numbers referenced in the following graphs are located in Section 7.

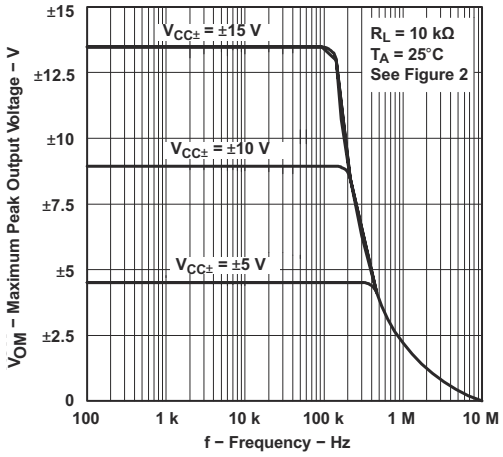


Figure 6-40. Maximum Peak Output Voltage vs Frequency

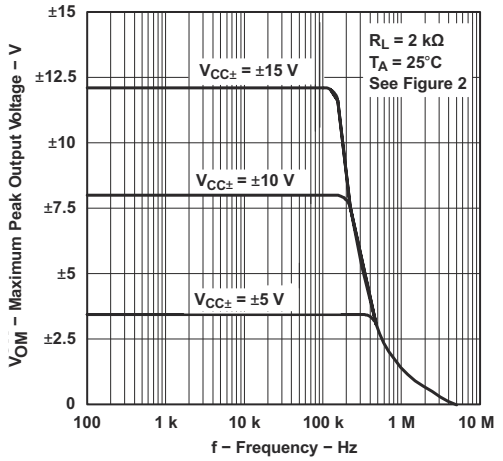


Figure 6-41. Maximum Peak Output Voltage vs Frequency

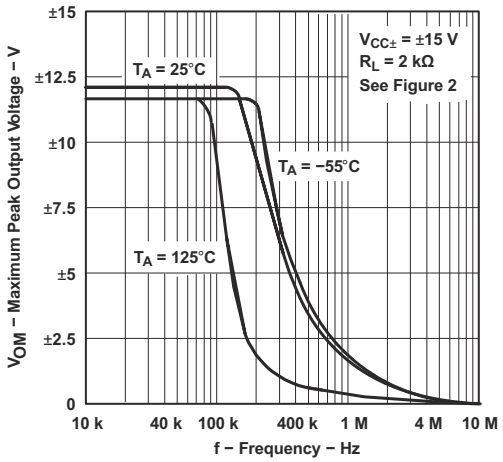


Figure 6-42. Maximum Peak Output Voltage vs Frequency

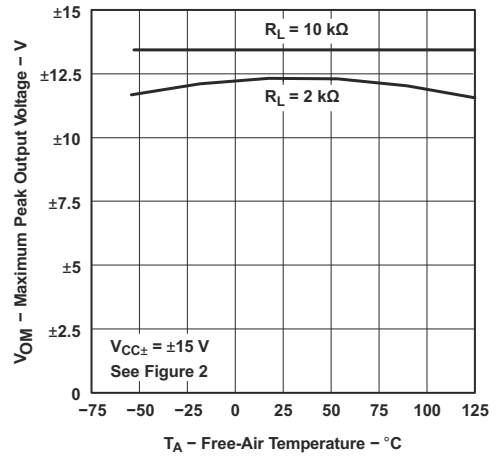


Figure 6-43. Maximum Peak Output Voltage vs Free-Air Temperature

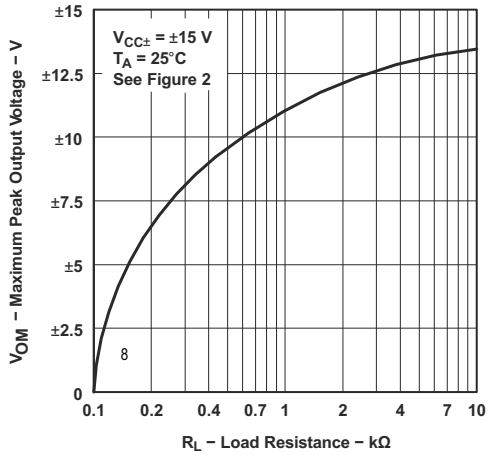


Figure 6-44. Maximum Peak Output Voltage vs Load Resistance

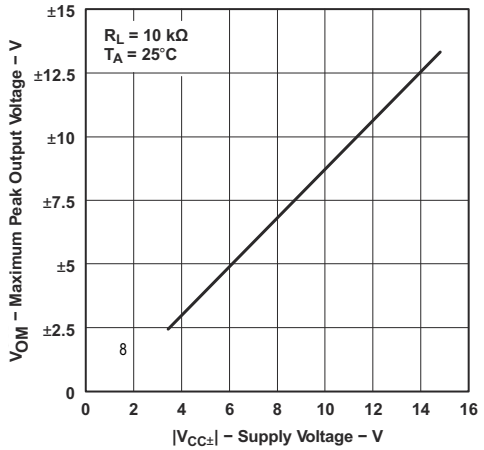


Figure 6-45. Maximum Peak Output Voltage vs Supply Voltage

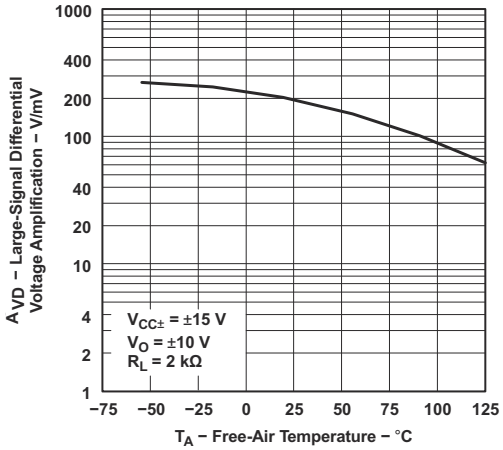


Figure 6-46. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

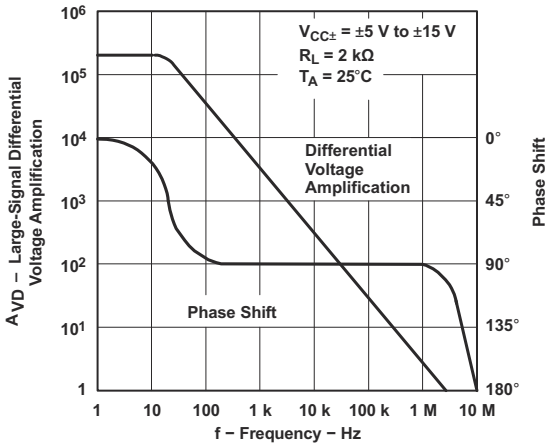


Figure 6-47. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

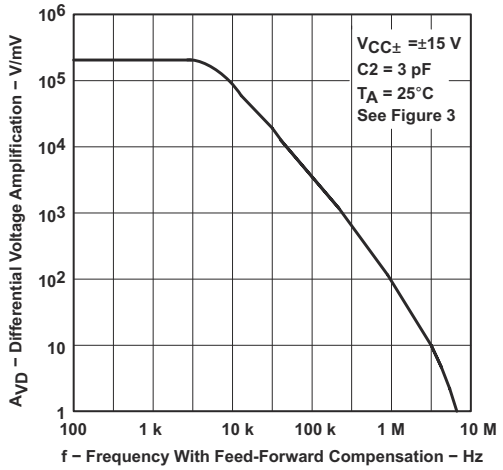


Figure 6-48. Differential Voltage Amplification vs Frequency with Feed-Forward Compensation

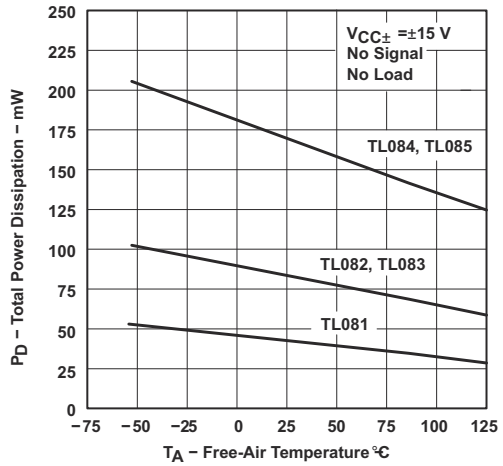


Figure 6-49. Total Power Dissipation vs Free-Air Temperature

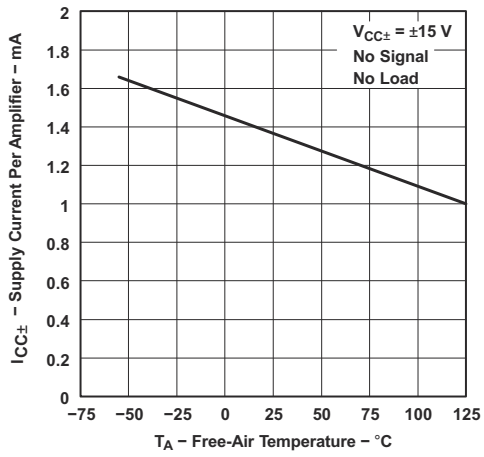


Figure 6-50. Supply Current per Amplifier vs Free-Air Temperature

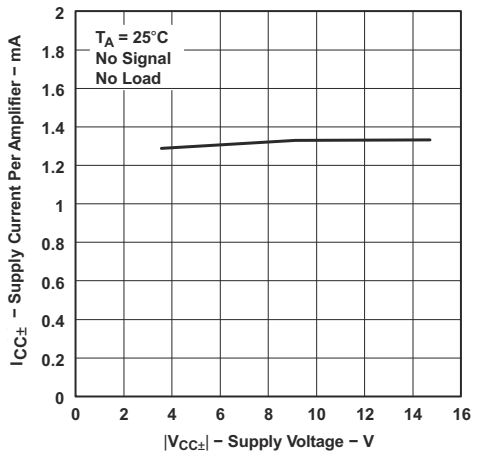


Figure 6-51. Supply Current per Amplifier vs Supply Voltage

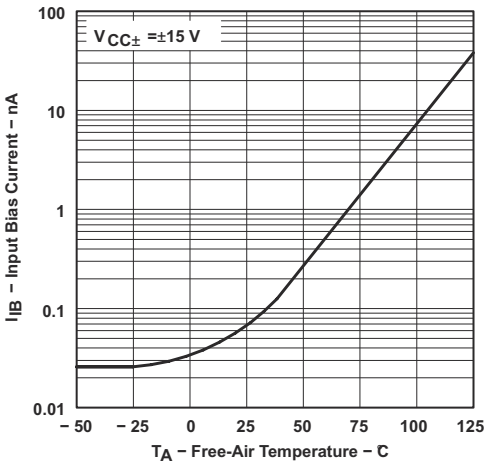


Figure 6-52. Input Bias Current vs Free-Air Temperature

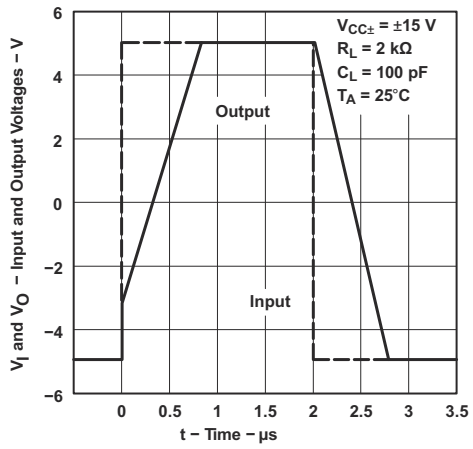


Figure 6-53. Voltage-Follower Large-Signal Pulse Response

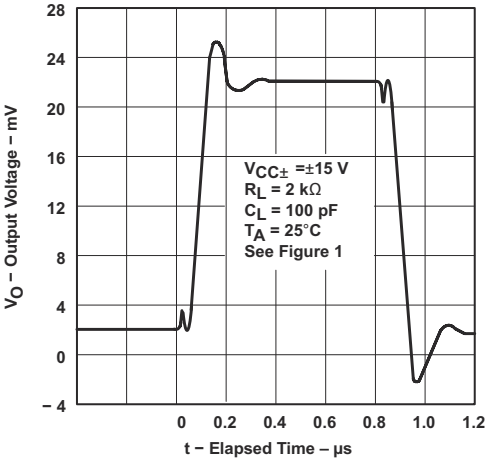


Figure 6-54. Output Voltage vs Elapsed Time

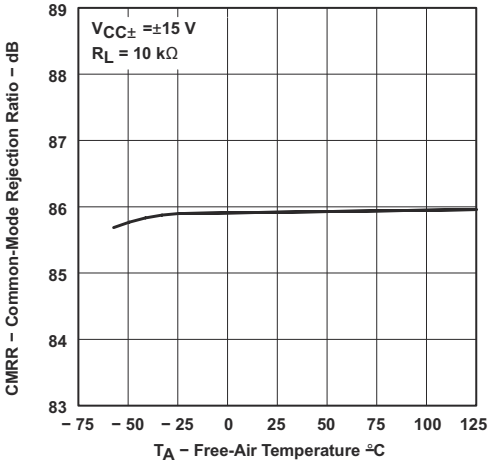


Figure 6-55. Common-Mode Rejection Ratio vs Free-Air Temperature

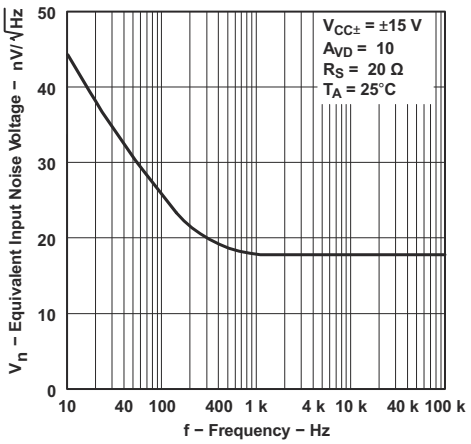


Figure 6-56. Equivalent Input Noise Voltage vs Frequency

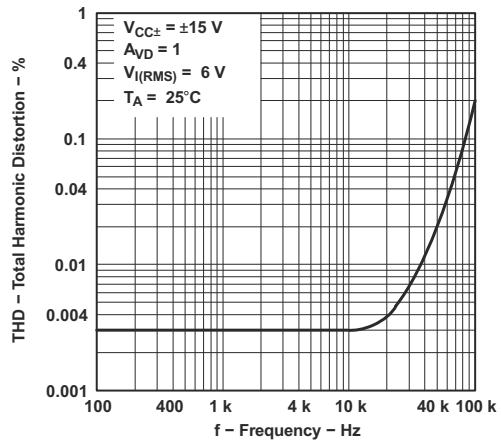


Figure 6-57. Total Harmonic Distortion vs Frequency

7 Parameter Measurement Information

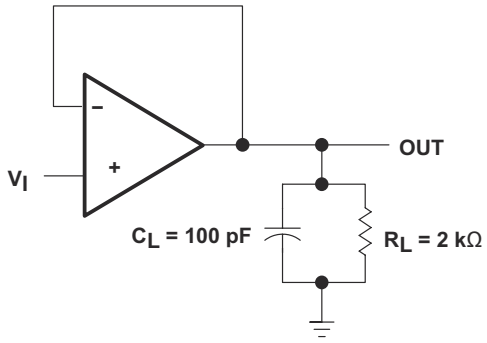


Figure 7-1. Test Figure 1

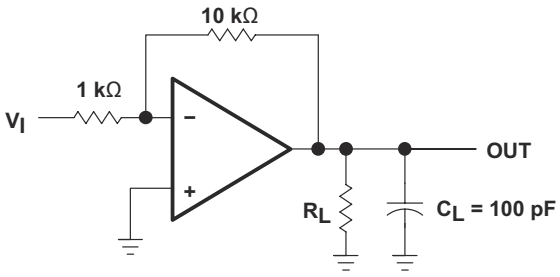


Figure 7-2. Test Figure 2

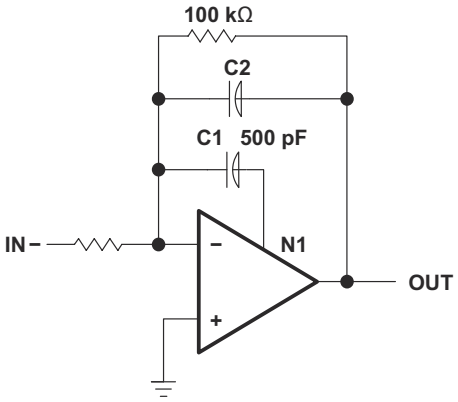


Figure 7-3. Test Figure 3

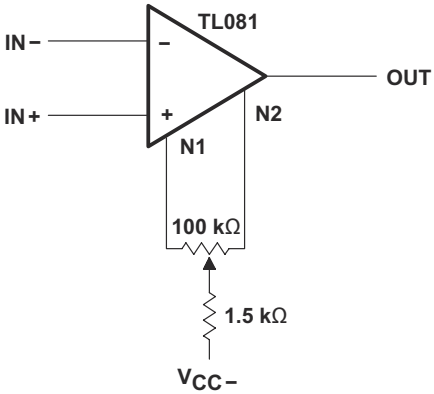


Figure 7-4. Test Figure 4

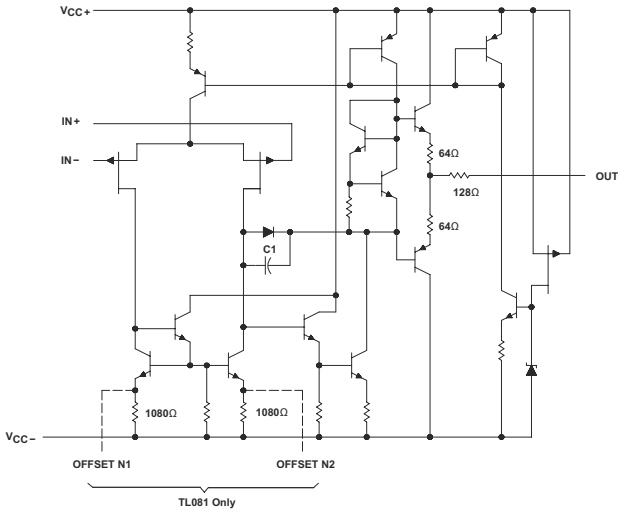
8 Detailed Description

8.1 Overview

The TL08xH family (TL081H, TL082H, and TL084H) is the next-generation family of the industry standard TL08x (TL081, TL082, and TL084) high-voltage general purpose amplifiers. These devices provide outstanding value for cost-sensitive applications requiring high slew rate with high voltage signals, such as motor drive and inverter systems.

A robust MUX-friendly input stage enhances flexibility in design, with common-mode voltage range extending to the positive rail as well as improved settling time in multi-channel applications. Low offset voltage (1 mV, typ) and low offset voltage drift (2 µV/°C) allows the TL08xH family to be used in rugged applications requiring precision current and voltage sensing. High voltage operation (up to 40 V) and high slew rate (20 V/µs) make the TL08xH family a premier choice for high-voltage applications with fast transients.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. These devices have a very low THD of 0.003% meaning that the TL08x devices will add little harmonic distortion when used in audio signal applications.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 13-V/µs slew rate.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TL08x series of operational amplifiers can be used in countless applications. The few applications in this section show principles used in all applications of these parts.

9.2 Typical Applications

9.2.1 Inverting Amplifier Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

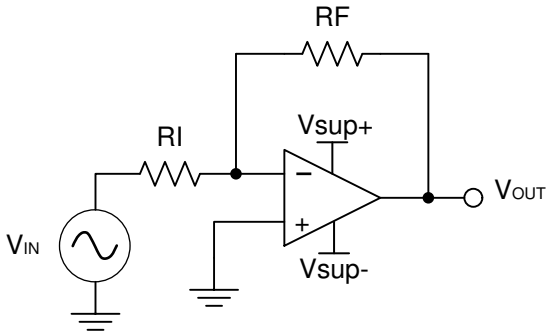


Figure 9-1. Schematic for Inverting Amplifier Application

9.2.1.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

9.2.1.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_V = \frac{VOUT}{VIN} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the kΩ range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose 10 kΩ for RI which means 36 kΩ will be used for RF. This was determined by Equation 3.

$$A_V = -\frac{RF}{RI} \quad (3)$$

9.2.1.3 Application Curve

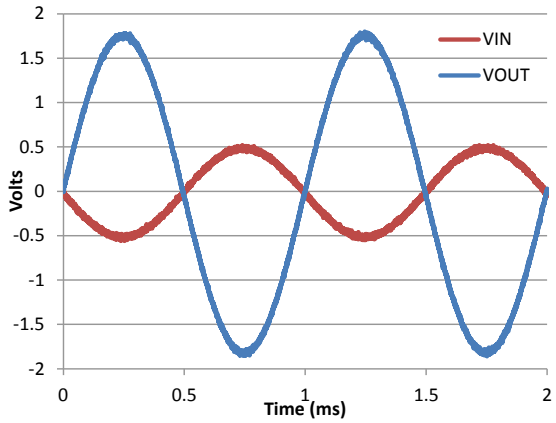


Figure 9-2. Input and output voltages of the inverting amplifier

9.3 System Examples

9.3.1 General Applications

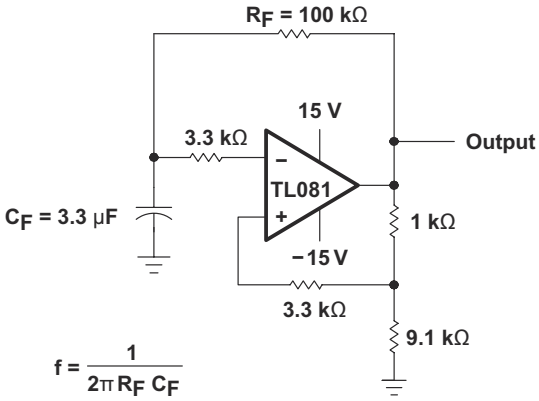


Figure 9-3. 0.5-Hz Square-Wave Oscillator

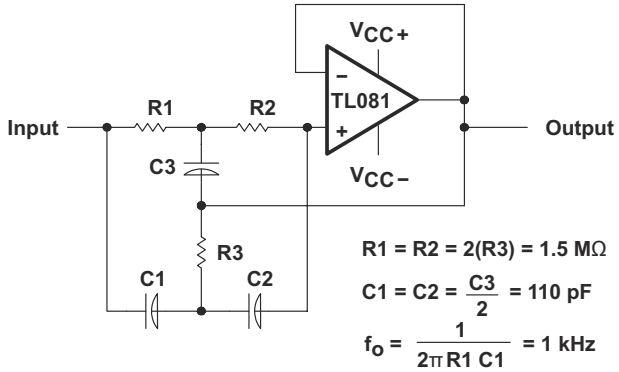


Figure 9-4. High-Q Notch Filter

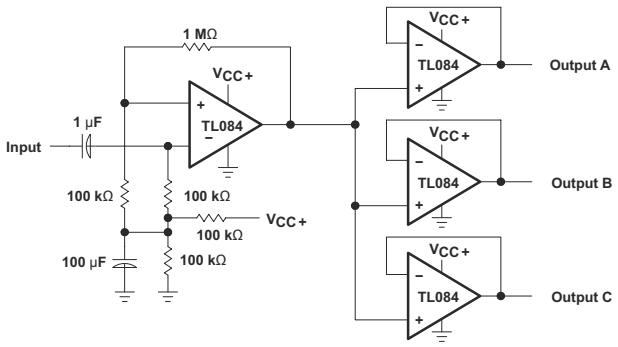
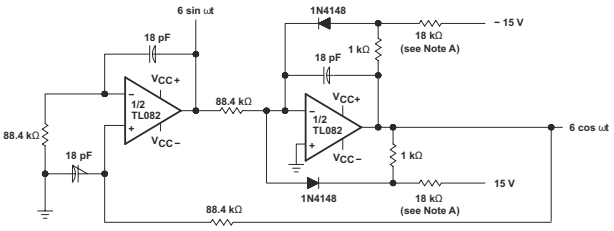


Figure 9-5. Audio-Distribution Amplifier



A. These resistor values may be adjusted for a symmetrical output.

Figure 9-6. 100-kHz Quadrature Oscillator

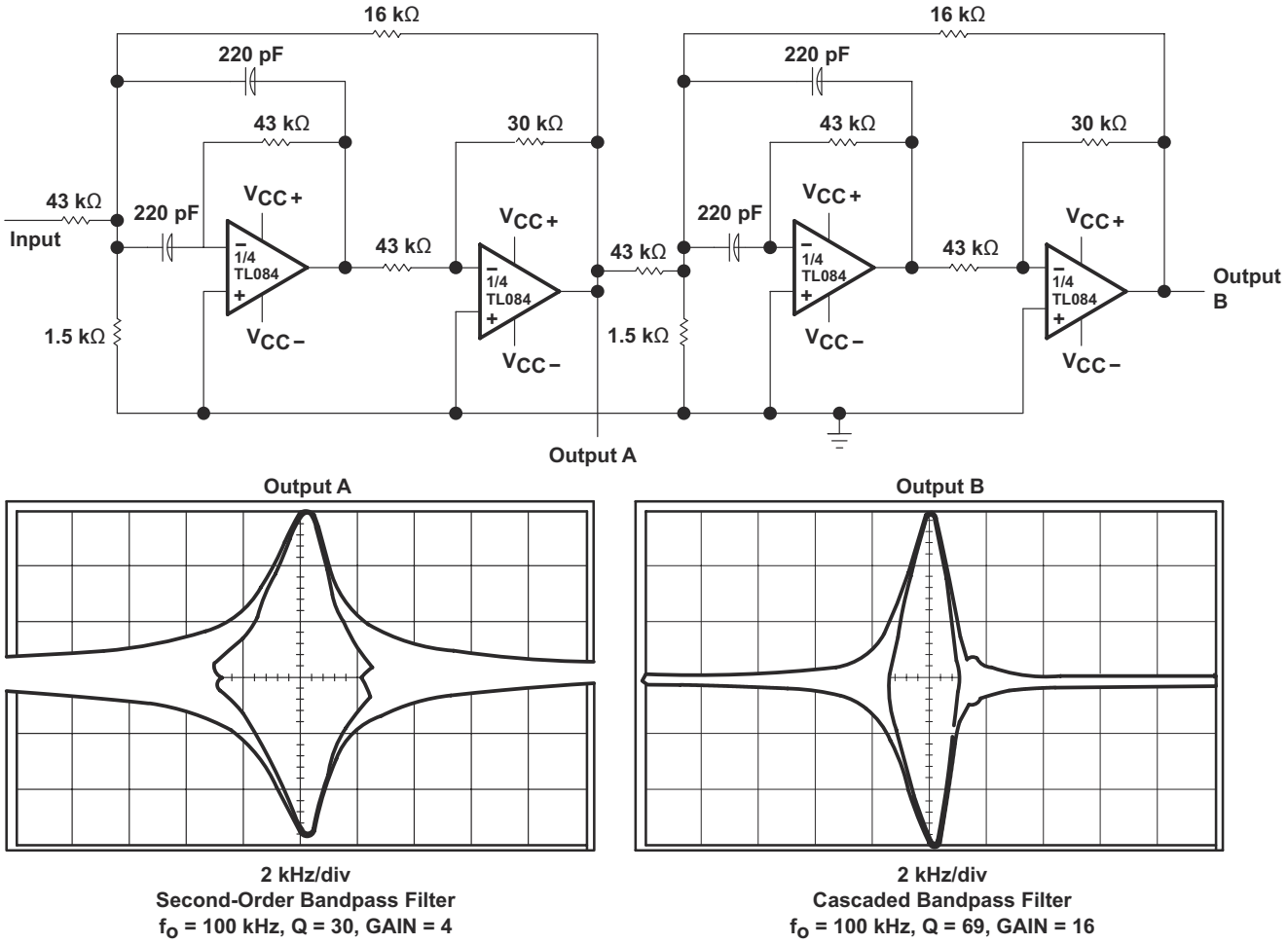


Figure 9-7. Positive-Feedback Bandpass Filter

10 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single-supply or outside the range of ±18 V for a dual-supply can permanently damage the device (see the *Section 6.2*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Section 11* .

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Section 11.2* .
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Examples

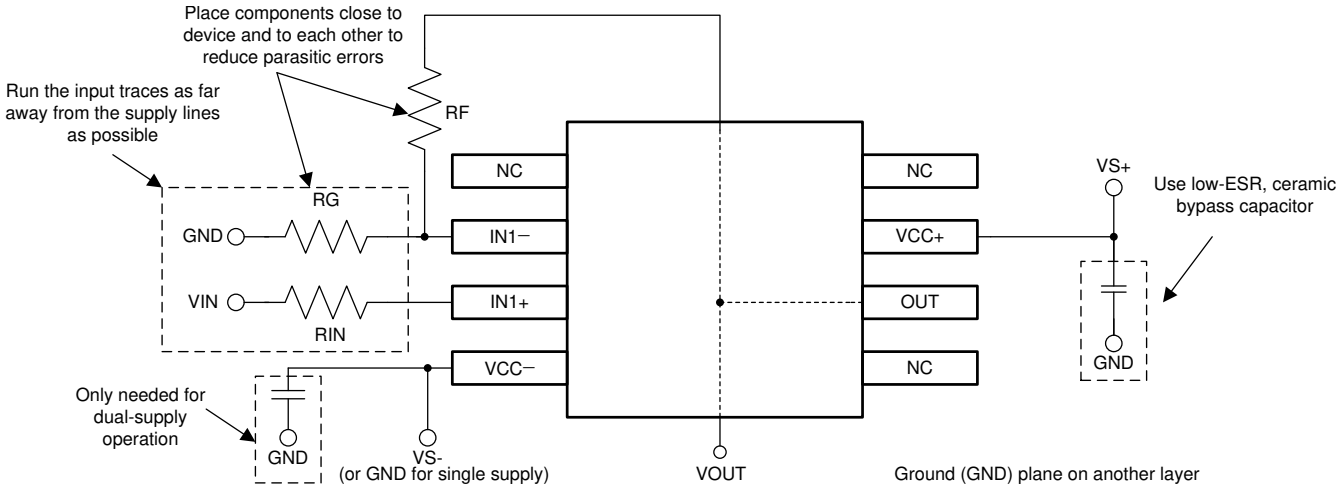


Figure 11-1. Operational Amplifier Board Layout for Noninverting Configuration

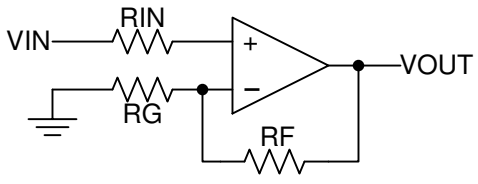


Figure 11-2. Operational Amplifier Schematic for Noninverting Configuration

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL081	Click here	Click here	Click here	Click here	Click here
TL081A	Click here	Click here	Click here	Click here	Click here
TL081B	Click here	Click here	Click here	Click here	Click here
TL082	Click here	Click here	Click here	Click here	Click here
TL082A	Click here	Click here	Click here	Click here	Click here
TL082B	Click here	Click here	Click here	Click here	Click here
TL084	Click here	Click here	Click here	Click here	Click here
TL084A	Click here	Click here	Click here	Click here	Click here
TL084B	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9851501Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB	Samples
5962-9851501QPA	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	9851501QPA TL082M	Samples
5962-9851503Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9851503Q2A TL084 MFKB	Samples
5962-9851503QCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-9851503QCA TL084MJB	Samples
TL081ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC	Samples
TL081ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC	Samples
TL081ACP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TL081ACP	Samples
TL081BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC	Samples
TL081BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC	Samples
TL081BCP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TL081BCP	Samples
TL081BCPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TL081BCP	Samples
TL081CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C	Samples
TL081CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C	Samples
TL081CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TL081CP	Samples
TL081CPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TL081CP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL081CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	T081	Samples
TL081ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	Samples
TL081IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I	Samples
TL081IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	TL081IP	Samples
TL082ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC	Samples
TL082ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	0 to 70	TL082ACP	Samples
TL082ACPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082A	Samples
TL082BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples
TL082BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL082BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	0 to 70	TL082BCP	Samples
TL082BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	0 to 70	TL082BCP	Samples
TL082CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C	Samples
TL082CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TL082CP	Samples
TL082CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082	Samples
TL082ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL082IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I	Samples
TL082IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	TL082IP	Samples
TL082IPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	TL082IP	Samples
TL082IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z082	Samples
TL082MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB	Samples
TL082MJG	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	TL082MJG	Samples
TL082MJGB	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	9851501QPA TL082M	Samples
TL084ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC	Samples
TL084ACN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TL084ACN	Samples
TL084ACNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084A	Samples
TL084BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples
TL084BCDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL084BCN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TL084BCN	Samples
TL084BCNE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TL084BCN	Samples
TL084CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C	Samples
TL084CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TL084CN	Samples
TL084CNE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TL084CN	Samples
TL084CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084	Samples
TL084CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084CPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	T084	Samples
TL084HIDR	PREVIEW	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL084HID	
TL084HIDYYR	PREVIEW	SOT-23-THN	DYY	14	3000	TBD	Call TI	Call TI	-40 to 125		
TL084HIPWR	PREVIEW	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL084PW	
TL084ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL084IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I	Samples
TL084IN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	TL084IN	Samples
TL084INE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	TL084IN	Samples
TL084MFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	TL084MFK	Samples
TL084MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9851503Q2A TL084 MFKB	Samples
TL084MJ	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	TL084MJ	Samples
TL084MJB	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-9851503QC A TL084MJB	Samples
TL084QD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples
TL084QDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples
TL084QDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples
TL084QDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TL082, TL082M, TL084, TL084M :

- Catalog: TL082, TL084
- Automotive: TL082-Q1, TL082-Q1
- Military: TL082M, TL084M

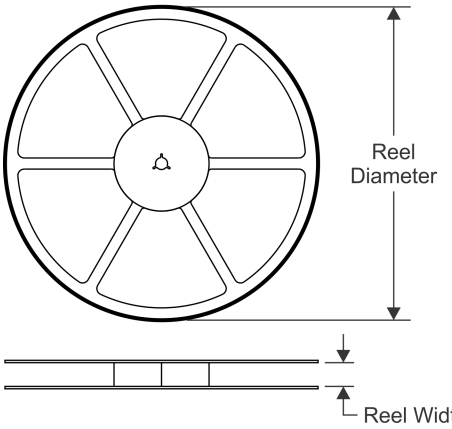
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

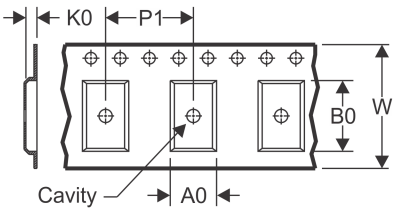
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

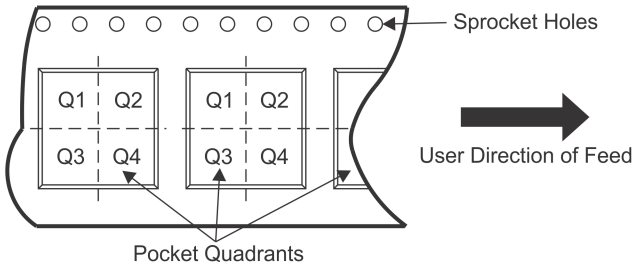


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

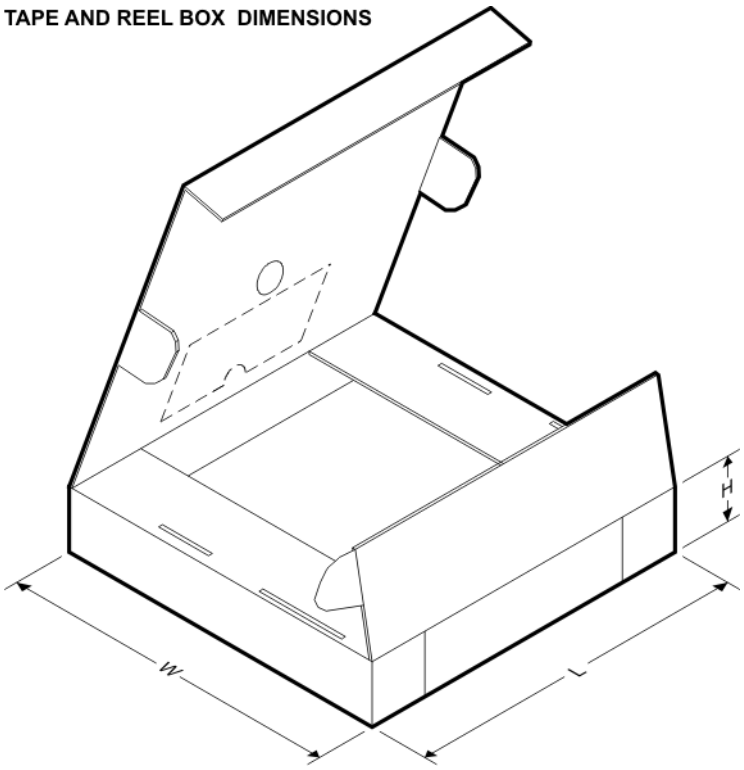


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL081ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL084BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL084CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



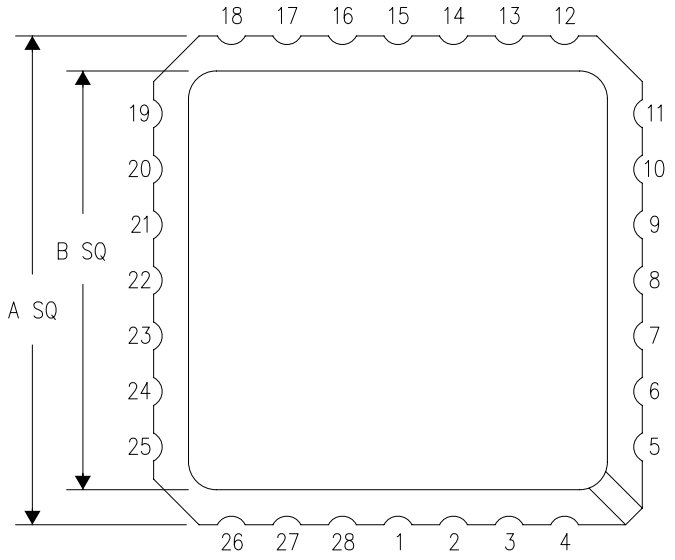
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL081ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082ACDR	SOIC	D	8	2500	853.0	449.0	35.0
TL082BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082CDR	SOIC	D	8	2500	853.0	449.0	35.0
TL082CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082CPWR	TSSOP	PW	8	2000	853.0	449.0	35.0

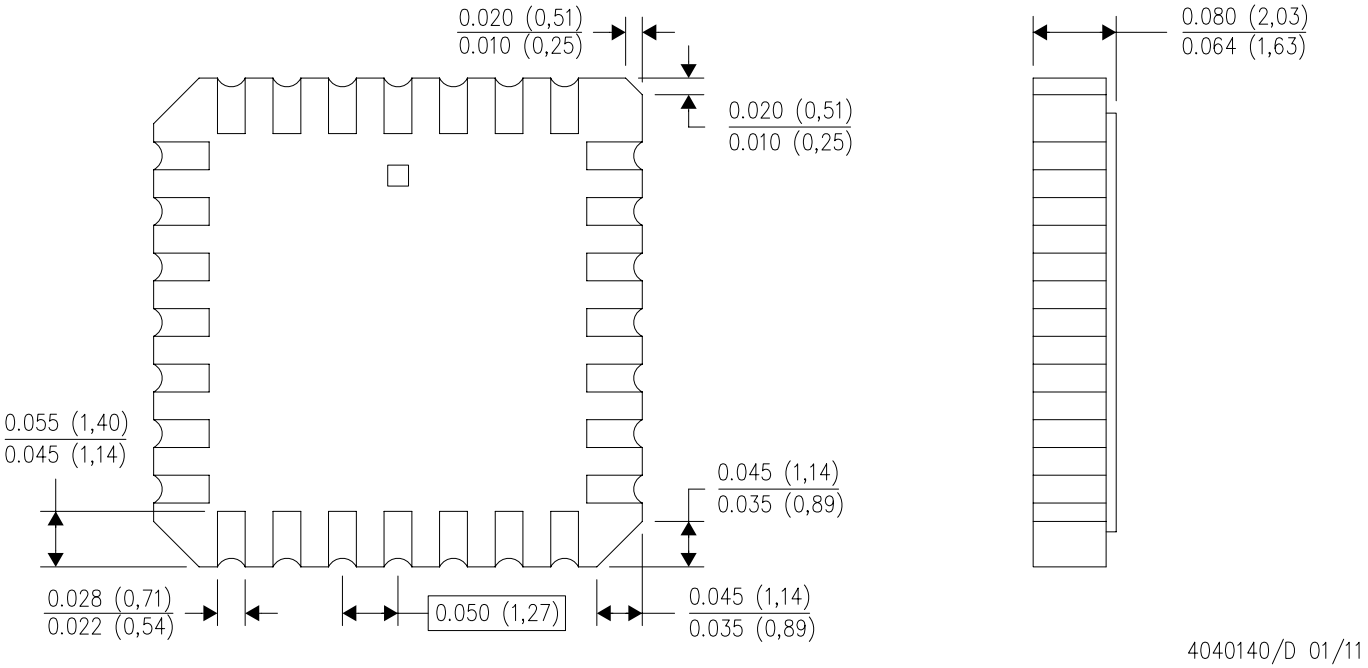
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL082IDR	SOIC	D	8	2500	853.0	449.0	35.0
TL082IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082IPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
TL084ACDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084ACDR	SOIC	D	14	2500	367.0	367.0	38.0
TL084ACNSR	SO	NS	14	2000	367.0	367.0	38.0
TL084BCDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084CDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084CDR	SOIC	D	14	2500	367.0	367.0	38.0
TL084CDRG4	SOIC	D	14	2500	333.2	345.9	28.6
TL084CNSR	SO	NS	14	2000	367.0	367.0	38.0
TL084CPWR	TSSOP	PW	14	2000	853.0	449.0	35.0
TL084IDR	SOIC	D	14	2500	333.2	345.9	28.6
TL084QDR	SOIC	D	14	2500	350.0	350.0	43.0
TL084QDRG4	SOIC	D	14	2500	350.0	350.0	43.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



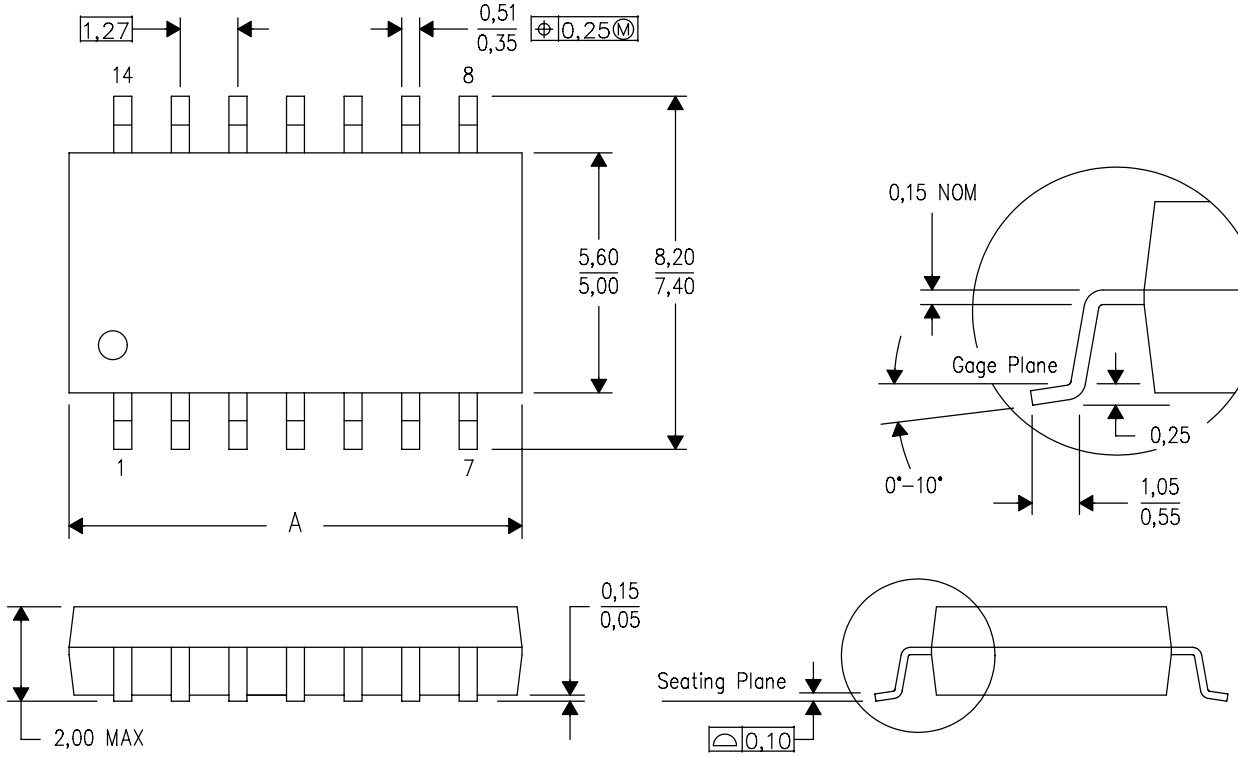
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

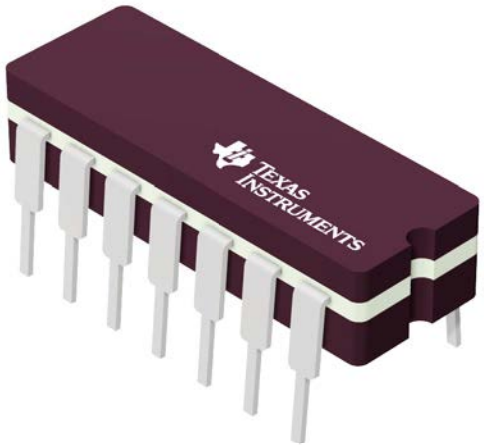
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

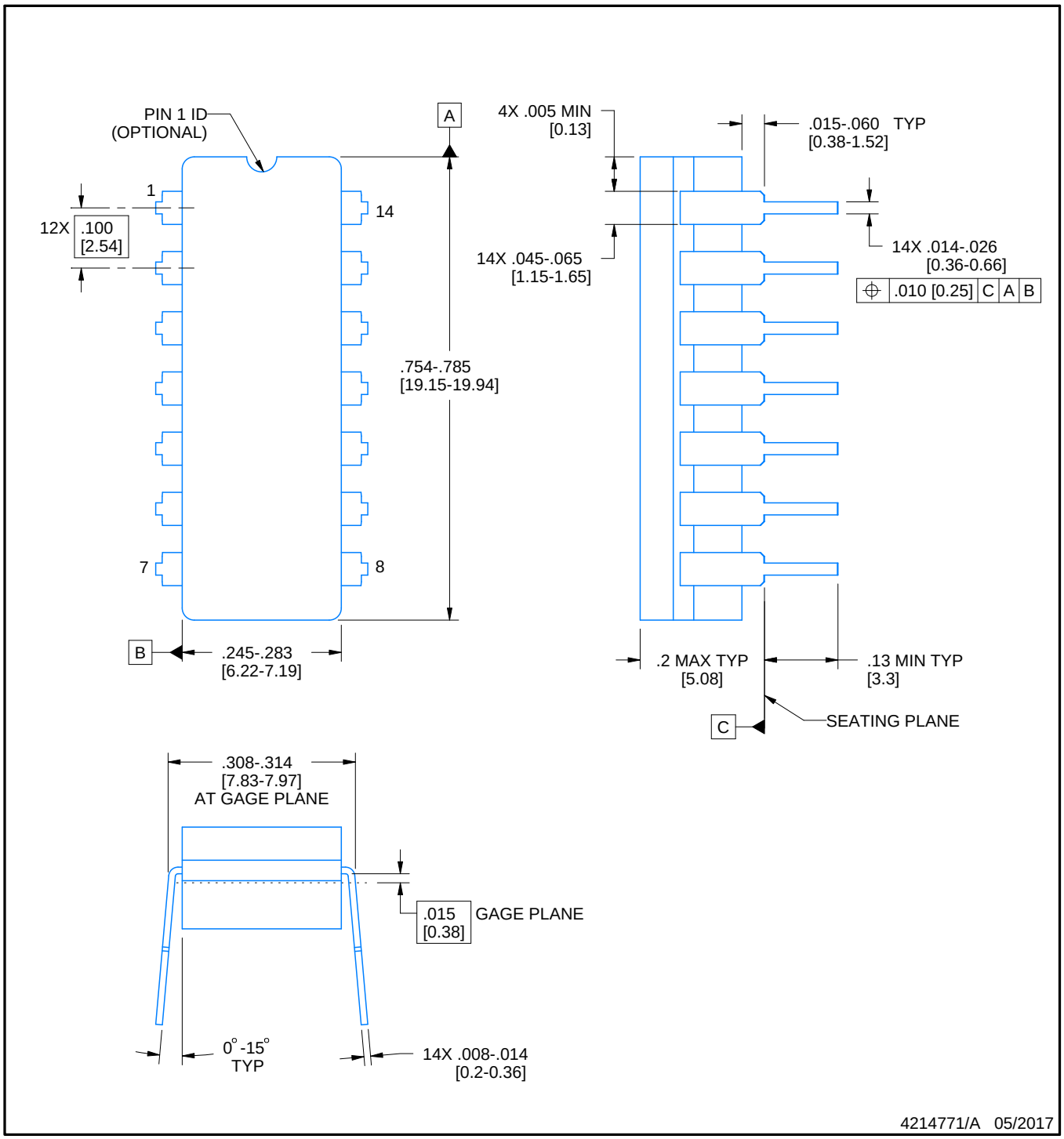
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

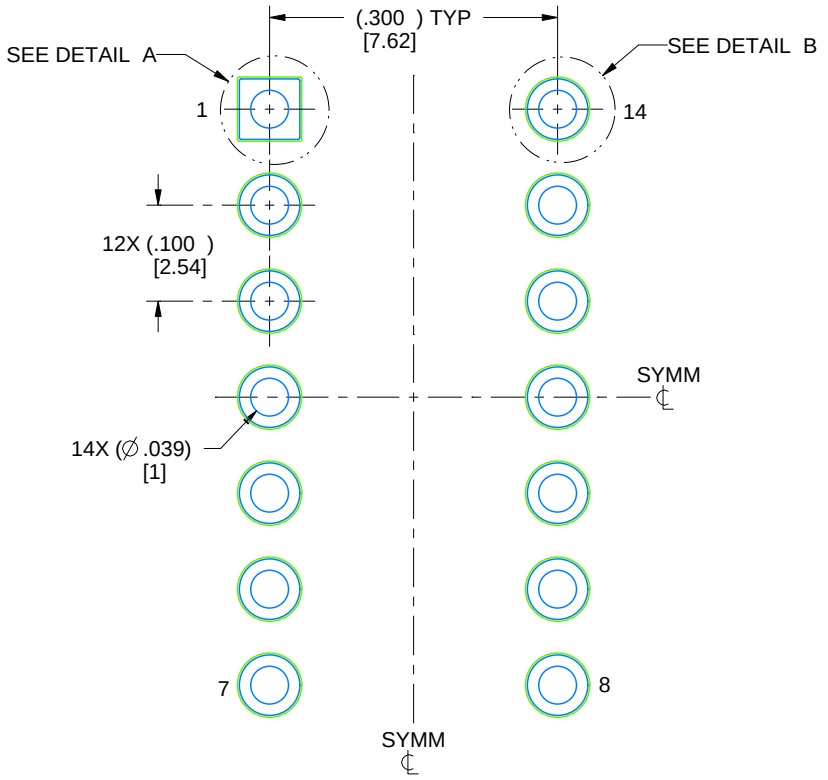
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

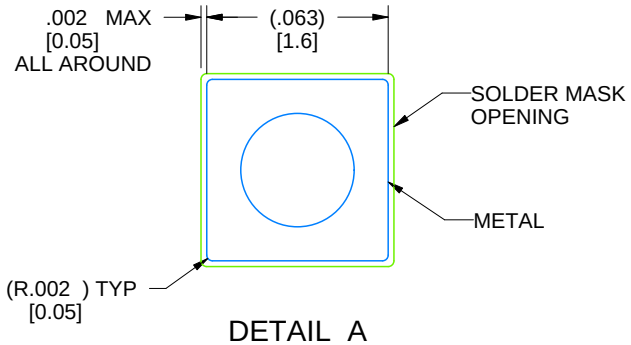
J0014A

CDIP - 5.08 mm max height

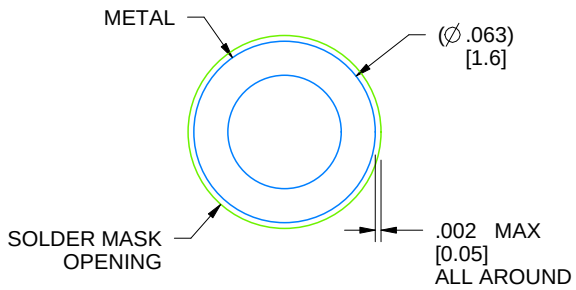
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



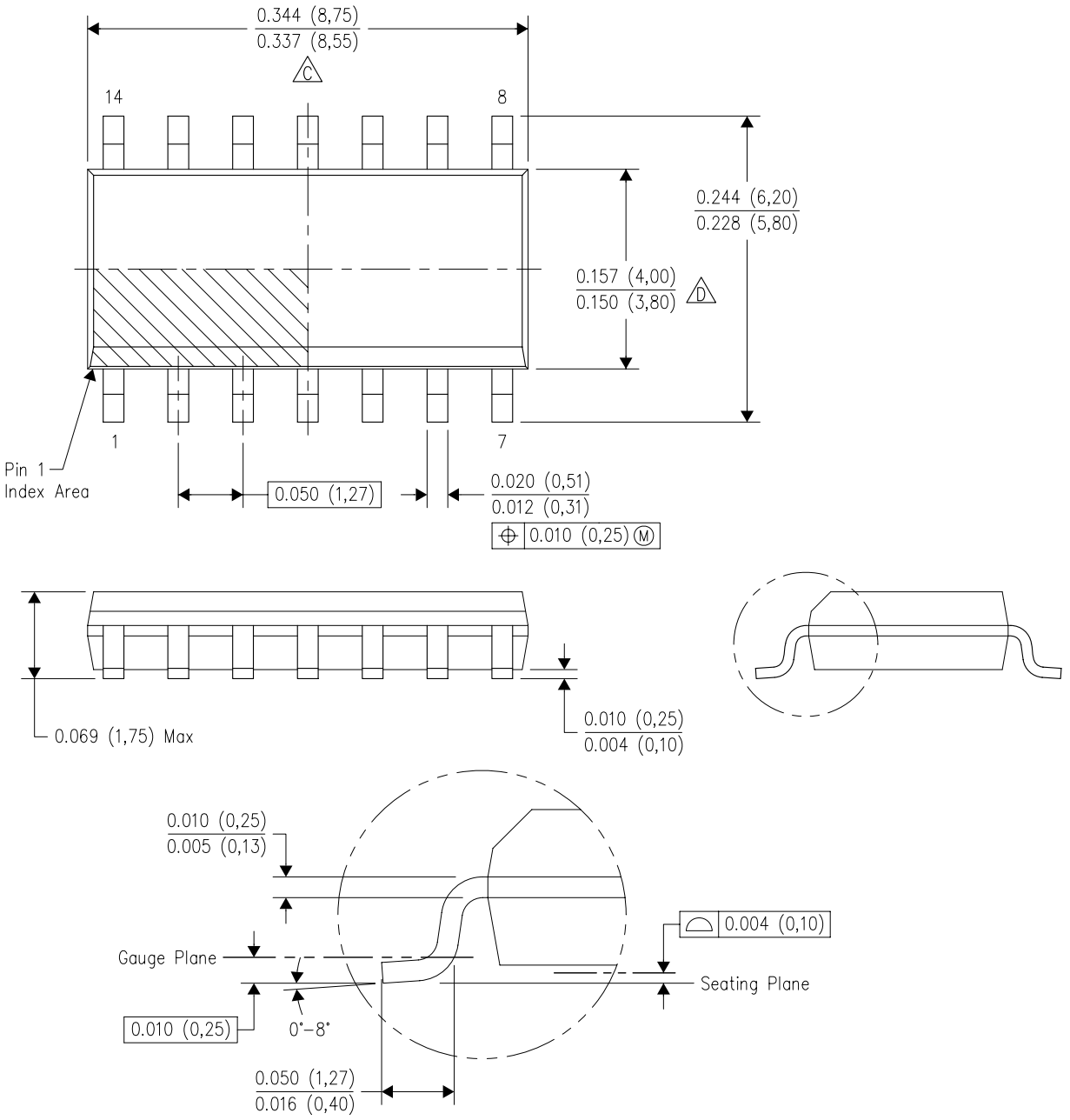
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

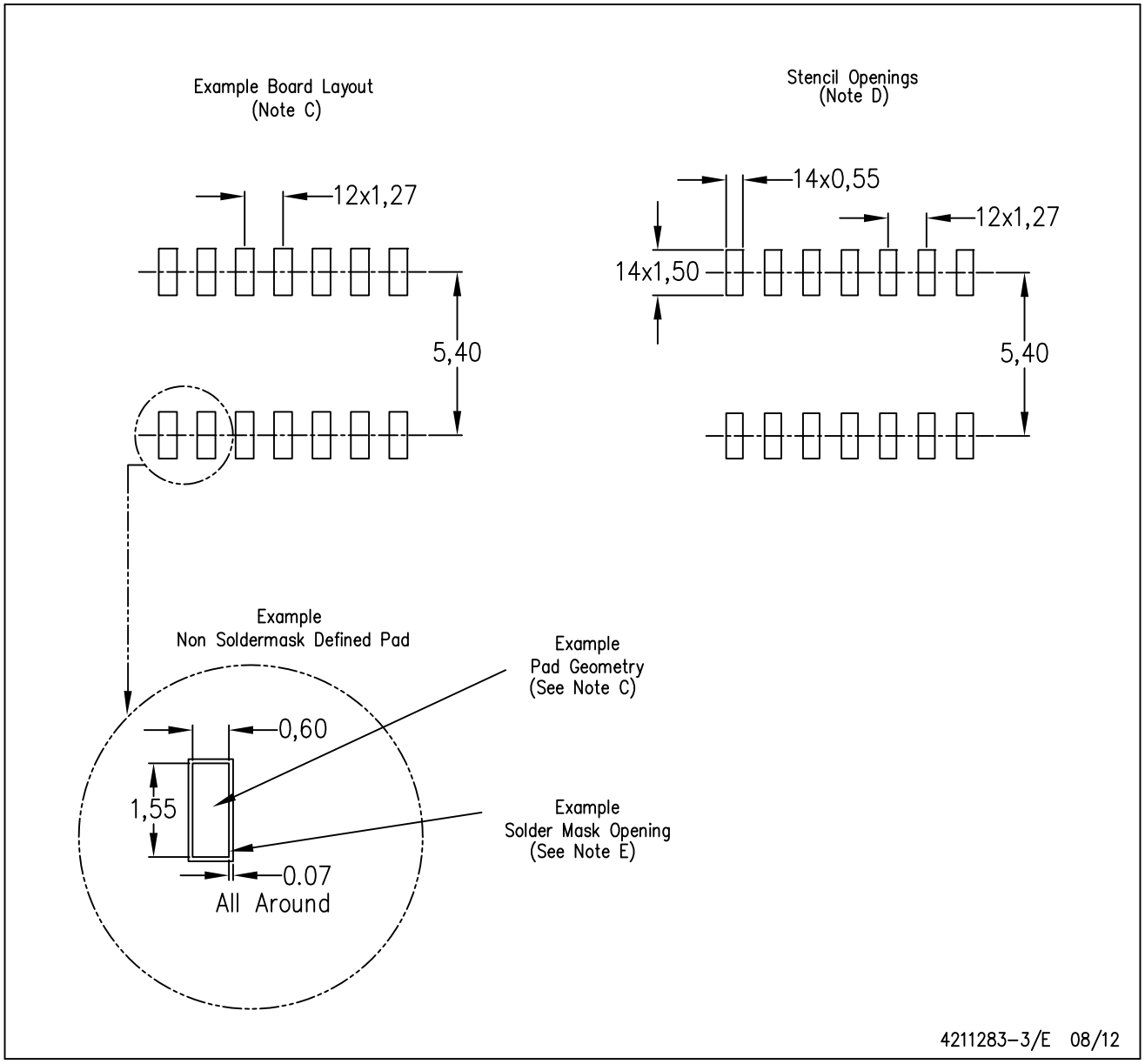
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

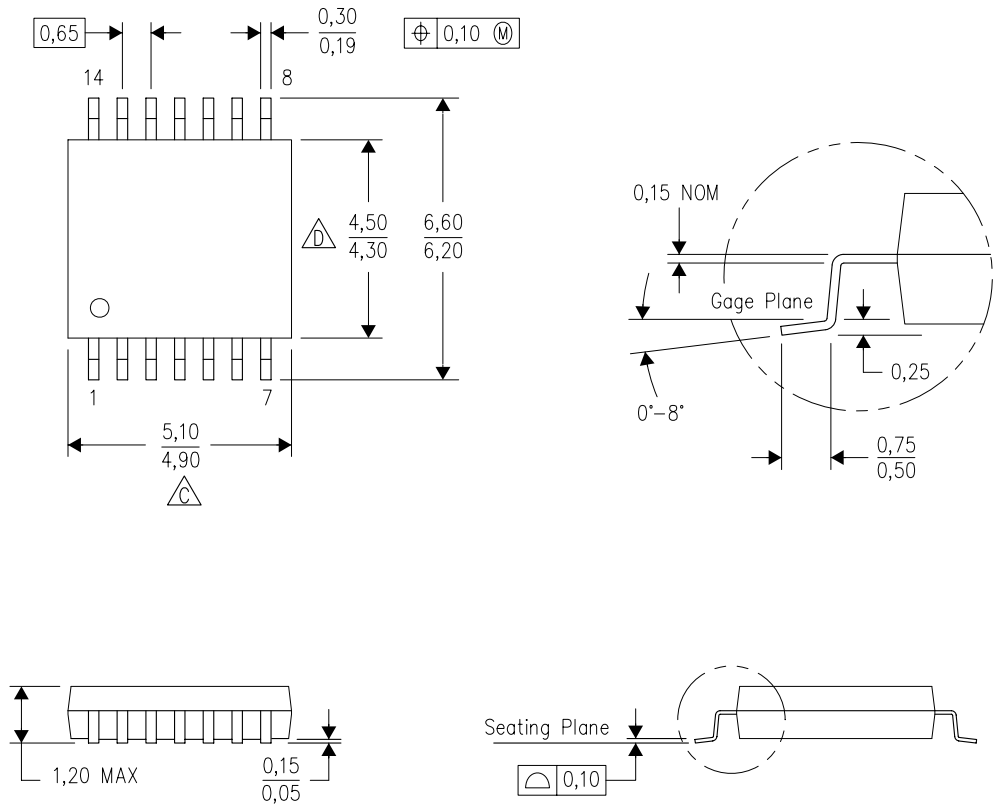
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

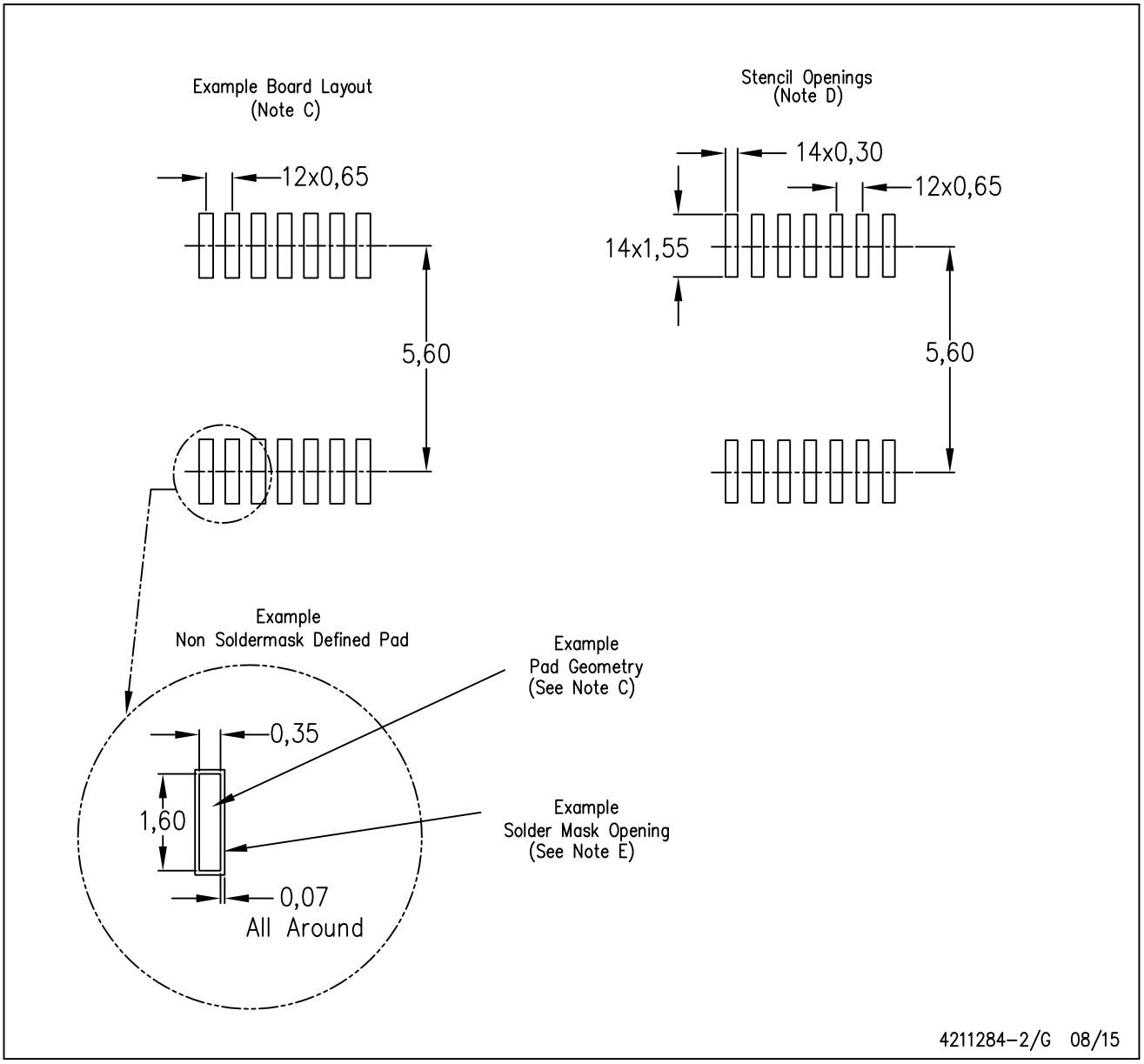
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



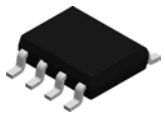
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

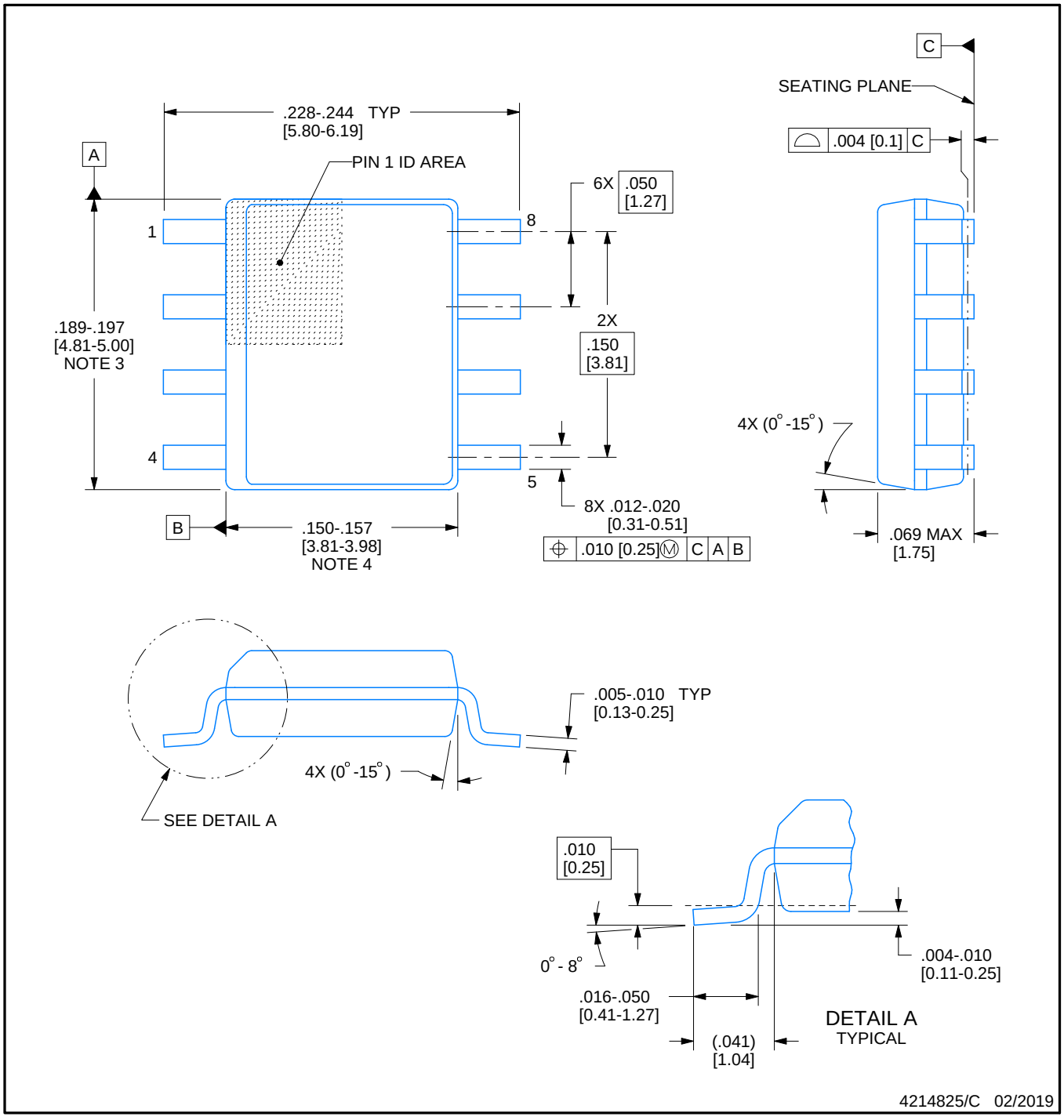


PACKAGE OUTLINE

D0008A

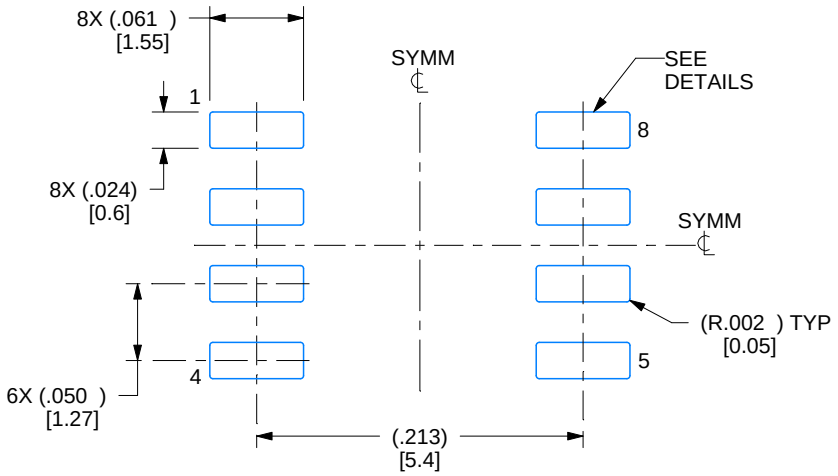
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

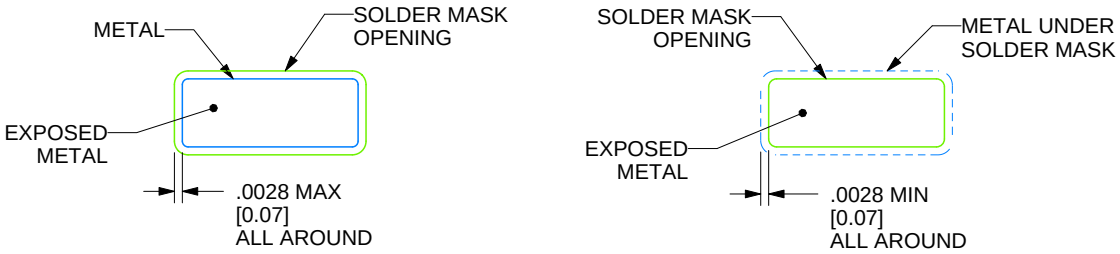


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

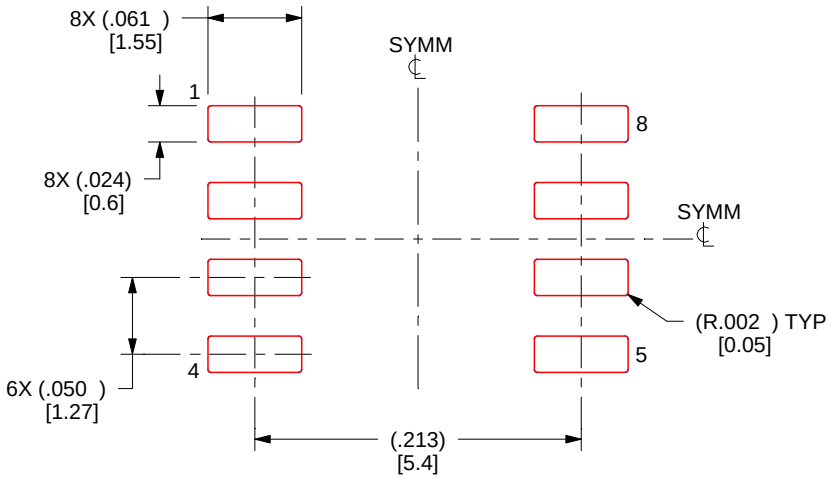
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

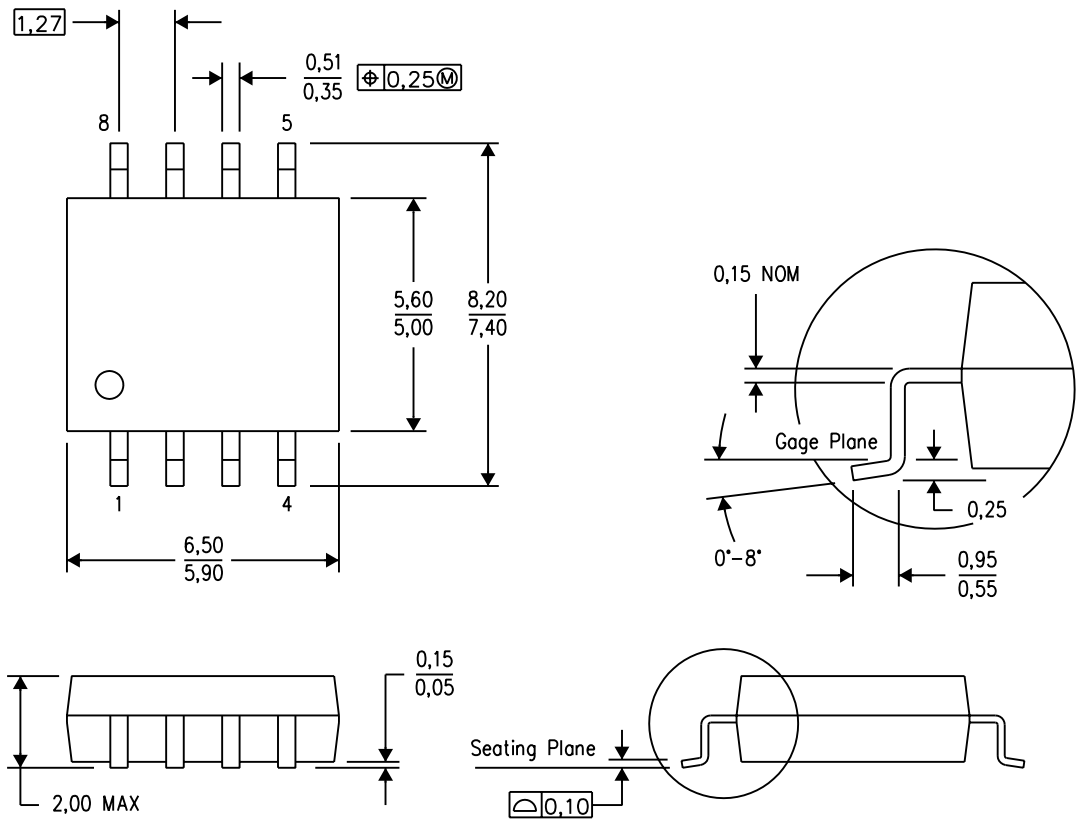
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

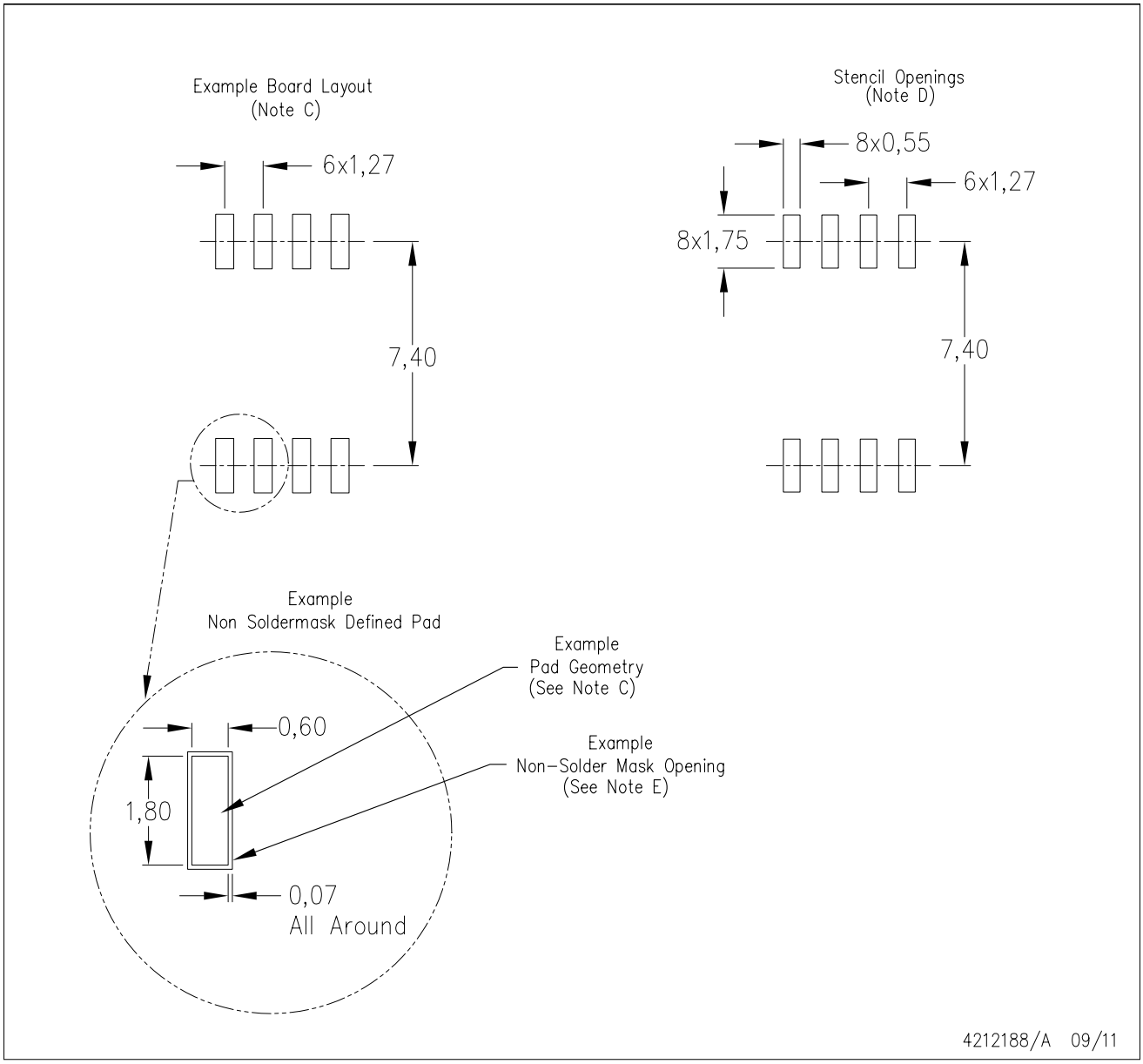
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

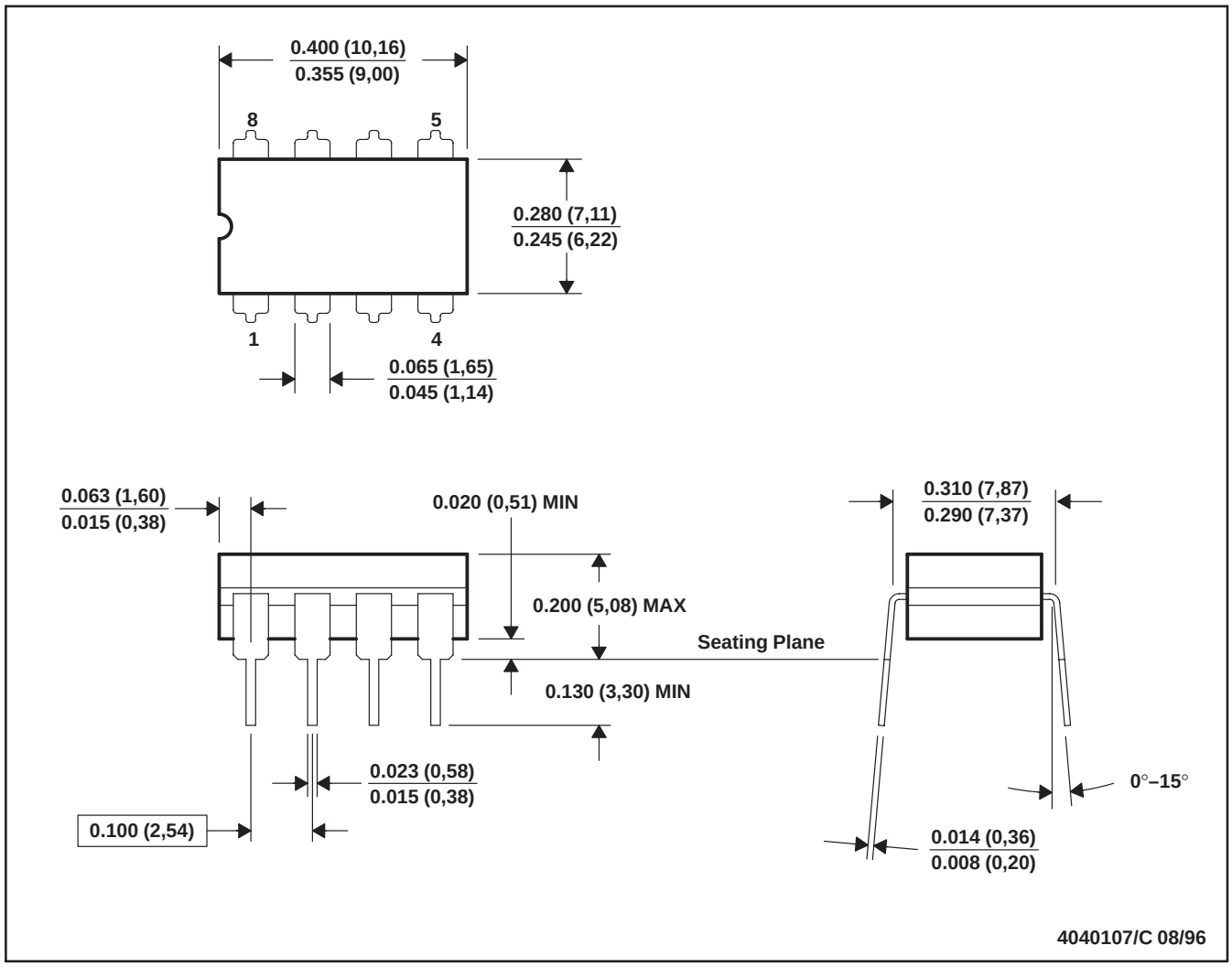
PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

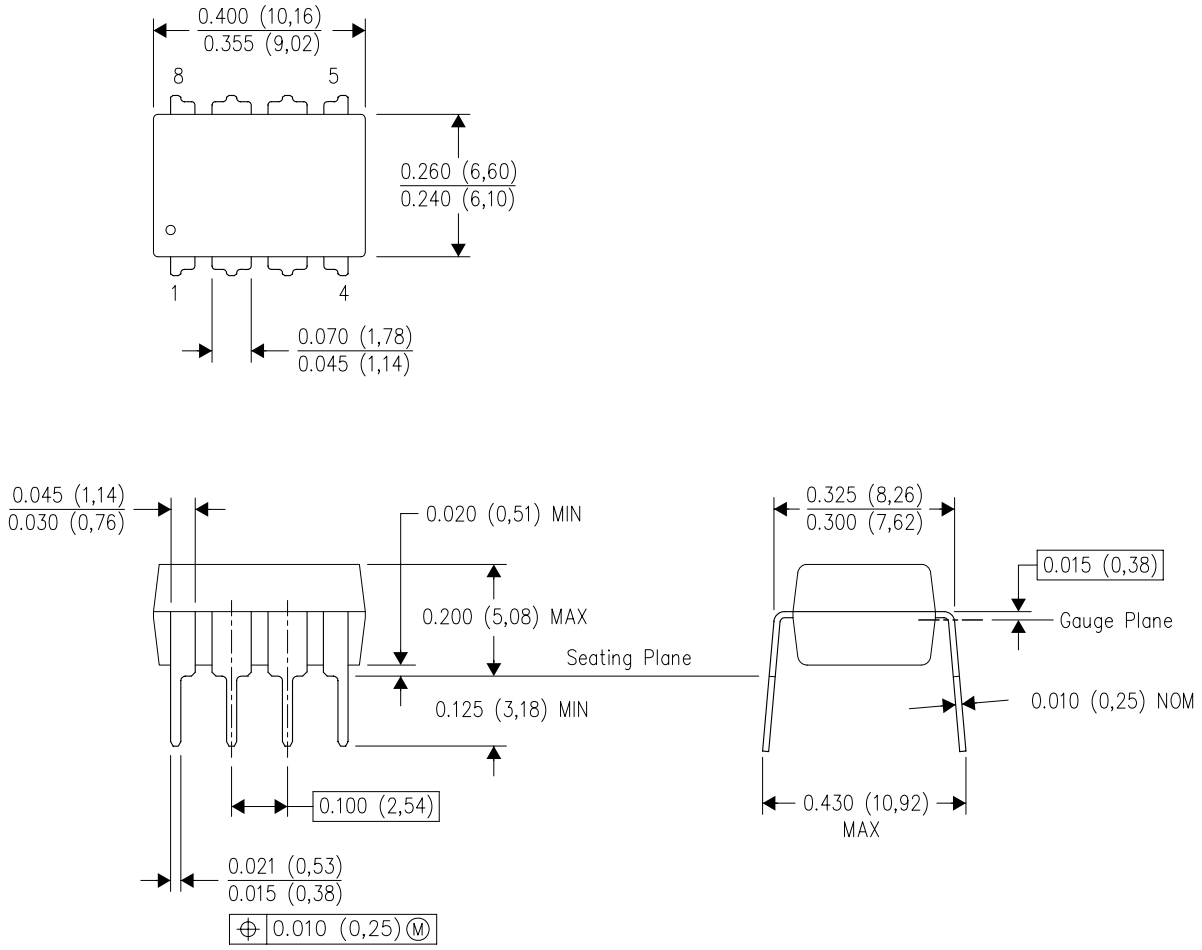
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

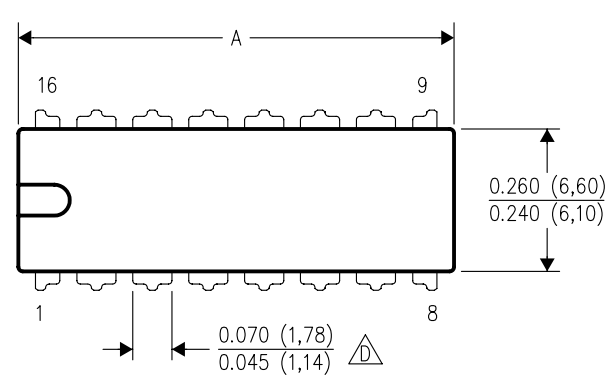


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

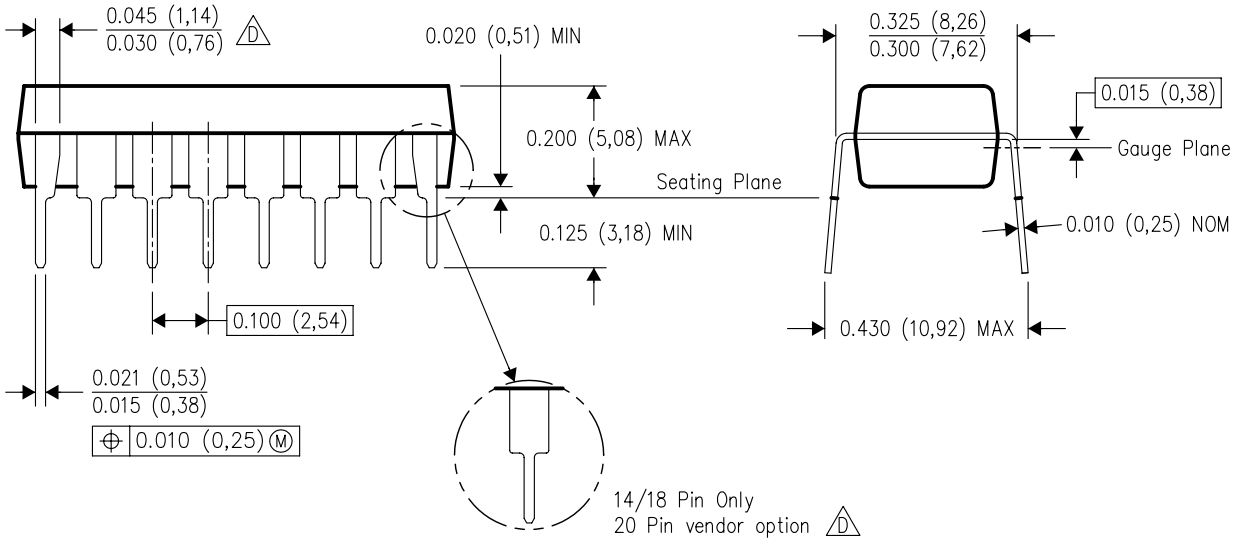
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

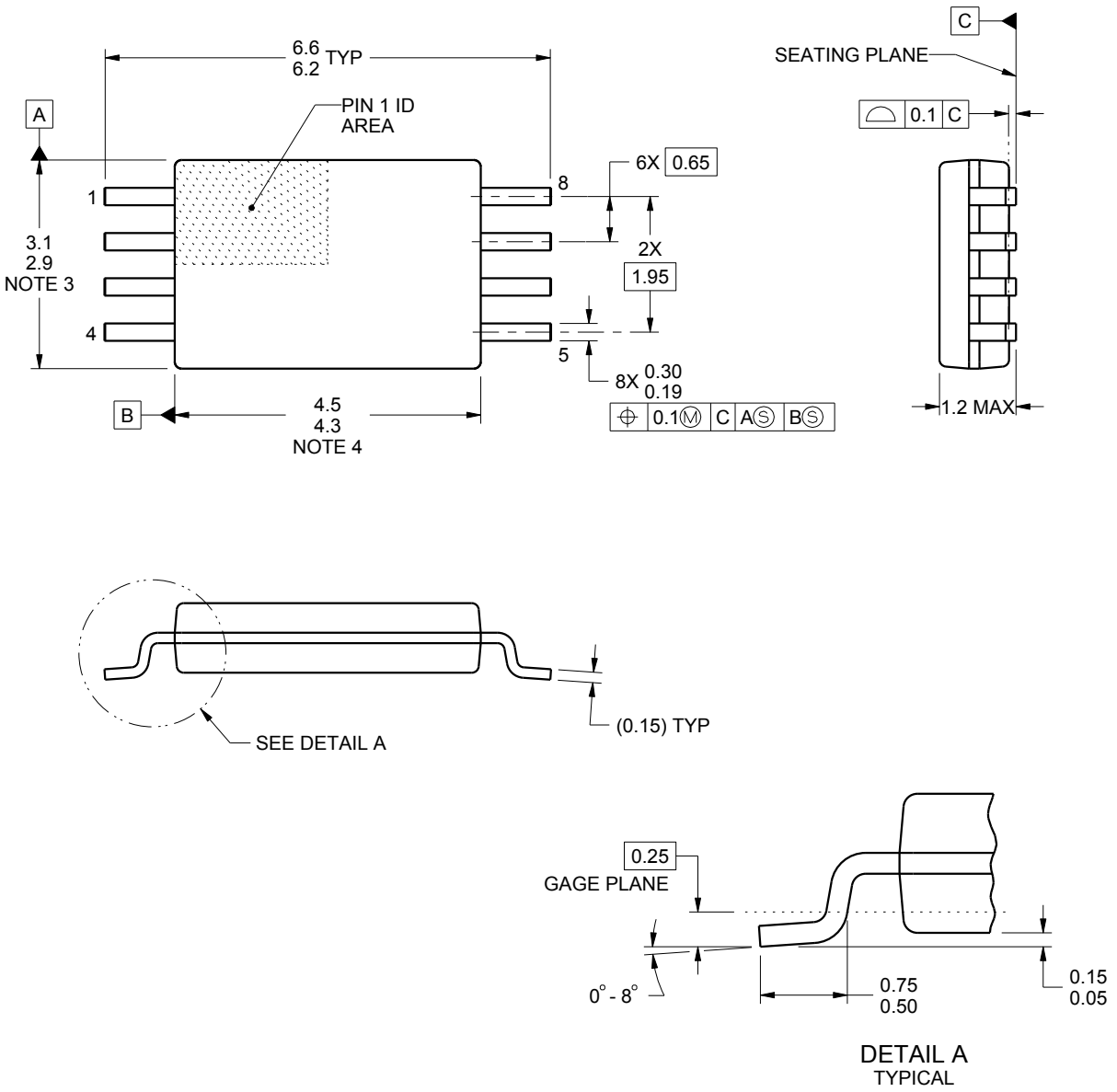
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0008A

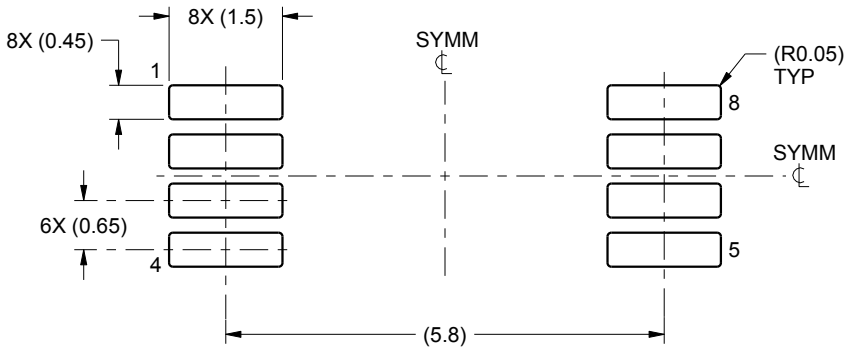
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

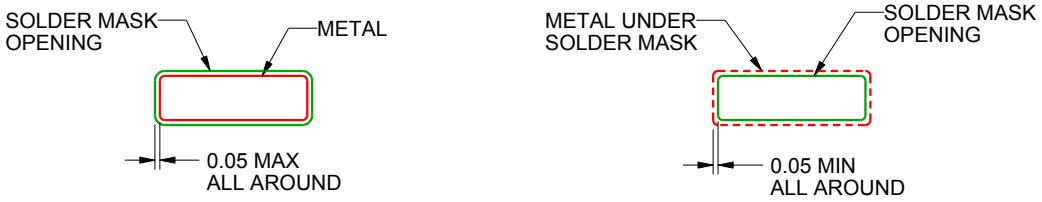


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

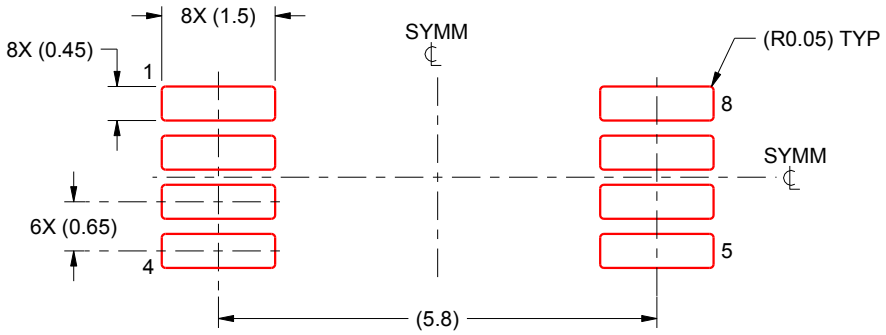


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Anexo XII.
Datasheet del LM3915.

LM3915 Dot/Bar Display Driver

Check for Samples: LM3915

FEATURES

- **3 dB/step, 30 dB Range**
- **Drives LEDs, LCDs, or Vacuum Fluorescents**
- **Bar or Dot Display Mode Externally Selectable by User**
- **Expandable to Displays of 90 dB**
- **Internal Voltage Reference from 1.2V to 12V**
- **Operates with Single Supply of 3V to 25V**
- **Inputs Operate Down to Ground**
- **Output Current Programmable from 1 mA to 30 mA**
- **Input Withstands ±35V without Damage or False Outputs**
- **Outputs are Current Regulated, Open Collectors**
- **Directly Drives TTL or CMOS**
- **The Internal 10-step Divider is Floating and can be Referenced to a Wide Range of Voltages**

  The LM3915 is Rated for Operation from 0°C to +70°C. The LM3915N-1 is Available in an 18-lead PDIP Package.

DESCRIPTION

The LM3915 is a monolithic integrated circuit that senses analog voltage levels and drives ten LEDs, LCDs or vacuum fluorescent displays, providing a logarithmic 3 dB/step analog display. One pin changes the display from a bar graph to a moving dot display. LED current drive is regulated and programmable, eliminating the need for current limiting resistors. The whole display system can operate from a single supply as low as 3V or as high as 25V.

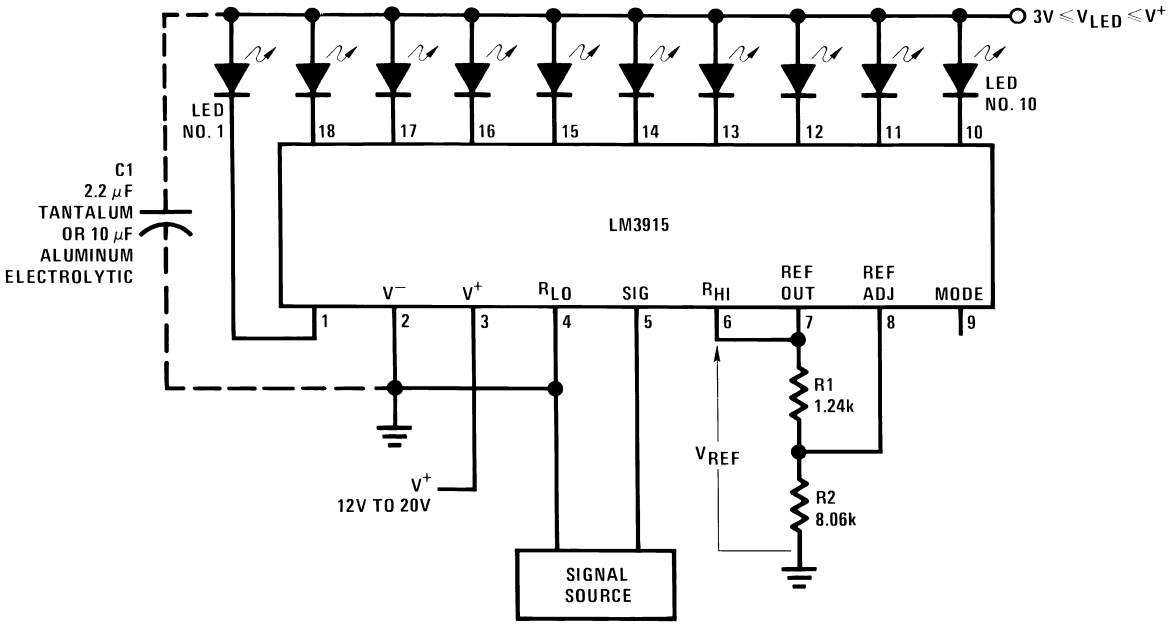
The IC contains an adjustable voltage reference and an accurate ten-step voltage divider. The high-impedance input buffer accepts signals down to ground and up to within 1.5V of the positive supply. Further, it needs no protection against inputs of ±35V. The input buffer drives 10 individual comparators referenced to the precision divider. Accuracy is typically better than 1 dB.

The LM3915's 3 dB/step display is suited for signals with wide dynamic range, such as audio level, power, light intensity or vibration. Audio applications include average or peak level indicators, power meters and RF signal strength meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

The LM3915 is extremely easy to apply. A 1.2V full-scale meter requires only one resistor in addition to the ten LEDs. One more resistor programs the full-scale anywhere from 1.2V to 12V independent of supply voltage. LED brightness is easily controlled with a single pot.

The LM3915 is very versatile. The outputs can drive LCDs, vacuum fluorescents and incandescent bulbs as well as LEDs of any color. Multiple devices can be cascaded for a dot or bar mode display with a range of 60 or 90 dB. LM3915s can also be cascaded with LM3914s for a linear/log display or with LM3916s for an extended-range VU meter.

Typical Applications



Notes: Capacitor C1 is required if leads to the LED supply are 6″ or longer.
Circuit as shown is wired for dot mode. For bar mode, connect pin 9 to pin 3. V_{LED} must be kept below 7V or dropping resistor should be used to limit IC power dissipation.

Figure 1. 0V to 10V Log Display

$$V_{REF} = 1.25V \left(1 + \frac{R2}{R1}\right) + R2 \times 80\ \mu A$$

$$I_{LED} = \frac{12.5V}{R1} + \frac{V_{REF}}{2.2\ k\Omega}$$

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Power Dissipation (3) PDIP (NFK)	1365 mW
Supply Voltage	25V
Voltage on Output Drivers	25V
Input Signal Overvoltage (4)	±35V
Divider Voltage	−100 mV to V^+
Reference Load Current	10 mA
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum junction temperature of the LM3915 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 55°C/W for the PDIP (NFK package).
(4) Pin 5 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.

ELECTRICAL CHARACTERISTICS(1)(2)

Parameter	Conditions(1)	Min	Typ	Max	Units
COMPARATOR					
Offset Voltage, Buffer and First Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, I_{LED} = 1 mA		3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, I_{LED} = 1 mA		3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{L(REF)}$ = 2 mA, I_{LED} = 10 mA	3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \le V_{IN} \le (V^+ - 1.5V)$		25	100	nA
Input Signal Overvoltage	No Change in Display	−35		35	V
VOLTAGE-DIVIDER					
Divider Resistance	Total, Pin 6 to 4	16	28	36	kΩ
Relative Accuracy (Input Change Between Any Two Threshold Points)	(3)	2.0	3.0	4.0	dB
Absolute Accuracy at Each Threshold Point	(3)				
	V_{IN} = −3, −6 dB	−0.5		+0.5	dB
	V_{IN} = −9 dB	−0.5		+0.65	dB
	V_{IN} = −12, −15, −18 dB	−0.5		+1.0	dB
	V_{IH} = −21, −24, −27 dB	−0.5		+1.5	dB

(1) Unless otherwise stated, all specifications apply with the following conditions:
$3\ V_{DC} \le V^+ \le 20\ V_{DC}$ $-0.015V \le V_{RLO} \le 12\ V_{DC}$ T_A = 25°C, $I_{L(REF)}$ = 0.2 mA, pin 9 connected to pin 3 (bar mode).
$3\ V_{DC} \le V_{LED} \le V^+$ $V_{REF}, V_{RHI}, V_{RLO} \le (V^+ - 1.5V)$
For higher power dissipations, pulse testing is used.$-0.015V \le V_{RHI} \le 12\ V_{DC}$ $0V \le V_{IN} \le V^+ - 1.5V$
(2) Pin 5 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.
(3) Accuracy is measured referred to 0 dB = + 10.000 V_{DC} at pin 5, with + 10.000 V_{DC} at pin 6, and 0.000 V_{DC} at pin 4. At lower full scale voltages, buffer and comparator offset voltage may add significant error. See Threshold Voltage.

ELECTRICAL CHARACTERISTICS[1][2] (continued)

Parameter	Conditions[1]	Min	Typ	Max	Units
VOLTAGE REFERENCE					
Output Voltage	0.1 mA ≤ $I_{L(REF)}$ ≤ 4 mA, $V^+ = V_{LED}$ = 5V	1.2	1.28	1.34	V
Line Regulation	3V ≤ V^+ ≤ 18V		0.01	0.03	%/V
Load Regulation	0.1 mA ≤ $I_{L(REF)}$ ≤ 4 mA, $V^+ = V_{LED}$ = 5V		0.4	2	%
Output Voltage Change with Temperature	0°C ≤ T_A ≤ +70°C, $I_{L(REF)}$ = 1 mA, $V^+ = V_{LED}$ = 5V		1		%
Adjust Pin Current			75	120	µA
OUTPUT DRIVERS					
LED Current	$V^+ = V_{LED}$ = 5V, $I_{L(REF)}$ = 1 mA	7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	V_{LED} = 5V, I_{LED} = 2 mA		0.12	0.4	mA
	V_{LED} = 5V, I_{LED} 20 mA		1.2	3	
LED Current Regulation	2V ≤ V_{LED} ≤ 17V, I_{LED} = 2 mA		0.1	0.25	mA
	I_{LED} = 20 mA		1	3	
Dropout Voltage	$I_{LED(ON)}$ = 20 mA, @ V_{LED} = 5V, ΔI_{LED} = 2 mA			1.5	V
Saturation Voltage	I_{LED} = 2.0 mA, $I_{L(REF)}$ = 0.4 mA		0.15	0.4	V
Output Leakage, Each Collector	(Bar Mode) [4]		0.1	10	µA
Output Leakage Pins 10–18	(Dot Mode) [4]		0.1	10	µA
Pin 1		60	150	450	µA
SUPPLY CURRENT					
Standby Supply Current (All Outputs Off)	V^+ = +5V, $I_{L(REF)}$ = 0.2 mA		2.4	4.2	mA
	V^+ = +20V, $I_{L(REF)}$ = 1.0 mA		6.1	9.2	mA

(4) Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+. LED #10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

THRESHOLD VOLTAGE[1]

Output	dB	Min	Typ	Max	Output	dB	Min	Typ	Max
1	−27	0.422	0.447	0.531	6	−12	2.372	2.512	2.819
2	−24	0.596	0.631	0.750	7	−9	3.350	3.548	3.825
3	−21	0.841	0.891	1.059	8	−6	4.732	5.012	5.309
4	−18	1.189	1.259	1.413	9	−3	6.683	7.079	7.498
5	−15	1.679	1.778	1.995	10	0	9.985	10	10.015

(1) Accuracy is measured referred to 0 dB = + 10.000 V_{DC} at pin 5, with + 10.000 V_{DC} at pin 6, and 0.000 V_{DC} at pin 4. At lower full scale voltages, buffer and comparator offset voltage may add significant error. See Threshold Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature

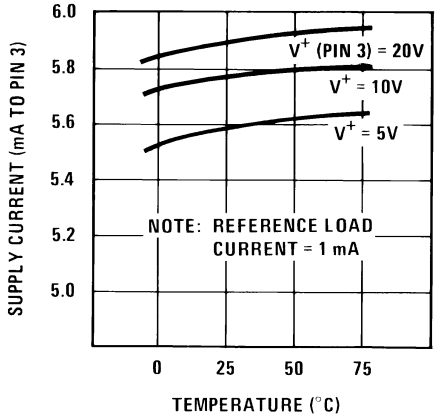


Figure 2.

Operating Input Bias Current vs Temperature

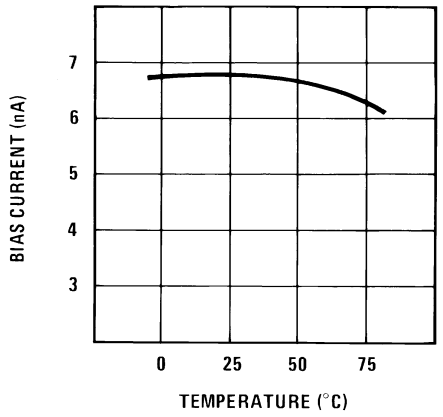


Figure 3.

Reference Voltage vs Temperature

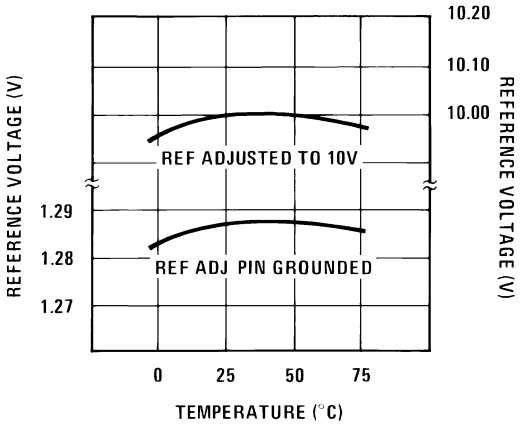


Figure 4.

Reference Adjust Pin Current vs Temperature

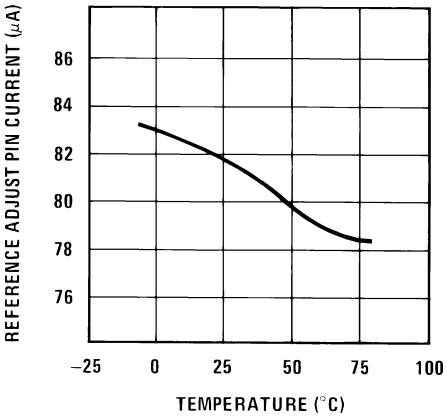


Figure 5.

LED Current-Regulation Dropout

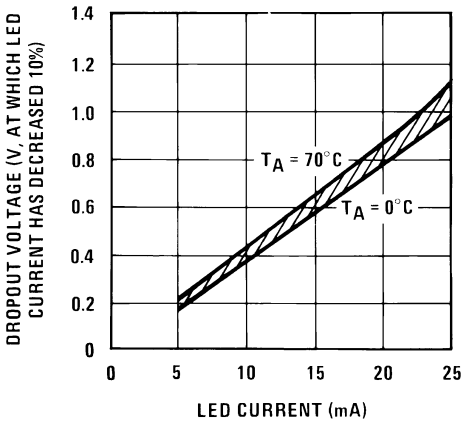


Figure 6.

LED Driver Saturation Voltage

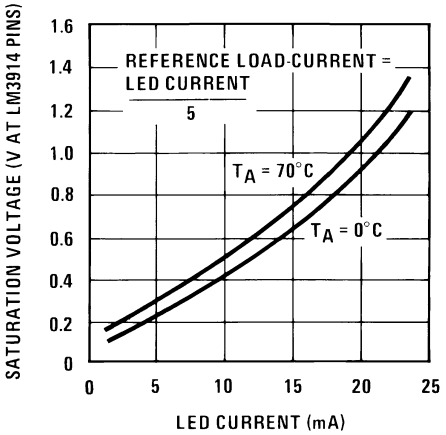


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Input Current Beyond Signal Range (Pin 5)

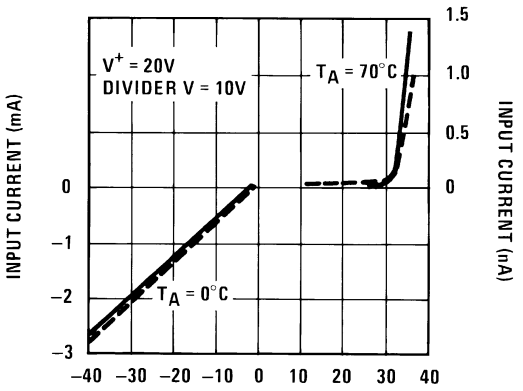


Figure 8.

LED Current vs Reference Loading

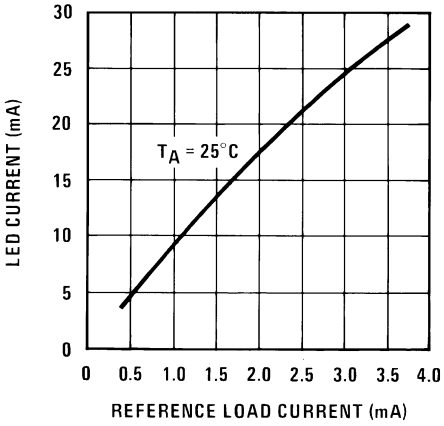


Figure 9.

LED Driver Current Regulation

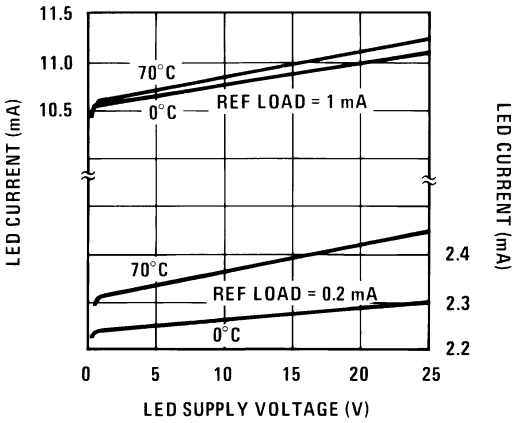


Figure 10.

Total Divider Resistance vs Temperature

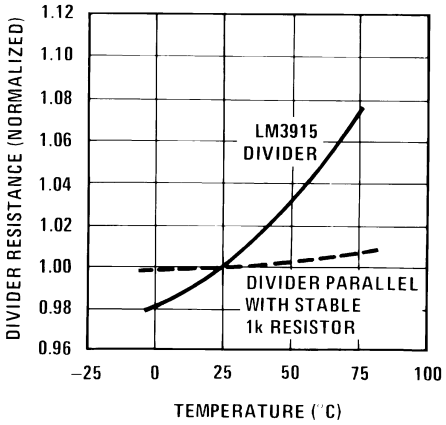


Figure 11.

Common-Mode Limits

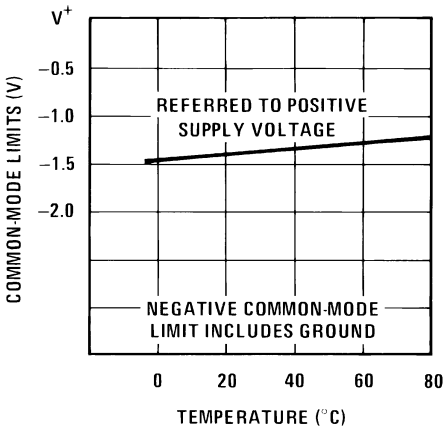


Figure 12.

Output Characteristics

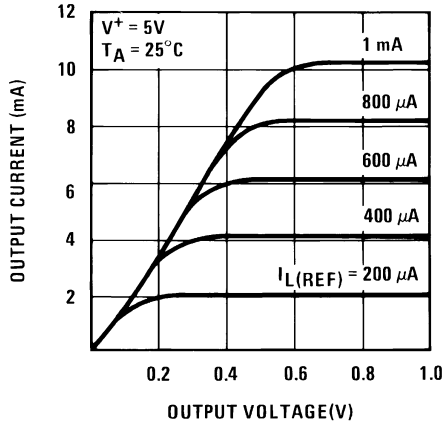
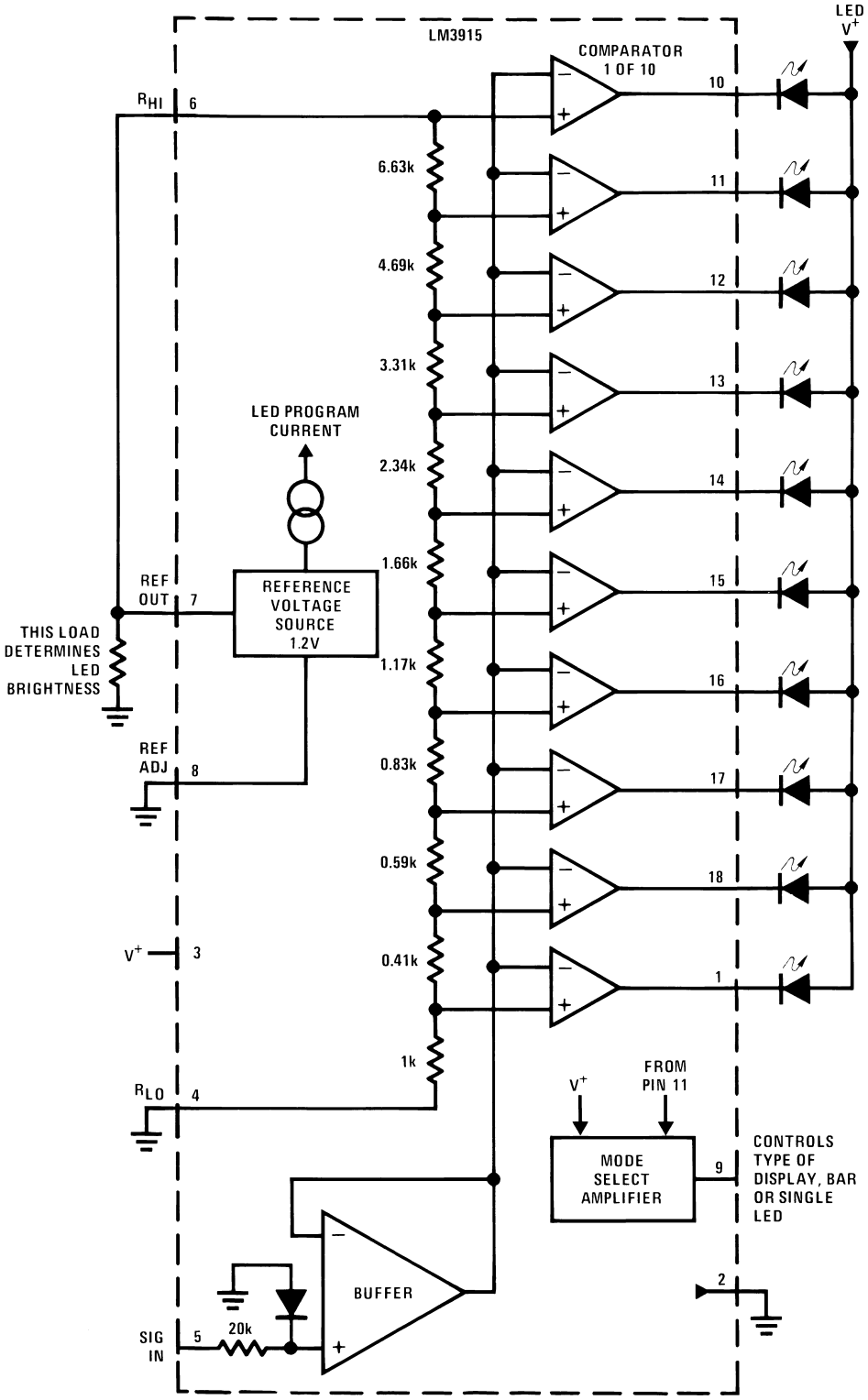


Figure 13.

BLOCK DIAGRAM

(Showing Simplest Application)



FUNCTIONAL DESCRIPTION

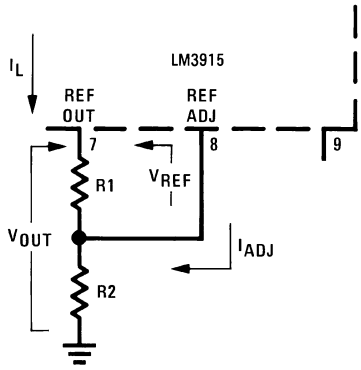
The simplified LM3915 block diagram is included to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. In this case, for each 3 dB that the input signal increases, a comparator will switch on another indicating LED. This resistor divider can be connected between any 2 voltages, providing that they are at least 1.5V below V^+ and no lower than V^-.

INTERNAL VOLTAGE REFERENCE

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2 \quad (1)$$



Since the 120 µA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes. For correct operation, reference load current should be between 80 µA and 5 mA. Load capacitance should be less than 0.05 µF.

CURRENT PROGRAMMING

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

The LM3915 outputs are current-limited NPN transistors as shown below. An internal feedback loop regulates the transistor drive. Output current is held at about 10 times the reference load current, independent of output voltage and processing variables, as long as the transistor is not saturated.

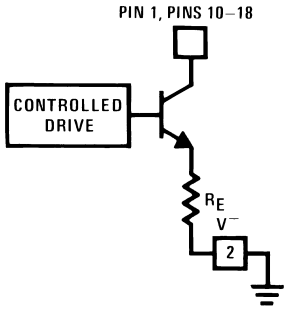


Figure 14. LM3915 Output Circuit

Outputs may be run in saturation with no adverse effects, making it possible to directly drive logic. The effective saturation resistance of the output transistors, equal to R_E plus the transistors' collector resistance, is about 50Ω. It's also possible to drive LEDs from rectified AC with no filtering. To avoid oscillations, the LED supply should be bypassed with a 2.2 µF tantalum or 10 µF aluminum electrolytic capacitor.

MODE PIN USE

Pin 9, the Mode Select input, permits chaining of multiple LM3915s, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

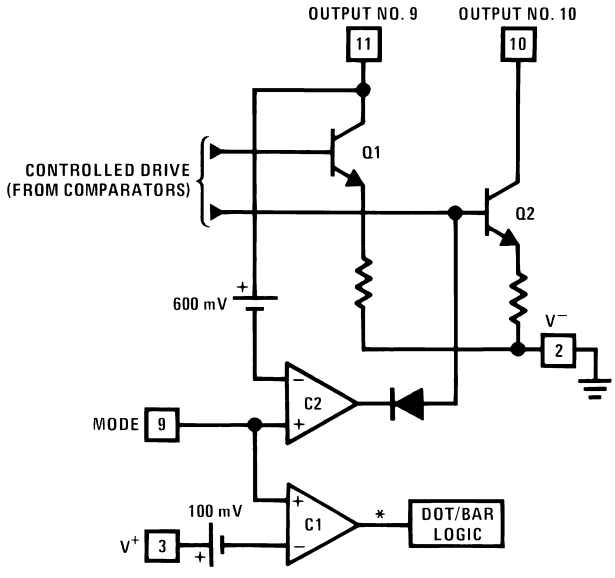
Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

Dot Display, Single LM3915 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* driver in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3915 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30 or more LED displays. The last LM3915 driver in the chain will have pin 9 left open. All previous drivers should have a 20k resistor in parallel with LED #9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.



*High for bar

Figure 15. Block Diagram of Mode Pin Function

DOT OR BAR MODE SELECTION

The voltage at pin 9 is sensed by comparator C1, nominally referenced to (V^+ − 100 mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

DOT MODE CARRY

In order for the display to make sense when multiple LM3915s are cascaded in dot mode, special circuitry has been included to shut off LED #10 of the first device when LED #1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted below.

As long as the input signal voltage is below the threshold of the second LM3915, LED #11 is off. Pin 9 of LM3915 #1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED #11, pin 9 of LM3915 #1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED #10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 µA) that is diverted from LED #9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 µA flowing through LED #11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of LM3915 #1 is held low enough to force LED #10 off when *any* higher LED is illuminated. While 100 µA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED #11 with a 10k resistor. The 1V IR drop is more than the 900 mV worst case required to hold off LED #10 yet small enough that LED #11 does not conduct significantly.

OTHER DEVICE CHARACTERISTICS

The LM3915 is relatively low-powered itself, and since any number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA. However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3916 with a 1 mA reference pin load (1.3k) would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An “overlap” is built in so that at no time are all segments completely off in the dot mode. Generally 1 LED fades in while the other fades out over a mV or more of range. The change may be much more rapid between LED #10 of one device and LED #1 of a *second* device “chained” to the first.

Application Hints

The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. Depending on the severity of the problem 0.05 µF to 2.2 µF decoupling capacitors from LED anode common to pin 2 will damp the circuit. If LED anode line wiring is inaccessible, often similar decoupling from pin 1 to pin 2 will be sufficient.

If LED turn ON seems slow (bar mode) or several LEDs light (dot mode), oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits. Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with at least a 0.001 µF capacitor, or up to 0.1 µF in noisy environments.

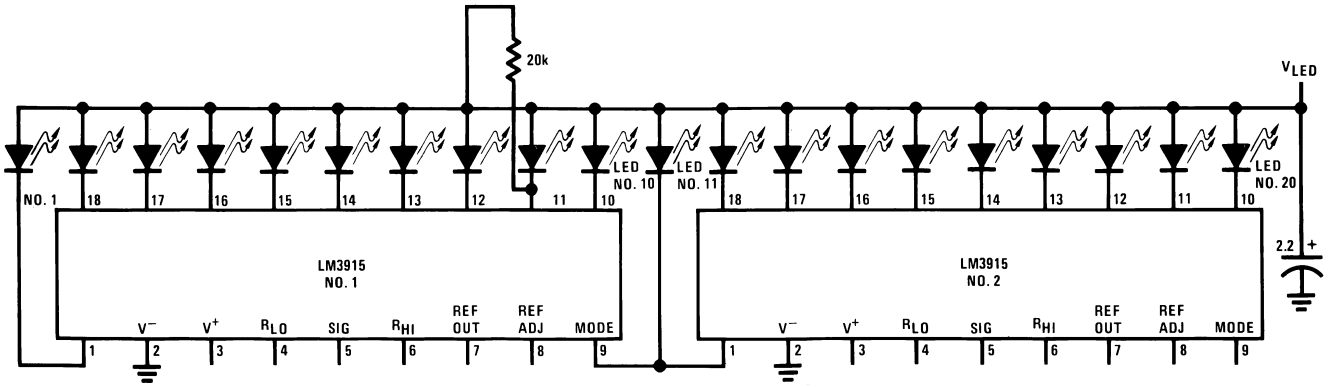


Figure 16. Cascading LM3915s in Dot Mode

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 µF solid tantalum capacitor to pin 2.

TIPS ON RECTIFIER CIRCUITS

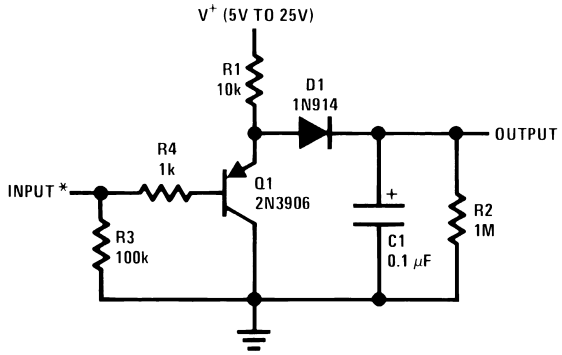
The simplest way to display an AC signal using the LM3915 is to apply it right to pin 5 unrectified. Since the LED illuminated represents the instantaneous value of the AC waveform, one can readily discern both peak and average values of audio signals in this manner. The LM3915 will respond to positive half-cycles only but will not be damaged by signals up to ±35V (or up to ±100V if a 39k resistor is in series with the input). It's recommended to use dot mode and to run the LEDs at 30 mA for high enough average intensity.

True average or peak detection requires rectification. If an LM3915 is set up with 10V full scale across its voltage divider, the turn-on point for the first LED is only 450 mV. A simple silicon diode rectifier won't work well at the low end due to the 600 mV diode threshold. The half-wave peak detector in *Figure 17* uses a PNP emitter-follower in front of the diode. Now, the transistor's base-emitter voltage cancels out the diode offset, within about 100 mV. This approach is usually satisfactory when a single LM3915 is used for a 30 dB display.

Display circuits using two or more LM3915s for a dynamic range of 60 dB or greater require more accurate detection. In the precision half-wave rectifier of *Figure 18* the effective diode offset is reduced by a factor equal to the open-loop gain of the op amp. Filter capacitor C2 charges through R3 and discharges through R2 and R3, so that appropriate selection of these values results in either a peak or an average detector. The circuit has a gain equal to R2/R1.

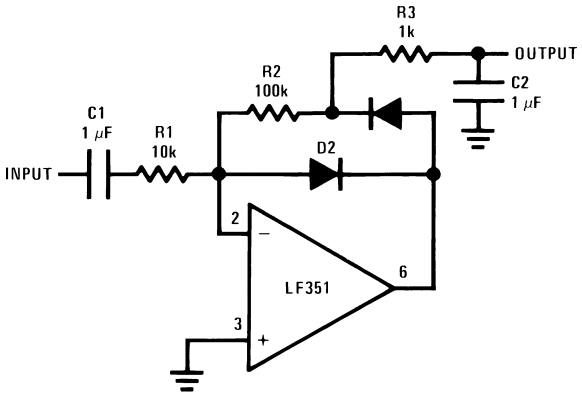
It's best to capacitively couple the input. Audio sources frequently have a small DC offset that can cause significant error at the low end of the log display. Op amps that slew quickly, such as the LF351, LF353, or LF356, are needed to faithfully respond to sudden transients. It may be necessary to trim out the op amp DC offset voltage to accurately cover a 60 dB range. Best results are obtained if the circuit is adjusted for the correct output when a low-level AC signal (10 mV to 20 mV) is applied, rather than adjusting for zero output with zero input.

For precision full-wave averaging use the circuit in Figure 19. Using 1% resistors for R1 through R4, gain for positive and negative signal differs by only 0.5 dB worst case. Substituting 5% resistors increases this to 2 dB worst case. (A 2 dB gain difference means that the display may have a ±1 dB error when the input is a nonsymmetrical transient). The averaging time constant is R5–C2. A simple modification results in the precision full-wave detector of Figure 20. Since the filter capacitor is not buffered, this circuit can drive only high impedance loads such as the input of an LM3915.



*DC Couple

Figure 17. Half-Wave Peak Detector



D1, D2: 1N914 or 1N4148

See Precision Half-Wave Rectifier Table

R1 = R2 for A_V = 1

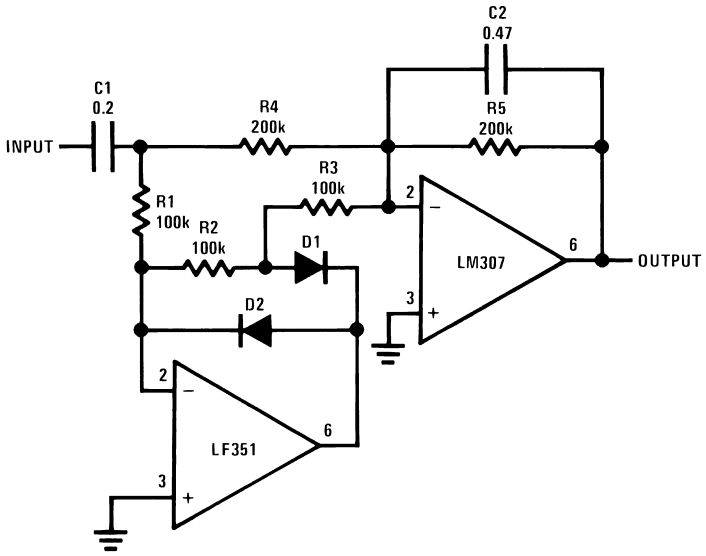
R1 = R2/R10 for A_V = 10

C1 = 10/R1

Figure 18. Precision Half-Wave Rectifier

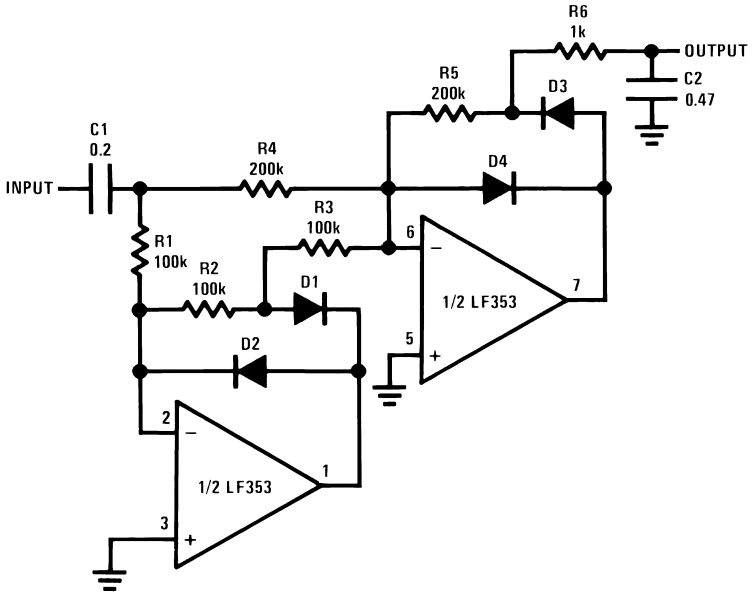
Precision Half-Wave Rectifier

	Average	Peak
R2	1k	100k
R3	100k	1k



D1, D2: 1N914 or 1N4148

Figure 19. Precision Full-Wave Average Detector



D1, D2, D3, D4: 1N914 or 1N4148

Figure 20. Precision Full-Wave Peak Detector

CASCADING THE LM3915

To display signals of 60 dB or 90 dB dynamic range, multiple LM3915s can be easily cascaded. Alternatively, it is possible to cascade an LM3915 with LM3914s for a log/linear display or with an LM3916 to get an extended range VU meter.

A simple, low cost approach to cascading two LM3915s is to set the reference voltages of the two chips 30 dB apart as in Figure 21. Potentiometer R1 is used to adjust the full scale voltage of LM3915 #1 to 316 mV nominally while the second IC's reference is set at 10V by R4. The drawback of this method is that the threshold of LED #1 is only 14 mV and, since the LM3915 can have an offset voltage as high as 10 mV, large errors can occur. This technique is not recommended for 60 dB displays requiring good accuracy at the first few display thresholds.

A better approach shown in Figure 22 is to keep the reference at 10V for both LM3915s and amplify the input signal to the lower LM3915 by 30 dB. Since two 1% resistors can set the amplifier gain within ±0.2 dB, a gain trim is unnecessary. However, an op amp offset voltage of 5 mV will shift the first LED threshold as much as 4 dB, so that an offset trim may be required. Note that a single adjustment can null out offset in both the precision rectifier and the 30 dB gain stage. Alternatively, instead of amplifying, input signals of sufficient amplitude can be fed directly to the lower LM3915 and *attenuated* by 30 dB to drive the second LM3915.

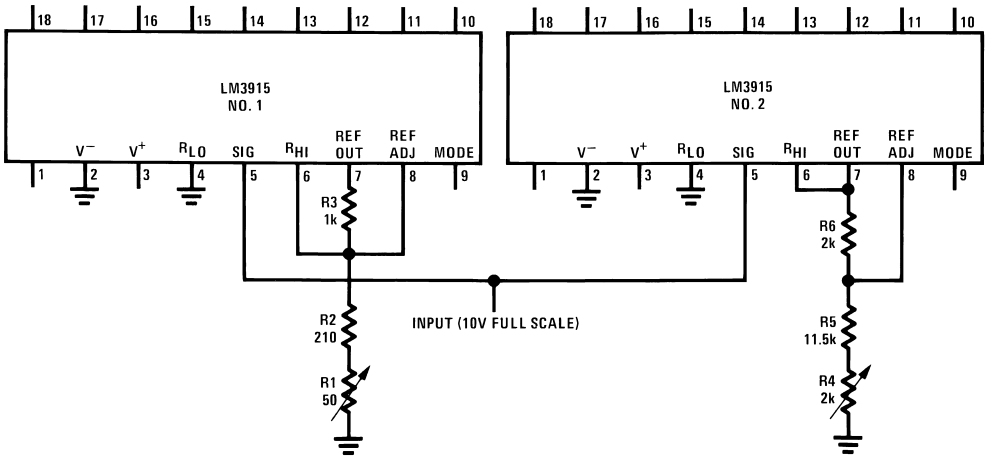


Figure 21. Low Cost Circuit for 60 dB Display

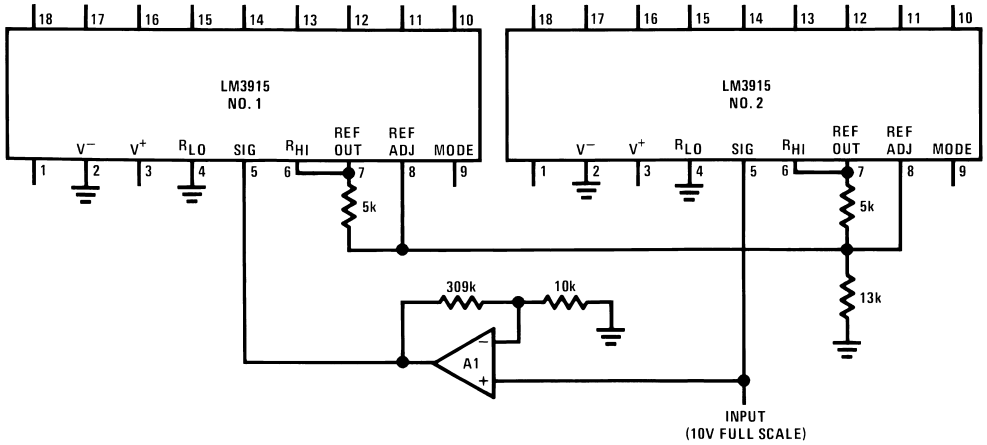


Figure 22. Improved Circuit for 60 dB Display

To extend this approach to get a 90 dB display, another 30 dB of amplification must be placed in the signal path ahead of the lowest LM3915. Extreme care is required as the lowest LM3915 displays input signals down to 0.5 mV! Several offset nulls may be required. High currents should not share the same path as the low level signal. Also power line wiring should be kept away from signal lines.

TIPS ON REFERENCE VOLTAGE AND LED CURRENT PROGRAMMING

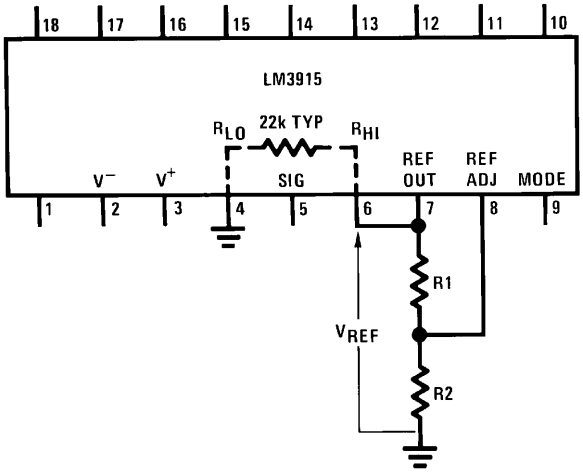
Single LM3915

The equations in Figure 23 illustrate how to choose resistor values to set reference voltage for the simple case where no LED intensity adjustment is required. A LED current of 10 mA to 20 mA generally produces adequate illumination. Having 10V full-scale across the internal voltage divider gives best accuracy by keeping signal level high relative to the offset voltage of the internal comparators. However, this causes 450 µA to flow from pin 7 into the divider which means that the LED current will be at least 5 mA. R1 will typically be between 1 kΩ and 2 kΩ. To trim the reference voltage, vary R2.

The circuit in Figure 24 shows how to add a LED intensity control which can vary LED current from 9 mA to 28 mA. The reference adjustment has some effect on LED intensity but the reverse is not true.

Multiple LM3915s

Figure 25 shows how to obtain a common reference trim and intensity control for two LM3915s. The two ICs may be connected in cascade for a 60 dB display or may be handling separate channels for stereo. This technique can be extended for larger numbers of LM3915s by varying the values of R1, R2 and R3 in inverse proportion to the number of devices tied in. The ICs' internal references track within 100 mV so that worst case error from chip to chip is only 0.1 dB for V_{REF} = 10V.

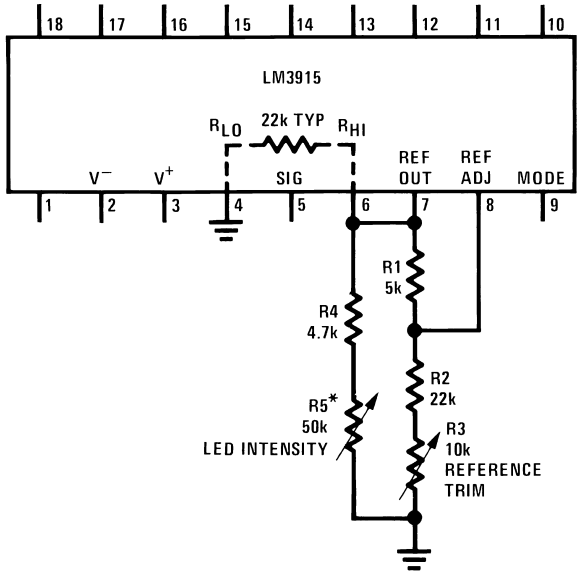


Adjust R2 to vary V_{REF}

$$\text{Pick R1} = \frac{12.5V}{I_{LED} - V_{REF}/2.2\,k\Omega}$$

$$\text{Pick R2} = \frac{(V_{REF} - 1.25V)}{(1.25V/R1) + 0.08\,mA}$$

Figure 23. Design Equations for Fixed LED Intensity



*9 mA < I_{LED} < 28 mA @ V_{REF} = 10V

Figure 24. Varying LED Intensity

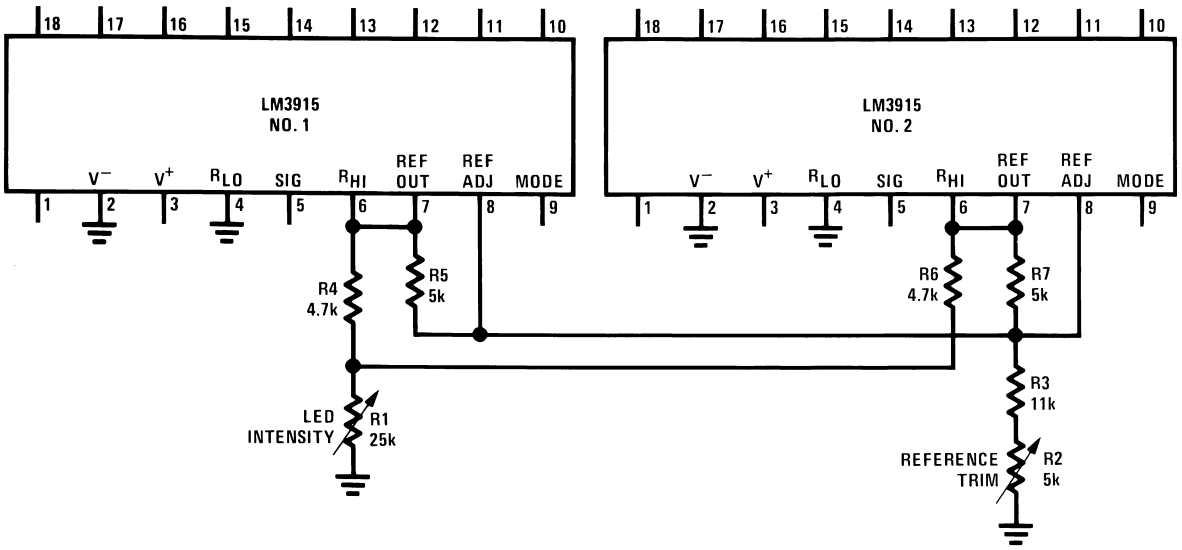


Figure 25. Independent Adjustment of Reference Voltage and LED Intensity for Multiple LM3915s

The scheme in Figure 26 is useful when the reference and LED intensity must be adjusted independently over a wide range. The R_{HI} voltage can be adjusted from 1.2V to 10V with no effect on LED current. Since the internal divider here does not load down the reference, minimum LED current is much lower. At the minimum recommended reference load of 80 µA, LED current is about 0.8 mA. The resistor values shown give a LED current range from 1.5 mA to 20 mA.

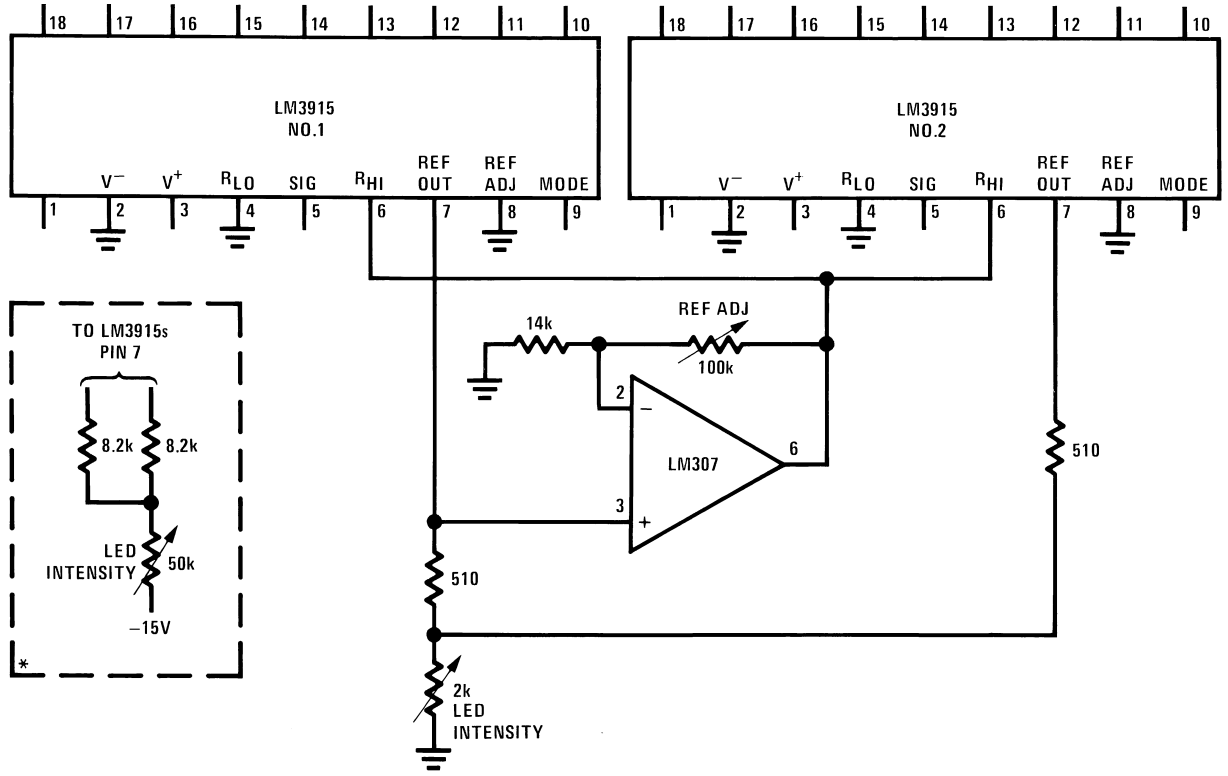
At the low end of the intensity adjustment, the voltage drop across the 510Ω current-sharing resistors is so small that chip to chip variation in reference voltage may yield a visible variation in LED intensity. The optional approach shown of connecting the bottom end of the intensity control pot to a negative supply overcomes this problem by allowing a larger voltage drop across the (larger) current-sharing resistors.

Other Applications

For increased resolution, it's possible to obtain a display with a smooth transition between LEDs. This is accomplished by varying the reference level at pin 6 by 3 dBp-p as shown in Figure 27. The signal can be a triangle, sawtooth or sine wave from 60 Hz to 1 kHz. The display can be run in either dot or bar mode.

When an exponentially decaying RC discharge waveform is applied to pin 5, the LM3915's outputs will switch at equal intervals. This makes a simple timer or sequencer. Each time interval is equal to RC/3. The output may be used to drive logic, opto-couplers, relays or PNP transistors, for example.

Typical Applications



*Optional circuit for improved intensity matching at low currents.
See text.

Figure 26. Wide-Range Adjustment of Reference Voltage and LED Intensity for Multiple LM3915s

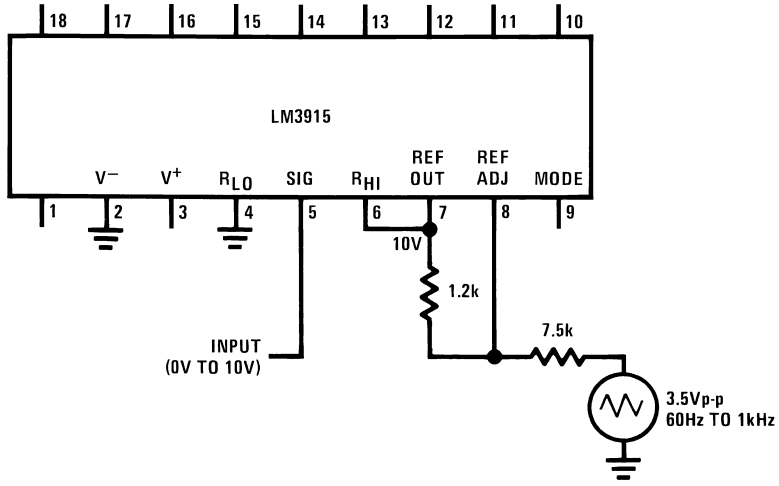
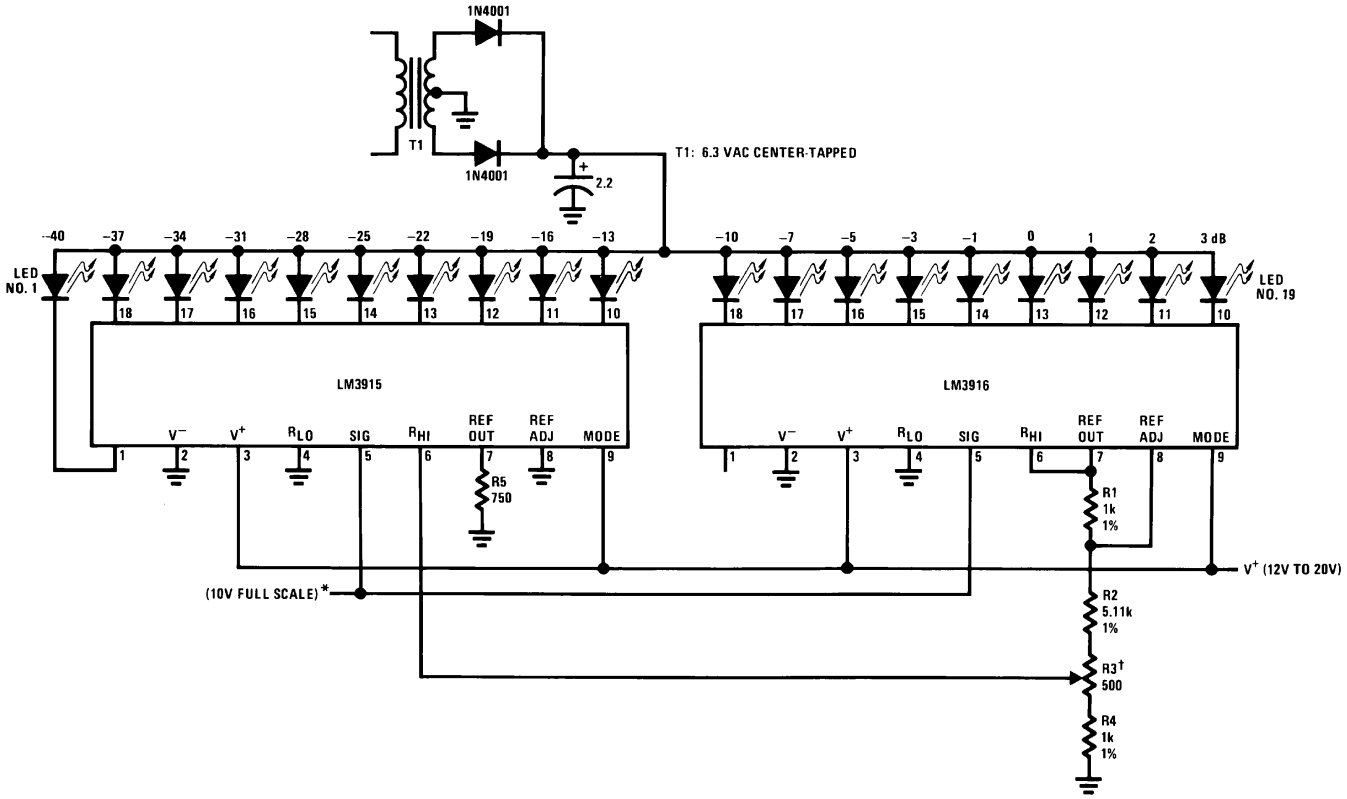


Figure 27. 0V to 10V Log Display with Smooth Transitions



This application shows that the LED supply requires minimal filtering.
*See Application Hints for optional Peak or Average Detector.
†Adjust R3 for 3 dB difference between LED #11 and LED #12.

Figure 28. Extended Range VU Meter

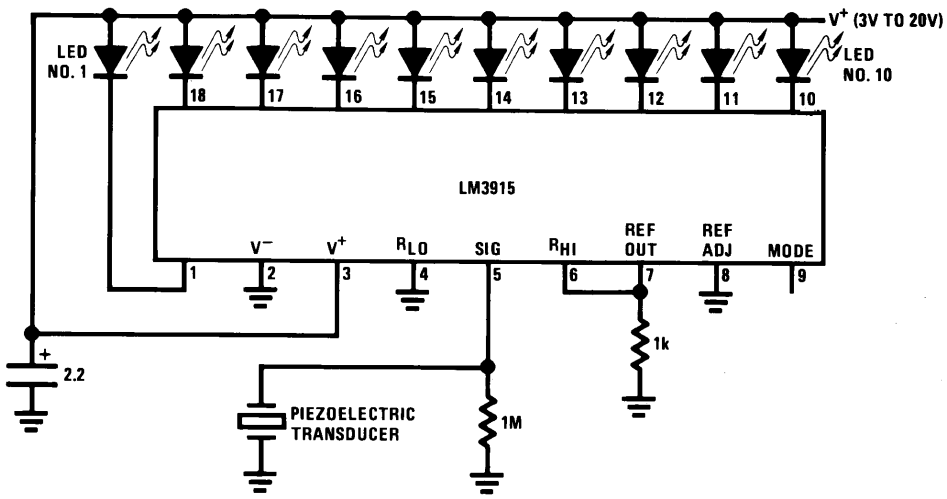
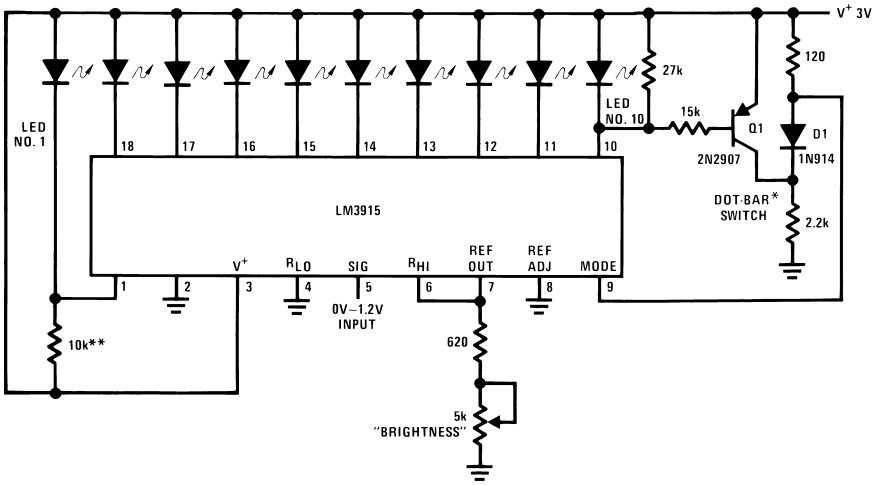


Figure 29. Vibration Meter

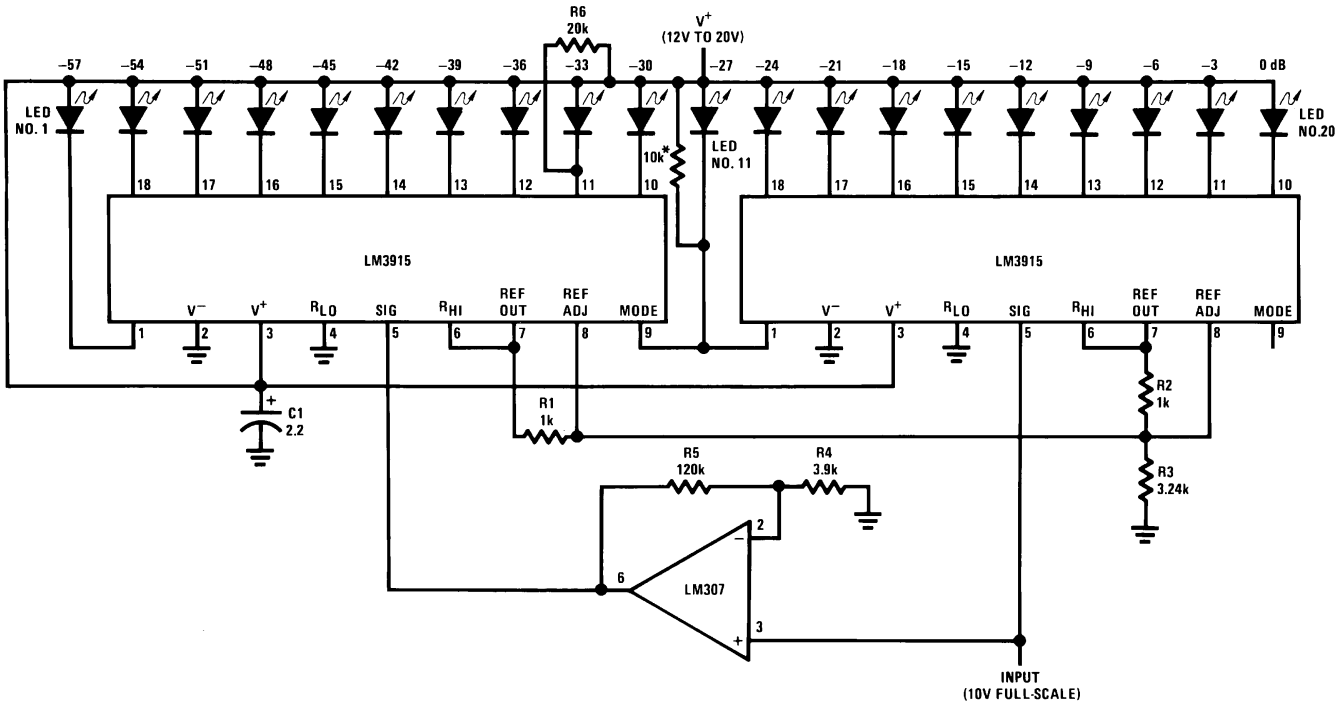
LED	Threshold
1	60 mV
2	80 mV
3	110 mV

LED	Threshold
4	160 mV
5	220 mV
6	320 mV
7	440 mV
8	630 mV
9	890 mV
10	1.25V



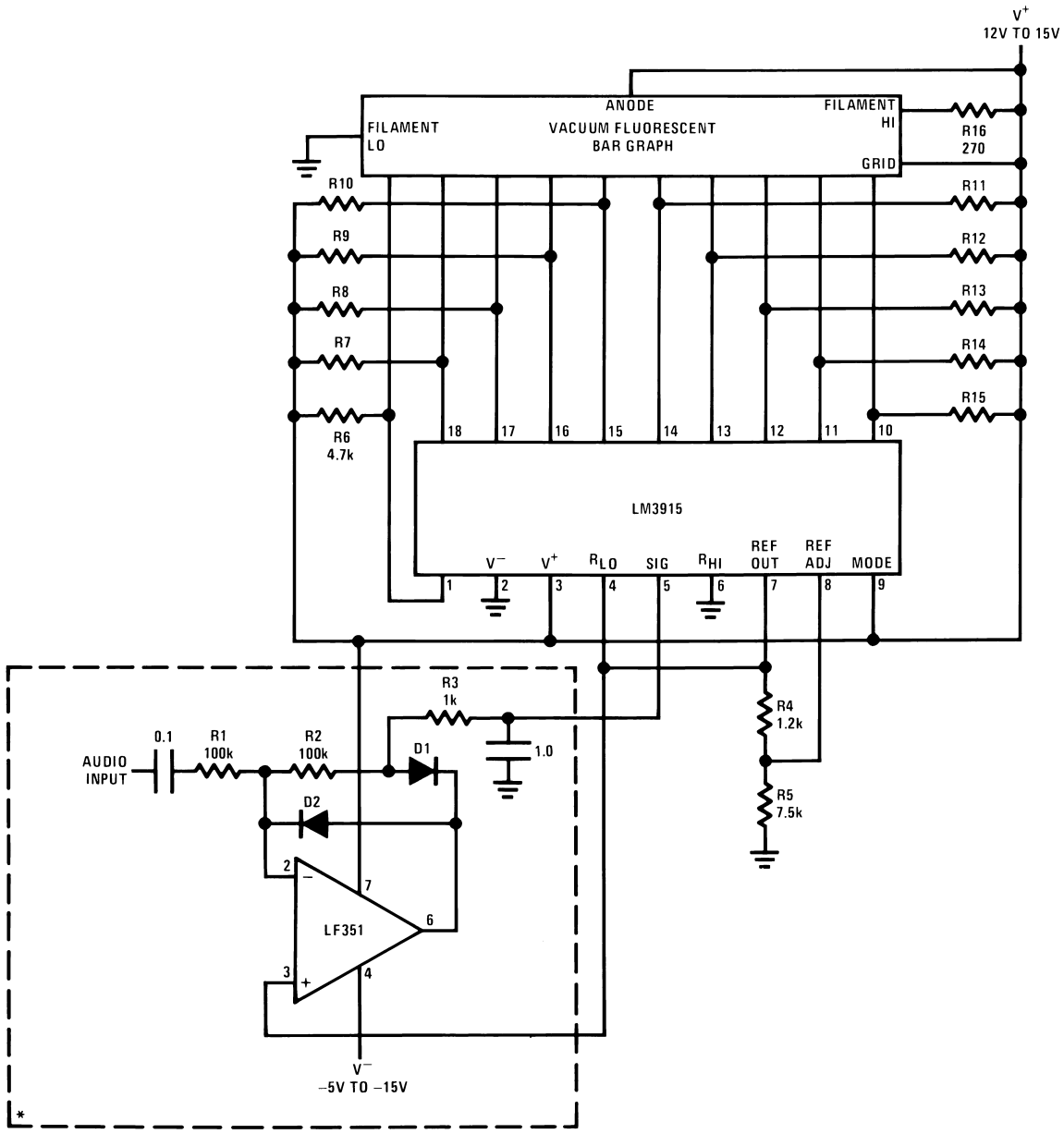
*The input to the dot bar switch may be taken from cathodes of other LEDs.
Display will change to bar as soon as the LED so selected begins to light.
**Optional. Shunts 100 µA auxiliary sink current away from LED #1.

Figure 30. Indicator and Alarm, Full-Scale Changes Display from Dot to Bar



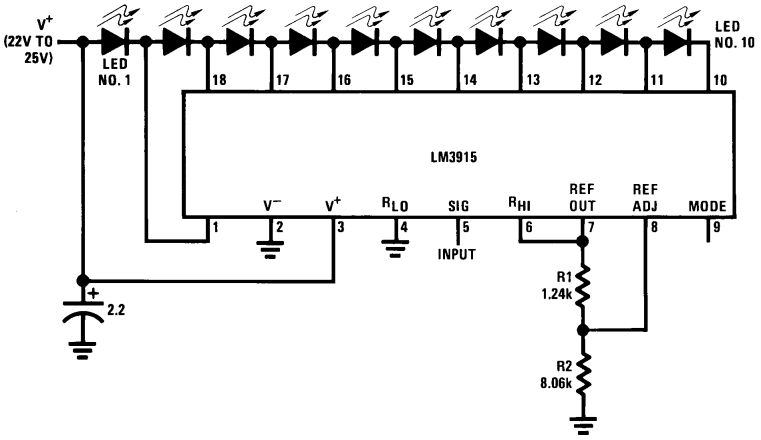
**Optional. Shunts 100 µA auxiliary sink current away from LED #11.

Figure 31. 60 dB Dot Mode Display



R7 thru R15: 10k ±10%
D1, D2: 1N914 or 1N4148
*Half-wave peak detector.
See Application Hints.

Figure 32. Driving Vacuum Fluorescent Display



Supply current drain is only 15 mA with ten LEDs illuminated.

Figure 33. Low Current Bar Mode Display

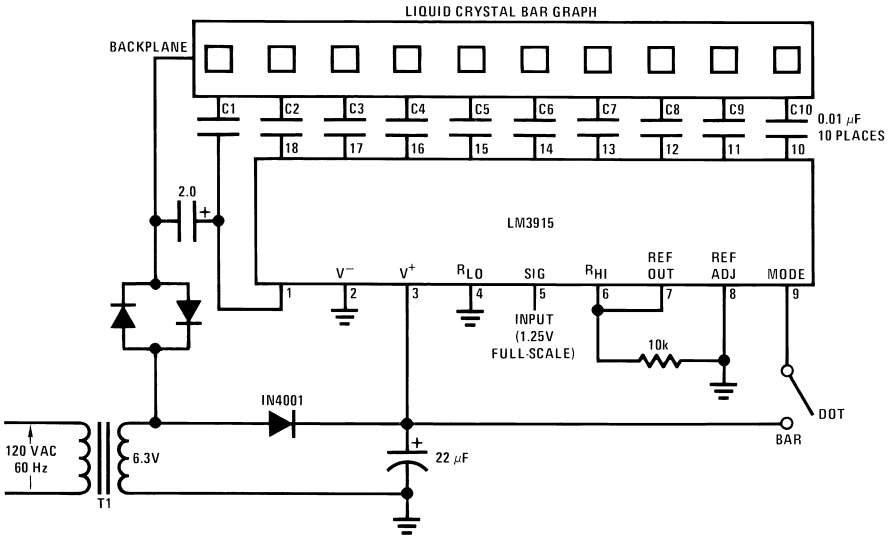
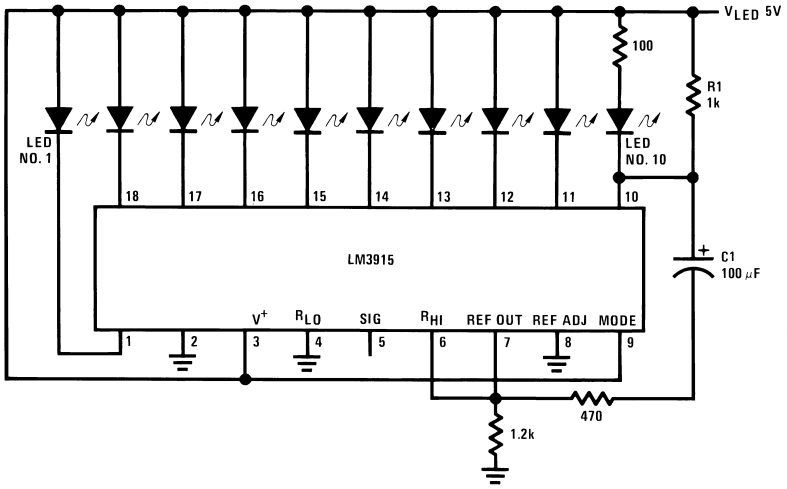
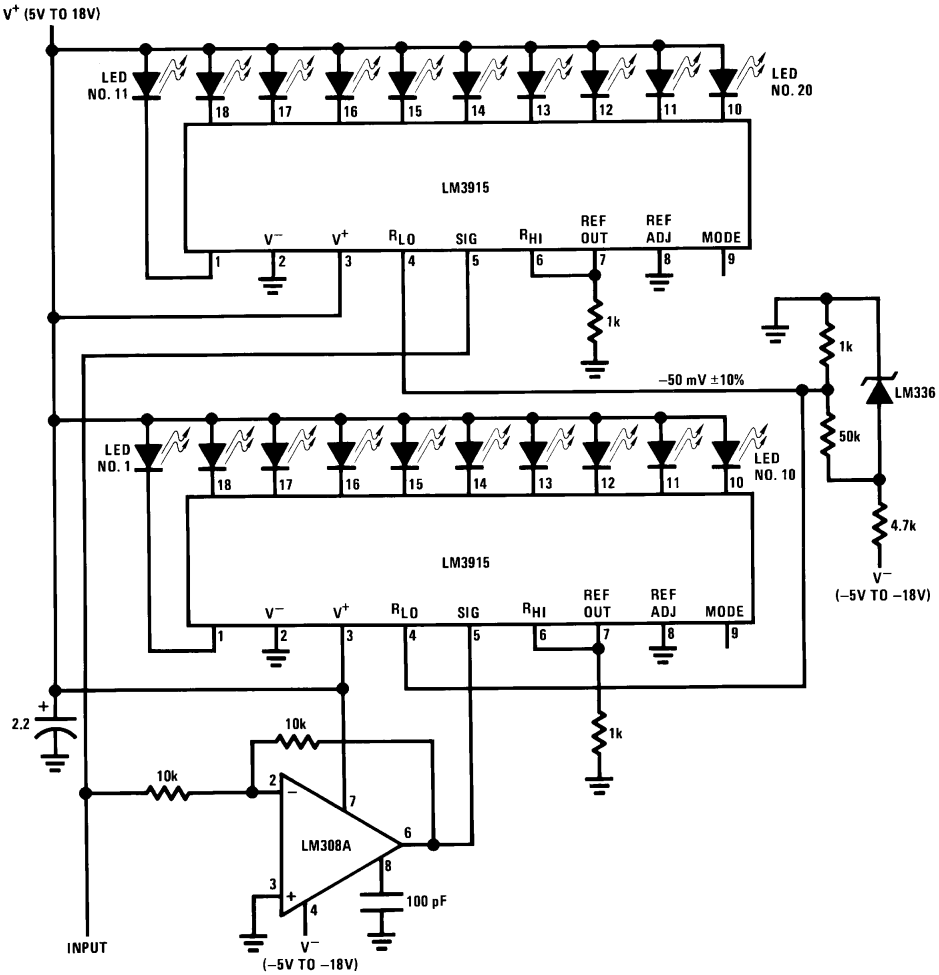


Figure 34. Driving Liquid Crystal Display



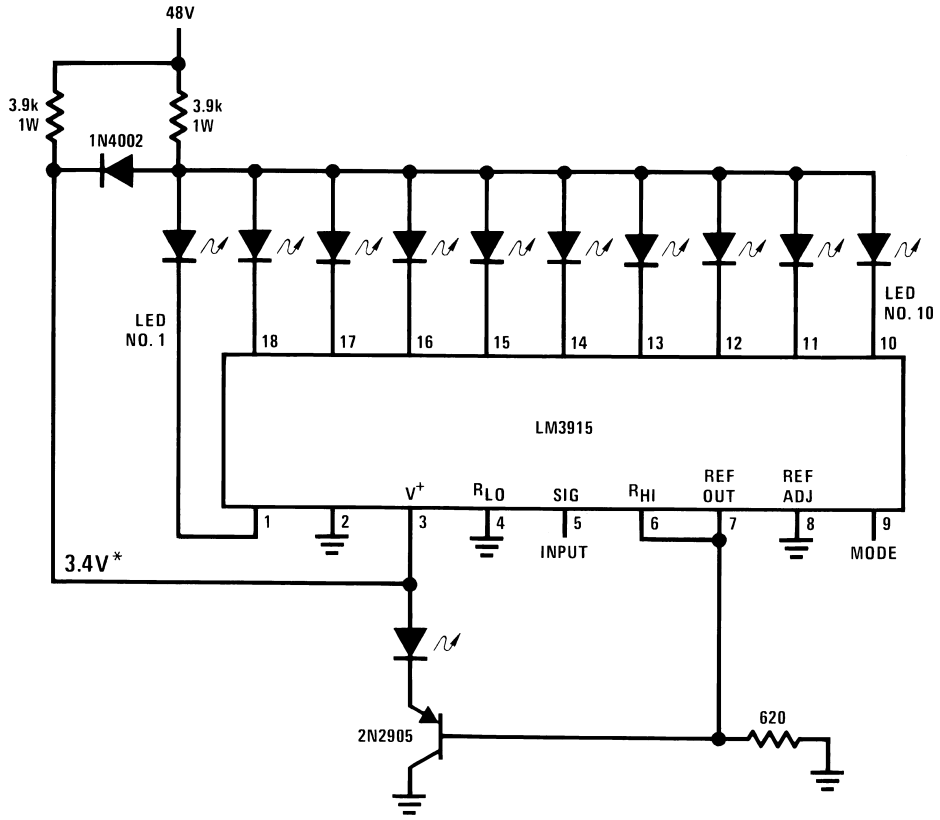
Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.

Figure 35. Bar Display with Alarm Flasher



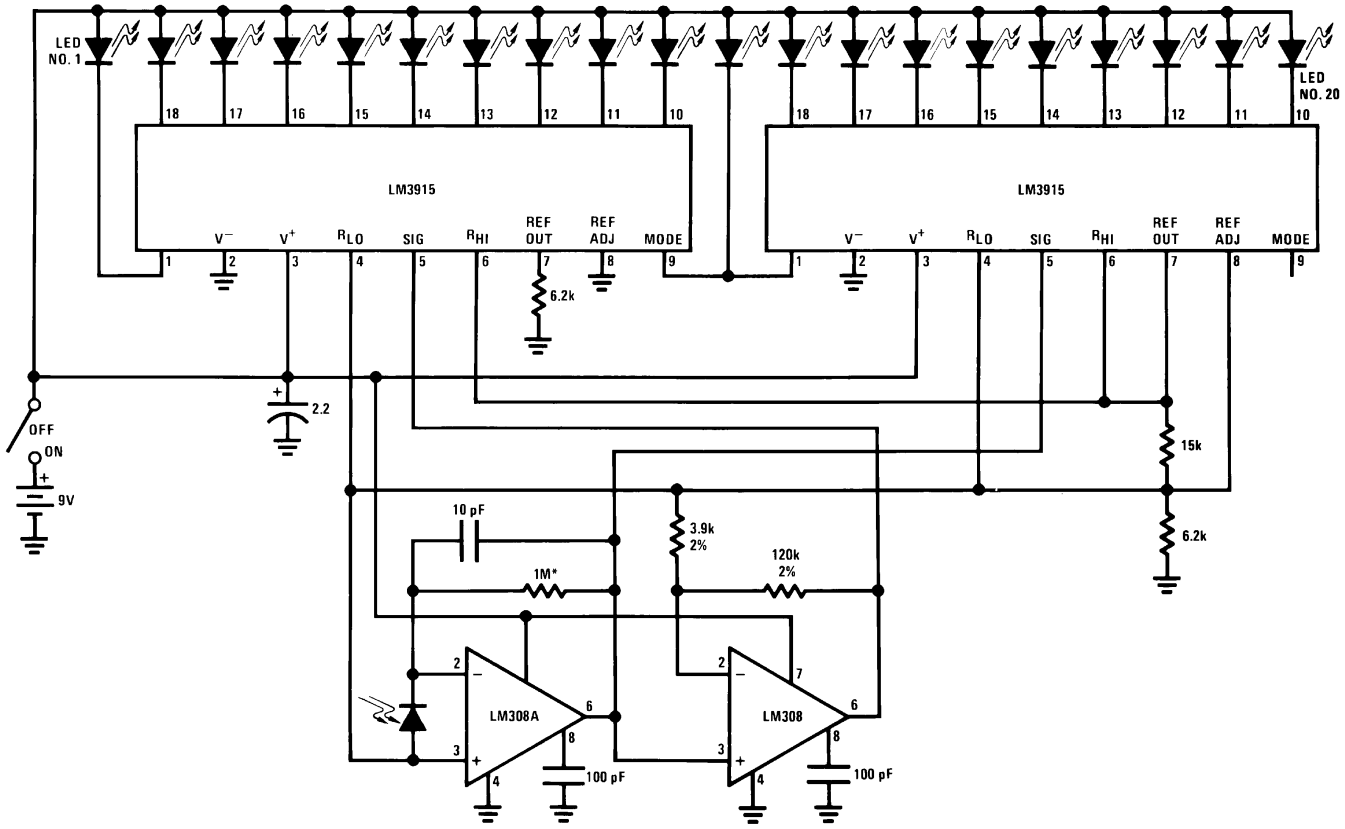
Logarithmic response allows coarse and fine adjustments without changing scale.
Resolution ranges from 10 mV at V_{IN} = 0 mV to 500 mV at V_{IN} = ±1.25V.

Figure 36. Precision Null Meter



The LED currents are approximately 10 mA, and the LM3915 outputs operate in saturation for minimum dissipation.
*This point is partially regulated and decreases in voltage with temperature. Voltage requirements of the LM3915 also decrease with temperature.

Figure 37. Operating with a High Voltage Supply (Dot Mode Only)



*Resistor value selects exposure
1/2 f/stop resolution
Ten f/stop range (1000:1)
Typical supply current is 8 mA.

Figure 38. Light Meter

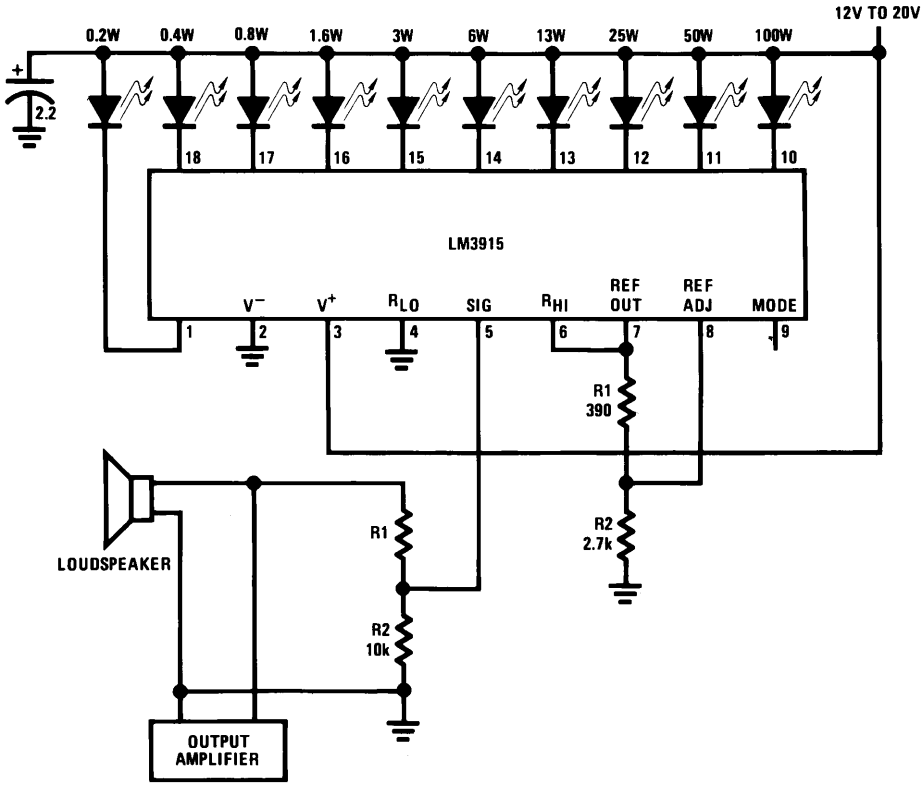
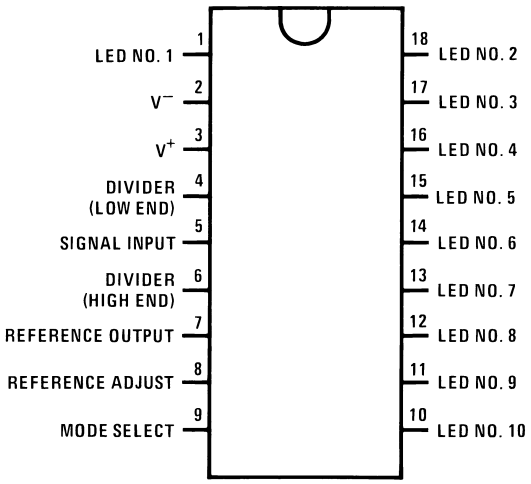


Figure 39. Audio Power Meter

Load Impedance	R1
4Ω	10k
8Ω	18k
16Ω	30k

Connection Diagram



*Discontinued, Life Time Buy date 12/20/99

Figure 40. PDIP Package
Top View
See Package Number NFK0018A

Definition of Terms

Absolute Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference adjust pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

Line Regulation: The average change in reference output voltage (V_{REF}) over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage over the specified range of load current ($I_{L(REF)}$).

Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

Relative Accuracy: The difference between any two adjacent threshold points. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	27

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3915N-1	ACTIVE	PDIP	NFK	18	20	TBD	Call TI	Call TI	0 to 70	LM3915N-1	Samples
LM3915N-1/NOPB	ACTIVE	PDIP	NFK	18	20	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	0 to 70	LM3915N-1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

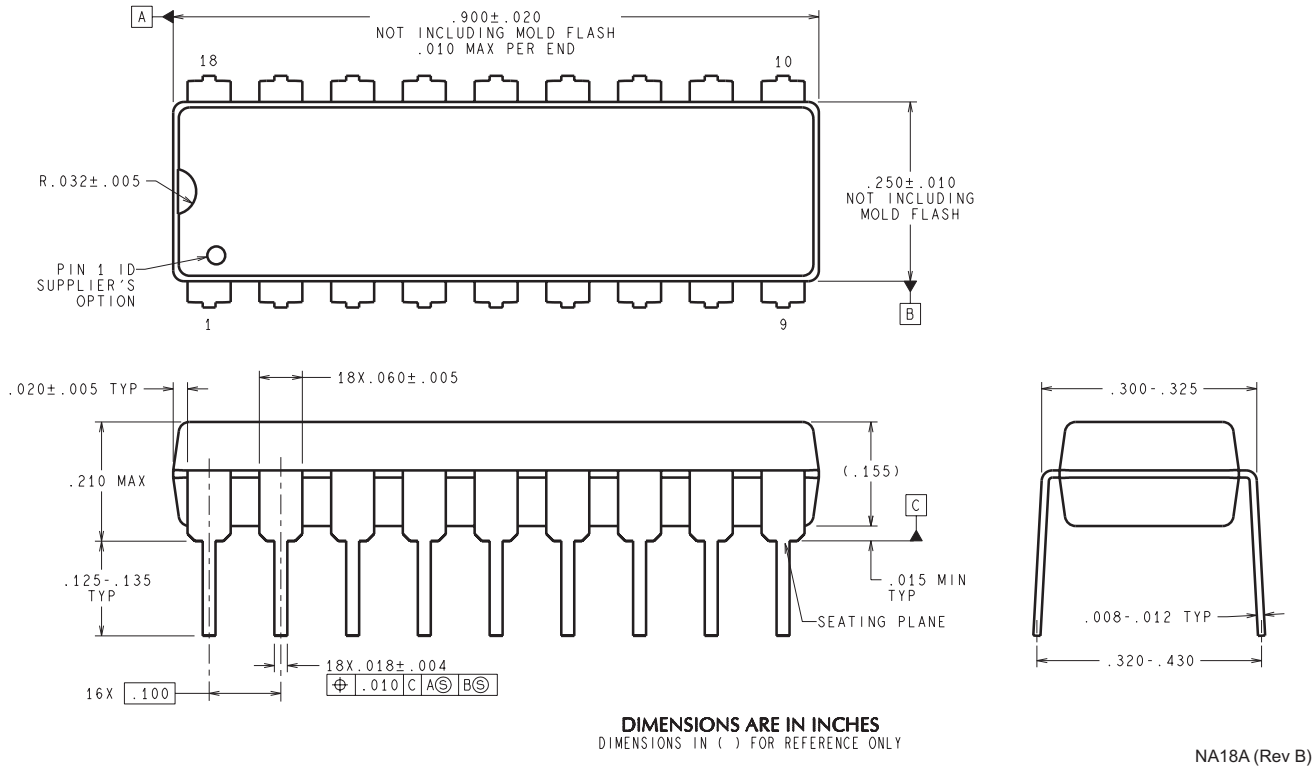
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

NFK0018A



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

NA18A (Rev B)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265