TRABAJO DE FIN DE GRADO

Título:

Diseño e implementación de un módulo didáctico para prácticas docentes de electrónica.

Autor: Ángel Hernández González

Tutores: D. Silvestre Rodríguez Pérez
Dña. Beatriz Rodríguez Mendoza

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INTRODUCCIÓN.

1.1 RESUMEN.

En este proyecto se propone el diseño e implementación en placa de circuito impreso o PCB (*Printed Circuit Board*) de un sistema electrónico que se empleará como módulo didáctico para la realización de experiencias prácticas orientadas a que el estudiante se familiarice con la utilización de los analizadores lógicos para el análisis y comprobación del funcionamiento de los elementos o bloques digitales de un circuito electrónico digital.

El módulo o sistema electrónico en el que se basa el módulo consiste en un conversor analógico-digital (A/D) basado en el método de conversión denominado contador-rampa. El conversor diseñado e implementado se puede utilizar como un CAD de 8 o de 4 bits de resolución, dependiendo del estado de la señal de control incluida para ese fin y que es accesible por el usuario. El conversor, además del contador binario, del CDA y del comparador en el que se basa cualquier CAD basado en el método contador-rampa, incorpora un contador BCD (*Binary Coded Decimal*) de dos dígitos, dos decodificadores BCD a 7 segmentos y dos visualizadores de 7 segmentos, cuya finalidad es la de mostrar el valor decimal de la palabra digital de salida resultante de la conversión.

Para su implementación, basada principalmente en la utilización de tecnología SMD, se ha usado la herramienta de software libre de modelado de circuitos impresos denominada KiCAD. La placa de circuito impreso diseñada, fácil de manejar, incorpora diversos puntos de prueba que sirven para analizar las diferentes señales analógicas y digitales presentes en el circuito.

1.2 ABSTRACT.

This project proposes the design and implementation on a printed circuit board or PCB (Printed Circuit Board) of an electronic system that will be used as a didactic module to carry out practical experiences oriented to familiarizing the student with the use of logic analyzers for the analysis and verification of the operation of the elements or digital blocks of a digital electronic circuit.

The module or electronic system which the module is based consists of an analog-digital (A / D) converter based on the conversion method called counter-ramp. The designed and implemented converter can be used as an 8 or 4-bit resolution ADC depending on the state of the control signal included for that purpose and which is accessible by the user. The converter, in addition to the binary counter, the DAC and the comparator on which any ADC based on the counter-ramp method is based, incorporates a two-digit BCD (Binary Coded Decimal) counter, two 7-segment BCD decoders and two displays of 7 segments, whose purpose is to show the decimal value of the digital output word resulting from the conversion.

For its implementation, based mainly on the use of SMD technology, was used the free software tool for printed circuit modeling called KiCAD. The designed printed circuit board, easy to handle, incorporates various test points that are used to analyze the different analog and digital signals present in the circuit.

MEMORIA

Capítulo 1: Introducción general. Objetivos.

1.1 Introducción general.

Los circuitos electrónicos se pueden dividir en dos grandes grupos: los analógicos y los digitales, teniendo ambos tipos de circuitos una gran importancia en el mundo tecnológico actual. Para entender su funcionamiento, es necesario comprender las diferencias que existen entre las señales analógicas y digitales que producen, así como conocer cuáles son las ventajas de un tipo de circuitos frente a los otros.

Las señales analógicas son aquellas que encontramos con mayor facilidad en la naturaleza y se caracterizan porque su magnitud es capaz de tomar cualquier valor, es decir, no es una señal cuantificada. En cambio, una señal digital es todo lo contrario, es una señal cuyos valores de amplitud sí están cuantificados, es decir, limitados a pertenecer a un conjunto de valores fijos o discretos. Las señales digitales son más inmunes al ruido que las analógicas, pero a costa de requerir un mayor ancho de banda para portar o transmitir la misma información. Además, las señales digitales son más fáciles de procesar, es decir, manipularlas matemáticamente para modificarlas, mejorarlas, almacenarlas e incluso representarlas.

Con el paso del tiempo, el avance de la tecnología ha hecho que hoy en día casi todos los equipos electrónicos incorporen elementos de procesamiento y de representación que requieren entradas digitales. De ahí nace la necesidad de disponer de circuitos electrónicos capaces de realizar la conversión de una señal de tipo analógica a digital, lo cual engloba un proceso de digitalización. El proceso de digitalizar una señal analógica puede implicar las operaciones de muestreo, cuantificación y codificación. En el proceso de muestreo se obtiene a partir de una señal analógica continua en el tiempo y en amplitud, una señal discretizada en el tiempo, pero continua en el dominio de amplitudes. El proceso de cuantificación consiste en representar la amplitud continua de la señal mediante un número finito o discreto de valores en los instantes determinados por el proceso de muestreo, y el de codificación, en asignar una palabra de un código digital a cada uno de los niveles de amplitud discretos obtenidos tras el proceso de cuantificación. Los circuitos electrónicos capaces de convertir señales de tipo analógico a digital y de digital a analógico, se denominan Convertidores o conversores de señal Analógica a Digital (CAD) y de señal Digital a Analógica (CDA), respectivamente.

1.2 Conversor analógico-digital: método contador-rampa.

Un conversor analógico-digital (CAD) es un dispositivo que ofrece una salida digital a partir de una señal analógica de entrada. El funcionamiento de un conversor se basa en comparar la tensión analógica de entrada al conversor (V_X), con una tensión de referencia (V_R) que varía a lo largo del tiempo. Es decir, consiste en variar una tensión de referencia hasta que la diferencia $|V_X-V_R|$ queda dentro del error de cuantificación que define las prestaciones del conversor. Las distintas formas de variar V_R con el tiempo definen los

diferentes métodos de conversión: el método contador-rampa, el de aproximaciones sucesivas, el de rampa doble, etc.

En la Figura 1.1 se muestra el diagrama de bloques de un CAD de 4 bits codificados en BCD (*Binary Coded Decimal*) basado en el método contador-rampa, que emplea un visualizador de 7 segmentos para representar el valor decimal de la palabra digital resultante de la conversión [1]. Como se puede observar, el CAD consta de un contador y un conversor digital-analógico (CDA) de 4 bits, un comparador y los circuitos electrónicos encargados de capturar, almacenar y representar el valor de la palabra digital resultante de la conversión. En el método contador-rampa se compara la entrada (V_X) con una tensión analógica de referencia (V_R) generada a través de un CDA y un contador, siendo la palabra digital resultante de la conversión, la salida del contador [2]. Al iniciar la conversión, el contador se pone a cero, y su salida se va incrementando hasta que la tensión de salida (V_R) del CDA rebasa el valor de la entrada, situación que es detectada por el comparador. Una vez V_R ha "alcanzado" a la entrada, finaliza la conversión analógica-digital, siendo la palabra digital resultante de la conversión, la salida del contador. En el conversor representado en la Figura 1.1, además del contador, del CDA y del comparador, se emplea un registro, un decodificador BCD a 7 segmentos y un visualizador de 7 segmentos para mostrar el valor decimal de la palabra digital de salida resultante de cada conversión.

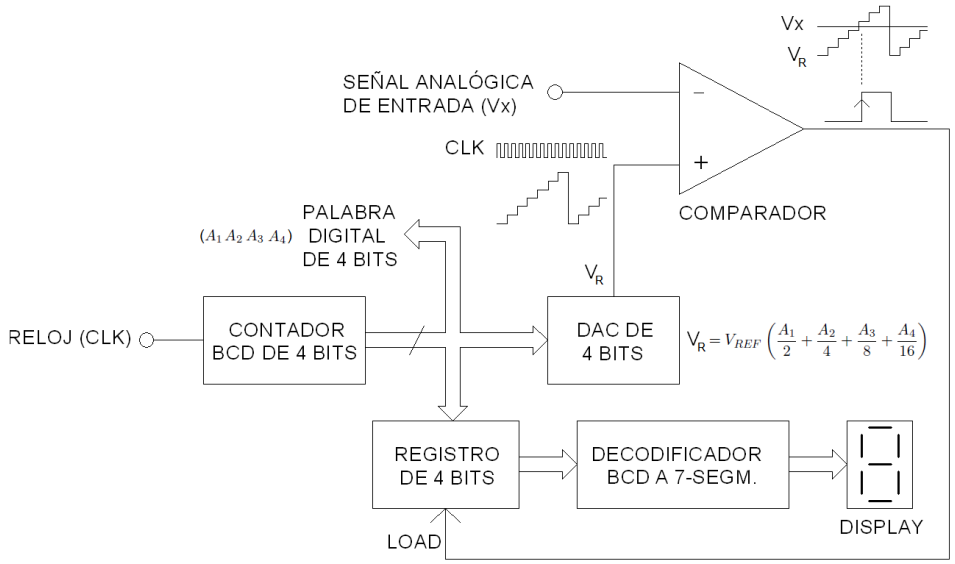

Figura 1.1. Diagrama de bloques de un CAD de 4 bits basado en el método contador-rampa.

1.3 Objetivos.

El objetivo de este Trabajo de Fin de Grado se ha centrado en el diseño y posterior implementación en placa de circuito impreso o PCB (*Printed Circuit Board*) de un conversor analógico-digital basado en el método contador-rampa a emplear como módulo didáctico en la realización de experiencias prácticas orientadas a que el estudiante se familiarice con la utilización de los analizadores lógicos para el análisis y comprobación del funcionamiento de los elementos o bloques digitales de un circuito electrónico digital. El diseño se basa en el CAD de cuatro bits propuesto en el guion de la práctica 2, denominada *El Analizador Lógico*, que se lleva a cabo en el módulo de Instrumentación Electrónica de la asignatura Técnicas Experimentales III, que se imparte en el tercer curso del Grado en Física de la Universidad de La Laguna [1].

En la Figura 1.2 se muestra el esquema general del conversor analógico-digital basado en el método contador-rampa que se ha diseñado e implementado en este trabajo. El conversor diseñado se puede utilizar como un CAD de 8 o de 4 bits, dependiendo del estado de la señal de control incluida para ese fin y que es accesible por el usuario, y que actúa sobre el bloque de multiplexores 2 a 1 que se encuentra a la entrada del conversor digital-analógico o CDA. Como se puede observar, la señal de entrada (V_X) se compara con una tensión analógica de referencia (V_R) que se genera a través de un contador binario y un CDA de 8 bits, siendo la palabra digital resultante de la conversión la salida del contador. El circuito también incorpora un contador BCD de dos dígitos de 4 bits cuya función es realizar una cuenta sincronizada con el contador binario de 8 bits, de tal forma que la palabra digital de salida del conversor analógico-digital también se encuentre disponible en formato BCD a la salida de dicho contador.

Al iniciar la conversión, los dos contadores se ponen a cero y sus salidas se van incrementando hasta que la tensión de salida (V_R) del CDA rebasa el valor de la tensión de entrada (V_X), situación que es detectada por el comparador. Una vez V_R ha rebasado a V_X, finaliza el proceso de conversión, siendo la palabra digital resultante de la conversión la salida de ambos contadores. El CAD emplea un registro de 8 bits, dos decodificadores BCD a 7 segmentos y dos visualizadores de 7 segmentos para capturar, almacenar y mostrar el valor decimal de la palabra digital de salida resultante de la conversión y que está disponible en código BCD a la salida del contador BCD de dos dígitos.

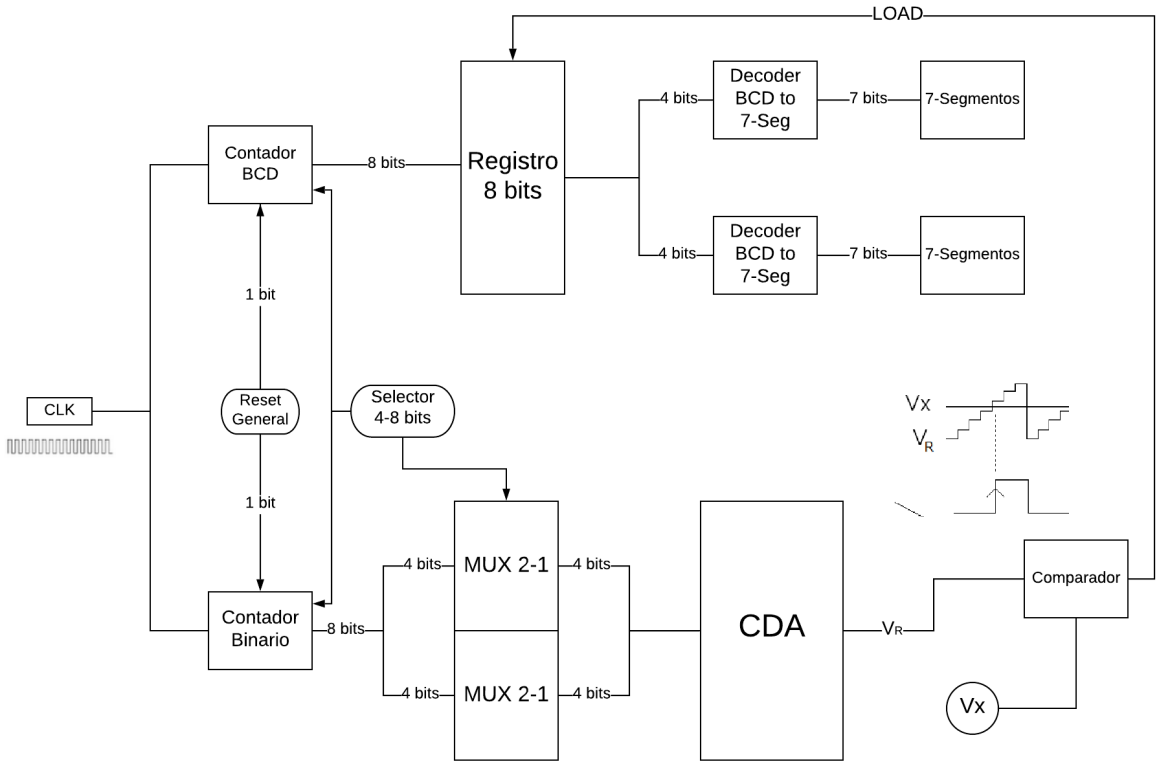

Figura 1.2. Esquema general del conversor analógico-digital de 8/4 bits basado en el método contador-rampa.

1.4 Estructura general del trabajo.

La memoria está dividida en 5 capítulos. El primero de ellos ofrece una breve introducción a este trabajo, los objetivos del mismo y la forma en que se estructura.

En el capítulo 2 se presenta el esquema electrónico y el diseño del sistema. Abordamos los dos modos de funcionamiento, para 4 y 8 bits, así como los componentes que van a formar parte de la placa. Este capítulo es el más extenso debido a que en él se explican cómo funcionan los diferentes componentes.

El capítulo 3 está dedicado a la elaboración de la placa de circuito impreso o PCB, la elección de las huellas para los componentes y su colocación siguiendo las reglas de diseño, así como del software empleado, el NewPCB.

Se concluirá el trabajo con el presupuesto, capítulo 4, y con la presentación en el capítulo 5 de los resultados y conclusiones, así como algunas propuestas de mejoras.

Capítulo 2: Diseño del sistema.

2.1 Introducción.

Como se comentó en el capítulo anterior, en este trabajo se ha llevado a cabo el diseño e implementación en PCB (*Printed Circuit Board*) de un conversor analógico-digital basado en el método contador-rampa a emplear como módulo didáctico en la realización de experiencias prácticas docentes.

En la Figura 2.1 se vuelve a mostrar el esquema general del conversor analógico-digital diseñado, el cual se puede utilizar como un CAD de 8 o de 4 bits de resolución, dependiendo del estado de la señal de control incluida para ese fin. Como se puede observar, la señal de entrada (V_X) se compara con una tensión analógica de referencia (V_R) generada mediante la utilización de un contador binario y un conversor digital-analógico o CDA de 8 bits, siendo la palabra digital resultante de la conversión la salida de dicho contador. El circuito incorpora un contador BCD de dos dígitos de 4 bits cuya función es realizar una cuenta sincronizada con el contador binario de 8 bits, de tal forma que la palabra digital de salida del CAD también se encuentra disponible en formato BCD.

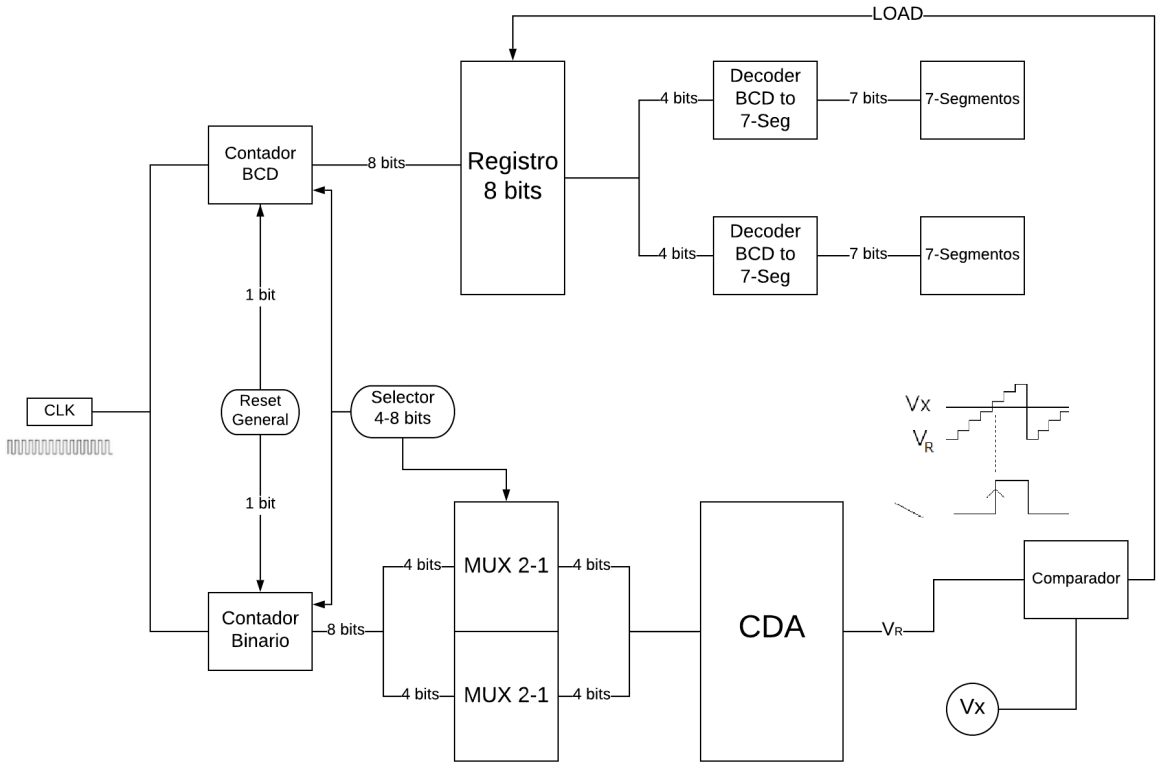

Figura 2.1. Esquema general del conversor analógico-digital de 8/4 bits diseñado.

Al iniciar la conversión, los dos contadores se ponen a cero y sus salidas se van incrementando hasta que la tensión de salida (V_R) del CDA supera el valor de la tensión de entrada a digitalizar (V_X), situación que es detectada por el comparador, el cual se encarga de indicar el final del proceso de conversión, siendo la palabra digital resultante la salida de ambos contadores. El CAD emplea un registro de 8 bits, dos decodificadores BCD a 7 segmentos y dos visualizadores de 7 segmentos para capturar, almacenar y mostrar el valor

decimal de la palabra digital de salida que en código BCD se encuentra disponible a la salida del contador BCD de dos dígitos.

En general, en el diagrama o esquema del conversor se pueden distinguir dos partes o ramas: la que emplea el contador binario de 8 bits para llevar a cabo la conversión analógica-digital propiamente dicha, y la que emplea el contador BCD de dos dígitos de 4 bits, cuya finalidad es la de permitir representar el valor resultante de la conversión en decimal. Tanto en el funcionamiento del CAD con 8 o 4 bits de resolución, ambas partes o ramas del conversor se sincronizan gracias a la señal de reloj general del sistema, la cual se muestra en la Figura 2.2.

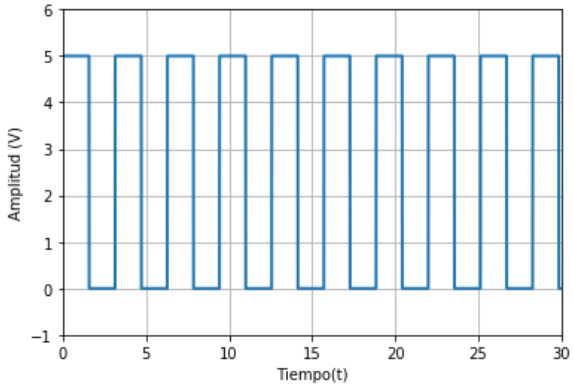

Figura 2.2. Señal de reloj del sistema (niveles TTL).

Cuando el conversor analógico-digital se utiliza con 8 bits de resolución, tanto el contador BCD de dos dígitos, como el contador binario de 8 bits, cuentan de manera sincronizada desde 0 hasta 99 de manera cíclica. Por el contrario, cuando se selecciona el funcionamiento con 4 bits, ambos contadores solo cuentan desde 0 hasta 9. Para permitir que el conversor pueda operar con 8 o 4 bits se ha incluido una señal de selección de 4-8 bits que actúa sobre ambos contadores y sobre la variable de selección de 8 multiplexores 2 a 1 (circuito integrado 74LS157), intercalados entre el contador binario y el conversor digital-analógico de 8 bits.

Dependiendo de la resolución seleccionada, 4 u 8 bits, ambos contadores deben contar desde 0 hasta 9 o 99, respectivamente. Para limitar la cuenta del contador binario hasta 9 o 99, ha sido necesario diseñar la lógica de puesta cero (*reset*) de dicho contador para limitar su cuenta hasta 9 o 99, en función de la resolución elegida.

A continuación, se describen las diferentes partes que componen el diagrama general del CAD diseñado.

2.2 Diseño electrónico: parte binaria.

La parte Binaria es la parte del circuito cuyos objetivos son los siguientes:

- Realizar una cuenta binaria desde 0 a 99, o desde 0 a 9, dependiendo de la resolución seleccionada, 8 o 4 bits, respectivamente. Se ha elegido que el máximo sea 99, ya que usaremos solamente dos visualizadores o *displays* de 7 segmentos.

- Convertir la señal digital procedente del contador binario en una señal analógica a través de un conversor digital-analógico o CDA.
- Por último, comparar la señal analógica de entrada (V_x) con la generada por el CDA (V_R), con la finalidad de indicar la finalización de la conversión, mediante la activación de una señal de LOAD a la rama o parte BCD.

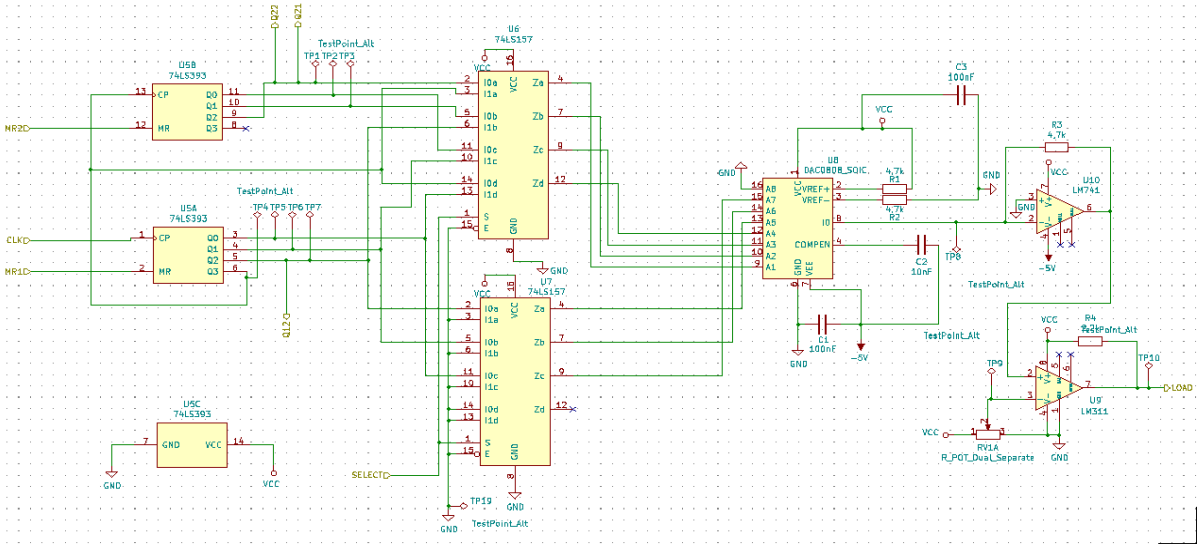

Figura 2.3. Visión general del esquema electrónico de la parte binaria.

En la Figura 2.3, se muestra una visión general del esquema electrónico de la parte binaria, en el cual se entrará en detalle en los próximos apartados. A continuación, se detalla el funcionamiento y conexionado de sus diferentes elementos

2.2.1 Contador Binario de 8 bits.

Para implementar el contador binario de 8 bits, que cuente desde 0 hasta 99, se ha utilizado el circuito integrado 74HCT393, que incluye dos contadores binarios de 4 bits cada uno. Los dos contadores se han conectado de tal manera que cada vez que el encargado de proporcionar los 4 bits menos significativos llegue a su cuenta máxima de 15 en decimal, el otro, encargado de proveer los 4 bits más significativos, sume uno al valor de su cuenta, tal y como se puede observar en la Figura 2.4.

0000 1111 (15) ⟶ 0001 0000 (16)

0001 1111 (31) ⟶ 0010 0000 (32)

Figura 2.4. Método de cuenta usado para contar desde 0 hasta 99.

En la Figura 2.5 se muestra el conexionado de los contadores, el U5A y U5B, que incorpora el circuito integrado 74HCT393. El U5A es el encargado de las “unidades”, es decir, de realizar la cuenta desde 0 hasta 15. Este contador posee cuatro salidas, que corresponden a los 4 bits menos significativos del número generado, y las siguientes dos entradas:

- La entrada CP es la entrada del reloj del contador. En este caso, se ha aplicado una señal de reloj de niveles TTL de frecuencia de 1 kHz. Esta señal es común al contador BCD.
- La entrada MR1, es un *Master Reset*, cuya función es la de poner a cero la salida del contador.

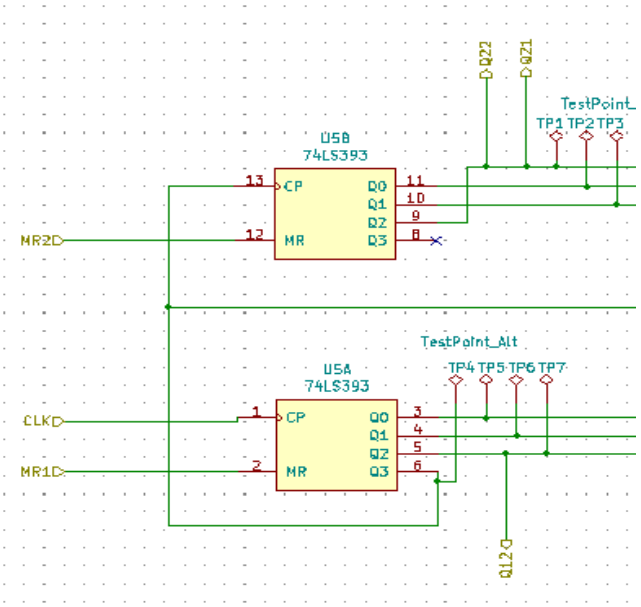

Figura 2.5. Montaje del circuito integrado 74CHT393.

En cuanto al segundo contador, el U5B, su funcionamiento es el de realizar las cuentas de las “decenas”, y presenta las mismas salidas y entradas que el U5A. En este caso, a su señal de reloj se conecta la salida Q3 del U5A, es decir, el bit más significativo de las “unidades”, de tal manera que cuando pase de 1 a 0, el contador U5B suma uno a su cuenta, tal y como se explicó en la Figura 2.4.

Las salidas Q2.2, Q2.1 y Q1.2 que se observan en el esquema, son herramientas del software, ya que se ha llevado a cabo un diseño jerárquico, sin embargo, tienen una utilidad que tiene que ver con la puesta a cero o reinicio de los contadores, que encontraremos más adelante, en el apartado 2.4.1. Estos tres bits serán utilizados para, con la lógica adecuada, detectar la combinación binaria 100 (01100100), para reiniciar en este momento ambos contadores binarios.

Como la cuenta máxima a realizar es desde 0 hasta el 99, el bit más significativo del contador U5B no se utiliza. Por último, indicar que se las salidas de ambos contadores son accesibles como puntos de test, de cara a la implementación en PCB.

2.2.2 Multiplexores 2 a 1

Para permitir que el conversor analógico-digital pueda operar con 8 o 4 bits, se han intercalado ocho multiplexores 2 a 1 entre el contador binario y el CDA. Como un circuito integrado 74LS157 incluye solo cuatro multiplexores, se han empleado dos. En las Figuras 2.6 y 2.7 se muestran los dos integrados, el U7 y U6, respectivamente. Los dos circuitos integrados se han conectado de tal manera que todos los multiplexores comparten la misma señal de selección *S*, que es la que permite elegir que el CAD opere con 8 o 4 bits de resolución.

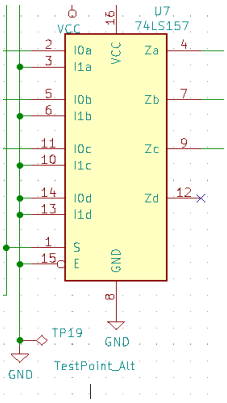

Figura 2.6. U7, selector LSB (74LS157)

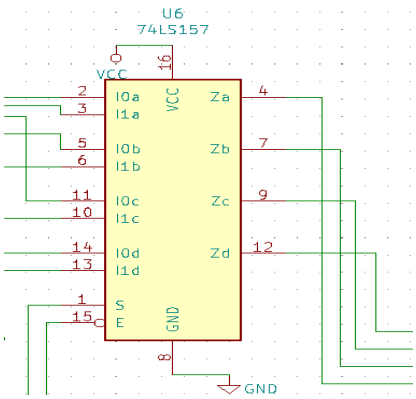

Figura 2.7. U6, selector MSB (74LS157)

Ambos circuitos integrados, el U7 y el U6, se encargan de suministrarle al CDA los cuatro bits menos significativos y más significativos, respectivamente. En cada multiplexor, Z_a representa el valor más significativo y Z_d el menos significativo. Como se indicó con anterioridad, S es la variable de selección, la cual permite elegir que a cada una de las salidas del multiplexor se encamine la entrada I0 (si S = 0), o I1 (si S = 1). Dependiendo de si el valor de *S* es un 0 o un 1 lógico, el conversor analógico-digital operará con una resolución de 8 o 4 bits, respectivamente.

En el esquema electrónico representado en la Figura 2.3 se puede apreciar el conexionado de los multiplexores. Si se selecciona S = 0 (funcionamiento con 8 bits), los multiplexores conectan las salidas de los dos contadores binarios U5A y U5B, directamente con las entradas del CDA. En cambio, si se selecciona S = 1 (4 bits), los multiplexores se encargan de conectar las cuatro salidas menos significativas del contador binario (salidas del U5A) con las cuatro entradas más significativas del CDA, poniendo el resto de las entradas del CDA a cero.

En la Tabla 2.1 se muestra cómo se conectan los terminales de salida del contador binario (integrado 74LS393) con las entradas de los multiplexores. También se indican cuáles de dichas entradas se ponen a cero, para permitir el funcionamiento del CAD con 4 bits de resolución. Las salidas de los multiplexores se conectan al CDA teniendo en cuenta que los terminales de entrada A1 y A8, corresponden al bit más y menos significativo respectivamente.

		Pines del Contador Binario	
		4bit (I1n)	**8bit (I0n)**
U6	**a**	6	9
	b	5	10
	c	4	11
	d	3	6
U7	**a**	GND	5
	b	GND	4
	c	GND	3
	d	GND	GND
Selector		1	0

Tabla 2.1. Distribución de los pines del contador 74LS393 en los selectores

2.2.3 Conversor de señal digital a analógica.

Para implementar el conversor digital-analógico (CDA) se ha empleado el circuito integrado DAC0808. Su función es la de generar la tensión analógica de referencia ($V_{DAC} = V_R$), que se compara con la señal analógica de entrada a digitalizar (V_X).

En este trabajo se ha optado por utilizar la configuración proporcionada por el fabricante que se muestra en la Figura 2.8. Como se puede observar, además del circuito integrado DAC0808, se ha utilizado el amplificador operacional µA741 para realizar la conversión corriente a tensión que permite obtener la señal analógica de referencia en forma de tensión. En esta misma figura se muestra el integrado LM311, cuya función es la de comparar la señal a digitalizar (V_X) con la de referencia (V_{DAC} o V_R). La salida del comparador se utiliza para indicar el instante en el que se debe capturar la palabra digital de salida del contador BCD, que corresponde al resultado de la digitalización. Para poder seleccionar diferentes valores de tensión de entrada se ha añadido un potenciómetro que permite fijar un valor de entrada desde 0V hasta 5V, aunque el rango de entrada del CAD diseñado abarca desde 0V hasta 3,86V o desde 0V hasta 2,81V, cuando se usa como un conversor de 8 o 4 bits, respectivamente, tal y como se verá a continuación.

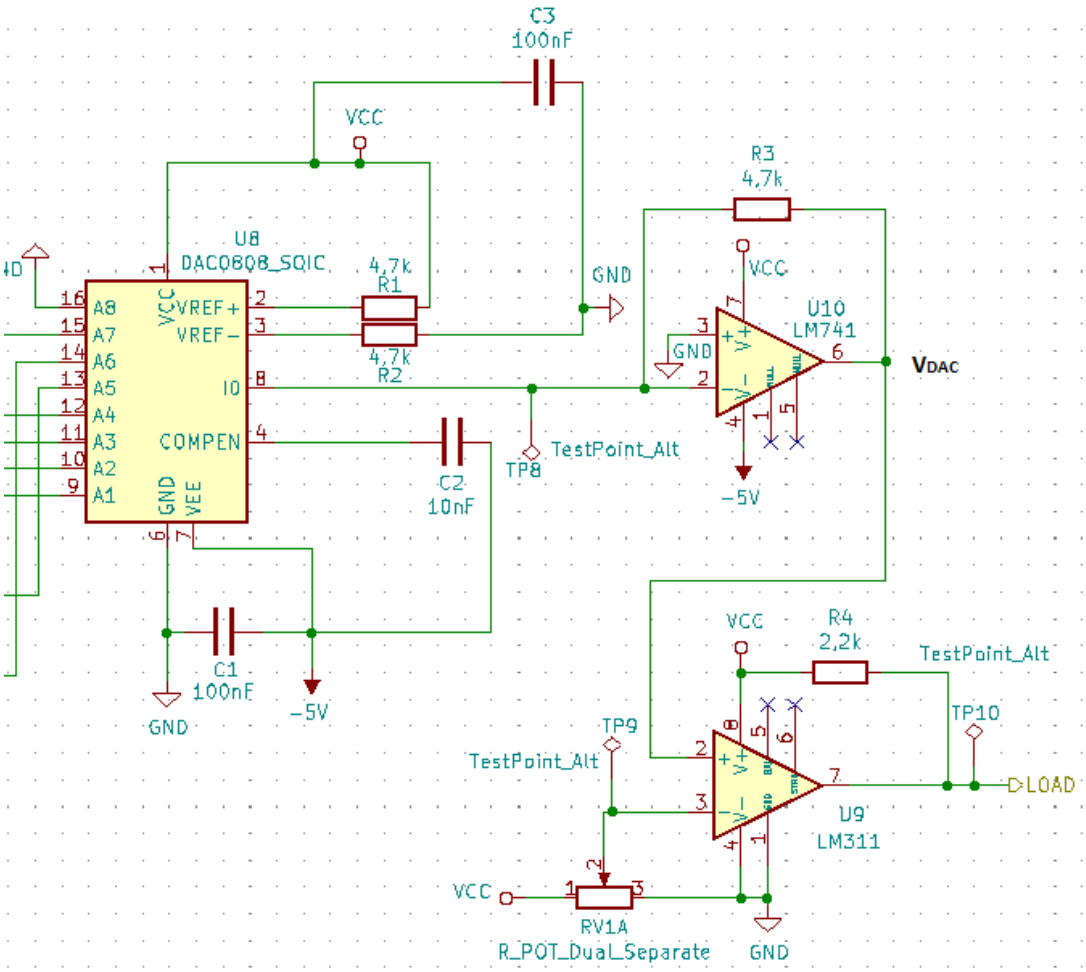

Figura 2.8. Configuración del DAC0808 y operacionales LM741 y LM311.

Según las hojas de características aportadas por el fabricante del DAC0808, la tensión de salida V_{DAC} del conjunto DAC0808 actuando conjuntamente con el amplificador operacional µA741 viene dada por:

$$V_{dac} = V_{ref} \sum_{i=1}^{8} * \frac{Ai}{2^i} = V_{ref} \left(\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256}\right) \quad (2.1)$$

Donde V_{ref} = 5V, y A_i representa el valor lógico de cada una de las entradas del conversor, siendo A_1 y A_8 la entrada más y menos significativa, respectivamente.

Cuando el conversor se utiliza como un CAD de 8 bits, los contadores realizan una cuenta desde 0 hasta 99 (01100011). Como el bit más significativo del contador binario nunca es un 1 lógico, el terminal de entrada A_8 del DAC0808 se ha puesto a cero, puesto que se ha buscado que el CAD diseñado tenga el mayor margen de entrada posible. Para esta situación, el margen de variación de V_{DAC} comprende desde 0V hasta 3,86V (ecuación 2.2), que en un CAD basado en el método contador-rampa es lo que fija el margen de entrada del conversor. En este caso, la resolución en voltaje del CAD, que corresponde al salto de tensión debido al bit menos significativo (A_7), es de 5V/128 = 39mV.

$$V_{DAC} = V_{ref} \sum_{i=1}^{8} * \frac{Ai}{2^i} = 5V \left(\frac{1}{2} + \frac{1}{4} + \frac{0}{8} + \frac{0}{16} + \frac{0}{32} + \frac{1}{64} + \frac{1}{128}\right) = 3{,}86V \quad (2.2)$$

Cuando el conversor se utiliza como un CAD de 4 bits, los contadores realizan una cuenta desde 0 hasta 9 (1001). En este caso, y también con la intención de conseguir el mayor margen de variación posible para V_{DAC} o V_R, los multiplexores 2 a 1 se encargan de encaminar los 4 bits menos significativos del contador BCD (los 4 bits correspondientes al contador de las "unidades"), hacia los 4 terminales de entrada del DAC0808 más significativos, aplicándole a las restantes entradas del conversor un 0 lógico. Para esta situación, el margen de variación de V_{DAC} va desde 0V hasta 2,81V (ecuación 2.3), siendo la resolución en voltaje de 5V/16 = 0,31V.

$$V_{DAC} = V_{ref} \sum_{i=1}^{8} * \frac{Ai}{2^i} = 5V \left(\frac{1}{2} + \frac{0}{4} + \frac{0}{8} + \frac{1}{16}\right) = 2{,}81V \quad (2.3)$$

2.3 Diseño electrónico: parte BCD

La parte o rama BCD es la parte del circuito cuyos objetivos son los siguientes:

- Realizar una cuenta en código BCD desde 0 hasta 99, o desde 0 hasta 9, dependiendo de la resolución seleccionada, 8 o 4 bits, respectivamente.
- Tras recibir la señal del comparador, capturar, almacenar y mostrar el valor decimal de la palabra digital de salida resultante de la conversión en dos visualizadores de 7 segmentos.

En la Figura 2.9 se muestra el esquema electrónico de la rama o parte que trabaja con datos binarios codificados en BCD. A continuación, se describen cada uno de los elementos que se muestran en el mismo.

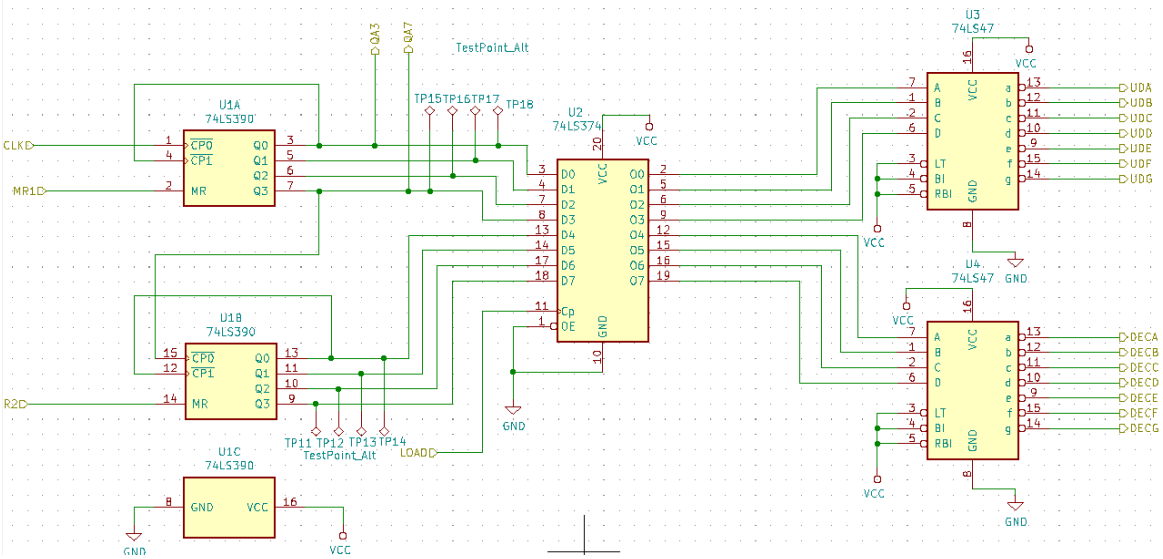

Figura 2.9. Esquema electrónico de la rama o parte BCD.

2.3.1 Contador BCD

Para implementar un contador BCD de dos dígitos se ha hecho uso del circuito integrado 74HCT390, que incluye dos contadores de 4 bits cada uno, que se pueden configurar para que cuenten en formato BCD. En la Figura 2.10 se muestra la forma de conectar ambos contadores, el UA1, que se encarga de la cuenta de las unidades y el U1B, que se encarga de las decenas. Para conseguir que ambos contadores cuenten de manera conjunta desde 0 hasta 99, basta con aprovechar el flanco de bajada que se produce en el bit más significativo de salida (Q_3) de U1A, cuando la cuenta pasa de 9 a 0 en decimal, como señal de reloj del contador U1B. Por otro lado, según las especificaciones del fabricante, para que cada contador cuente en formato BCD, hay que conectar su salida Q_0 con la entrada CP1 e introducir la señal de reloj del sistema a través de la entrada CP0 (tabla 2.2).

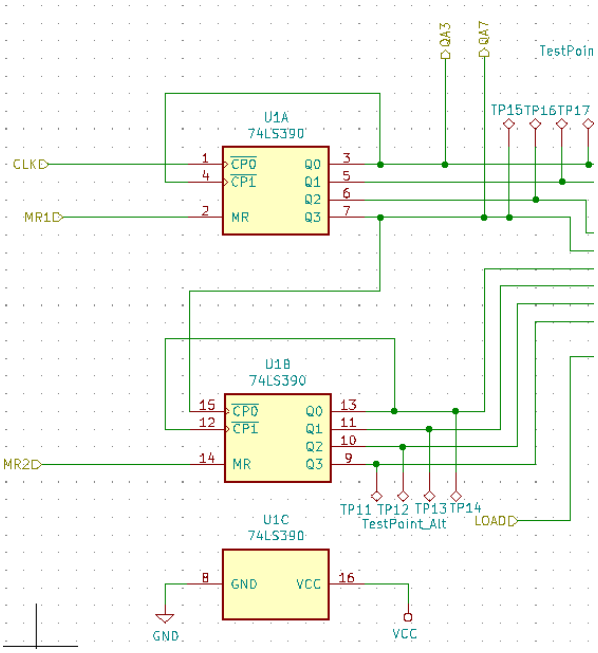

Figura 2.10. Configuración Contadores BCD (74LS390)

Los contadores BCD disponen de una señal de *Master-Reset,* que funcionan de la misma manera que las del contador binario, es decir, al introducir un 1 lógico, dichos contadores mantendrán su salida a cero, lo cual se ha utilizado para manejar los reinicios o puesta a cero del circuito, de los cual se hablará más adelante. Por último, indicar que las salidas de ambos contadores son accesibles como puntos de test, de cara a su implementación en PCB.

BCD COUNT SEQUENCE FOR 1/2 THE 390

COUNT	OUTPUTS			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Output nQ0 connected to n$\overline{CP1}$ with counter input on n$\overline{CP0}$.

B-QUINARY COUNT SEQUENCE FOR 1/2 THE 390

COUNT	OUTPUTS			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	H	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

Output nQ3 connected to n$\overline{CP0}$ with counter input on n$\overline{CP1}$.

Tabla 2.2. Configuración del 74LS390 en BCD y *B-Quinary.*

2.3.2 Registro de 8 bits.

Una vez que la tensión de referencia generada por el CDA rebasa el valor de la tensión de entrada, situación que es detectada e indicada por el comparador (integrado LM311), finaliza el proceso de conversión, siendo la palabra digital resultante de la conversión, la salida de ambos contadores. Es justo en ese momento cuando el registro de 8 bits, tras la indicación del comparador, debe capturar y almacenar la salida del contador BCD, para su posterior representación o visualización.

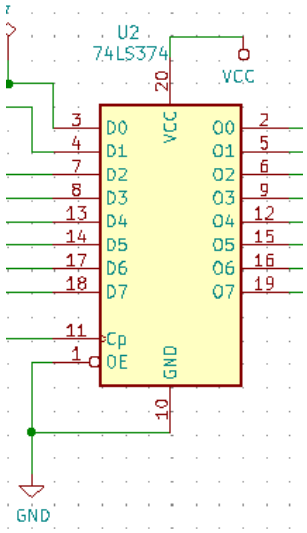

Figura 2.11. Configuración del registro de 8 bits (74LS374).

Para implementar el registro de 8 bits se ha hecho uso del circuito integrado 74LS374 (Figura 2.11). Se trata de un integrado que consta de ocho biestables tipo D, capaces de almacenar y mostrar en sus ocho salidas (O7, O6, …, O0) los valores lógicos de los 8 bits aplicados a sus entradas (D7, D6, …, D0), justo en el momento en el que la señal CP se produzca una transición de baja a alta (tabla 2.3). En definitiva, cuando se produzca un flanco de subida en CP, el valor de lo que haya en cada entrada DX es capturado y mostrado en la salida correspondiente, OX. Este registro capturará la salida de los dos contadores BCD,

independientemente de que el conversor se utilice como un CAD de 8 o 4 bits. En el caso de 4 bits, los cuatro bits más significativos correspondientes al dígito de las decenas son cero.

Function	Inputs			Outputs	Internal
	$\overline{OE}$	CP	Dx	Qx	$\overline{Qx}$
High-Z	H	L	X	Z	NC
	H	H	X	Z	NC
Load Register	L	↑	L	L	H
	L	↑	H	H	L
	H	↑	L	Z	H
	H	↑	H	Z	L

Tabla 2.3. Relación entradas/salidas del 74LS374

2.3.3 Decodificadores BCD a 7 segmentos y visualizadores de 7 segmentos.

La función de los dos decodificadores BCD a 7 segmentos y de los dos visualizadores de 7 segmentos es la de mostrar el valor decimal de la palabra digital de salida resultante de la conversión y que está disponible en código BCD a la salida del registro. Un decodificador y visualizador se usan para los 4 bits que representan las decenas, y el otro decodificador y visualizador para los 4 bits de las unidades.

En la Figura 2.12 se muestran los dos decodificadores BCD a 7 segmentos configurados según las especificaciones proporcionadas por el fabricante. En este trabajo se ha optado por utilizar visualizadores o *displays* de 7 segmentos de ánodo común, lo que justifica la utilización de los circuitos integrados 74LS47, diseñados para trabajar con este tipo de visualizadores.

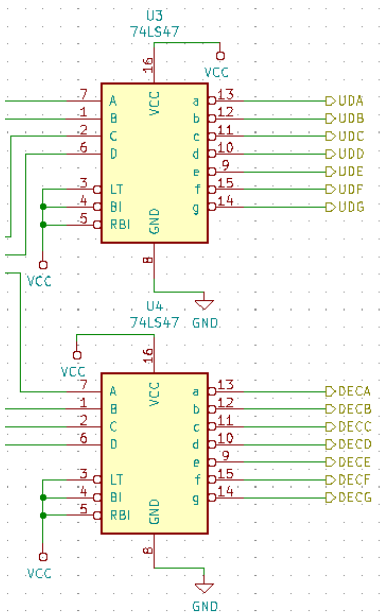

Figura 2.12. Decodificadores BCD a 7 Segmentos (74LS47).

En la Figura 2.13 se observa el esquema electrónico de los dos visualizadores de 7 segmentos junto al módulo BCD. Este tipo de visualizadores se basa en la utilización de siete diodos LED cuyos ánodos están conectados entre sí, constituyendo los cátodos los terminales de entrada del visualizador. Si se conectan los ánodos a una tensión de 5V, cada diodo LED

se iluminará cuando en su cátodo se aplique como entrada un nivel bajo, es decir, un cero lógico.

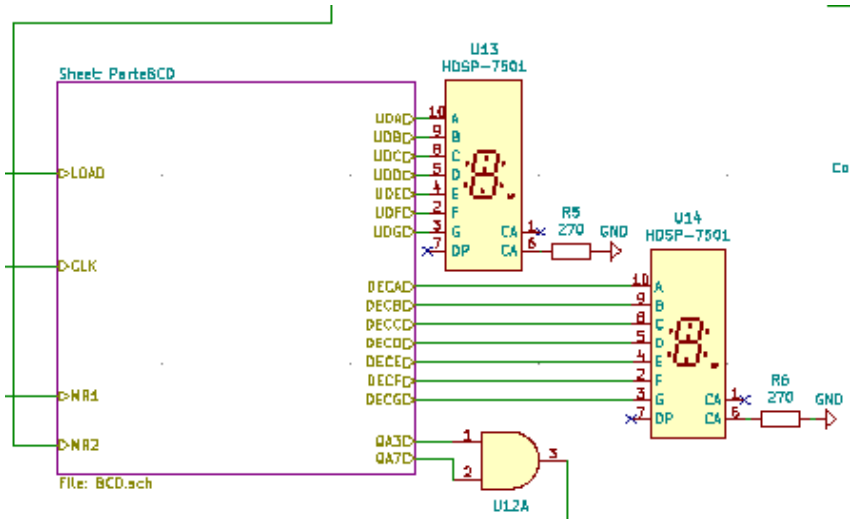

Figura 2.13. Visualizadores o *displays* junto al módulo BCD.

2.4 Diseño electrónico general.

En la Figura 2.14 se muestra el esquema electrónico general del circuito diseñado, donde los dos rectángulos representan, dentro del diseño jerárquico, la parte BCD y binaria. El que se encuentra en la parte inferior izquierda corresponde a la parte BCD, ya que tiene los dos *displays* conectados a él, siendo el de la parte superior derecha el que alberga la parte binaria.

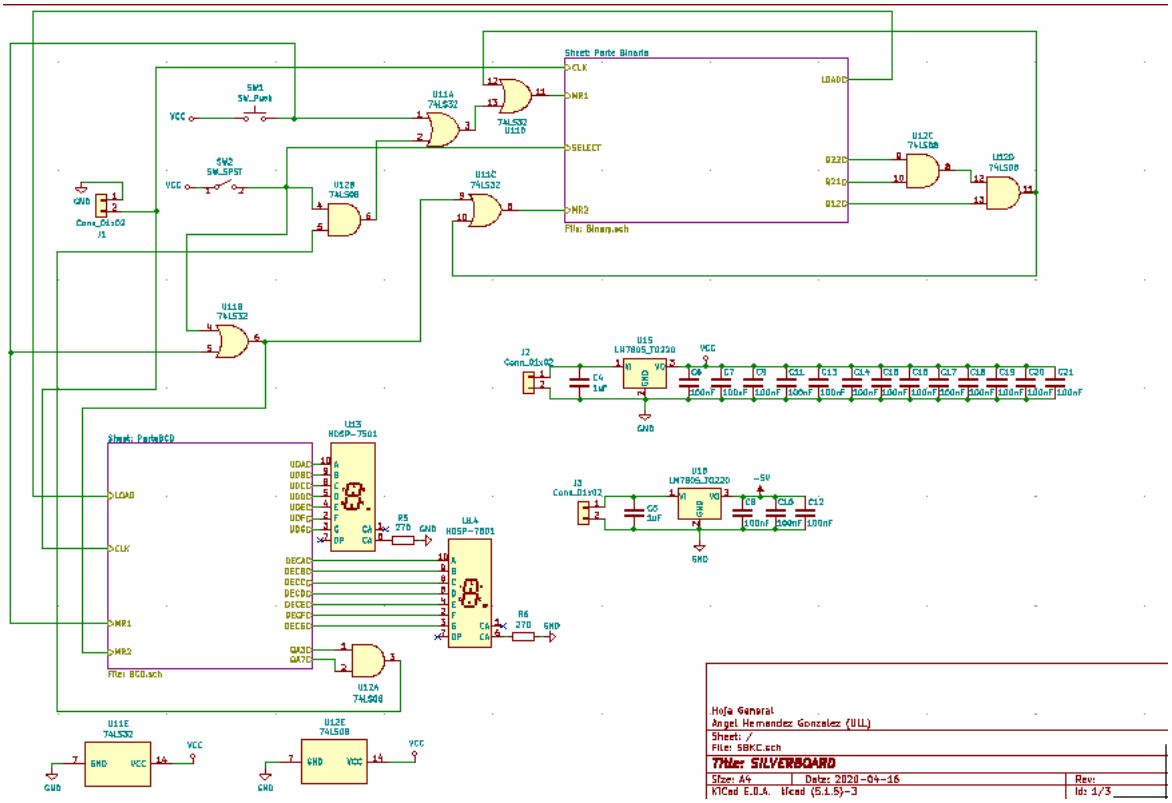

Figura 2.14. Esquema electrónico general.

La señal de reloj del sistema se deberá aplicar de manera externa mediante la utilización de un generador de señales. Para ello, en el diseño se ha incorporado un conector que permite aplicar señal de salida del generador mediante cables tipo banana-cocodrilo, por ejemplo (Figura 2.15).

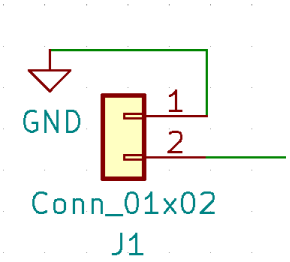

Figura 2.15. Esquema de un conector.

Otra conexión que se necesita desde el exterior de la placa es la alimentación de +5V y -5V, necesaria para alimentar los integrados (Figura 2.16). En este caso, se han usado conectores del mismo tipo que el indicado con anterioridad, que mediante la utilización de reguladores de tensión LM7805 y LM7905, permite alimentar el circuito con +5V y -5V respectivamente.

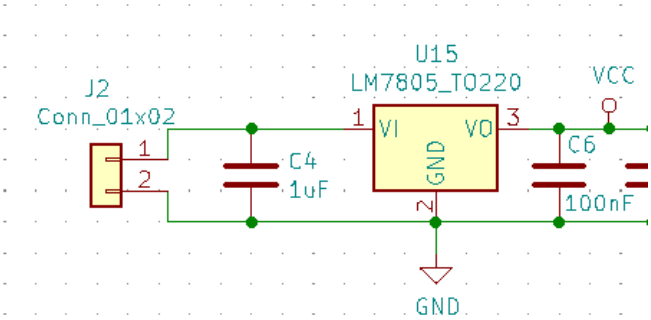

Figura 2.16. Regulador de tensión +5V.

También se ha tenido en cuenta la inclusión de condensadores de desacoplo. Este tipo de condensadores son indispensables en las placas PCB. Los condensadores de desacoplo se encargan de proteger a los circuitos integrados de ruidos eléctricos de alta frecuencia, derivándolos a tierra. Estos condensadores pueden encontrarse por cualquier lugar de la placa, pero preferiblemente se deben situar lo más cerca posible de los circuitos integrados (se verá en el apartado 3.3), así que cada integrado tendrá un condensador de desacoplo asociado. Otra cosa a tener en cuenta, es que también hay que incluir un condensador de desacoplo por cada voltaje, es decir, en nuestro caso, habrá condensadores de desacoplo para la línea de +5V y la de -5V. El CDA y el LM741 son los únicos integrados que tendrán dos condensadores de desacoplo, ya que ambos se alimentan con +5V y -5V. En definitiva, se han utilizado 12 condensadores para la línea de +5V y 2 para la de -5V, todos ellos de 100nF, como se puede observar en la Figura 2.17.

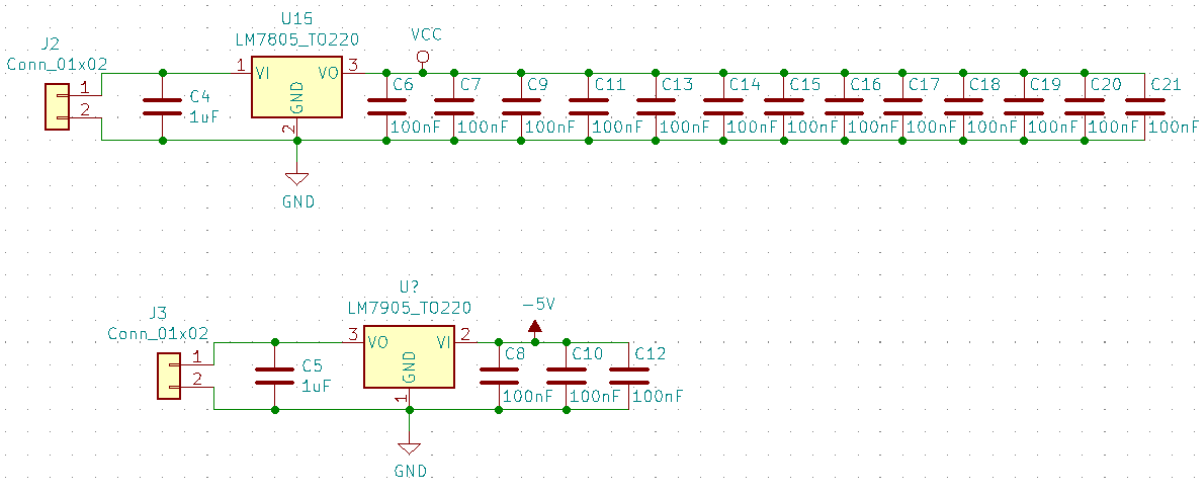

Figura 2.17. Reguladores +5V y -5V con sus correspondientes condensadores de desacoplo.

También se han incluido dos interruptores, un *switch* y un pulsador (Figura 2.18). El pulsador se ha usado como mando de control para activar la puesta a cero o reset general. Al pulsarlo, todos los contadores se inicializarán poniendo sus salidas a cero. El *switch* está asociado con la selección del modo de operación del CAD en cuanto al número de bits a emplear. Cuando el *switch* está abierto, el conversor actuará como un CAD de 8 bits, actuando como un CAD de 4 bits, cuando el *switch* está cerrado.

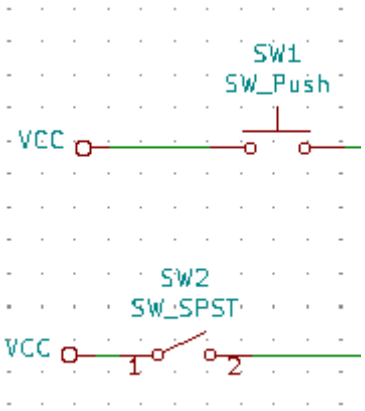

Figura 2.18. Interruptor y pulsador utilizados.

2.4.1 Lógica de reinicio de los contadores.

En este apartado se describe la lógica necesaria para reiniciar o poner a cero los contadores. En primer lugar, vamos a comprobar cuáles son las condiciones de puesta a cero que necesitan los cuatro contadores:

- Contador menos significativo o de las unidades de la parte BCD.

  Este contador se encarga de contar desde el 0 hasta el 9, y sólo requiere de la puesta a cero cuando se active el pulsador del *reset* general del sistema.

- Contador más significativo o de las decenas de la parte BCD:

  Este contador se encarga de contar las decenas de la palabra digital en BCD, pero básicamente lo que hace es contar de 0 hasta 9 e incrementar la cuenta cada vez que el contador de las unidades llega hasta 9. Este contador se deberá resetear cuando se active el reset general del sistema o cuando se esté en el modo de operación de 4 bits, es decir, cuando el interruptor o *switch* esté cerrado, dejando pasar un 1 lógico. Por ese motivo, se ha usado una puerta lógica OR de dos entradas (U11B de la Figura 2.14) cuyas entradas son el reset del sistema y el *switch*, para controlar la puesta a cero de este contador.

- Contador de los 4 bits menos significativos de la parte binaria:

  En este caso la situación es un poco más complicada debido a que los contadores binarios no se detienen de forma natural ni en el 9 ni en el 99. Por tanto, estos contadores presentan más condiciones de puesta a cero o *reset*. Este contador se deberá resetear cuando se pulse la señal de *reset* del circuito, y el resto de condiciones dependerán del modo de operación del CAD. Cuando estemos en el modo de 4 bits, necesitaremos que este contador se ponga a cero cuando llegue a 9. Para ello, se han usado dos puertas AND de dos entradas (U12A y U12B de la Figura 2.14) conectadas en cascada, que proporcionarán un 1 lógico cuando se dé el número 10 en el contador binario y además se esté en el modo de 4 bits. Como el 10 en binario es 1010, las entradas de dichas puertas AND serán los bits Q3 y Q1 del contador binario menos significativo y el *switch*. Cuando estemos en el modo de 8 bits, cuando la salida de los 8 bits del contador binario llegue a 99, también será necesario poner a cero ambos contadores binarios. Por este motivo se han incluido dos puertas OR de dos entradas (U11A y U11D de la Figura 2.14) cuyas entradas son la salida de las dos puertas AND anteriormente mencionadas, la señal de reset general y la de puesta a cero de ambos contadores cuando la cuenta conjunta de ambos contadores haya llegado a 99.

- Contador de los 4 bits más significativos de la parte binaria:

  Este último contador también se deberá resetear cuando se active el reset general del sistema o cuando se esté en el modo de operación de 4 bits, es decir, cuando el interruptor o *switch* esté cerrado. La detección de una u otra condición ya ha sido implementada a través de la puerta OR de dos entradas U11B, cuya salida se podría utilizar también para resetear este contador. Ahora bien, esta no es su única condición de *reset*, puesto que este contador también se tiene que poner a cero cuando la cuenta conjunta de ambos contadores binarios haya llegado a 99, es decir, cuando aparezca el 100, que en binario es el 1100100. Para ello, se ha utilizado dos puertas AND (U12C y U12D de la Figura 2.14) de dos entradas conectadas en cascada, cuyas entradas son los bits 7, 6 y 3 de la palabra digital de 8 bits. Para terminar de construir el circuito de control de puesta a cero de este contador, se necesita

emplear una puerta OR de dos entradas (U11C de la Figura 2.14) que permita unir las dos condiciones mencionadas (salidas de U11B y U11C).

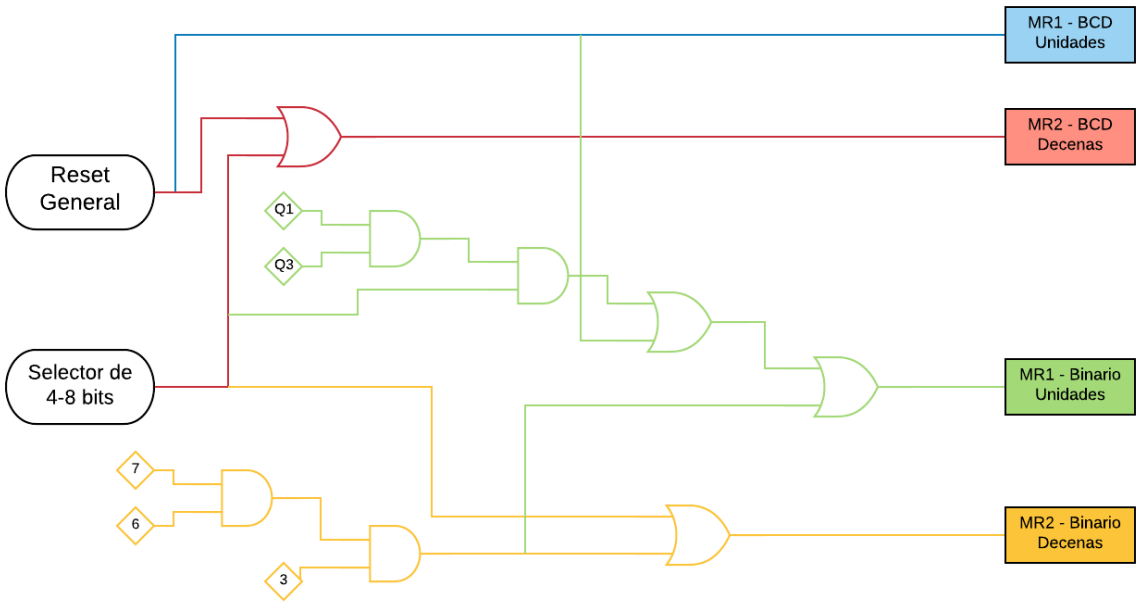

Figura 2.19. Esquema de puesta a cero o de *reset* de los contadores.

En la Figura 2.19 se muestra el circuito de puesta a cero de todos los contadores. Como se puede observar se han empleado cuatro puertas OR y cuatro puertas AND de dos entradas, que se han implementado con ayuda de los integrados 74LS08 y el 74LS32, que incluyen 4 puertas AND y 4 puertas OR de dos entradas, respectivamente.

2.5 Software KiCad.

Para crear la PCB (*Printed Circuito Board*) del circuito electrónico diseñado se hace uso del software KiCAD, cuyo logotipo se muestra en la Figura 2.20.

Figura 2.20. Logotipo del software KiCad.

KiCad es un entorno EDA (*Electronic Design Automation*) o paquete de software libre, creado en 1992 por Jean-Pierre Charras y enfocado a la automatización de diseño de circuitos electrónicos. KiCad es muy flexible y adaptable, permite la edición de esquemas electrónicos y el diseño de circuitos impresos modernos de forma sencilla e intuitiva. Por otro lado, los circuitos se pueden diseñar con múltiples capas y ser visualizados en 3D [6]. KiCad como software libre, es un software gratuito que crece gracias a las aportaciones de diferentes personas, las cuales tienen el derecho para ejecutar, copiar, distribuir, estudiar, cambiar y mejorar el software.

Este software presenta las siguientes herramientas de trabajo:

- Kicad: administrador de proyectos.
- Eeschema: Permite la captura y edición del esquema del circuito que se va a realizar y en el que se definirán las conexiones entre los diversos componentes. Se trata de un entorno gráfico fácil de entender, que ha permitido crear un diseño en bloques con diferentes jerarquías, como los realizados para los módulos Binario y BCD de este proyecto. También, permite crear y editar gran número de símbolos o componentes personalizados, así como, la asignación de sus huellas, etc.
- Cvpcb: Permite la asignación de huellas o *footprints* de los encapsulados a los componentes o símbolos utilizados en el esquema electrónico.
- Pcbnew: Es el entorno de diseño para la creación de los circuitos impresos o PCBs. Una vez generada, con Eeschema, la lista de conexiones o *Netlist,* existente entre los diferentes componentes que forman parte del esquema electrónico, se emplea esta herramienta para establecer la posición y orientación de cada componente en la placa, así como su trazado de pistas.
- Gerbview: Visualizador de los ficheros Gerber, útiles para la fabricación automatizada de las placas de circuito impreso.

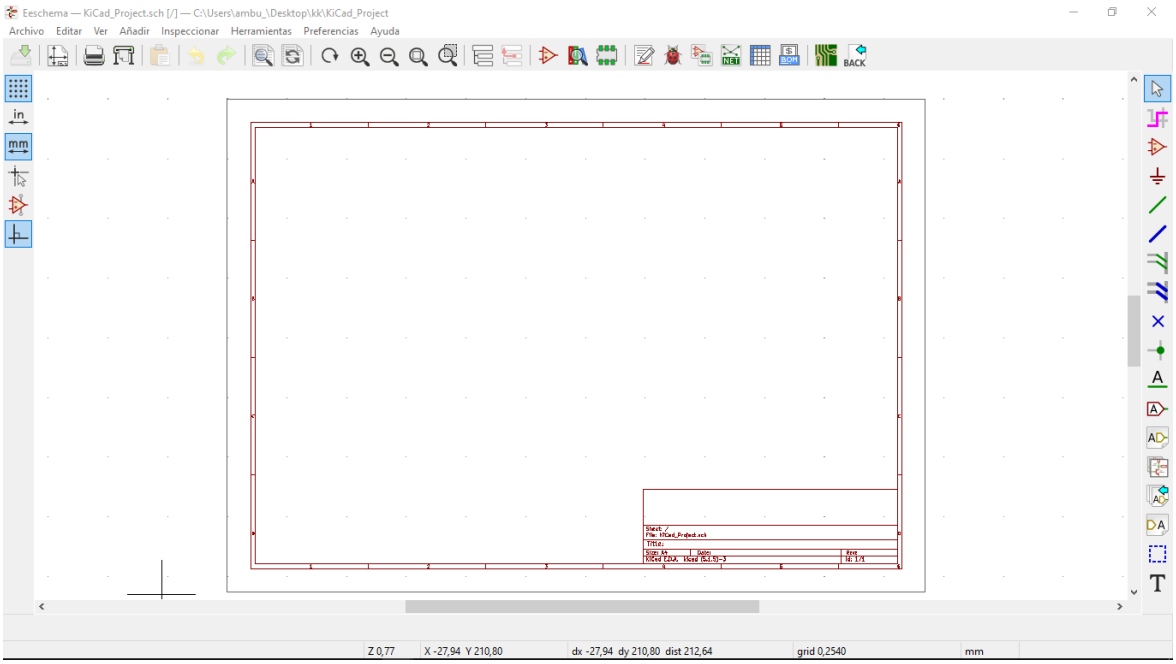

Figura 2.21. Ventana de trabajo principal del EESCHEMA.

Las herramientas más importantes del entorno gráfico son EESCHEMA (Figura 2.21) y PCBnew (Figura 3.5). Por otro lado, en concreto para este proyecto, se ha hecho uso de la amplia librería de componentes incorporada en EESCHEMA, por lo que no ha sido necesario emplear la herramienta de creación de nuevos componentes o *Symbol Library Editor.*

El flujo de trabajo con EESCHEMA ha sido el siguiente, una vez seleccionados cada uno de los componentes que forman parte del circuito, asignado las huellas de los encapsulados de estos componentes, creado los bloques de jerarquía y definido todas las conexiones entre ellos y el resto de los componentes, se procede a ejecutar las herramientas

finales de este proceso, como son: Annotate, que permite asignar referencias a todos los componentes, minimizando el número de encapsulados empleados, ERC, o Chequeo de las Reglas de Diseño (*Electrical Rules Check*) que permite detectar los errores cometidos durante la realización del esquema según una tabla de conexionado previamente configurada, BOM o lista de materiales (*Bill of material*) permite obtener una lista de todos los componentes empleados y finalmente Netlist o lista de todos los componentes con las conexiones que existen entre ellos. Los ficheros resultantes de este post-proceso, son los siguientes:

- ERC (Control de reglas eléctricas): realizar este procedimiento permite ver los errores cometidos durante la realización del esquema.

- BOM (Lista de materiales): genera un archivo con una lista de todos los componentes del circuito. Incluye información sobre su referencia, generada en el *annotate*, sobre su valor, su huella y una pequeña descripción.

- *Netlist* (Lista de redes): se encarga de generar un archivo con una lista que comprende todos los componentes y las conexiones de los mismos. Tiene como objetivo transferir esta información al programa de creación de PCB. Si por algún motivo debemos cambiar algo del esquema, se debe crear un nuevo *netlist* y pasarlo al programa de creación de PCB de nuevo.

Estos archivos generados, así como, el listado de las Huellas de los encapsulados de los componentes empleados, se adjuntan en el Anexo I: archivos EESCHEMA, del presente proyecto.

Capítulo 3: Diseño de la placa de circuito impreso.

En este capítulo se describirá el diseño de la placa de circuito impreso o PCB del circuito electrónico descrito en el Capítulo 2. Como se comentó en dicho capítulo, una parte del proceso en EESCHEMA consistió en seleccionar las huellas de los componentes. Por definición, una huella o *footprint* es la impresión del encapsulado del componente, y está formada por un dibujo del contorno, texto y un conjunto de *pads* necesarios para conectar todos los terminales del componente con las pistas de cobre del circuito impreso. La Figura 3.1 muestra la ventana de la herramienta, anteriormente descrita Cvpcb, para la asignación de huellas a los componentes.

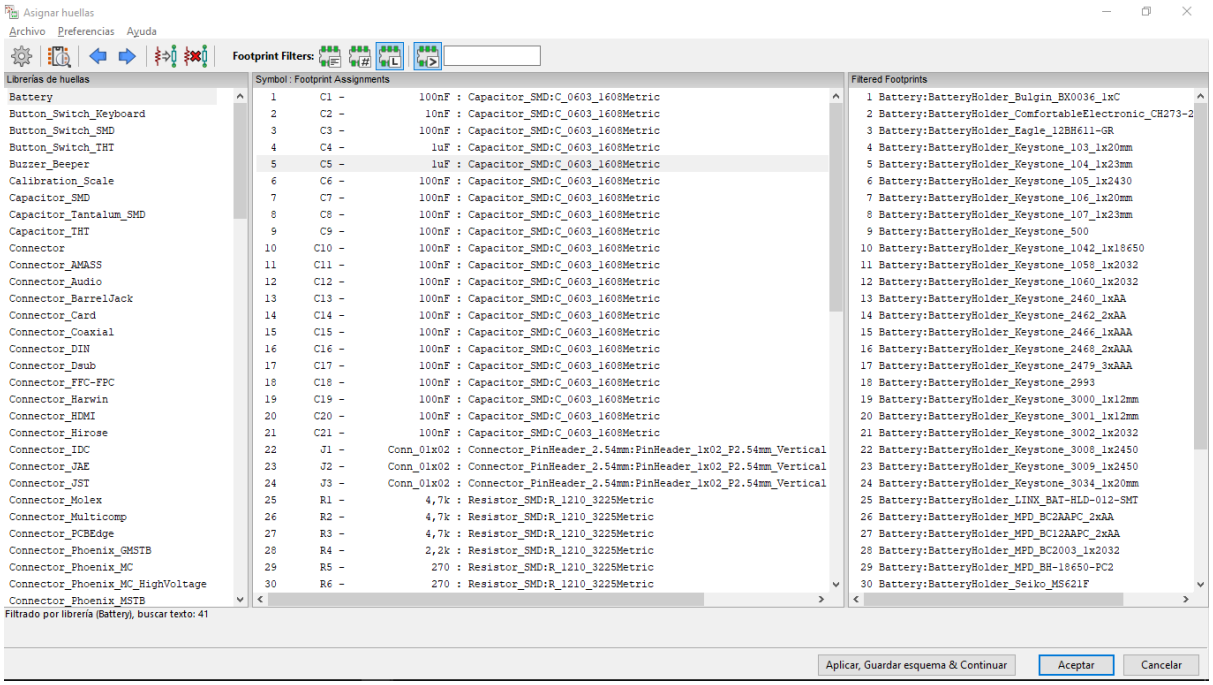

Figura 3.1. Ventana Cvpcb de selección de huellas.

Este procedimiento es importante, ya que dependiendo de las huellas que se elijan, la placa tendrá diferentes características. En nuestro caso, se ha decidido implementar una placa con configuración Tipo1C, esto es, montaje de componentes en una sola cara de la placa y componentes basados en tecnología SMD (*Surface Mounted Device*), cuyos encapsulados de pequeño tamaño son soldados sobre la propia superficie de la PCB en la que son colocados y en THD (*Through-Hole Device*) cuyos pines atraviesan la placa. En concreto, para este proyecto, se ha reservado la tecnología THD únicamente para los conectores de entrada y salida. Esta decisión se ha llevado a cabo debido a que se desea tener una placa accesible y fácil de manejar, que no requiera costes muy elevados de montaje y que permita a los estudiantes realizar la práctica sin demasiada complicación. También se ha tenido en cuenta la disponibilidad de las librerías que presenta el KiCad, teniendo un amplio rango de selección para casi todos los componentes de la placa. La lista de huellas utilizadas para nuestros componentes se encuentra en el Anexo II: Lista de huellas de componentes.

En cuanto a los circuitos integrados, se ha buscado en sus hojas de datos los diferentes encapsulados en los que se suministran. Por ejemplo, los multiplexores 2 a 1, se

pueden adquirir en diferentes encapsulados. Entre ellos están los encapsulados SMD tipo SOIC (*Small Outline Integrated Circuit*) o SOP (*Small Outline Package*), de la Figura 3.2,-muy utilizados para la automatización de procesos de montajes de PCBs, ya que la forma de su patillaje permite a la máquina un montaje más directo. La otra modalidad, sería con encapsulado tipo THD, que como se puede observar en la Figura 3.3, se trata de un encapsulado DIP (*Dual In-line Package*) con dos filas de terminales doblados en ángulo recto respecto a la base. Este tipo de encapsulado es más adecuado en placas cuyo montaje se realiza a mano, se precisan de taladros para dejar pasar los pines y se sueldan al *pad*. Como se ha comentado con anterioridad, en el presente proyecto, se ha decidido utilizar tecnología SMD para casi todos los encapsulados, resistencias y condensadores, debido a su reducido tamaño y a su instalación inmediata, ya sea de forma automatizada o a mano. En el Anexo V: Hojas de datos del fabricante, se recogen las hojas de características los componentes empleados.

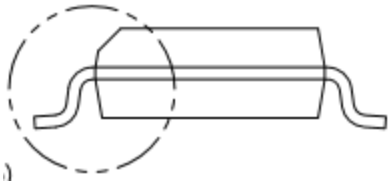

Figura 3.2. Componente SMD.

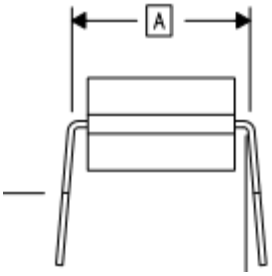

Figura 3.3. Componente THD.

3.1 Pcbnew: software de creación de PCB.

Una vez terminado el esquema electrónico, realizados todos los procedimientos de control y todas las huellas seleccionadas, procede pasar a la creación de la placa PCB con ayuda la herramienta PCBnew de KiCAD. En este caso, el flujo de trabajo es el siguiente, a partir del archivo *Netlist,* el programa carga sobre la zona de trabajo las huellas de los encapsulados de los componentes y sus respectivas conexiones, que se establecieron en el esquema electrónico.

Este software aporta muchas opciones para trabajar. En la Figura 3.4 se puede observar el entorno de trabajo. Entre las opciones básicas que presentan los editores de este tipo, destacan: Administrador de capas, a la derecha de la figura, donde se puede seleccionar entre todas las capas físicas o de documentación posibles de una placa. También se pueden editar huellas desde aquí, así como actualizar nuestro *Netlist* si añadimos algún elemento nuevo en el esquema electrónico. Tenemos también disponible un chequeo de las reglas eléctricas (DRC), al igual que se tenía en EESCHEMA y las herramientas para editar *pads*, vías y pistas. En cuanto a las pistas, además, incluye un apartado en la que nos permite hacer un *Autorruteo,* es decir, establecer el camino descrito por las pistas de cobre que unen los componentes, optimizando tanto los recorridos como los anchos de las pistas.

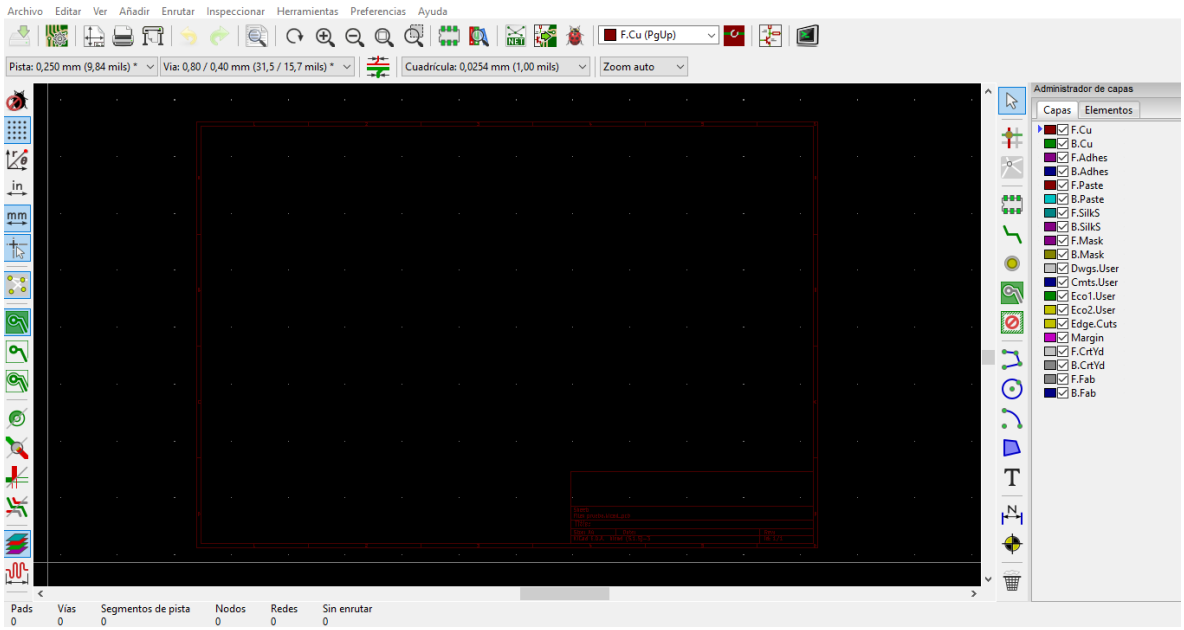

Figura 3.4. Ventana de trabajo principal de Pcbnew.

3.2 Reglas de diseño.

Una vez se tengan los elementos con sus correspondientes conexiones, hay que decidir cuál es la mejor forma posible de colocar los componentes. Esto no se hará a la ligera, ya que requiere del cumplimiento de una serie de reglas de diseño [3] en cuanto a la ubicación, orientación, y separación entre ellos.

Con este fin, se ha llevado a cabo el siguiente flujo de trabajo. Lo primero es establecer las unidades de medida, los milímetros (mm), y fijar la rejilla de trabajo del sistema en una medida adecuada para que los componentes queden perfectamente alineados. Se ha elegido una cuadrícula de 0,0127mm. Ya con estos parámetros fijados, se hace una primera colocación de los componentes de forma rápida para poder establecer los límites del espacio de trabajo, esto es, el tamaño de la placa. El tamaño de la placa es de 77,6 x 82,5mm. El borde de la placa se puede editar en cualquier momento, por si se nos queda algún componente fuera o sin espacio, poder expandir el área destinada a la realización de la placa. Por último, tendremos que elegir dos parámetros más antes de empezar a colocar los componentes: el ancho de las pistas y el tamaño de las vías. El ancho de la pista se escoge teniendo en cuenta el espesor de cobre de la placa (35µm en FR4), las corrientes, el incremento de temperatura y el proceso de fabricación químico. El ancho elegido para las pistas es de 0,4mm. Por último, especificaremos las capas que vamos a usar, en nuestro caso, dos capas conductoras de cobre, la capa TOP y la capa BOT. La capa TOP es la capa en la que se montan los componentes y donde estarán la gran parte de las pistas de cobre. La capa BOT servirá como puente para colocar aquellas conexiones que sea imposible situar en la capa TOP. Los *pads* de los componentes con encapsulado THD se incluirán en la capa TOP, ya que al atravesar con sus pines la placa, permiten hacer conexiones en la capa BOT. Para hacer que coincidan ambas capas, debemos añadir marcas fiduciales, esto es, un marcador referencial que está en la esquina superior de ambas caras, y que debemos hacer coincidir en el proceso de transferencia del diseño a la placa.

Una vez establecidos los parámetros iniciales, comienza el proceso del diseño de la placa PCB y la colocación de los componentes.

3.3 Colocación de los componentes.

La colocación de los componentes se debe hacer de forma lógica [3]. Como diseñadores debemos tener una idea aproximada de cómo deseamos que sea la placa y a partir de ahí, empezar a aplicar las distintas reglas de diseño. En la Figura 3.5 se muestra cómo se han situado los componentes en la placa.

Los integrados, resistencias y condensadores están centrados en la placa, con una separación mínima entre componentes de 0,5mm. Los elementos que requieran accesibilidad desde el exterior se han colocado cerca de los bordes de la placa, como, por ejemplo, los puntos de test y los conectores, tanto para la señal TTL como para los ±5V de la alimentación. Estos elementos precisan de un cableado externos, ya sea para alimentarlos o para medir y, por lo tanto, es más cómodo situarlos en los bordes. Estos componentes deberán estar separados al menos 2mm del borde de la placa. Los visualizadores o *displays* se han localizado en una de las esquinas de la placa.

En la Figura 3.5 también se puede ver que cada integrado posee un condensador en la parte superior, estos son los condensadores de desacoplo anteriormente mencionados, que se encargan de evitar fenómenos como la diafonía, parásitos inductivos o capacitivos, etc. Cada integrado deberá tener un condensador de desacoplo por cada alimentación que reciba. Todos los integrados del circuito tienen solo uno, el de +5V, excepto el DAC0808 y el LM741 que tienen dos, ya que se alimentan a ±5V.

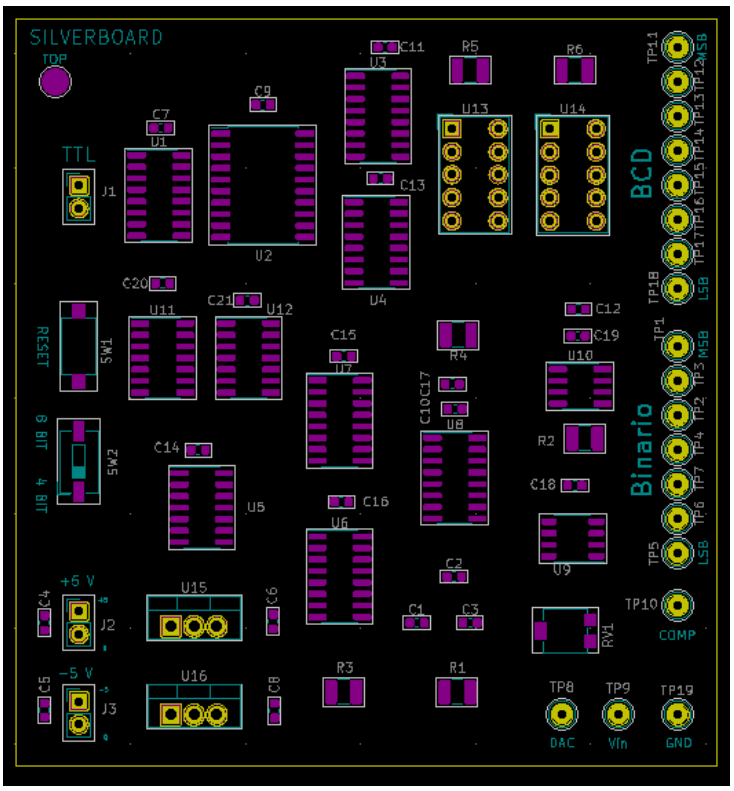

Figura 3.5. Colocación de componentes en la PCB con Pcbnew.

3.4 Pistas y texto.

Tras localizar los componentes, hay que proceder a trazar las pistas. Las conexiones ya están establecidas gracias a que exportamos el *Netlist* desde el software EESCHEMA y el ancho de las pistas está fijado desde el inicio de este proceso, así que solo se tienen que ir trazando estas pistas manualmente, respetando el espaciado entre ellas, evitando que se crucen, o que transcurran paralelas durante el menor recorrido posible, evitando así interferencias entre señales que transcurran por pistas próximas. El proceso puede resultar tedioso debido a la gran cantidad de elementos que hay en la placa, por ese motivo, se ha recurrido a la herramienta *"Freerouting"* que viene incluida dentro del paquete PCBnew de KiCad, y el cual necesita de la utilización del archivo SPECCTRA. El programa comienza con la creación de las pistas en la cara TOP. Cuando no pueda trazar una pista, creará una vía para poder realizar la conexión a través de la capa BOT. Cuando se realicen todas las conexiones, comenzará un proceso de optimización de distancias entre pistas y del número de pistas utilizadas. Cuando la optimización se detenga, tras realizar algunas operaciones de intercambio de ficheros, automáticamente obtendremos en nuestro programa, la misma placa PCB, pero ahora con las pistas trazadas. Además de trazar las pistas, hay que añadir en la cara TOP zonas de relleno de cobre. Estas zonas se utilizan para la supresión de ruido o para el aislamiento de señales. En este caso, esta capa se corresponderá con la señal GND, simplificando muchas de las conexiones de nuestra placa. En las Figuras 3.6 y 3.7 se muestran la capa TOP y BOT, respectivamente, ya terminadas y trazadas, únicamente quedaría aplicar texto a nuestra placa.

Como ayuda o guía para los estudiantes, se ha añadido texto en la cara TOP de la placa. Este texto comprende:

- Indicativos de los 3 conectores, indicando cual es la entrada TTL de reloj y cuáles son las entradas de +5V, -5V y GND.
- Los puntos de test del CDA, V_{IN} y GND, tienen cada uno una etiqueta para identificarlos inmediatamente.
- Las dos filas de terminales o puntos de prueba o test de los dos contadores incorporan un texto que los identifica. Además, se indica cuáles son sus bits más y menos significativos.

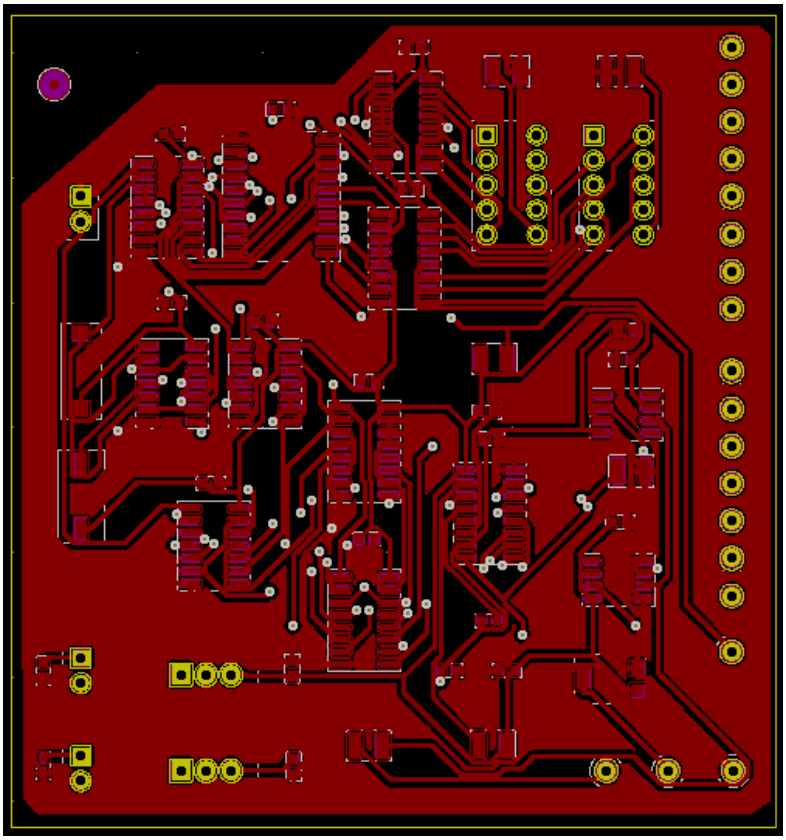

Figura 3.6. Capa TOP con pistas y vías.

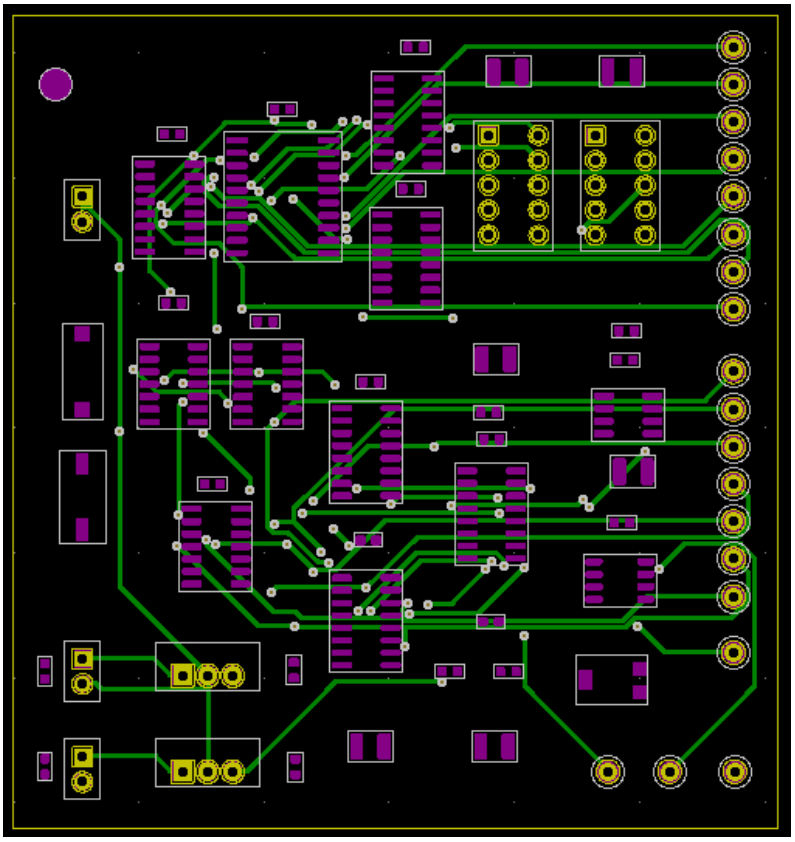

Figura 3.7. Capa BOT con pistas y vías.

Capítulo 4: Presupuesto.

4.1 Coste material.

COMPONENTE	CANTIDAD	COSTE UNITARIO	COSTE TOTAL
Condensador SMD 100nF	18	0,35 €	6,30 €
Condensador SMD 1uF	2	0,35 €	0,70 €
Condensador SMD 10nF	1	0,35 €	0,35 €
Conectores	3	0,05 €	0,16 €
Resistencia SMD 4,7K	3	0,01 €	0,03 €
Resistencia SMD 2,2k	1	0,00 €	0,00 €
Resistencia SMD 270	2	0,01 €	0,01 €
Potenciómetro SMD	1	1,05 €	1,05 €
Pulsador	1	0,42 €	0,42 €
Interruptor	1	2,56 €	2,56 €
Puntos de test	19	0,12 €	2,28 €
C.I. 74LS390	1	1,26 €	1,26 €
C.I. 74LS374	1	0,91 €	0,91 €
C.I. 74LS47	2	1,65 €	3,30 €
C.I. 74LS393	1	2,33 €	2,33 €
C.I. 74LS157	2	0,91 €	1,82 €
DAC0808	1	2,04 €	2,04 €
LM311	1	2,32 €	2,32 €
LM741	1	0,78 €	0,78 €
C.I. 74LS32	1	0,66 €	0,66 €
C.I. 74LS08	1	0,66 €	0,66 €
Display 7 segmentos	2	2,74 €	5,48 €
LM7805	2	1,37 €	2,74 €
Placa de cobre doble cara	1	3,90 €	3,90 €

TOTAL	42,07€

Datos extraídos de RS España [4]. Este proyecto no se ha implementado, pero se ha calculado el presupuesto como si se quisiera realizar esta placa.

4.2 Coste de mano de obra.

CONCEPTO	CANTIDAD (h)	COSTE UNITARIO (€/h)	COSTE TOTAL
Análisis y diseño	30	28,00 €	840,00 €
Implementación*	9	20,00 €	180,00 €
Documentación	20	18,00 €	360,00 €

TOTAL	1.380,00 €

El coste de la mano de obra se ha calculado en base al tiempo utilizado en el desarrollo de los apartados de análisis y diseño y de la documentación recogida en este documento. En cuanto a la implementación, aunque no se ha realizado, se ha estimado el tiempo de montaje en comparación con el tiempo empleado en la realización de una placa de características similares.

4.3 Coste total.

COSTE TOTAL	
Coste material	42,06 €
Coste Mano de obra	1.380,00 €
Gastos Generales	85,32 €
Beneficio industrial	213,31 €

TOTAL PROYECTO	1.720,69 €

El coste total se ha calculado aplicando porcentajes obtenidos del Reglamento General LCAP [5] a los valores calculados en los apartados anteriores. Los porcentajes correspondientes son del 6% para los gastos generales y del 15% para el beneficio industrial. Ambos porcentajes se aplican tanto al coste material como a la mano de obra.

Por último, se presenta el cálculo del coste por unidad suponiendo que se fabrican 100 y 1000 placas. En ambos casos, el coste debido al tiempo de análisis y diseño, y el de documentación no varían con respecto al de fabricación de una placa. El tiempo de implementación se ha reducido a tres horas por placa implementada. De esta manera, los resultados obtenidos son los siguientes:

Concepto	Coste unitario	Cantidad	Coste Total
Placa	42,07 €	100,00 €	4.207,00 €
Análisis y diseño	28,00 €	30,00 h	840,00 €
Implementación	20,00 €	300,00 h	6.000,00 €
Documentación	18,00 €	20,00 h	360,00 €
TOTAL (100 placas)			11.407,00 €

Concepto	Coste unitario	Cantidad	Coste Total
Placa	42,07 €	1.000,00 €	42.070,00 €
Análisis y diseño	28,00 €	30,00 h	840,00 €
Implementación	20,00 €	3.000,00 h	60.000,00 €
Documentación	18,00 €	20,00 h	360,00 €
TOTAL (1000 placas)			103.270,00 €

Como se puede observar, para el caso de 100 placas, el total asciende a 11.407 €, lo que corresponde a un coste unitario por placa de **114,07 €.** Para 1000 placas, el total es 103.270 €, lo que supone un coste unitario de **103,27 €.**

Capítulo 5: Resultados y conclusiones.

Este trabajo se ha centrado en el diseño de un conversor analógico-digital basado en el método contador-rampa con la finalidad de utilizarlo como módulo didáctico en la realización de experiencias prácticas orientadas familiarizarse con el uso de los analizadores lógicos para el análisis y comprobación del funcionamiento de los elementos o bloques digitales de un circuito electrónico digital. Gracias a la realización de este trabajo, se ha conseguido mejorar el diseño del esquema electrónico de la práctica original que se lleva a cabo en el módulo de Instrumentación Electrónica de la asignatura Técnicas Experimentales III, que se imparte en el tercer curso del Grado en Física de la ULL [1], en lo que respecta a permitir su funcionamiento con 4 u 8 bits. En la Figura 5.1 se muestra el esquema electrónico del circuito diseñado.

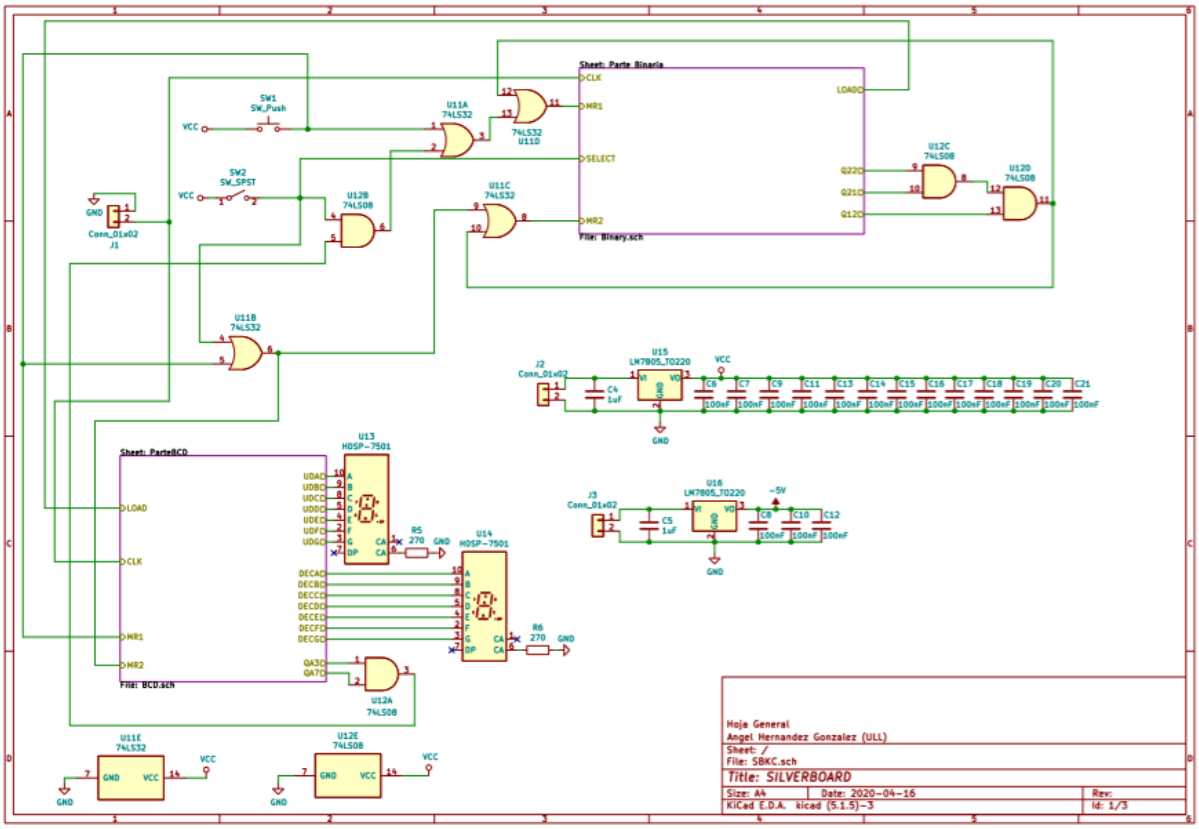

Figura 5.1. Esquema electrónico de la placa.

Otro resultado ha sido el diseño de la placa de circuito impreso o PCB necesaria para implementar el circuito. Su tamaño es de 77,6 x 82,5 mm, lo que se ha conseguido gracias al uso de componentes basados en tecnología SMD. En las Figuras 5.2 y 5.3 se puede observar un modelo 3D de la placa, tanto de su cara TOP como de su cara BOT.

Con la finalidad de que la placa de circuito impreso sea fácil de usar y de conexión inmediata, se han incorporado señalizaciones o etiquetas tanto para las conexiones como para los terminales de pruebas o test (Figuras 5.4 y 5.5).

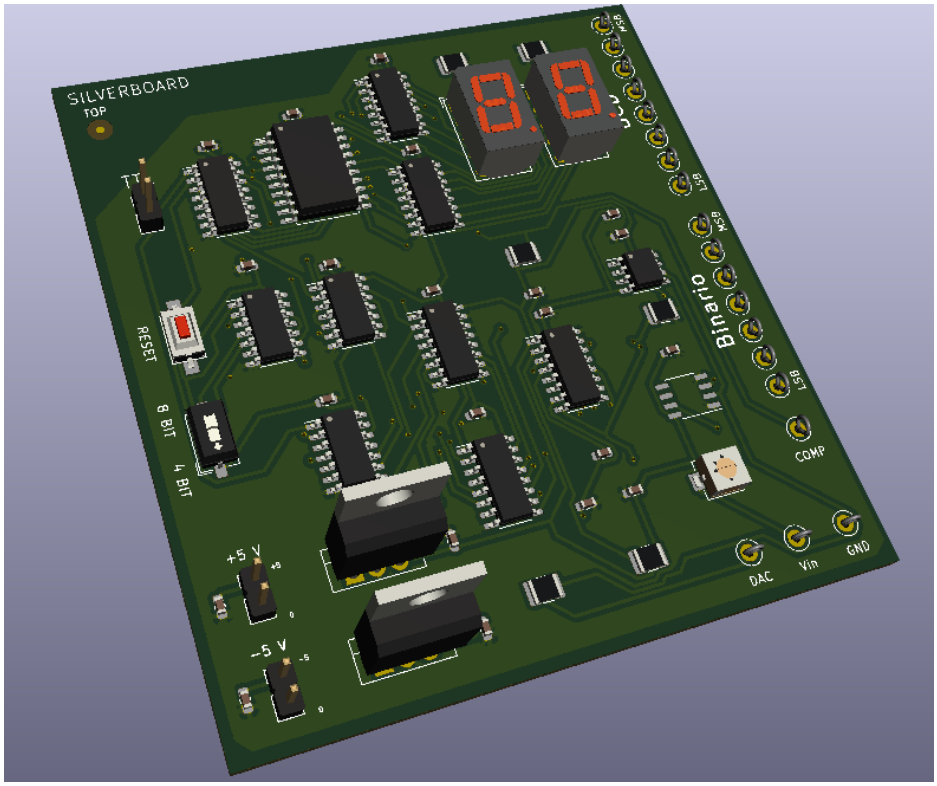

Figura 5.2. Cara TOP de la placa.

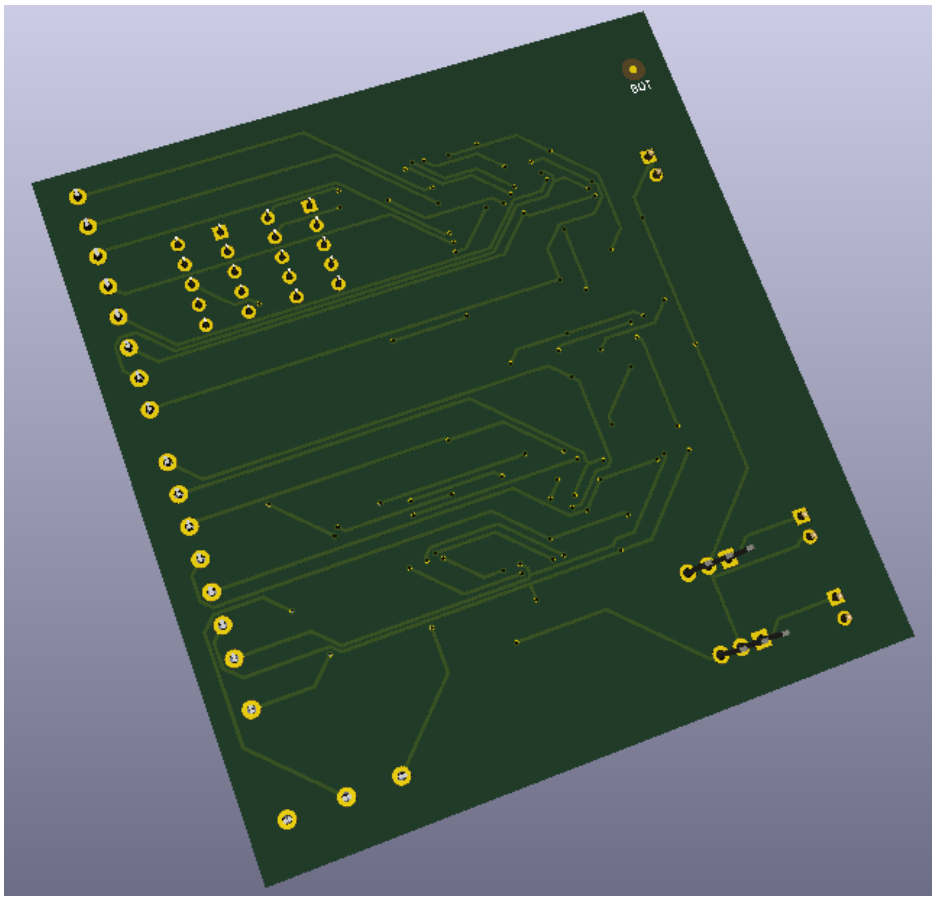

Figura 5.3. Cara BOT de la placa.

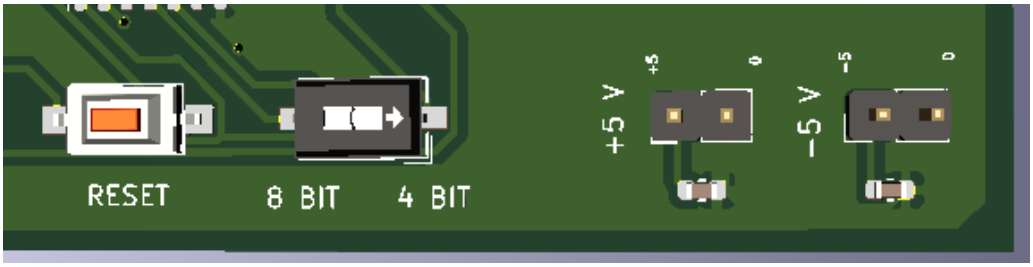

Figura 5.4. Señalización de alimentación e interruptores.

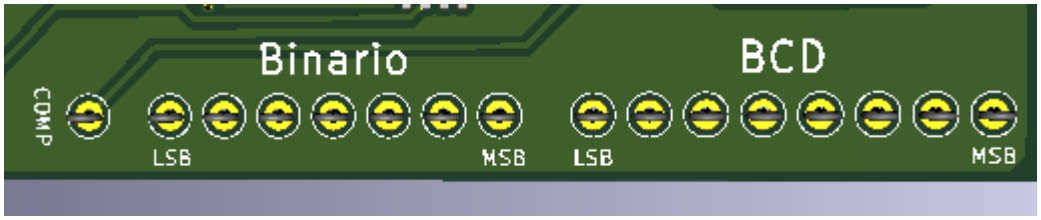

Figura 5.5. Señalización de los puntos de test.

La realización física de la placa de circuito impreso no ha sido posible debido a que la ejecución de este Trabajo de Fin de Grado, en su etapa final, ha coincidido con el período de alarma del “COVID-19”. En este mismo sentido, tampoco se ha podido llevar a cabo la implementación en placa de prototipo (*protoboard*) del circuito, ya que no se podía acceder a los laboratorios de la Universidad de La Laguna y, tampoco se disponía de material ni de la instrumentación electrónica necesaria para llevarlo a cabo. Sin embargo, la implementación de la misma se podrá hacer sin problemas usando los datos recogidos en este documento. Aun así, a continuación, se enumeran diversas mejoras que se podrían aplicar a la hora de hacer dicha implementación:

- Incorporar en la placa una fuente de alimentación que evite la necesidad de un conexionado exterior para disponer de las tensiones de +5V y -5V.
- Incluir un circuito oscilador que genere la señal de reloj general.
- Diseñar un soporte físico para la placa de circuito impreso que le proporcione un aspecto más comercial como producto final.

Conclusions.

This work has focused on the design of an analog-to-digital converter based on the counter-ramp method in order to use it as a didactic module in the realization of practical experiences oriented to familiarizing with the use of logic analyzers for the analysis and testing the operation of the elements or digital blocks of a digital electronic circuit. Thanks to the completion of this work, it has been possible to improve the design of the electronic schematic of the original practice that is carried out in the Electronic Instrumentation module of the Experimental Techniques III course, which is taught in the third year of the Physic's degree of the ULL [1], in regards to allowing its operation with 4 or 8 bits. Figure 5.1 shows the electronic schematic of the designed circuit.

Another result has been the design of the printed circuit board or PCB necessary to implement the circuit. Its size is 77.6 x 82.5 mm, which has been achieved thanks to the use of components based on SMD technology. In Figures 5.2 and 5.3 you can see a 3D model of the board, both its TOP and BOT faces.

In order to make the printed circuit board easy to use and for immediate connection, signs or labels have been incorporated for both the connections and the test terminals (Figures 5.4 and 5.5).

The physical realization of the printed circuit board has not been possible because the execution of this Final Degree Project, in its final stage, has coincided with the alarm period of "COVID-19". In this same sense, it has not been possible to carry out the implementation of the circuit's prototype board, since it was not possible to access the laboratories of the University of La Laguna and neither was available the material or the electronic instrumentation necessary to carry it out. However, its implementation can be done without problems using the data collected in this document. Even so, below, several improvements that could be applied when making such an implementation are listed:

- Incorporate in the board a power supply that avoids the need for an external connection to have voltages of + 5V and -5V.
- Include an oscillator circuit that generates the general clock signal.
- Design a physical support for the printed circuit board that gives it a more commercial appearance as a final product.

Glosario.

BCD: *Binary Coded Decimal.*
BOM: *Bill of Materials.*
BOT: *Capa inferior de la placa.*
CAD: *Conversor analógico digital.*
CDA: *Conversor digital analógico.*
CI: *Circuito Integrado.*
EDA: *Electronic Desing Automation.*
ERC: *Electric Rules Check.*
GND: *Ground.*
LCAP: *Ley de Contratos de las Administraciones Públicas.*
LED: *Light-Emitting Diode.*
LSB: *Less Significative Bit.*
MR1: *Master-Reset 1.*
MR2: *Master-Reset 2.*
MSB: *More Significative Bit.*
MUX: *Multiplexor.*
PCB: *Printed Board Circuit.*
SMD: *Surface Mounted Device.*
SOIC: *Small Outline Integrated Circuit.*
SOP: *Small Outline Package.*
THD: *Through-Hole Device.*
TOP: *Capa superior de la placa.*
TTL: *Transistor to Transistor Logic.*

Lista de figuras y tablas.

FIGURAS:

TABLAS:

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[3] Beatriz Rodríguez Mendoza, “Apuntes de la asignatura de Diseño y Tecnología de Circuitos impresos”, 2019.

[4] RS Componentes, [En línea]: https://es.rs-online.com/, 7 de junio de 2020.

[5] Real Decreto 1098/2001, de 12 de octubre, artículo 131.

[6] KiCAD, [En línea]: https://kicad-pcb.org/, 7 de junio de 2020.

ANEXOS.

Anexo I: Archivos de salida del software EESCHEMA.

Informe ERC.

Informe ERC (20/05/2020 13:25:30, Codificación UTF8)

***** Hoja /
ErrType(3): Pin connected to other pins, but not driven by any pin
@(167,64 mm, 127,00 mm): El pin 1 (Entrada de alimentación) del componente U16 no está alimentado (red 1).
ErrType(3): Pin connected to other pins, but not driven by any pin
@(154,94 mm, 96,52 mm): El pin 1 (Entrada de alimentación) del componente U15 no está alimentado (red 4).

***** Hoja /Parte Binaria/

***** Hoja /ParteBCD/
ErrType(3): Pin connected to other pins, but not driven by any pin
@(195,83 mm, 139,70 mm): El pin 1 (Entrada de alimentación) del componente #PWR0105 no está alimentado (red 14).

**Mensajes ERC: 3. Errores0, Avisos 3

BOM (Bill of materials).

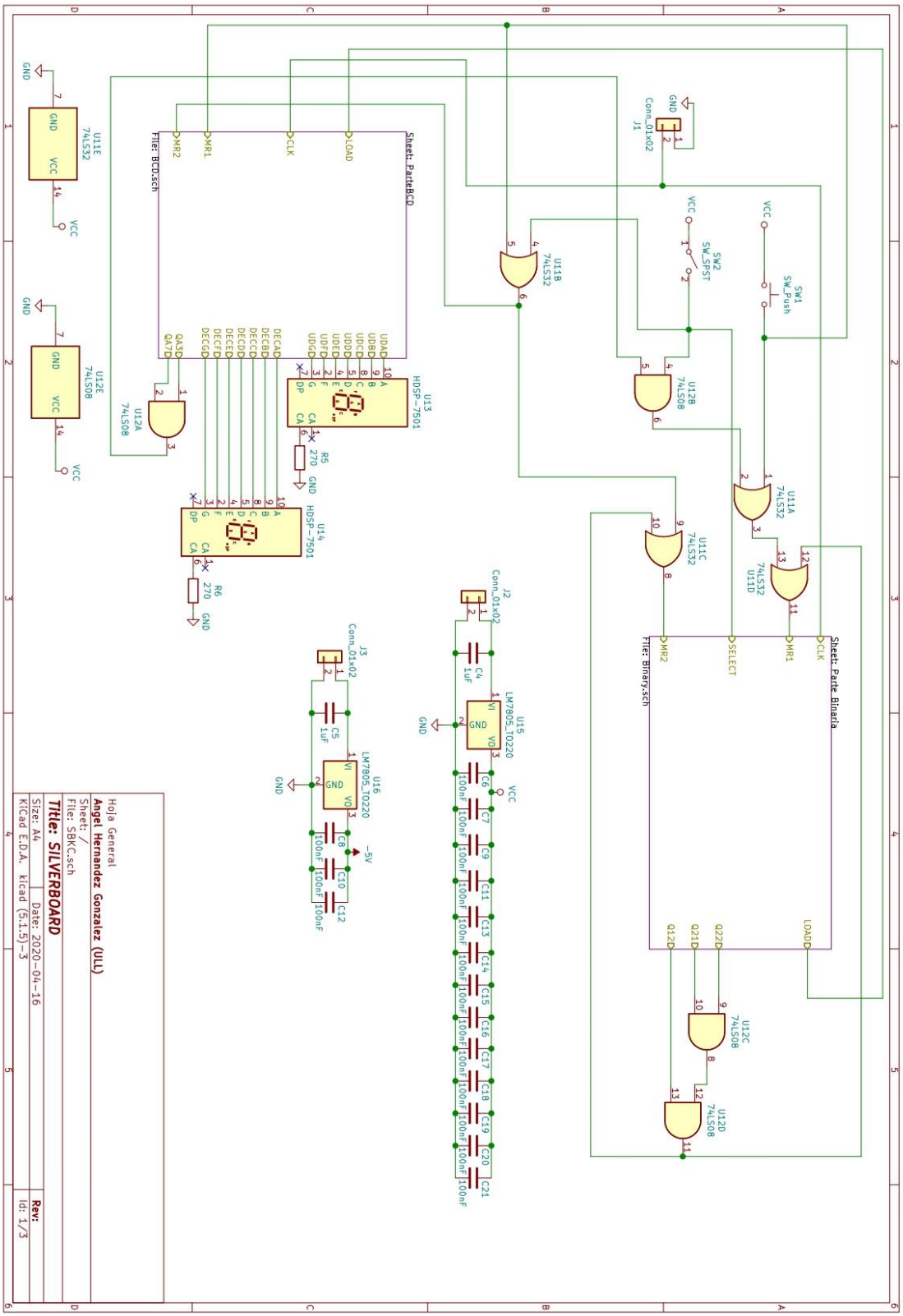
"Source:" "C:\Users\ambu_\Desktop\SBKC\SBKC\SBKC.sch"
"Date:" "20/04/2020 10:41:36"
"Tool:" "Eeschema (5.1.5)-3"
"Component Count:" "49"

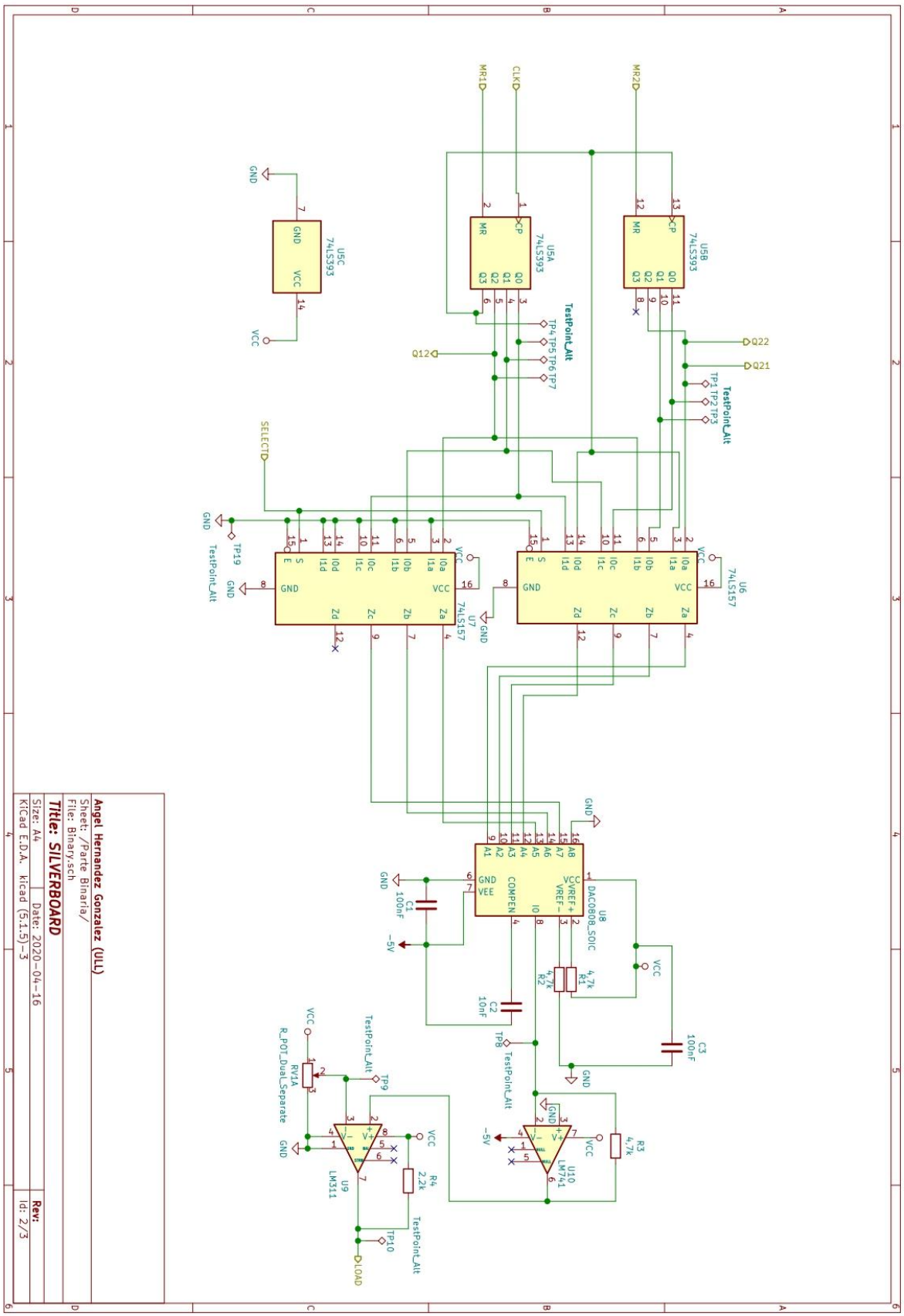
"Ref"	"Value"	"Part"	"Footprint"	"Description"	"Vendor"
"C1"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C2"	"10nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C3"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C4"	"1uF"	"Device:C"	""	"Unpolarized capacitor"	""
"C5"	"1uF"	"Device:C"	""	"Unpolarized capacitor"	""
"C6"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C7"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C8"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C9"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C10"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C11"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""

```
"C12"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C13"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C14"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C15"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C16"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C17"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C18"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C19"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C20"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""
"C21"	"100nF"	"Device:C"	""	"Unpolarized capacitor"	""

"J1"	"Conn_01x02"	"Connector_Generic:Conn_01x02"	""	"Generic connector, single row, 01x02, script generated (kicad-library-utils/schlib/autogen/connector/)"	""
"J2"	"Conn_01x02"	"Connector_Generic:Conn_01x02"	""	"Generic connector, single row, 01x02, script generated (kicad-library-utils/schlib/autogen/connector/)"	""
"J3"	"Conn_01x02"	"Connector_Generic:Conn_01x02"	""	"Generic connector, single row, 01x02, script generated (kicad-library-utils/schlib/autogen/connector/)"	""

"R1"	"4,7k"	"Device:R"	""	"Resistor"	""
"R2"	"4,7k"	"Device:R"	""	"Resistor"	""
"R3"	"4,7k"	"Device:R"	""	"Resistor"	""
"R4"	"2,2k"	"Device:R"	""	"Resistor"	""
"R5"	"270"	"Device:R"	""	"Resistor"	""
"R6"	"270"	"Device:R"	""	"Resistor"	""
"RV1"	"R_POT_Dual_Separate"	"Device:R_POT_Dual_Separate"""	"Dual potentiometer, separate units"	""

"SW1"	"SW_Push"	"Switch:SW_Push"	""	"Push button switch, generic, two pins"	""
"SW2"	"SW_DPDT_x2"	"Switch:SW_DPDT_x2"	""	"Switch, dual pole double throw, separate symbols"	""

"U1"	"74LS390"	"74xx:74LS390"	"Package_SO:SOIC-16_3.9x9.9mm_P1.27mm"	"Dual BCD 4-bit counter"
"U2"	"74LS374"	"74xx:74LS374"	"Package_SO:SOIC-20W_7.5x12.8mm_P1.27mm"	"8-bit Register, 3-state outputs"	""
"U3"	"74LS47"	"74xx:74LS47"	"Package_SO:SOIC-16_3.9x9.9mm_P1.27mm"	"BCD to 7-segment Driver, Open Collector, 30V outputs"	""
"U4"	"74LS47"	"74xx:74LS47"	"Package_SO:SOIC-16_3.9x9.9mm_P1.27mm"	"BCD to 7-segment Driver, Open Collector, 30V outputs"	""
"U5"	"74LS393"	"74xx:74LS393"	"Package_SO:SOIC-14_3.9x8.7mm_P1.27mm"	"Dual BCD 4-bit counter"
"U6"	"74LS157"	"74xx:74LS157"	"Package_SO:SOIC-16_3.9x9.9mm_P1.27mm"	"Quad 2 to 1 line Multiplexer"	""
"U7"	"74LS157"	"74xx:74LS157"	"Package_SO:SOIC-16_3.9x9.9mm_P1.27mm"	"Quad 2 to 1 line Multiplexer"	""
"U8"	"DAC0808_SOIC"	"Analog_DAC:DAC0808_SOIC"	"Package_SO:SOIC-16_3.9x9.9mm_P1.27mm"	"8-bit multiplying DAC"	""
"U9"	"LM311"	"Comparator:LM311"	""	"Voltage Comparator, DIP-8/SOIC-8/SSOP-8"	""
"U10"	"LM741"	"Amplifier_Operational:LM741"	""	"Operational Amplifier, DIP-8/TO-99-8"	""
"U11"	"74LS32"	"74xx:74LS32"	""	"Quad 2-input OR"	""
"U12"	"74LS08"	"74xx:74LS08"	""	"Quad And2"	""
```

"U13" "HDSP-7501" "Display_Character:HDSP-7501" "Display_7Segment:HDSP-A151""One digit 7 segment high efficiency red, common anode" ""
"U14" "HDSP-7501" "Display_Character:HDSP-7501" "Display_7Segment:HDSP-A151""One digit 7 segment high efficiency red, common anode" ""
"U15" "LM7805_TO220" "Regulator_Linear:LM7805_TO220" "Package_TO_SOT_THT:TO-220-3_Vertical"
"Positive 1A 35V Linear Regulator, Fixed Output 5V, TO-220" ""
"U16" "LM7805_TO220" "Regulator_Linear:LM7805_TO220" "Package_TO_SOT_THT:TO-220-3_Vertical"
"Positive 1A 35V Linear Regulator, Fixed Output 5V, TO-220" ""

Anexo II: Esquemas electrónicos.




MR1
CLK
MR2
U5C
74LS393
U5A
74LS393
U5B
74LS393
GND
VCC
Q12
Q22
Q21
TestPoint_Alt
SELECT
TP19
U7
74LS157
U6
74LS157
U8
DAC0808_SOIC
C1
100nF
-5V
C2
10nF
C3
100nF
R1
4,7k
R2
4,7k
R3
4,7k
R4
2,2k
RV1A
R_POT_Dual_Separate
U9
LM311
U10
LM741
TP8
TP9
TP10
LOAD
Angel Hernandez Gonzalez (ULL)
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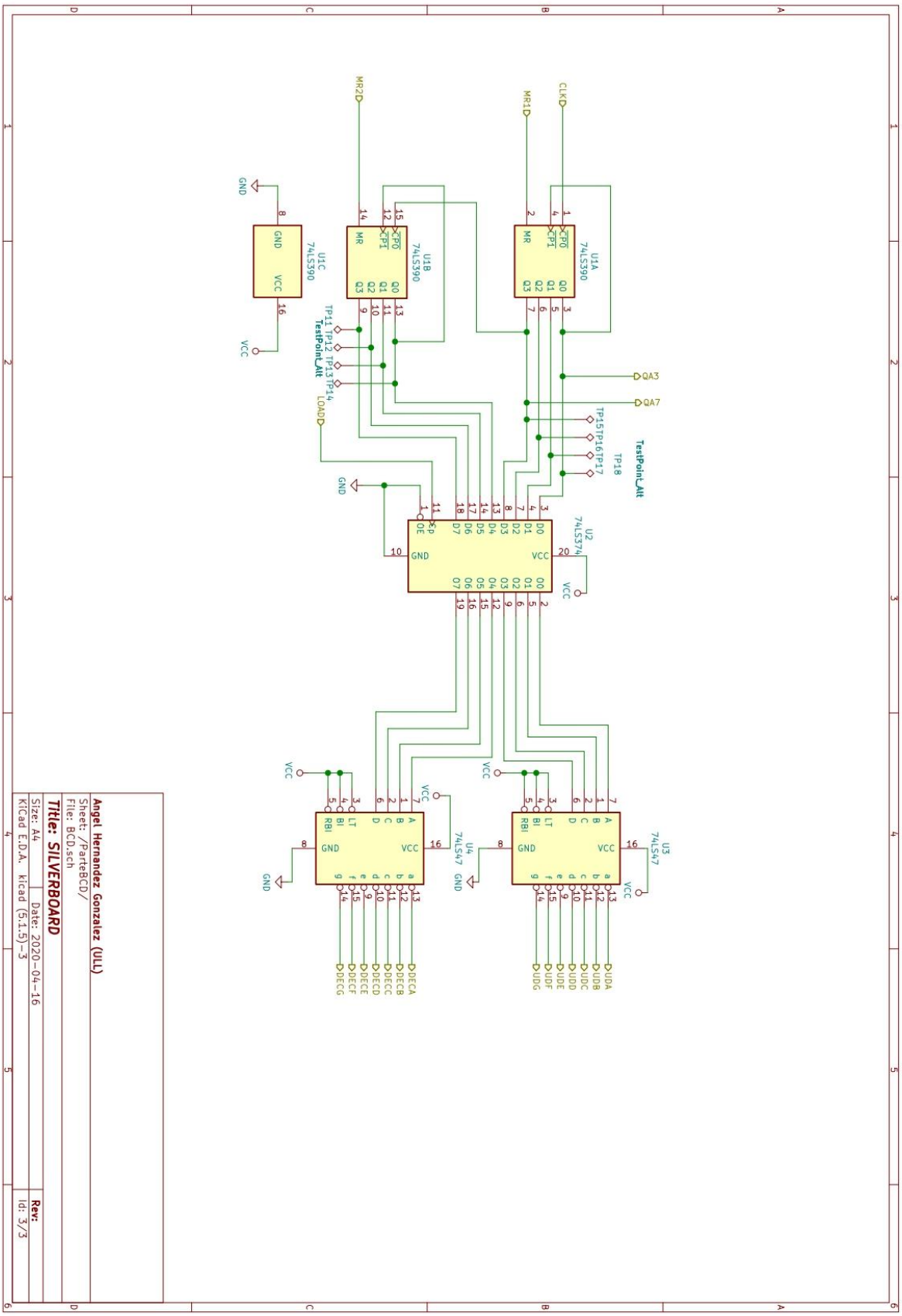
File: Binary.sch
Title: SILVERBOARD
Size: A4
Date: 2020-04-16
KiCad E.D.A. kicad (5.1.5)-3
Rev:
Id: 2/3

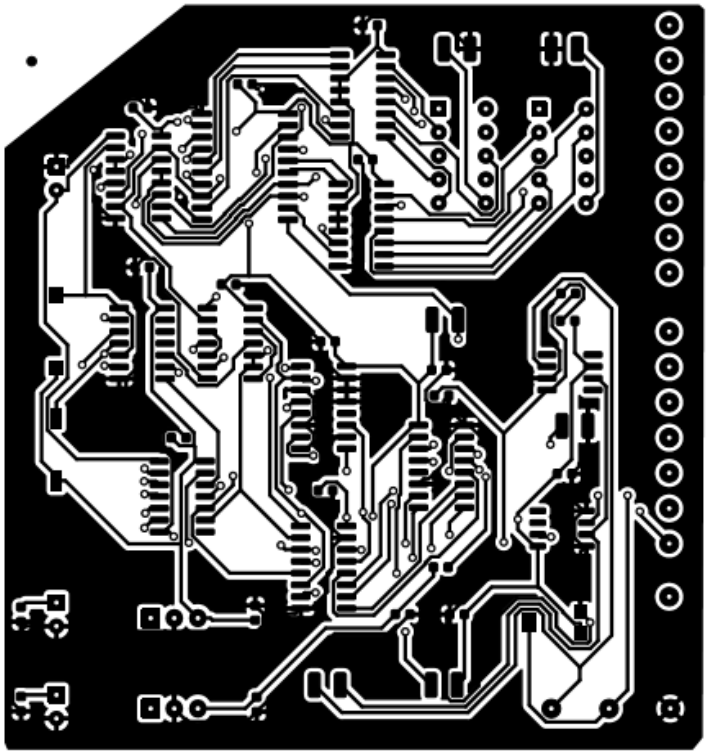

MR2D
CLKD
MR1D
GND
VCC
U1C
74LS390
U1B
74LS390
U1A
74LS390
TP11
TP12
TP13
TP14
TestPoint_Alt
LOAD
QA3
QA7
TP15
TP16
TP17
TP18
U2
74LS374
U3
74LS47
U4
74LS47
DECA
DECB
DECC
DECD
DECE
DECF
DECG
UDA
UDB
UDC
UDD
UDE
UDF
UDG
Angel Hernandez Gonzalez (ULL)
Sheet: /ParteBCD/
File: BCD.sch
Title: SILVERBOARD
Size: A4
Date: 2020-04-16
KiCad E.D.A. kicad (5.1.5)-3
Rev:
Id: 3/3

Anexo III: Lista de huellas de componentes.

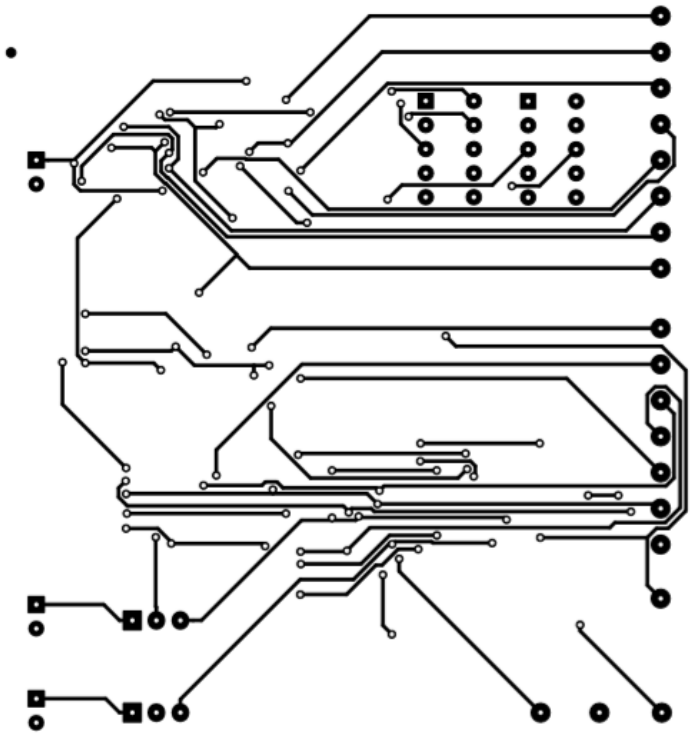
Condensadores: *Capacitor_SMD:C_0603Metric*
Conectores: *Conector_PinHeader_1x02_2.45mm_Vertical*
Resistencias: *Resistor_SMD:R_1210_3225Metric*
Resistencia Variable: *Potentiometer_SMD_ACP_CA9-VSMD_Vertical*
Pulsador reset general: *SW_PUSH_SPST_NO_Alps_SKRK*
Interruptor: *SW_DIP_SPSTx01_Slide_6.7x4.1mm_W6.73mm_P2.54mm_LowProfile_JPin*
TestPoint: *TestPoint_Loop_D2.50mm_Drill1.0mm_LowProfile*
U1: *(74LS390) Package_SO:SOIC-16_3.9x9.9mm_P1.27mm*
U2: (*74LS374) Package_SO:SOIC-20W_7.5x12.8mm_P1.27mm*
U3: *(74LS47) Package_SO:SOIC-16_3.9x9.9mm_P1.27mm*
U4: *(74LS47) Package_SO:SOIC-16_3.9x9.9mm_P1.27mm*
U5: *(74LS393) Package_SO:SOIC-14_3.9x8.7mm_P1.27mm*
U6: *(74LS157) Package_SO:SOIC-16_3.9x9.9mm_P1.27mm*
U7: *(74LS157) Package_SO:SOIC-16_3.9x9.9mm_P1.27mm*
U8: *(DAC0808) Package_SO:SOIC-16_3.9x9.9mm_P1.27mm*
U9: *(LM311) Package_SO:SOP-8_3.9x4.9mm_P1.27mm*
U10: *(LM741) Package_SO:SOIC-8_3.9x4.9mm_P1.27mm*
U11: *(74LS32) Package_SO:SOIC-14_3.9x8.7mm_P1.27mm*
U12: *(74LS08) Package_SO:SOIC-14_3.9x8.7mm_P1.27mm*
U13: *(DISPLAY7SEG) Display_7Segment:HDSP-A151*
U14: *(DISPLAY7SEG) Display_7Segment:HDSP-A151*
U15: *(7805) Package_TO_SOT_THT:TO-220-3_Vertical*
U16: *(7905) Package_TO_SOT_THT:TO-220-3_Vertical*

Anexo IV: Fotolitos.

Capa TOP.



Capa BOT.



Anexo V: Hojas de datos de fabricantes.

1. Condensadores.

VISHAY
www.vishay.com

VJ Commercial Series
Vishay Vitramon

Surface Mount Multilayer Ceramic Chip Capacitors for Commercial Applications

FEATURES

- C0G (NP0) and X7R dielectrics offered
- C0G (NP0) is an ultra-stable dielectric offering a very low Temperature Coefficient of Capacitance (TCC)
- C0G (NP0) offers low dissipation
- Excellent aging characteristics
- Ideal for decoupling and filtering (X7R)
- Ideal for surge suppression and high voltage applications
- Wide range of case sizes, voltage ratings and capacitance values
- Wet build process
- Reliable Noble Metal Electrode (NME) system
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb RoHS COMPLIANT HALOGEN FREE GREEN (5-2008) Available

APPLICATIONS

- Timing and tuning circuits
- Sensor and scanner applications
- Decoupling and filtering
- Surge suppression

ELECTRICAL SPECIFICATIONS

C0G (NP0) DIELECTRIC

GENERAL SPECIFICATION
Note
Electrical characteristics at +25 °C unless otherwise specified

Operating Temperature: -55 °C to +150 °C
(above +125 °C changed characteristics)

Capacitance Range: 1 pF to 56 nF

Voltage Range: 25 V_{DC} to 1000 V_{DC}

Temperature Coefficient of Capacitance (TCC):
0 ppm/°C ± 30 ppm/°C from -55 °C to +125 °C

Dissipation Factor (DF):
0.1 % maximum at 1.0 V_{RMS} and
1 MHz for values ≤ 1000 pF
0.1 % maximum at 1.0 V_{RMS} and
1 kHz for values > 1000 pF

Insulating Resistance:
at +25 °C 100 000 MΩ min. or 1000 ΩF whichever is less
at +125 °C 10 000 MΩ min. or 100 ΩF whichever is less

Aging Rate: 0 % maximum per decade

Dielectric Strength Test:
performed per method 103 of EIA 198-2-E.
Applied test voltages

≤ 200 V_{DC}-rated:	250 % of rated voltage
500 V_{DC}-rated:	200 % of rated voltage
630 V_{DC},1000 V_{DC}-rated:	150 % of rated voltage

X7R DIELECTRIC

GENERAL SPECIFICATION
Note
Electrical characteristics at +25 °C unless otherwise specified

Operating Temperature: -55 °C to +150 °C
(above +125 °C changed characteristics)

Capacitance Range: 120 pF to 6.8 µF

Voltage Range: 16 V_{DC} to 1000 V_{DC}

Temperature Coefficient of Capacitance (TCC):
± 15 % from -55 °C to +125 °C, with 0 V_{DC} applied

Dissipation Factor (DF):
16 V / 25 V ratings: 3.5 % maximum at 1.0 V_{RMS} and 1 kHz
> 25 V ratings: 2.5 % maximum at 1.0 V_{RMS} and 1 kHz

Insulating Resistance:
at +25 °C 100 000 MΩ min. or 1000 ΩF whichever is less
at +125 °C 10 000 MΩ min. or 100 ΩF whichever is less

Aging Rate: 1 % maximum per decade

Dielectric Strength Test:
performed per method 103 of EIA 198-2-E.
Applied test voltages

≤ 250 V_{DC}-rated:	250 % of rated voltage
500 V_{DC}-rated:	min. 150 % of rated voltage
630 V_{DC}, 1000 V_{DC}-rated:	min. 120 % of rated voltage

QUICK REFERENCE DATA				
DIELECTRIC	CASE	MAXIMUM VOLTAGE (V)	CAPACITANCE	
			MINIMUM	MAXIMUM
C0G (NP0)	0402	100	1.0 pF	220 pF
	0603	200	1.0 pF	1.0 nF
	0805	500	1.0 pF	4.7 nF
	1206	630	1.0 pF	10 nF
	1210	630	56 pF	12 nF
	1808	1000	18 pF	10 nF
	1812	1000	39 pF	22 nF
	1825	500	100 pF	39 nF
	2220	1000	270 pF	47 nF
	2225	1000	270 pF	56 nF
X7R	0402	100	120 pF	47 nF
	0603	200	330 pF	150 nF
	0805	250	330 pF	470 nF
	1206	630	330 pF	1.0 µF
	1210	630	390 pF	1.0 µF
	1808	1000	470 pF	270 nF
	1812	1000	1.0 nF	1.0 µF
	1825	1000	10 nF	2.7 µF
	2220	500	15 nF	2.2 µF
	2225	1000	33 nF	4.7 µF
	3640	500	27 nF	6.8 µF

Note

- Detail ratings see "Selection Chart"

ORDERING INFORMATION

VJ0805 (1)	Y	102	K	X	A	A	T	### (3)
CASE CODE	DIELECTRIC	CAPACITANCE NOMINAL CODE	CAPACITANCE TOLERANCE	TERMINATION	DC VOLTAGE RATING (2)	MARKING	PACKAGING	PROCESS CODE
0402 0603 0805 1206 1210 1808 1812 1825 2220 2225 3640	A = C0G (NP0) Y = X7R	Expressed in picofarads (pF). The first two digits are significant, the third is a multiplier. **Examples:** 1R8 = 1.8 pF 102 = 1000 pF	B = ± 0.10 pF C = ± 0.25 pF D = ± 0.5 pF F = ± 1 % G = ± 2 % J = ± 5 % K = ± 10 % M = ± 20 % **Note** C0G (NP0): B, C, D < 10 pF F, G, J, K ≥ 10 pF X7R: J, K, M	X = Ni barrier 100 % tin plated matte finish F, E = AgPd (4) B = polymer 100 % tin plated matte finish (5)	J = 16 V X = 25 V A = 50 V B = 100 V C = 200 V P = 250 V E = 500 V L = 630 V G = 1000 V	A = unmarked M = marked **Note** Marking is only available for 0805 and 1206 with termination code "X" / "B"	C = 7" reel / paper tape T = 7" reel / plastic tape P = 11 1/4"/13" reel / paper tape R = 11 1/4"/13" reel / plastic tape O = 7" reel / flamed paper tape I = 11 1/4" / 13"reel / flamed paper tape **Note** "I" and "O" are used for "F", "E" termination size 0402 / 0603 / 0805	

Notes

(1) Case size designator may be replaced by four digit drawing number used to control non-standard products and / or special requirements

(2) DC voltage rating should not be exceeded in application. Other application factors may affect the MLCC performance. Consult for questions: mlcc@vishay.com

(3) Process code may be added with up to three digits, used to control non-standard products and / or special requirements

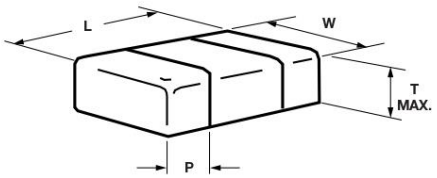
(4) Termination code "E" is for conductive epoxy assembly

(5) Selected values available, contact mlcc@vishay.com for list of released ratings

ENVIRONMENTAL STATUS

TERMINATION CODE	TERMINATION DESCRIPTION	RoHS COMPLIANT	VISHAY GREEN
X	Ni barrier 100 % tin plated matte finish	Yes	Yes
E	AgPd	Yes	Yes
B	Polymer layer, 100 % tin plated matte finish	Yes	No
F	AgPd	Yes	No

DIMENSIONS in inches (millimeters)



CASE CODE	STYLE	LENGTH (L)	WIDTH (W)	MAXIMUM THICKNESS (T)	TERMINATION (P)	
					MINIMUM	MAXIMUM
0402	VJ0402	0.040 + 0.004 / - 0.002 (1.00 + 0.10 / - 0.05)	0.020 + 0.004 / - 0.002 (0.50 + 0.10 / - 0.05)	0.024 (0.60)	0.004 (0.10)	0.016 (0.41)
0603	VJ0603	0.063 ± 0.006 (1.60 ± 0.15)	0.031 ± 0.006 (0.80 ± 0.15)	0.038 (0.97)	0.012 (0.30)	0.018 (0.46)
0805	VJ0805	0.079 ± 0.008 (2.00 ± 0.20)	0.049 ± 0.008 (1.25 ± 0.20)	0.057 (1.45)	0.010 (0.25)	0.028 (0.71)
1206	VJ1206	0.126 ± 0.010 (3.20 ± 0.25)	0.063 ± 0.010 (1.60 ± 0.25)	0.067 (1.70)	0.010 (0.25)	0.028 (0.71)
1210	VJ1210	0.126 ± 0.010 (3.20 ± 0.25)	0.098 ± 0.010 (2.50 ± 0.25)	0.067 (1.70)	0.010 (0.25)	0.028 (0.71)
1808	VJ1808	0.180 ± 0.012 (4.57 ± 0.30)	0.080 ± 0.010 (2.03 ± 0.25)	0.086 (2.18)	0.010 (0.25)	0.030 (0.76)
1812	VJ1812	0.177 ± 0.012 (4.50 ± 0.30)	0.126 ± 0.008 (3.20 ± 0.20)	0.086 (2.18)	0.010 (0.25)	0.030 (0.76)
1825	VJ1825	0.177 ± 0.012 (4.50 ± 0.30)	0.252 ± 0.010 (6.40 ± 0.25)	0.086 (2.18)	0.010 (0.25)	0.030 (0.76)
2220	VJ2220	0.220 ± 0.010 (5.59 ± 0.25)	0.200 ± 0.010 (5.08 ± 0.25)	0.086 (2.18)	0.010 (0.25)	0.030 (0.76)
2225	VJ2225	0.220 ± 0.010 (5.59 ± 0.25)	0.250 ± 0.010 (6.35 ± 0.25)	0.086 (2.18)	0.010 (0.25)	0.030 (0.76)
3640	VJ3640	0.360 ± 0.015 (9.14 ± 0.38)	0.400 ± 0.015 (10.20 ± 0.38)	0.086 (2.18)	0.010 (0.25)	0.030 (0.76)

Note

- Polymer (B-termination) have increased dimensions: length 0.006"(0.15 mm)

SELECTION CHART

DIELECTRIC		C0G (NP0)																			
STYLE		VJ0402			VJ0603			VJ0805				VJ1206 (1)					VJ1210 (1)				
CASE CODE		0402			0603			0805				1206					1210				
VOLTAGE (V_{DC})		25	50	100	50	100	200	50	100	200	500	50	100	200	500	630	50	100	200	500	630
VOLTAGE CODE		X	A	B	A	B	C	A	B	C	E	A	B	C	E	L	A	B	C	E	L
CAP. CODE	CAP.																				
1R0	1.0 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
1R2	1.2 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
1R5	1.5 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
1R8	1.8 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
2R2	2.2 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
2R7	2.7 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
3R3	3.3 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
3R9	3.9 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
4R7	4.7 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
5R6	5.6 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
6R8	6.8 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
8R2	8.2 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
100	10 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
120	12 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
150	15 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
180	18 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
220	22 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
270	27 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
330	33 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
390	39 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
470	47 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••					
560	56 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••				•	•
680	68 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••				•	•
820	82 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••				•	•
101	100 pF	••	••	••	••	••	••	••	••	••	••	•	•	•	•	•				•	•
121	120 pF	••	••	••	••	••	••	••	••	••	••	•	•	•	•	•	•	•	•	•	•
151	150 pF	••	••		••	••	••	••	••	••	••	•	•	•	•	•	•	•	•	•	•
181	180 pF	••	••		••	••	•	••	••	••	••	•	•	•	•	•	•	•	•	•	•
221	220 pF	••	••		••	••	•	••	••	••	•	•	•	•	•	•	•	•	•	•	•
271	270 pF				••	••	•	••	••	••	•	•	•	•	•	•	•	•	•	•	•
331	330 pF				••	••		••	••	••	•	•	•	•	•	•	•	•	•	•	•
391	390 pF				••	••		••	••	••	•	•	•	•	•	•	•	•	•	•	•
471	470 pF				••			••	••	•	•	•	•	•	•	•	•	•	•	•	•
561	560 pF				••			••	••	•		•	•	•	•	•	•	•	•	•	•
681	680 pF				••			••	••	•		•	•	•	•	•	•	•	•	•	•
821	820 pF				••			••	••	•		•	•	•	•	•	•	•	•	•	•
102	1.0 nF				••			••	••	•		•	•	•	•	•	•	•	•	•	•
122	1.2 nF							••	•			•	•	•			•	•	•	•	•
152	1.5 nF							••	•			•	•	•			•	•	•	•	•
182	1.8 nF							•				•	•	•			•	•	•	•	•
222	2.2 nF							•				•	•	•			•	•	•		
272	2.7 nF							•				•	•	•			•	•	•		
332	3.3 nF							•				•	•	•			•	•	•		
392	3.9 nF							•				•	•				•	•	•		
472	4.7 nF							•				•	•				•	•	•		
562	5.6 nF											•	•				•	•	•		
682	6.8 nF											•	•				•	•	•		
822	8.2 nF											•	•				•	•	•		
103	10 nF											•	•				•	•			
123	12 nF																•	•			
153	15 nF																				
183	18 nF																				
223	22 nF																				
273	27 nF																				
333	33 nF																				
393	39 nF																				
473	47 nF																				
563	56 nF																				

Notes

RoHS-compliant

•• Paper tape • Plastic tape

(1) See soldering recommendations within this data book, or visit www.vishay.com/doc?45034

SELECTION CHART

DIELECTRIC		C0G (NP0)													
STYLE		VJ1808 (1)					VJ1812 (1)					VJ1825 (1)			
CASE CODE		1808					1812					1825			
VOLTAGE (V_{DC})		50	100	200	500	1000	50	100	200	500	1000	50	100	200	500
VOLTAGE CODE		A	B	C	E	G	A	B	C	E	G	A	B	C	E
CAP. CODE	CAP.														
1R0	1.0 pF														
1R2	1.2 pF														
1R5	1.5 pF														
1R8	1.8 pF														
2R2	2.2 pF														
2R7	2.7 pF														
3R3	3.3 pF														
3R9	3.9 pF														
4R7	4.7 pF														
5R6	5.6 pF														
6R8	6.8 pF														
8R2	8.2 pF														
100	10 pF														
120	12 pF														
150	15 pF														
180	18 pF					•									
220	22 pF			•		•									
270	27 pF			•		•									
330	33 pF			•		•									
390	39 pF			•		•	•	•	•	•	•				
470	47 pF			•		•	•	•	•	•	•				
560	56 pF			•		•	•	•	•	•	•				
680	68 pF			•		•	•	•	•	•	•				
820	82 pF			•		•	•	•	•	•	•				
101	100 pF			•		•	•	•	•	•	•				•
121	120 pF			•	•	•	•	•	•	•	•				•
151	150 pF			•	•	•	•	•	•	•	•				•
181	180 pF			•	•	•	•	•	•	•	•				•
221	220 pF	•	•	•	•	•	•	•	•	•	•				•
271	270 pF	•	•	•	•	•	•	•	•	•	•				•
331	330 pF	•	•	•	•	•	•	•	•	•	•				•
391	390 pF	•	•	•	•	•	•	•	•	•	•				•
471	470 pF	•	•	•	•	•	•	•	•	•	•				•
561	560 pF	•	•	•	•	•	•	•	•	•	•				•
681	680 pF	•	•	•	•	•	•	•	•	•	•				•
821	820 pF	•	•	•	•	•	•	•	•	•	•				•
102	1.0 nF	•	•	•	•	•	•	•	•	•	•	•	•	•	•
122	1.2 nF	•	•	•	•		•	•	•	•	•	•	•	•	•
152	1.5 nF	•	•	•	•		•	•	•	•	•	•	•	•	•
182	1.8 nF	•	•	•	•		•	•	•	•	•	•	•	•	•
222	2.2 nF	•	•	•			•	•	•	•	•	•	•	•	•
272	2.7 nF	•	•	•			•	•	•	•		•	•	•	•
332	3.3 nF	•	•	•			•	•	•	•		•	•	•	•
392	3.9 nF	•	•	•			•	•	•	•		•	•	•	•
472	4.7 nF	•	•	•			•	•	•	•		•	•	•	•
562	5.6 nF	•	•	•			•	•	•	•		•	•	•	•
682	6.8 nF	•	•	•			•	•	•	•		•	•	•	•
822	8.2 nF	•	•				•	•	•	•		•	•	•	•
103	10 nF	•					•	•	•	•		•	•	•	•
123	12 nF						•	•	•			•	•	•	
153	15 nF						•	•				•	•	•	
183	18 nF						•					•	•	•	
223	22 nF						•					•	•	•	
273	27 nF											•	•	•	
333	33 nF											•	•		
393	39 nF											•			
473	47 nF														
563	56 nF														

Notes

RoHS-compliant

• Plastic tape

(1) See soldering recommendations within this data book, or visit www.vishay.com/doc?45034

SELECTION CHART

DIELECTRIC		C0G (NP0)										
STYLE		VJ2220 (1)						VJ2225 (1)				
CASE CODE		2220						2225				
VOLTAGE (V_{DC})		50	100	200	500	630	1000	50	100	200	500	1000
VOLTAGE CODE		A	B	C	E	L	G	A	B	C	E	G
CAP. CODE	CAP.											
1R0	1.0 pF											
1R2	1.2 pF											
1R5	1.5 pF											
1R8	1.8 pF											
2R2	2.2 pF											
2R7	2.7 pF											
3R3	3.3 pF											
3R9	3.9 pF											
4R7	4.7 pF											
5R6	5.6 pF											
6R8	6.8 pF											
8R2	8.2 pF											
100	10 pF											
120	12 pF											
150	15 pF											
180	18 pF											
220	22 pF											
270	27 pF											
330	33 pF											
390	39 pF											
470	47 pF											
560	56 pF											
680	68 pF											
820	82 pF											
101	100 pF											
121	120 pF											
151	150 pF											
181	180 pF											
221	220 pF											
271	270 pF	•	•	•	•	•	•					•
331	330 pF	•	•	•	•	•	•					•
391	390 pF	•	•	•	•	•	•					•
471	470 pF	•	•	•	•	•	•				•	•
561	560 pF	•	•	•	•	•	•				•	•
681	680 pF	•	•	•	•	•	•				•	•
821	820 pF	•	•	•	•	•	•				•	•
102	1.0 nF	•	•	•	•	•	•			•	•	•
122	1.2 nF	•	•	•	•	•	•	•	•	•	•	•
152	1.5 nF	•	•	•	•	•	•	•	•	•	•	•
182	1.8 nF	•	•	•	•	•	•	•	•	•	•	•
222	2.2 nF	•	•	•	•	•	•	•	•	•	•	•
272	2.7 nF	•	•	•	•	•	•	•	•	•	•	•
332	3.3 nF	•	•	•	•	•	•	•	•	•	•	•
392	3.9 nF	•	•	•	•	•	•	•	•	•	•	•
472	4.7 nF	•	•	•	•	•	•	•	•	•	•	
562	5.6 nF	•	•	•	•	•		•	•	•	•	
682	6.8 nF	•	•	•				•	•	•	•	
822	8.2 nF	•	•	•				•	•	•	•	
103	10 nF	•	•	•				•	•	•	•	
123	12 nF	•	•	•				•	•	•	•	
153	15 nF	•	•	•				•	•	•		
183	18 nF	•	•					•	•	•		
223	22 nF	•	•					•	•	•		
273	27 nF	•	•					•	•	•		
333	33 nF	•	•					•	•	•		
393	39 nF	•						•	•	•		
473	47 nF	•						•	•			
563	56 nF							•				

Notes

RoHS-compliant

• Plastic tape

(1) See soldering recommendations within this data book, or visit www.vishay.com/doc?45034

SELECTION CHART

DIELECTRIC		X7R															
STYLE		VJ0402				VJ0603					VJ0805						
CASE CODE		0402				0603					0805						
VOLTAGE (V_{DC})		16	25	50	100	16	25	50	100	200	16	25	50	100	200	250
VOLTAGE CODE		J	X	A	B	J	X	A	B	C	J	X	A	B	C	P
CAP. CODE	CAP.															
121	120 pF	••	••	••	••											
151	150 pF	••	••	••	••											
181	180 pF	••	••	••	••											
221	220 pF	••	••	••	••											
271	270 pF	••	••	••	••											
331	330 pF	••	••	••	••			••	••	••					••	
391	390 pF	••	••	••	••	••	••	••	••	••					••	
471	470 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	
561	560 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	
681	680 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	
821	820 pF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	
102	1.0 nF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••
122	1.2 nF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••
152	1.5 nF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••
182	1.8 nF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••
222	2.2 nF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••
272	2.7 nF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••
332	3.3 nF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••
392	3.9 nF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••
472	4.7 nF	••	••	••	••	••	••	••	••	••	••	••	••	••	••	••
562	5.6 nF	••	••	••		••	••	••	••		••	••	••	••	••	••
682	6.8 nF	••	••	••		••	••	••	••		••	••	••	••	••	••
822	8.2 nF	••	••	••		••	••	••	••		••	••	••	••	••	••
103	10 nF	••	••	••		••	••	••	••		••	••	••	••	••	•
123	12 nF	••	••			••	••	••	••		••	••	••	••	••	•
153	15 nF	••	••			••	••	••	••		••	••	••	••	•	•
183	18 nF	••	••			••	••	••	••		••	••	••	••	•	•
223	22 nF	••				••	••	••	••		••	••	••	••	•	•
273	27 nF	••				••	••	••	••		••	••	••	••	•	
333	33 nF	••				••	••	••	••		••	••	••	•		
393	39 nF	••				••	••	••	••		••	••	••	•		
473	47 nF	••				••	••	••			••	••	••	•		
563	56 nF					••	••	••			••	••	••	•		
683	68 nF					••	••	••			••	••	•	•		
823	82 nF					••	••	••			••	••	•	•		
104	100 nF					••	••	••			••	••	•	•		
124	120 nF					••					••	••	•			
154	150 nF					••					•	•	•			
184	180 nF										•	•				
224	220 nF										•	•				
274	270 nF										•	•				
334	330 nF										•	•				
394	390 nF										•					
474	470 nF										•					
564	560 nF															
684	680 nF															
824	820 nF															
105	1.0 µF															
125	1.2 µF															
155	1.5 µF															
185	1.8 µF															
225	2.2 µF															
275	2.7 µF															
335	3.3 µF															
395	3.9 µF															
475	4.7 µF															
565	5.6 µF															
685	6.8 µF															

Notes

RoHS-compliant

•• Paper tape • Plastic tape

SELECTION CHART

DIELECTRIC		X7R															
STYLE		VJ1206 (1)								VJ1210 (1)							
CASE CODE		1206								1210							
VOLTAGE (V_{DC})		16	25	50	100	200	250	500	630	16	25	50	100	200	250	500	630
VOLTAGE CODE		J	X	A	B	C	P	E	L	J	X	A	B	C	P	E	L
CAP. CODE	CAP.																
121	120 pF																
151	150 pF																
181	180 pF																
221	220 pF																
271	270 pF																
331	330 pF							••	••								
391	390 pF							••	••								•
471	470 pF		••	••	••	••		••	••								•
561	560 pF		••	••	••	••		••	••								•
681	680 pF		••	••	••	••		••	••								•
821	820 pF		••	••	••	••		••	••								•
102	1.0 nF	••	••	••	••	••		••	••							•	•
122	1.2 nF	••	••	••	••	••		••	••							•	•
152	1.5 nF	••	••	••	••	••		••	••							•	•
182	1.8 nF	••	••	••	••	••		••	••							•	•
222	2.2 nF	••	••	••	••	••		••	••							•	•
272	2.7 nF	••	••	••	••	••		••	••							•	•
332	3.3 nF	••	••	••	••	••		••	••					•		•	•
392	3.9 nF	••	••	••	••	••		••	••					•		•	•
472	4.7 nF	••	••	••	••	••		••	••					•		•	•
562	5.6 nF	••	••	••	••	••		•	•					•		•	•
682	6.8 nF	••	••	••	••	••		•	•					•		•	•
822	8.2 nF	••	••	••	••	••		•	•					•		•	•
103	10 nF	••	••	••	••	••	•	•	•	•	•	•	•	•		•	•
123	12 nF	••	••	••	••	••	•	•	•	•	•	•	•	•		•	•
153	15 nF	••	••	••	••	••	•	•	•	•	•	•	•	•		•	•
183	18 nF	••	••	••	••	••	•	•	•	•	•	•	•	•		•	•
223	22 nF	••	••	••	••	••	•			•	•	•	•	•		•	•
273	27 nF	••	••	••	••	••	•			•	•	•	•	•		•	•
333	33 nF	••	••	••	••	••	•			•	•	•	•	•	•	•	•
393	39 nF	••	••	••	••	•	•			•	•	•	•	•	•	•	•
473	47 nF	••	••	••	••	•	•			•	•	•	•	•	•	•	•
563	56 nF	••	••	••	••	•	•			•	•	•	•	•	•		
683	68 nF	••	••	••	••	•	•			•	•	•	•	•	•		
823	82 nF	••	••	•	•	•	•			•	•	•	•	•	•		
104	100 nF	••	••	•	•	•	•			•	•	•	•	•	•		
124	120 nF	••	••	•	•					•	•	•	•	•			
154	150 nF	••	••	•	•					•	•	•	•	•			
184	180 nF	••	••	•	•					•	•	•	•	•			
224	220 nF	•	•	•	•					•	•	•	•				
274	270 nF	•	•	•	•					•	•	•	•				
334	330 nF	•	•	•						•	•	•	•				
394	390 nF	•	•	•						•	•	•	•				
474	470 nF	•	•	•						•	•	•	•				
564	560 nF	•	•							•	•	•					
684	680 nF	•	•							•	•	•					
824	820 nF	•	•							•	•	•					
105	1.0 µF	•	•							•	•	•					
125	1.2 µF																
155	1.5 µF																
185	1.8 µF																
225	2.2 µF																
275	2.7 µF																
335	3.3 µF																
395	3.9 µF																
475	4.7 µF																
565	5.6 µF																
685	6.8 µF																

Notes

RoHS-compliant

•• Paper tape • Plastic tape

(1) See soldering recommendations within this data book, or visit www.vishay.com/doc?45034

SELECTION CHART

DIELECTRIC		X7R																		
STYLE		VJ1808 (1)					VJ1812 (1)								VJ1825 (1)						
CASE CODE		1808					1812								1825						
VOLTAGE (V_{DC})		50	100	200	500	1000	25	50	100	200	250	500	630	1000	25	50	100	200	250	500	1000
VOLTAGE CODE		A	B	C	E	G	X	A	B	C	P	E	L	G	X	A	B	C	P	E	G
CAP. CODE	CAP.																				
121	120 pF																				
151	150 pF																				
181	180 pF																				
221	220 pF																				
271	270 pF																				
331	330 pF																				
391	390 pF																				
471	470 pF					•															
561	560 pF					•															
681	680 pF					•															
821	820 pF					•															
102	1.0 nF				•	•						•	•	•							
122	1.2 nF				•	•						•	•	•							
152	1.5 nF				•	•						•	•	•							
182	1.8 nF				•	•						•	•	•							
222	2.2 nF				•	•						•	•	•							
272	2.7 nF				•	•						•	•	•							
332	3.3 nF				•	•						•	•	•							
392	3.9 nF				•	•						•	•	•							
472	4.7 nF			•	•	•						•	•	•							
562	5.6 nF			•	•	•						•	•	•							
682	6.8 nF			•	•	•						•	•	•							
822	8.2 nF			•	•	•						•	•	•							
103	10 nF	•	•	•	•	•				•		•	•	•	•	•	•	•	•	•	•
123	12 nF	•	•	•	•					•		•	•	•	•	•	•	•	•	•	•
153	15 nF	•	•	•	•					•		•	•	•	•	•	•	•	•	•	•
183	18 nF	•	•	•	•					•		•	•	•	•	•	•	•	•	•	•
223	22 nF	•	•	•	•		•	•	•	•		•	•	•	•	•	•	•	•	•	•
273	27 nF	•	•	•	•		•	•	•	•		•	•	•	•	•	•	•	•	•	•
333	33 nF	•	•	•			•	•	•	•		•	•		•	•	•	•	•	•	•
393	39 nF	•	•	•			•	•	•	•		•	•		•	•	•	•	•	•	•
473	47 nF	•	•	•			•	•	•	•		•	•		•	•	•	•	•	•	•
563	56 nF	•	•	•			•	•	•	•		•	•		•	•	•	•	•	•	•
683	68 nF	•	•	•			•	•	•	•		•	•		•	•	•	•	•	•	
823	82 nF	•	•	•			•	•	•	•		•	•		•	•	•	•	•	•	
104	100 nF	•	•	•			•	•	•	•	•	•	•		•	•	•	•	•	•	
124	120 nF	•	•				•	•	•	•	•				•	•	•	•	•	•	
154	150 nF	•	•				•	•	•	•	•				•	•	•	•	•	•	
184	180 nF	•	•				•	•	•	•	•				•	•	•	•	•	•	
224	220 nF	•					•	•	•	•	•				•	•	•	•	•		
274	270 nF	•					•	•	•	•	•				•	•	•	•	•		
334	330 nF						•	•	•	•	•				•	•	•	•	•		
394	390 nF						•	•	•	•					•	•	•	•	•		
474	470 nF						•	•	•	•					•	•	•	•	•		
564	560 nF						•	•	•						•	•	•	•	•		
684	680 nF						•	•	•						•	•	•	•	•		
824	820 nF						•	•	•						•	•	•	•	•		
105	1.0 µF						•	•							•	•	•	•	•		
125	1.2 µF														•	•	•				
155	1.5 µF														•	•	•				
185	1.8 µF														•	•					
225	2.2 µF														•						
275	2.7 µF														•						
335	3.3 µF																				
395	3.9 µF																				
475	4.7 µF																				
565	5.6 µF																				
685	6.8 µF																				

Notes

RoHS-compliant

• Plastic tape

(1) See soldering recommendations within this data book, or visit www.vishay.com/doc?45034

SELECTION CHART

DIELECTRIC		X7R														
STYLE		VJ2220 (1)				VJ2225 (1)						VJ3640 (1)				
CASE CODE		2220				2225						3640				
VOLTAGE (V_{DC})		50	100	200	500	25	50	100	200	500	1000	25	50	100	200	500
VOLTAGE CODE		A	B	C	E	X	A	B	C	E	G	X	A	B	C	E
CAP. CODE	CAP.															
121	120 pF															
151	150 pF															
181	180 pF															
221	220 pF															
271	270 pF															
331	330 pF															
391	390 pF															
471	470 pF															
561	560 pF															
681	680 pF															
821	820 pF															
102	1.0 nF															
122	1.2 nF															
152	1.5 nF															
182	1.8 nF															
222	2.2 nF															
272	2.7 nF															
332	3.3 nF															
392	3.9 nF															
472	4.7 nF															
562	5.6 nF															
682	6.8 nF															
822	8.2 nF															
103	10 nF															
123	12 nF															
153	15 nF				•											
183	18 nF				•											
223	22 nF				•											
273	27 nF				•										•	•
333	33 nF				•	•	•	•	•	•	•				•	•
393	39 nF				•	•	•	•	•	•	•				•	•
473	47 nF				•	•	•	•	•	•	•				•	•
563	56 nF				•	•	•	•	•	•	•				•	•
683	68 nF				•	•	•	•	•	•	•				•	•
823	82 nF				•	•	•	•	•	•	•				•	•
104	100 nF			•	•	•	•	•	•	•	•				•	•
124	120 nF			•	•	•	•	•	•	•					•	•
154	150 nF			•	•	•	•	•	•	•					•	•
184	180 nF			•	•	•	•	•	•	•		•	•	•	•	•
224	220 nF		•	•	•	•	•	•	•	•		•	•	•	•	•
274	270 nF	•	•	•		•	•	•	•	•		•	•	•	•	•
334	330 nF	•	•	•		•	•	•	•	•		•	•	•	•	•
394	390 nF	•	•	•		•	•	•	•			•	•	•	•	•
474	470 nF	•	•	•		•	•	•	•			•	•	•	•	•
564	560 nF	•	•	•		•	•	•	•			•	•	•	•	•
684	680 nF	•	•	•		•	•	•	•			•	•	•	•	•
824	820 nF	•	•	•		•	•	•	•			•	•	•	•	
105	1.0 µF	•	•	•		•	•	•	•			•	•	•	•	
125	1.2 µF	•	•			•	•	•	•			•	•	•	•	
155	1.5 µF	•				•	•	•				•	•	•	•	
185	1.8 µF	•				•	•	•				•	•	•	•	
225	2.2 µF	•				•	•					•	•	•		
275	2.7 µF					•	•					•	•	•		
335	3.3 µF					•						•	•	•		
395	3.9 µF					•						•	•	•		
475	4.7 µF					•						•	•			
565	5.6 µF											•				
685	6.8 µF											•				

Notes

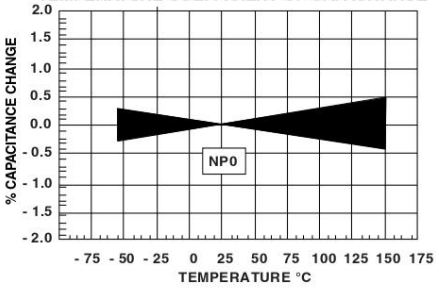
RoHS-compliant

• Plastic tape

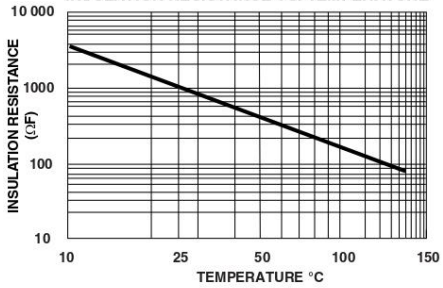
(1) See soldering recommendations within this data book, or visit www.vishay.com/doc?45034

C0G (NP0) DIELECTRIC - TYPICAL PARAMETERS

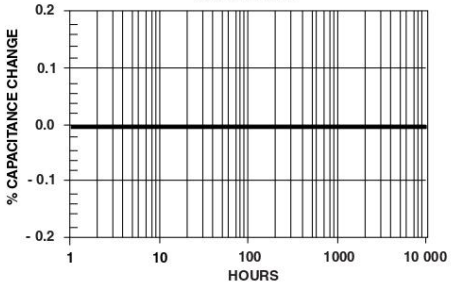
TEMPERATURE COEFFICIENT OF CAPACITANCE



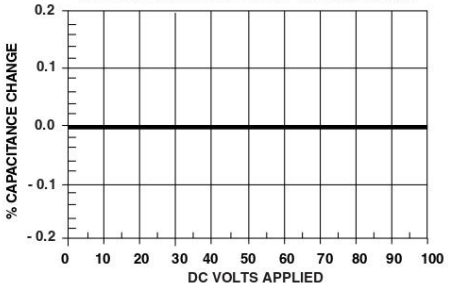
INSULATION RESISTANCE VS. TEMPERATURE



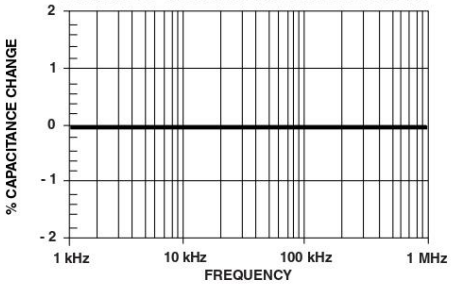
AGING RATE



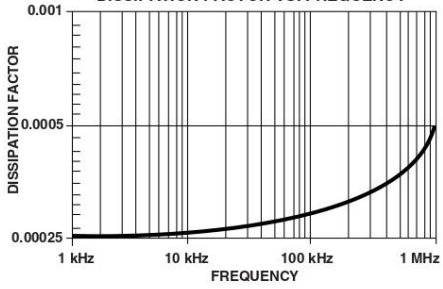
VOLTAGE COEFFICIENT OF CAPACITANCE



CHANGE OF CAPACITANCE WITH FREQUENCY

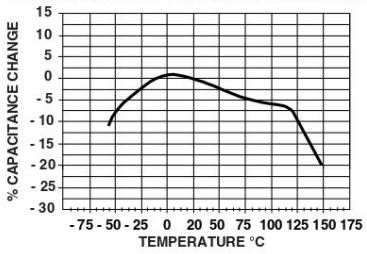


DISSIPATION FACTOR VS. FREQUENCY

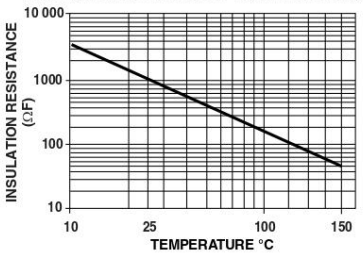


X7R DIELECTRIC - TYPICAL PARAMETERS

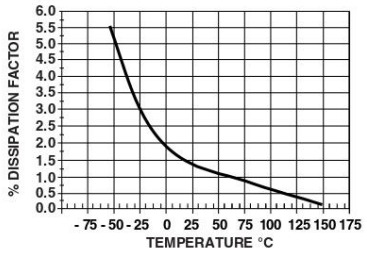
TEMPERATURE COEFFICIENT OF CAPACITANCE



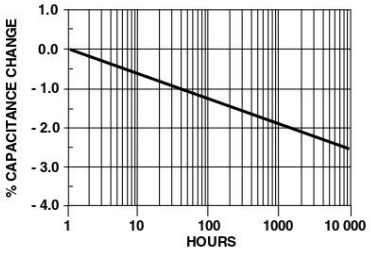
INSULATION RESISTANCE VS. TEMPERATURE



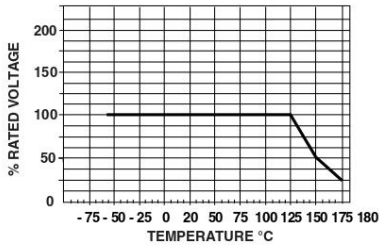
DISSIPATION FACTOR VS. TEMPERATURE



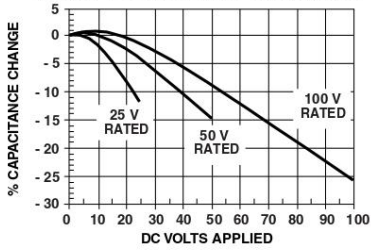
AGING RATE



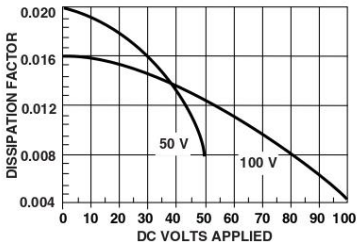
RATED VOLTAGE VS. TEMPERATURE



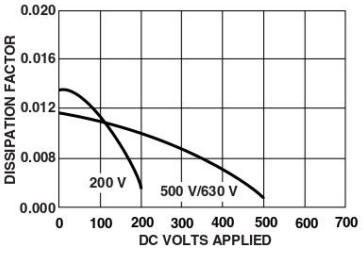
VOLTAGE COEFFICIENT OF CAPACITANCE



DISSIPATION FACTOR VS. VOLTAGE



DISSIPATION FACTOR VS. VOLTAGE



STANDARD PACKAGING QUANTITIES (1)(2)(3)

CASE CODE	TAPE SIZE	7" REEL QUANTITIES		11 1/4" AND 13" REEL QUANTITIES	
		PAPER TAPE PACKAGING CODE "C" / "O"	PLASTIC TAPE PACKAGING CODE "T"	PAPER TAPE PACKAGING CODE "P" / "I"	PLASTIC TAPE PACKAGING CODE "R"
0402	8 mm	5000	n/a	10 000	n/a
0603 (4)	8 mm	4000	4000	10 000	10 000
0805 (4)	8 mm	3000	3000	10 000	10 000
1206 (4)	8 mm	3000	2500 / 3000	10 000	9000 / 10 000
1210 (4)	8 mm	n/a	2000 / 2500 / 3000	n/a	9000 / 10 000
1808	12 mm	n/a	2000	n/a	10 000
1812	12 mm	n/a	1000	n/a	4000
1825	12 mm	n/a	1000	n/a	4000
2220	12 mm	n/a	1000	n/a	4000
2225	12 mm	n/a	1000	n/a	4000
3640	16 mm	n/a	500	n/a	n/a

Notes

(1) Vishay Vitramon uses embossed plastic carrier tape
(2) REFERENCE: EIA standard RS 481 - "Taping of Surface Mount Components for Automatic Placement"
(3) n/a = not available
(4) Packaging "C" / "P" / "O" / "I" and "T" / "R" or lower quantities can depend from product thickness

STORAGE AND HANDLING CONDITIONS

(1) Store the components at 5 °C to 40 °C ambient temperature and ≤ 70 % relative humidity conditions.
(2) The product is recommended to be used within a time-frame of 2 years after shipment.
Check solderability in case extended shelf life beyond the expiry date is needed.

Precautions:

a. Do not store products in an environment containing corrosive elements, especially where chloride gas, sulfide gas, acid, alkali, salt or the like are present. This may cause corrosion or oxidization of the terminations, which can easily lead to poor soldering.
b. Store products on the shelf and avoid exposure to moisture or dust.
c. Do not expose products to excessive shock, vibration, direct sunlight and so on.

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Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

2. Conectores.

42375

ENG. NO: A-42375-0002/0036	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABA154
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-4020	A-42375-0002	20	22-28-4200	A-42375-0020
03	22-28-4030	A-42375-0003	21	22-28-4210	A-42375-0021
04	22-28-4040	A-42375-0004	22	22-28-4220	A-42375-0022
05	22-28-4050	A-42375-0005	23	22-28-4230	A-42375-0023
06	22-28-4060	A-42375-0006	24	22-28-4240	A-42375-0024
07	22-28-4070	A-42375-0007	25	22-28-4250	A-42375-0025
08	22-28-4080	A-42375-0008	26	22-28-4260	A-42375-0026
09	22-28-4090	A-42375-0009	27	22-28-4270	A-42375-0027
10	22-28-4100	A-42375-0010	28	22-28-4280	A-42375-0028
11	22-28-4110	A-42375-0011	29	22-28-4290	A-42375-0029
12	22-28-4120	A-42375-0012	30	22-28-4300	A-42375-0030
13	22-28-4130	A-42375-0013	31	22-28-4310	A-42375-0031
14	22-28-4140	A-42375-0014	32	22-28-4320	A-42375-0032
15	22-28-4150	A-42375-0015	33	22-28-4330	A-42375-0033
16	22-28-4160	A-42375-0016	34	22-28-4340	A-42375-0034
17	22-28-4170	A-42375-0017	35	22-28-4350	A-42375-0035
18	22-28-4180	A-42375-0018	36	22-28-4360	A-42375-0036
19	22-28-4190	A-42375-0019			

ENG. NO: A-42375-0037/0071	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABB208
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	.100 / 2.54
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	.100 / 2.54
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-4023	A-42375-0037	20	22-28-4203	A-42375-0055
03	22-28-4033	A-42375-0038	21	22-28-4213	A-42375-0056
04	22-28-4043	A-42375-0039	22	22-28-4223	A-42375-0057
05	22-28-4053	A-42375-0040	23	22-28-4233	A-42375-0058
06	22-28-4063	A-42375-0041	24	22-28-4243	A-42375-0059
07	22-28-4073	A-42375-0042	25	22-28-4253	A-42375-0060
08	22-28-4083	A-42375-0043	26	22-28-4263	A-42375-0061
09	22-28-4093	A-42375-0044	27	22-28-4273	A-42375-0062
10	22-28-4103	A-42375-0045	28	22-28-4283	A-42375-0063
11	22-28-4113	A-42375-0046	29	22-28-4293	A-42375-0064
12	22-28-4123	A-42375-0047	30	22-28-4303	A-42375-0065
13	22-28-4133	A-42375-0048	31	22-28-4313	A-42375-0066
14	22-28-4143	A-42375-0049	32	22-28-4323	A-42375-0067
15	22-28-4153	A-42375-0050	33	22-28-4233	A-42375-0068
16	22-28-4163	A-42375-0051	34	22-28-4343	A-42375-0069
17	22-28-4173	A-42375-0052	35	22-28-4353	A-42375-0070
18	22-28-4183	A-42375-0053	36	22-28-4363	A-42375-0071
19	22-28-4193	A-42375-0054			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 2 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V 1).DOC

42375

ENG. NO: A-42375-0002/0036

HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABA154
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-4020	A-42375-0002	20	22-28-4200	A-42375-0020
03	22-28-4030	A-42375-0003	21	22-28-4210	A-42375-0021
04	22-28-4040	A-42375-0004	22	22-28-4220	A-42375-0022
05	22-28-4050	A-42375-0005	23	22-28-4230	A-42375-0023
06	22-28-4060	A-42375-0006	24	22-28-4240	A-42375-0024
07	22-28-4070	A-42375-0007	25	22-28-4250	A-42375-0025
08	22-28-4080	A-42375-0008	26	22-28-4260	A-42375-0026
09	22-28-4090	A-42375-0009	27	22-28-4270	A-42375-0027
10	22-28-4100	A-42375-0010	28	22-28-4280	A-42375-0028
11	22-28-4110	A-42375-0011	29	22-28-4290	A-42375-0029
12	22-28-4120	A-42375-0012	30	22-28-4300	A-42375-0030
13	22-28-4130	A-42375-0013	31	22-28-4310	A-42375-0031
14	22-28-4140	A-42375-0014	32	22-28-4320	A-42375-0032
15	22-28-4150	A-42375-0015	33	22-28-4330	A-42375-0033
16	22-28-4160	A-42375-0016	34	22-28-4340	A-42375-0034
17	22-28-4170	A-42375-0017	35	22-28-4350	A-42375-0035
18	22-28-4180	A-42375-0018	36	22-28-4360	A-42375-0036
19	22-28-4190	A-42375-0019			

ENG. NO: A-42375-0037/0071

HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABB208
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	.100 / 2.54
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	.100 / 2.54
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-4023	A-42375-0037	20	22-28-4203	A-42375-0055
03	22-28-4033	A-42375-0038	21	22-28-4213	A-42375-0056
04	22-28-4043	A-42375-0039	22	22-28-4223	A-42375-0057
05	22-28-4053	A-42375-0040	23	22-28-4233	A-42375-0058
06	22-28-4063	A-42375-0041	24	22-28-4243	A-42375-0059
07	22-28-4073	A-42375-0042	25	22-28-4253	A-42375-0060
08	22-28-4083	A-42375-0043	26	22-28-4263	A-42375-0061
09	22-28-4093	A-42375-0044	27	22-28-4273	A-42375-0062
10	22-28-4103	A-42375-0045	28	22-28-4283	A-42375-0063
11	22-28-4113	A-42375-0046	29	22-28-4293	A-42375-0064
12	22-28-4123	A-42375-0047	30	22-28-4303	A-42375-0065
13	22-28-4133	A-42375-0048	31	22-28-4313	A-42375-0066
14	22-28-4143	A-42375-0049	32	22-28-4323	A-42375-0067
15	22-28-4153	A-42375-0050	33	22-28-4233	A-42375-0068
16	22-28-4163	A-42375-0051	34	22-28-4343	A-42375-0069
17	22-28-4173	A-42375-0052	35	22-28-4353	A-42375-0070
18	22-28-4183	A-42375-0053	36	22-28-4363	A-42375-0071
19	22-28-4193	A-42375-0054			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 2 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V 1).DOC

42375

ENG. NO: A-42375-0072/0106	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABB228
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	.100 / 2.54
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	.100 / 2.54
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-4026	A-42375-0072	20	22-28-4206	A-42375-0090
03	22-28-4036	A-42375-0073	21	22-28-4216	A-42375-0091
04	22-28-4046	A-42375-0074	22	22-28-4226	A-42375-0092
05	22-28-4056	A-42375-0075	23	22-28-4236	A-42375-0093
06	22-28-4066	A-42375-0076	24	22-28-4246	A-42375-0094
07	22-28-4076	A-42375-0077	25	22-28-4256	A-42375-0095
08	22-28-4086	A-42375-0078	26	22-28-4266	A-42375-0096
09	22-28-4096	A-42375-0079	27	22-28-4276	A-42375-0097
10	22-28-4106	A-42375-0080	28	22-28-4286	A-42375-0098
11	22-28-4116	A-42375-0081	29	22-28-4296	A-42375-0099
12	22-28-4126	A-42375-0082	30	22-28-4306	A-42375-0100
13	22-28-4136	A-42375-0083	31	22-28-4316	A-42375-0101
14	22-28-4146	A-42375-0084	32	22-28-4326	A-42375-0102
15	22-28-4156	A-42375-0085	33	22-28-4336	A-42375-0103
16	22-28-4166	A-42375-0086	34	22-28-4346	A-42375-0104
17	22-28-4176	A-42375-0087	35	22-28-4356	A-42375-0105
18	22-28-4186	A-42375-0088	36	22-28-4366	A-42375-0106
19	22-28-4196	A-42375-0089			

ENG. NO: A-42375-0107/0141	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ATA154
PIN LENGTH: L	.530 / 13.46
MATING LENGTH: M	.320 / 8.13
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.120 / 3.05
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-4021	A-42375-0107	20	22-28-4201	A-42375-0125
03	22-28-4031	A-42375-0108	21	22-28-4211	A-42375-0126
04	22-28-4041	A-42375-0109	22	22-28-4221	A-42375-0127
05	22-28-4051	A-42375-0110	23	22-28-4231	A-42375-0128
06	22-28-4061	A-42375-0111	24	22-28-4241	A-42375-0129
07	22-28-4071	A-42375-0112	25	22-28-4251	A-42375-0130
08	22-28-4081	A-42375-0113	26	22-28-4261	A-42375-0131
09	22-28-4091	A-42375-0114	27	22-28-4271	A-42375-0132
10	22-28-4101	A-42375-0115	28	22-28-4281	A-42375-0133
11	22-28-4111	A-42375-0116	29	22-28-4291	A-42375-0134
12	22-28-4121	A-42375-0117	30	22-28-4301	A-42375-0135
13	22-28-4131	A-42375-0118	31	22-28-4311	A-42375-0136
14	22-28-4141	A-42375-0119	32	22-28-4321	A-42375-0137
15	22-28-4151	A-42375-0120	33	22-28-4331	A-42375-0138
16	22-28-4161	A-42375-0121	34	22-28-4341	A-42375-0139
17	22-28-4171	A-42375-0122	35	22-28-4351	A-42375-0140
18	22-28-4181	A-42375-0123	36	22-28-4361	A-42375-0141
19	22-28-4191	A-42375-0124			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 3 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: A-42375-0142/0176	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ATB208
PIN LENGTH: L	.530 / 13.46
MATING LENGTH: M	.320 / 8.13
GOLD POINT: G	.140 / 3.56
PC TAIL LENGTH: P	.120 / 3.05
TIN: T	.135 / 3.43
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-4024	A-42375-0142	20	22-28-4204	A-42375-0160
03	22-28-4034	A-42375-0143	21	22-28-4214	A-42375-0161
04	22-28-4044	A-42375-0144	22	22-28-4224	A-42375-0162
05	22-28-4054	A-42375-0145	23	22-28-4234	A-42375-0163
06	22-28-4064	A-42375-0146	24	22-28-4244	A-42375-0164
07	22-28-4074	A-42375-0147	25	22-28-4254	A-42375-0165
08	22-28-4084	A-42375-0148	26	22-28-4264	A-42375-0166
09	22-28-4094	A-42375-0149	27	22-28-4274	A-42375-0167
10	22-28-4104	A-42375-0150	28	22-28-4284	A-42375-0168
11	22-28-4114	A-42375-0151	29	22-28-4294	A-42375-0169
12	22-28-4124	A-42375-0152	30	22-28-4304	A-42375-0170
13	22-28-4134	A-42375-0153	31	22-28-4314	A-42375-0171
14	22-28-4144	A-42375-0154	32	22-28-4324	A-42375-0172
15	22-28-4154	A-42375-0155	33	22-28-4334	A-42375-0173
16	22-28-4164	A-42375-0156	34	22-28-4344	A-42375-0174
17	22-28-4174	A-42375-0157	35	22-28-4354	A-42375-0175
18	22-28-4184	A-42375-0158	36	22-28-4364	A-42375-0176
19	22-28-4194	A-42375-0159			

ENG. NO: A-42375-0177/0211	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ATB228
PIN LENGTH: L	.530 / 13.46
MATING LENGTH: M	.320 / 8.13
GOLD POINT: G	.140 / 3.56
PC TAIL LENGTH: P	.120 / 3.05
TIN: T	.135 / 3.43
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-4027	A-42375-0177	20	22-28-4207	A-42375-0195
03	22-28-4037	A-42375-0178	21	22-28-4217	A-42375-0196
04	22-28-4047	A-42375-0179	22	22-28-4227	A-42375-0197
05	22-28-4057	A-42375-0180	23	22-28-4237	A-42375-0198
06	22-28-4067	A-42375-0181	24	22-28-4247	A-42375-0199
07	22-28-4077	A-42375-0182	25	22-28-4257	A-42375-0200
08	22-28-4087	A-42375-0183	26	22-28-4267	A-42375-0201
09	22-28-4097	A-42375-0184	27	22-28-4277	A-42375-0202
10	22-28-4107	A-42375-0185	28	22-28-4287	A-42375-0203
11	22-28-4117	A-42375-0186	29	22-28-4297	A-42375-0204
12	22-28-4127	A-42375-0187	30	22-28-4307	A-42375-0205
13	22-28-4137	A-42375-0188	31	22-28-4317	A-42375-0206
14	22-28-4147	A-42375-0189	32	22-28-4327	A-42375-0207
15	22-28-4157	A-42375-0190	33	22-28-4337	A-42375-0208
16	22-28-4167	A-42375-0191	34	22-28-4347	A-42375-0209
17	22-28-4177	A-42375-0192	35	22-28-4357	A-42375-0210
18	22-28-4187	A-42375-0193	36	22-28-4367	A-42375-0211
19	22-28-4197	A-42375-0194			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 4 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: A-42375-0212/0246	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AMA154
PIN LENGTH: L	.505 / 12.83
MATING LENGTH: M	.295 / 7.49
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.120 / 3.05
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-4022	A-42375-0212	20	22-28-4202	A-42375-0230
03	22-28-4032	A-42375-0213	21	22-28-4212	A-42375-0231
04	22-28-4042	A-42375-0214	22	22-28-4222	A-42375-0232
05	22-28-4052	A-42375-0215	23	22-28-4232	A-42375-0233
06	22-28-4062	A-42375-0216	24	22-28-4242	A-42375-0234
07	22-28-4072	A-42375-0217	25	22-28-4252	A-42375-0235
08	22-28-4082	A-42375-0218	26	22-28-4262	A-42375-0236
09	22-28-4092	A-42375-0219	27	22-28-4272	A-42375-0237
10	22-28-4102	A-42375-0220	28	22-28-4282	A-42375-0238
11	22-28-4112	A-42375-0221	29	22-28-4292	A-42375-0239
12	22-28-4122	A-42375-0222	30	22-28-4302	A-42375-0240
13	22-28-4132	A-42375-0223	31	22-28-4312	A-42375-0241
14	22-28-4142	A-42375-0224	32	22-28-4322	A-42375-0242
15	22-28-4152	A-42375-0225	33	22-28-4332	A-42375-0243
16	22-28-4162	A-42375-0226	34	22-28-4342	A-42375-0244
17	22-28-4172	A-42375-0227	35	22-28-4352	A-42375-0245
18	22-28-4182	A-42375-0228	36	22-28-4362	A-42375-0246
19	22-28-4192	A-42375-0229			

ENG. NO: A-42375-0247/0281	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AMB208
PIN LENGTH: L	.505 / 12.83
MATING LENGTH: M	.295 / 7.49
GOLD POINT: G	.140 / 3.56
PC TAIL LENGTH: P	.120 / 3.05
TIN: T	.135 / 3.43
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-4025	A-42375-0247	20	22-28-4205	A-42375-0265
03	22-28-4035	A-42375-0248	21	22-28-4215	A-42375-0266
04	22-28-4045	A-42375-0249	22	22-28-4225	A-42375-0267
05	22-28-4055	A-42375-0250	23	22-28-4235	A-42375-0268
06	22-28-4065	A-42375-0251	24	22-28-4245	A-42375-0269
07	22-28-4075	A-42375-0252	25	22-28-4255	A-42375-0270
08	22-28-4085	A-42375-0253	26	22-28-4265	A-42375-0271
09	22-28-4095	A-42375-0254	27	22-28-4275	A-42375-0272
10	22-28-4105	A-42375-0255	28	22-28-4285	A-42375-0273
11	22-28-4115	A-42375-0256	29	22-28-4295	A-42375-0274
12	22-28-4125	A-42375-0257	30	22-28-4305	A-42375-0275
13	22-28-4135	A-42375-0258	31	22-28-4315	A-42375-0276
14	22-28-4145	A-42375-0259	32	22-28-4325	A-42375-0277
15	22-28-4155	A-42375-0260	33	22-28-4335	A-42375-0278
16	22-28-4165	A-42375-0261	34	22-28-4345	A-42375-0279
17	22-28-4175	A-42375-0262	35	22-28-4355	A-42375-0280
18	22-28-4185	A-42375-0263	36	22-28-4365	A-42375-0281
19	22-28-4195	A-42375-0264			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 5 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: A-42375-0282/0316	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AMB228
PIN LENGTH: L	.505 / 12.83
MATING LENGTH: M	.295 / 7.49
GOLD POINT: G	.140 / 3.56
PC TAIL LENGTH: P	.120 / 3.05
TIN: T	.135 / 3.43
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-4028	A-42375-0282	20	22-28-4208	A-42375-0300
03	22-28-4038	A-42375-0283	21	22-28-4218	A-42375-0301
04	22-28-4048	A-42375-0284	22	22-28-4228	A-42375-0302
05	22-28-4058	A-42375-0285	23	22-28-4238	A-42375-0303
06	22-28-4068	A-42375-0286	24	22-28-4248	A-42375-0304
07	22-28-4078	A-42375-0287	25	22-28-4258	A-42375-0305
08	22-28-4088	A-42375-0288	26	22-28-4268	A-42375-0306
09	22-28-4098	A-42375-0289	27	22-28-4278	A-42375-0307
10	22-28-4108	A-42375-0290	28	22-28-4288	A-42375-0308
11	22-28-4118	A-42375-0291	29	22-28-4298	A-42375-0309
12	22-28-4128	A-42375-0192	30	22-28-4308	A-42375-0310
13	22-28-4138	A-42375-0293	31	22-28-4318	A-42375-0311
14	22-28-4148	A-42375-0294	32	22-28-4328	A-42375-0312
15	22-28-4158	A-42375-0295	33	22-28-4338	A-42375-0313
16	22-28-4168	A-42375-0296	34	22-28-4348	A-42375-0314
17	22-28-4178	A-42375-0297	35	22-28-4358	A-42375-0315
18	22-28-4188	A-42375-0298	36	22-28-4368	A-42375-0316
19	22-28-4198	A-42375-0299			

ENG. NO: A-42375-0317/0351	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ADA154
PIN LENGTH: L	.465 / 11.81
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.135 / 3.43
TIN: T	OVERALL
CKTS:	2-36
KINKS:	SMES-42003
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-5020	A-42375-0317	20	22-28-5200	A-42375-0335
03	22-28-5030	A-42375-0318	21	22-28-5210	A-42375-0336
04	22-28-5040	A-42375-0319	22	22-28-5220	A-42375-0337
05	22-28-5050	A-42375-0320	23	22-28-5230	A-42375-0338
06	22-28-5060	A-42375-0321	24	22-28-5240	A-42375-0339
07	22-28-5070	A-42375-0322	25	22-28-5250	A-42375-0340
08	22-28-5080	A-42375-0323	26	22-28-5260	A-42375-0341
09	22-28-5090	A-42375-0324	27	22-28-5270	A-42375-0342
10	22-28-5100	A-42375-0325	28	22-28-5280	A-42375-0343
11	22-28-5110	A-42375-0326	29	22-28-5290	A-42375-0344
12	22-28-5120	A-42375-0327	30	22-28-5300	A-42375-0345
13	22-28-5130	A-42375-0328	31	22-28-5310	A-42375-0346
14	22-28-5140	A-42375-0329	32	22-28-5320	A-42375-0347
15	22-28-5150	A-42375-0330	33	22-28-5330	A-42375-0348
16	22-28-5160	A-42375-0331	34	22-28-5340	A-42375-0349
17	22-28-5170	A-42375-0332	35	22-28-5350	A-42375-0350
18	22-28-5180	A-42375-0333	36	22-28-5360	A-42375-0351
19	22-28-5190	A-42375-0334			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 6 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: A-42375-0352/0386	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ADB208
PIN LENGTH: L	.465 / 11.81
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	.100 / 2.54
PC TAIL LENGTH: P	.135 / 3.43
TIN: T	.100 / 2.54
CKTS:	2-36
KINKS:	SMES-42003
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-5023	A-42375-0352	20	22-28-5203	A-42375-0370
03	22-28-5033	A-42375-0353	21	22-28-5213	A-42375-0371
04	22-28-5043	A-42375-0354	22	22-28-5223	A-42375-0372
05	22-28-5053	A-42375-0355	23	22-28-5233	A-42375-0373
06	22-28-5063	A-42375-0356	24	22-28-5243	A-42375-0374
07	22-28-5073	A-42375-0357	25	22-28-5253	A-42375-0375
08	22-28-5083	A-42375-0358	26	22-28-5263	A-42375-0376
09	22-28-5093	A-42375-0359	27	22-28-5273	A-42375-0377
10	22-28-5103	A-42375-0360	28	22-28-5283	A-42375-0378
11	22-28-5113	A-42375-0361	29	22-28-5293	A-42375-0379
12	22-28-5123	A-42375-0362	30	22-28-5303	A-42375-0380
13	22-28-5133	A-42375-0363	31	22-28-5313	A-42375-0381
14	22-28-5143	A-42375-0364	32	22-28-5323	A-42375-0382
15	22-28-5153	A-42375-0365	33	22-28-5333	A-42375-0383
16	22-28-5163	A-42375-0366	34	22-28-5343	A-42375-0384
17	22-28-5173	A-42375-0367	35	22-28-5353	A-42375-0385
18	22-28-5183	A-42375-0368	36	22-28-5363	A-42375-0386
19	22-28-5193	A-42375-0369			

ENG. NO: A-42375-0387/0421	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ADB228
PIN LENGTH: L	.465 / 11.81
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	.100 / 2.54
PC TAIL LENGTH: P	.135 / 3.43
TIN: T	.100 / 2.54
CKTS:	2-36
KINKS:	SMES-42003
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-5026	A-42375-0387	20	22-28-5206	A-42375-0405
03	22-28-5036	A-42375-0388	21	22-28-5216	A-42375-0406
04	22-28-5046	A-42375-0389	22	22-28-5226	A-42375-0407
05	22-28-5056	A-42375-0390	23	22-28-5236	A-42375-0408
06	22-28-5066	A-42375-0391	24	22-28-5246	A-42375-0409
07	22-28-5076	A-42375-0392	25	22-28-5256	A-42375-0410
08	22-28-5086	A-42375-0393	26	22-28-5266	A-42375-0411
09	22-28-5096	A-42375-0394	27	22-28-5276	A-42375-0412
10	22-28-5106	A-42375-0395	28	22-28-5286	A-42375-0413
11	22-28-5116	A-42375-0396	29	22-28-5296	A-42375-0414
12	22-28-5126	A-42375-0397	30	22-28-5306	A-42375-0415
13	22-28-5136	A-42375-0398	31	22-28-5316	A-42375-0416
14	22-28-5146	A-42375-0399	32	22-28-5326	A-42375-0417
15	22-28-5156	A-42375-0400	33	22-28-5336	A-42375-0418
16	22-28-5166	A-42375-0401	34	22-28-5346	A-42375-0419
17	22-28-5176	A-42375-0402	35	22-28-5356	A-42375-0420
18	22-28-5186	A-42375-0403	36	22-28-5366	A-42375-0421
19	22-28-5196	A-42375-0404			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 7 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: A-42375-0422/0456	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AYA154
PIN LENGTH: L	.545 / 13.84
MATING LENGTH: M	.320 / 8.13
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.135 / 3.43
TIN: T	OVERALL
CKTS:	2-36
KINKS:	SMES-42003
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-5021	A-42375-0422	20	22-28-5201	A-42375-0440
03	22-28-5031	A-42375-0423	21	22-28-5211	A-42375-0441
04	22-28-5041	A-42375-0424	22	22-28-5221	A-42375-0442
05	22-28-5051	A-42375-0425	23	22-28-5231	A-42375-0443
06	22-28-5061	A-42375-0426	24	22-28-5241	A-42375-0444
07	22-28-5071	A-42375-0427	25	22-28-5251	A-42375-0445
08	22-28-5081	A-42375-0428	26	22-28-5261	A-42375-0446
09	22-28-5091	A-42375-0429	27	22-28-5271	A-42375-0447
10	22-28-5101	A-42375-0430	28	22-28-5281	A-42375-0448
11	22-28-5111	A-42375-0431	29	22-28-5291	A-42375-0449
12	22-28-5121	A-42375-0432	30	22-28-5301	A-42375-0450
13	22-28-5131	A-42375-0433	31	22-28-5311	A-42375-0451
14	22-28-5141	A-42375-0434	32	22-28-5321	A-42375-0452
15	22-28-5151	A-42375-0435	33	22-28-5331	A-42375-0453
16	22-28-5161	A-42375-0436	34	22-28-5341	A-42375-0454
17	22-28-5171	A-42375-0437	35	22-28-5351	A-42375-0455
18	22-28-5181	A-42375-0438	36	22-28-5361	A-42375-0456
19	22-28-5191	A-42375-0439			

ENG. NO: A-42375-0457/0491	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AYB208
PIN LENGTH: L	.545 / 13.84
MATING LENGTH: M	.320 / 8.13
GOLD POINT: G	.140 / 3.56
PC TAIL LENGTH: P	.135 / 3.43
TIN: T	.135 / 3.43
CKTS:	2-36
KINKS:	SMES-42003
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-5024	A-42375-0457	20	22-28-5204	A-42375-0475
03	22-28-5034	A-42375-0458	21	22-28-5214	A-42375-0476
04	22-28-5044	A-42375-0459	22	22-28-5224	A-42375-0477
05	22-28-5054	A-42375-0460	23	22-28-5234	A-42375-0478
06	22-28-5064	A-42375-0461	24	22-28-5244	A-42375-0479
07	22-28-5074	A-42375-0462	25	22-28-5254	A-42375-0480
08	22-28-5084	A-42375-0463	26	22-28-5264	A-42375-0481
09	22-28-5094	A-42375-0464	27	22-28-5274	A-42375-0482
10	22-28-5104	A-42375-0465	28	22-28-5284	A-42375-0483
11	22-28-5114	A-42375-0466	29	22-28-5294	A-42375-0484
12	22-28-5124	A-42375-0467	30	22-28-5304	A-42375-0485
13	22-28-5134	A-42375-0468	31	22-28-5314	A-42375-0486
14	22-28-5144	A-42375-0469	32	22-28-5324	A-42375-0487
15	22-28-5154	A-42375-0470	33	22-28-5334	A-42375-0488
16	22-28-5164	A-42375-0471	34	22-28-5344	A-42375-0489
17	22-28-5174	A-42375-0472	35	22-28-5354	A-42375-0490
18	22-28-5184	A-42375-0473	36	22-28-5364	A-42375-0491
19	22-28-5194	A-42375-0474			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 8 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: A-42375-0492/0526	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AYB228
PIN LENGTH: L	.545 / 13.84
MATING LENGTH: M	.320 / 8.13
GOLD POINT: G	.140 / 3.56
PC TAIL LENGTH: P	.135 / 3.43
TIN: T	.135 / 3.43
CKTS:	2-36
KINKS:	SMES-42003
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-5027	A-42375-0492	20	22-28-5207	A-42375-0510
03	22-28-5037	A-42375-0493	21	22-28-5217	A-42375-0511
04	22-28-5047	A-42375-0494	22	22-28-5227	A-42375-0512
05	22-28-5057	A-42375-0495	23	22-28-5237	A-42375-0513
06	22-28-5067	A-42375-0496	24	22-28-5247	A-42375-0514
07	22-28-5077	A-42375-0497	25	22-28-5257	A-42375-0515
08	22-28-5087	A-42375-0498	26	22-28-5267	A-42375-0516
09	22-28-5097	A-42375-0499	27	22-28-5277	A-42375-0517
10	22-28-5107	A-42375-0500	28	22-28-5287	A-42375-0518
11	22-28-5117	A-42375-0501	29	22-28-5297	A-42375-0519
12	22-28-5127	A-42375-0502	30	22-28-5307	A-42375-0520
13	22-28-5137	A-42375-0503	31	22-28-5317	A-42375-0521
14	22-28-5147	A-42375-0504	32	22-28-5327	A-42375-0522
15	22-28-5157	A-42375-0505	33	22-28-5337	A-42375-0523
16	22-28-5167	A-42375-0506	34	22-28-5347	A-42375-0524
17	22-28-5177	A-42375-0507	35	22-28-5357	A-42375-0525
18	22-28-5187	A-42375-0508	36	22-28-5367	A-42375-0526
19	22-28-5197	A-42375-0509			

ENG. NO: A-42375-0527/0561	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ARA154
PIN LENGTH: L	.520 / 13.21
MATING LENGTH: M	.295 / 7.49
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.135 / 3.43
TIN: T	OVERALL
CKTS:	2-36
KINKS:	SMES-42003
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-5022	A-42375-0527	20	22-28-5202	A-42375-0545
03	22-28-5032	A-42375-0528	21	22-28-5212	A-42375-0546
04	22-28-5042	A-42375-0529	22	22-28-5222	A-42375-0547
05	22-28-5052	A-42375-0530	23	22-28-5232	A-42375-0548
06	22-28-5062	A-42375-0531	24	22-28-5242	A-42375-0549
07	22-28-5072	A-42375-0532	25	22-28-5252	A-42375-0550
08	22-28-5082	A-42375-0533	26	22-28-5262	A-42375-0551
09	22-28-5092	A-42375-0534	27	22-28-5272	A-42375-0552
10	22-28-5102	A-42375-0535	28	22-28-5282	A-42375-0553
11	22-28-5112	A-42375-0536	29	22-28-5292	A-42375-0554
12	22-28-5122	A-42375-0537	30	22-28-5302	A-42375-0555
13	22-28-5132	A-42375-0538	31	22-28-5312	A-42375-0556
14	22-28-5142	A-42375-0539	32	22-28-5322	A-42375-0557
15	22-28-5152	A-42375-0540	33	22-28-5332	A-42375-0558
16	22-28-5162	A-42375-0541	34	22-28-5342	A-42375-0559
17	22-28-5172	A-42375-0542	35	22-28-5352	A-42375-0560
18	22-28-5182	A-42375-0543	36	22-28-5362	A-42375-0561
19	22-28-5192	A-42375-0544			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 9 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V 1).DOC

42375

ENG. NO: A-42375-0562/0596	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ARB208
PIN LENGTH: L	.520 / 13.21
MATING LENGTH: M	.295 / 7.49
GOLD POINT: G	.140 / 3.56
PC TAIL LENGTH: P	.135 / 3.43
TIN: T	.135 / 3.43
CKTS:	2-36
KINKS:	SMES-42003
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-5025	A-42375-0562	20	22-28-5205	A-42375-0580
03	22-28-5035	A-42375-0563	21	22-28-5215	A-42375-0581
04	22-28-5045	A-42375-0564	22	22-28-5225	A-42375-0582
05	22-28-5055	A-42375-0565	23	22-28-5235	A-42375-0583
06	22-28-5065	A-42375-0566	24	22-28-5245	A-42375-0584
07	22-28-5075	A-42375-0567	25	22-28-5255	A-42375-0585
08	22-28-5085	A-42375-0568	26	22-28-5265	A-42375-0586
09	22-28-5095	A-42375-0569	27	22-28-5275	A-42375-0587
10	22-28-5105	A-42375-0570	28	22-28-5285	A-42375-0588
11	22-28-5115	A-42375-0571	29	22-28-5295	A-42375-0589
12	22-28-5125	A-42375-0572	30	22-28-5305	A-42375-0590
13	22-28-5135	A-42375-0573	31	22-28-5315	A-42375-0591
14	22-28-5145	A-42375-0574	32	22-28-5325	A-42375-0592
15	22-28-5155	A-42375-0575	33	22-28-5335	A-42375-0593
16	22-28-5165	A-42375-0576	34	22-28-5345	A-42375-0594
17	22-28-5175	A-42375-0577	35	22-28-5355	A-42375-0595
18	22-28-5185	A-42375-0578	36	22-28-5365	A-42375-0596
19	22-28-5195	A-42375-0579			

ENG. NO: A-42375-0597/0631	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ARB228
PIN LENGTH: L	.520 / 13.21
MATING LENGTH: M	.295 / 7.49
GOLD POINT: G	.140 / 3.56
PC TAIL LENGTH: P	.135 / 3.43
TIN: T	.135 / 3.43
CKTS:	2-36
KINKS:	SMES-42003
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	22-28-5028	A-42375-0597	20	22-28-5208	A-42375-0615
03	22-28-5038	A-42375-0598	21	22-28-5218	A-42375-0616
04	22-28-5048	A-42375-0599	22	22-28-5228	A-42375-0617
05	22-28-5058	A-42375-0600	23	22-28-5238	A-42375-0618
06	22-28-5068	A-42375-0601	24	22-28-5248	A-42375-0619
07	22-28-5078	A-42375-0602	25	22-28-5258	A-42375-0620
08	22-28-5088	A-42375-0603	26	22-28-5268	A-42375-0621
09	22-28-5098	A-42375-0604	27	22-28-5278	A-42375-0622
10	22-28-5108	A-42375-0605	28	22-28-5288	A-42375-0623
11	22-28-5118	A-42375-0606	29	22-28-5298	A-42375-0624
12	22-28-5128	A-42375-0607	30	22-28-5308	A-42375-0625
13	22-28-5138	A-42375-0608	31	22-28-5318	A-42375-0626
14	22-28-5148	A-42375-0609	32	22-28-5328	A-42375-0627
15	22-28-5158	A-42375-0610	33	22-28-5338	A-42375-0628
16	22-28-5168	A-42375-0611	34	22-28-5348	A-42375-0629
17	22-28-5178	A-42375-0612	35	22-28-5358	A-42375-0630
18	22-28-5188	A-42375-0613	36	22-28-5368	A-42375-0631
19	22-28-5198	A-42375-0614			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 10 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V 1).DOC

42375

ENG. NO: A-42375-0667/0699	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABB208
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	.100 / 2.54
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	.100 / 2.54
CKTS:	4-36
KINKS:	NO
VOIDED CKTS:	4
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02			20	42375-0683	A-42375-0683
03			21	42375-0684	A-42375-0684
04	42375-0667	A-42375-0667	22	42375-0685	A-42375-0685
05	42375-0668	A-42375-0668	23	42375-0686	A-42375-0686
06	22-30-3060	A-42375-0669	24	42375-0687	A-42375-0687
07	42375-0670	A-42375-0670	25	42375-0688	A-42375-0688
08	42375-0671	A-42375-0671	26	42375-0689	A-42375-0689
09	42375-0672	A-42375-0672	27	42375-0690	A-42375-0690
10	42375-0673	A-42375-0673	28	42375-0691	A-42375-0691
11	42375-0674	A-42375-0674	29	42375-0692	A-42375-0692
12	22-30-3120	A-42375-0675	30	42375-0693	A-42375-0693
13	42375-0676	A-42375-0676	31	42375-0694	A-42375-0694
14	42375-0677	A-42375-0677	32	42375-0695	A-42375-0695
15	42375-0678	A-42375-0678	33	42375-0696	A-42375-0696
16	42375-0679	A-42375-0679	34	42375-0697	A-42375-0697
17	42375-0680	A-42375-0680	35	42375-0698	A-42375-0698
18	42375-0681	A-42375-0681	36	42375-0699	A-42375-0699
19	42375-0682	A-42375-0682			

ENG. NO: A-42375-0700/0732	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ADB208
PIN LENGTH: L	.465 /11.81
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	.100 / 2.54
PC TAIL LENGTH: P	.135 / 3.43
TIN: T	.100 / 2.54
CKTS:	4-36
KINKS:	SMES-42003
VOIDED CKTS:	4
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02			20	42375-0716	A-42375-0716
03			21	42375-0717	A-42375-0717
04	42375-0700	A-42375-0700	22	42375-0718	A-42375-0718
05	42375-0701	A-42375-0701	23	42375-0719	A-42375-0719
06	22-30-3061	A-42375-0702	24	42375-0720	A-42375-0720
07	42375-0703	A-42375-0703	25	42375-0721	A-42375-0721
08	42375-0704	A-42375-0704	26	42375-0722	A-42375-0722
09	42375-0705	A-42375-0705	27	42375-0723	A-42375-0723
10	42375-0706	A-42375-0706	28	42375-0724	A-42375-0724
11	42375-0707	A-42375-0707	29	42375-0725	A-42375-0725
12	42375-0708	A-42375-0708	30	42375-0726	A-42375-0726
13	42375-0709	A-42375-0709	31	42375-0727	A-42375-0727
14	42375-0710	A-42375-0710	32	42375-0728	A-42375-0728
15	42375-0711	A-42375-0711	33	42375-0729	A-42375-0729
16	42375-0712	A-42375-0712	34	42375-0730	A-42375-0730
17	42375-0713	A-42375-0713	35	42375-0731	A-42375-0731
18	42375-0714	A-42375-0714	36	42375-0732	A-42375-0732
19	42375-0715	A-42375-0715			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 11 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V 1).DOC

42375

ENG. NO: A-42375-0836/0870	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-BSA154
PIN LENGTH: L	.630 / 16.00
MATING LENGTH: M	.405/10.29
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.135/3.43
TIN: T	OVERALL
CKTS:	2-36
KINKS:	SMES-42003
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02		A-42375-0836	20	22-30-3203	A-42375-0854
03	22-30-3033	A-42375-0837	21	22-30-3213	A-42375-0855
04	22-30-3043	A-42375-0838	22	22-30-3223	A-42375-0856
05	22-30-3053	A-42375-0839	23	22-30-3233	A-42375-0857
06	22-30-3063	A-42375-0840	24	22-30-3243	A-42375-0858
07	22-30-3073	A-42375-0841	25	22-30-3253	A-42375-0859
08	22-30-3083	A-42375-0842	26	22-30-3263	A-42375-0860
09	22-30-3093	A-42375-0843	27	22-30-3273	A-42375-0861
10	22-30-3103	A-42375-0844	28	22-30-3283	A-42375-0862
11	22-30-3113	A-42375-0845	29	22-30-3293	A-42375-0863
12	22-30-3123	A-42375-0846	30	22-30-3303	A-42375-0864
13	22-30-3133	A-42375-0847	31	22-30-3313	A-42375-0865
14	22-30-3143	A-42375-0848	32	22-30-3323	A-42375-0866
15	22-30-3153	A-42375-0849	33	22-30-3333	A-42375-0867
16	22-30-3163	A-42375-0850	34	22-30-3343	A-42375-0868
17	22-30-3173	A-42375-0851	35	22-30-3353	A-42375-0869
18	22-30-3183	A-42375-0852	36	22-30-3363	A-42375-0870
19	22-30-3193	A-42375-0853			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 12 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V 1).DOC

42375

ENG. NO: A-42375-0871/0904	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ATA154
PIN LENGTH: L	.530 / 13.46
MATING LENGTH: M	.320 / 8.13
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.120 / 3.05
TIN: T	OVERALL
CKTS:	3-36
KINKS:	NO
VOIDED CKTS:	2
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02			20	22-30-3204	A-42375-0888
03	22-30-3034	A-42375-0871	21	22-30-3214	A-42375-0889
04	22-30-3044	A-42375-0872	22	22-30-3224	A-42375-0890
05	22-30-3054	A-42375-0873	23	22-30-3234	A-42375-0891
06	22-30-3064	A-42375-0874	24	22-30-3244	A-42375-0892
07	22-30-3074	A-42375-0875	25	22-30-3254	A-42375-0893
08	22-30-3084	A-42375-0876	26	22-30-3264	A-42375-0894
09	22-30-3094	A-42375-0877	27	22-30-3274	A-42375-0895
10	22-30-3104	A-42375-0878	28	22-30-3284	A-42375-0896
11	22-30-3114	A-42375-0879	29	22-30-3294	A-42375-0897
12	22-30-3124	A-42375-0880	30	22-30-3304	A-42375-0898
13	22-30-3134	A-42375-0881	31	22-30-3314	A-42375-0899
14	22-30-3144	A-42375-0882	32	22-30-3324	A-42375-0900
15	22-30-3154	A-42375-0883	33	22-30-3334	A-42375-0901
16	22-30-3164	A-42375-0884	34	22-30-3344	A-42375-0902
17	22-30-3174	A-42375-0885	35	22-30-3354	A-42375-0903
18	22-30-3184	A-42375-0886	36	22-30-3364	A-42375-0904
19	22-30-3194	A-42375-0887			

ENG. NO: A-42375-0973/1001	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABA154
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	OVERALL
CKTS:	8-36
KINKS:	NO
VOIDED CKTS:	3,8
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02			20	42375-0985	A-42375-0985
03			21	42375-0986	A-42375-0986
04			22	42375-0987	A-42375-0987
05			23	42375-0988	A-42375-0988
06			24	42375-0989	A-42375-0989
07			25	42375-0990	A-42375-0990
08	42375-0973	A-42375-0973	26	42375-0991	A-42375-0991
09	42375-0974	A-42375-0974	27	42375-0992	A-42375-0992
10	22-30-3107	A-42375-0975	28	42375-0993	A-42375-0993
11	42375-0976	A-42375-0976	29	42375-0994	A-42375-0994
12	42375-0977	A-42375-0977	30	42375-0995	A-42375-0995
13	42375-0978	A-42375-0978	31	42375-0996	A-42375-0996
14	42375-0979	A-42375-0979	32	42375-0997	A-42375-0997
15	42375-0980	A-42375-0980	33	42375-0998	A-42375-0998
16	42375-0981	A-42375-0981	34	42375-0999	A-42375-0999
17	42375-0982	A-42375-0982	35	42375-1000	A-42375-1000
18	42375-0983	A-42375-0983	36	42375-1001	A-42375-1001
19	42375-0984	A-42375-0984			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 13 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V 1).DOC

42375

ENG. NO: A-42375-1105/1139	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABB208
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	.100 / 2.54
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	.100 / 2.54
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	2
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	42375-1105	A-42375-1105	20	42375-1123	A-42375-1123
03	42375-1106	A-42375-1106	21	42375-1124	A-42375-1124
04	42375-1107	A-42375-1107	22	42375-1125	A-42375-1125
05	42375-1108	A-42375-1108	23	42375-1126	A-42375-1126
06	42375-1109	A-42375-1109	24	42375-1127	A-42375-1127
07	42375-1110	A-42375-1110	25	42375-1128	A-42375-1128
08	42375-1111	A-42375-1111	26	42375-1129	A-42375-1129
09	22-30-3099	A-42375-1112	27	42375-1130	A-42375-1130
10	42375-1113	A-42375-1113	28	42375-1131	A-42375-1131
11	42375-1114	A-42375-1114	29	42375-1132	A-42375-1132
12	42375-1115	A-42375-1115	30	42375-1133	A-42375-1133
13	42375-1116	A-42375-1116	31	42375-1134	A-42375-1134
14	42375-1117	A-42375-1117	32	42375-1135	A-42375-1135
15	42375-1118	A-42375-1118	33	42375-1136	A-42375-1136
16	42375-1119	A-42375-1119	34	42375-1137	A-42375-1137
17	42375-1120	A-42375-1120	35	42375-1138	A-42375-1138
18	42375-1121	A-42375-1121	36	42375-1139	A-42375-1139
19	42375-1122	A-42375-1122			

ENG. NO: 42375-1244/1278	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABA154
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	2
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-1244	20	42375-1262
03	42375-1245	21	42375-1263
04	42375-1246	22	42375-1264
05	42375-1247	23	42375-1265
06	42375-1248	24	42375-1266
07	42375-1249	25	42375-1267
08	42375-1250	26	42375-1268
09	42375-1251	27	42375-1269
10	42375-1252	28	42375-1270
11	42375-1253	29	42375-1271
12	42375-1254	30	42375-1272
13	42375-1255	31	42375-1273
14	42375-1256	32	42375-1274
15	42375-1257	33	42375-1275
16	42375-1258	34	42375-1276
17	42375-1259	35	42375-1277
18	42375-1260	36	42375-1278
19	42375-1261		

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 14 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V 1).DOC

42375

ENG. NO: 42375-1349/1382	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABA154
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.230 / 5.84
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.135 / 3.43
TIN: T	OVERALL
CKTS:	3-36
KINKS:	SMES-42003
VOIDED CKTS:	2
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02		20	42375-1366
03	42375-1349	21	42375-1367
04	42375-1350	22	42375-1368
05	42375-1351	23	42375-1369
06	42375-1352	24	42375-1370
07	42375-1353	25	42375-1371
08	42375-1354	26	42375-1372
09	42375-1355	27	42375-1373
10	42375-1356	28	42375-1374
11	42375-1357	29	42375-1375
12	42375-1358	30	42375-1376
13	42375-1359	31	42375-1377
14	42375-1360	32	42375-1378
15	42375-1361	33	42375-1379
16	42375-1362	34	42375-1380
17	42375-1363	35	42375-1381
18	42375-1364	36	42375-1382
19	42375-1365		

ENG. NO: 42375-1515/1548	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABB208
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.230 / 5.84
GOLD POINT: G	.140 / 3.56
PC TAIL LENGTH: P	.135 / 3.43
TIN: T	.100 / 2.54
CKTS:	3-36
KINKS:	SMES-42003
VOIDED CKTS:	2
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02		20	42375-1532
03	42375-1515	21	42375-1533
04	42375-1516	22	42375-1534
05	42375-1517	23	42375-1535
06	42375-1518	24	42375-1536
07	42375-1519	25	42375-1537
08	42375-1520	26	42375-1538
09	42375-1521	27	42375-1539
10	42375-1522	28	42375-1540
11	42375-1523	29	42375-1541
12	42375-1524	30	42375-1542
13	42375-1525	31	42375-1543
14	42375-1526	32	42375-1544
15	42375-1527	33	42375-1545
16	42375-1528	34	42375-1546
17	42375-1529	35	42375-1547
18	42375-1530	36	42375-1548
19	42375-1531		

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 15 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: 42375-1720/1753	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABB208
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	.140 / 3.56
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	.100 / 2.54
CKTS:	3-36
KINKS:	NO
VOIDED CKTS:	3
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02		20	42375-1737
03	42375-1720	21	42375-1738
04	42375-1721	22	42375-1739
05	42375-1722	23	42375-1740
06	42375-1723	24	42375-1741
07	42375-1724	25	42375-1742
08	42375-1725	26	42375-1743
09	42375-1726	27	42375-1744
10	42375-1727	28	42375-1745
11	42375-1728	29	42375-1746
12	42375-1729	30	42375-1747
13	42375-1730	31	42375-1748
14	42375-1731	32	42375-1749
15	42375-1732	33	42375-1750
16	42375-1733	34	42375-1751
17	42375-1734	35	42375-1752
18	42375-1735	36	42375-1753
19	42375-1736		

ENG. NO: 42375-1855/1889	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-CJA154
PIN LENGTH: L	.700 / 17.78
MATING LENGTH: M	.488 / 12.40
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.122 / 3.10
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-1855	20	42375-1873
03	42375-1856	21	42375-1874
04	42375-1857	22	42375-1875
05	42375-1858	23	42375-1876
06	42375-1859	24	42375-1877
07	42375-1860	25	42375-1878
08	42375-1861	26	42375-1879
09	42375-1862	27	42375-1880
10	42375-1863	28	42375-1881
11	42375-1864	29	42375-1882
12	42375-1865	30	42375-1883
13	42375-1866	31	42375-1884
14	42375-1867	32	42375-1885
15	42375-1868	33	42375-1886
16	42375-1869	34	42375-1887
17	42375-1870	35	42375-1888
18	42375-1871	36	42375-1889
19	42375-1872		

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 16 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: 42375-1922/1956	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AEA154
PIN LENGTH: L	.470 / 11.94
MATING LENGTH: M	.190 / 4.83
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.190 / 4.83
TIN: T	.200 / 5.08
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-1922	20	42375-1940
03	42375-1923	21	42375-1941
04	42375-1924	22	42375-1942
05	42375-1925	23	42375-1943
06	42375-1926	24	42375-1944
07	42375-1927	25	42375-1945
08	42375-1928	26	42375-1946
09	42375-1929	27	42375-1947
10	42375-1930	28	42375-1948
11	42375-1931	29	42375-1949
12	42375-1932	30	42375-1950
13	42375-1933	31	42375-1951
14	42375-1934	32	42375-1952
15	42375-1935	33	42375-1953
16	42375-1936	34	42375-1954
17	42375-1937	35	42375-1955
18	42375-1938	36	42375-1956
19	42375-1939		

ENG. NO: 42375-2246/2275	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABA154
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	OVERALL
CKTS:	7-36
KINKS:	NO
VOIDED CKTS:	2,7
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02		20	42375-2259
03		21	42375-2260
04		22	42375-2261
05		23	42375-2262
06		24	42375-2263
07	42375-2246	25	42375-2264
08	42375-2247	26	42375-2265
09	42375-2248	27	42375-2266
10	42375-2249	28	42375-2267
11	42375-2250	29	42375-2268
12	42375-2251	30	42375-2269
13	42375-2252	31	42375-2270
14	42375-2253	32	42375-2271
15	42375-2254	33	42375-2272
16	42375-2255	34	42375-2273
17	42375-2256	35	42375-2274
18	42375-2257	36	42375-2275
19	42375-2258		

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 17 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: 42375-2486/2520	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AFB208
PIN LENGTH: L	.475 / 12.07
MATING LENGTH: M	.232 / 5.89
GOLD POINT: G	.150 / 3.81
PC TAIL LENGTH: P	.153 / 3.89
TIN: T	.100 / 2.54
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-2486	19	42375-2503
03	42375-2487	20	42375-2504
	68300-2008	21	42375-2505
04	42375-2488	22	42375-2506
05	42375-2489	23	42375-2507
06	42375-2490	24	42375-2508
07	42375-2491	25	42375-2509
08	42375-2492	26	42375-2510
09	42375-2493	27	42375-2511
10	42375-2494	28	42375-2512
11	42375-2495	29	42375-2513
12	42375-2496	30	42375-2514
13	42375-2497	31	42375-2515
14	42375-2498	32	42375-2516
15	42375-2499	33	42375-2517
16	42375-2500	34	42375-2518
17	42375-2501	35	42375-2519
18	42375-2502	36	42375-2520

ENG. NO: 42375-2521/2555	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AFB228
PIN LENGTH: L	.475 / 12.07
MATING LENGTH: M	.232 / 5.89
GOLD POINT: G	.150 / 3.81
PC TAIL LENGTH: P	.153 / 3.89
TIN: T	.100 / 2.54
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-2521	20	42375-2539
03	42375-2522	21	42375-2540
04	42375-2523	22	42375-2541
05	42375-2524	23	42375-2542
06	42375-2525	24	42375-2543
07	42375-2526	25	42375-2544
08	42375-2527	26	42375-2545
09	42375-2528	27	42375-2546
10	42375-2529	28	42375-2547
11	42375-2530	29	42375-2548
12	42375-2531	30	42375-2549
13	42375-2532	31	42375-2550
14	42375-2533	32	42375-2551
15	42375-2534	33	42375-2552
16	42375-2535	34	42375-2553
17	42375-2536	35	42375-2554
18	42375-2537	36	42375-2555
19	42375-2538		

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 18 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: 42375-2801/2835	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-HDB228
PIN LENGTH: L	1.200 / 30.48
MATING LENGTH: M	1.000 / 25.40
GOLD POINT: G	.200 / 5.08
PC TAIL LENGTH: P	.110 / 2.79
TIN: T	.200 / 5.08
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0043

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-2801	20	42375-2819
03	42375-2802	21	42375-2820
04	42375-2803	22	42375-2821
05	42375-2804	23	42375-2822
06	42375-2805	24	42375-2823
07	42375-2806	25	42375-2824
08	42375-2807	26	42375-2825
09	42375-2808	27	42375-2826
10	42375-2809	28	42375-2827
11	42375-2810	29	42375-2828
12	42375-2811	30	42375-2829
13	42375-2812	31	42375-2830
14	42375-2813	32	42375-2831
15	42375-2814	33	42375-2832
16	42375-2815	34	42375-2833
17	42375-2816	35	42375-2834
18	42375-2817	36	42375-2835
19	42375-2818		

ENG. NO: 42375-2836/2870	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-EMA154
PIN LENGTH: L	.925 / 23.50
MATING LENGTH: M	.625 / 15.88
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.210 / 5.33
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-2836	20	42375-2854
03	42375-2837	21	42375-2855
04	42375-2838	22	42375-2856
05	42375-2839	23	42375-2857
06	42375-2840	24	42375-2858
07	42375-2841	25	42375-2859
08	42375-2842	26	42375-2860
09	42375-2843	27	42375-2861
10	42375-2844	28	42375-2862
11	42375-2845	29	42375-2863
12	42375-2846	30	42375-2864
13	42375-2847	31	42375-2865
14	42375-2848	32	42375-2866
15	42375-2849	33	42375-2867
16	42375-2850	34	42375-2868
17	42375-2851	35	42375-2869
18	42375-2852	36	42375-2870
19	42375-2853		

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
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DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V. 1).DOC

42375

ENG. NO: 42375-3044/3078	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-KHB208
PIN LENGTH: L	1.430 / 36.32
MATING LENGTH: M	.867 / 22.02
GOLD POINT: G	.200 / 5.08
PC TAIL LENGTH: P	.473 / 12.01
TIN: T	.200 / 5.08
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0043

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-3044	20	42375-3062
03	42375-3045	21	42375-3063
04	42375-3046	22	42375-3064
05	42375-3047	23	42375-3065
06	42375-3048	24	42375-3066
07	42375-3049	25	42375-3067
08	42375-3050	26	42375-3068
09	42375-3051	27	42375-3069
10	42375-3052	28	42375-3070
11	42375-3053	29	42375-3071
12	42375-3054	30	42375-3072
13	42375-3055	31	42375-3073
14	42375-3056	32	42375-3074
15	42375-3057	33	42375-3075
16	42375-3058	34	42375-3076
17	42375-3059	35	42375-3077
18	42375-3060	36	42375-3078
19	42375-3061		

ENG. NO: 42375-3114/3148	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-BXA154
PIN LENGTH: L	.645 / 16.38
MATING LENGTH: M	.431 / 10.95
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.124 / 3.15
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-3114	20	42375-3132
03	42375-3115	21	42375-3133
04	42375-3116	22	42375-3134
05	42375-3117	23	42375-3135
06	42375-3118	24	42375-3136
07	42375-3119	25	42375-3137
08	42375-3120	26	42375-3138
09	42375-3121	27	42375-3139
10	42375-3122	28	42375-3140
11	42375-3123	29	42375-3141
12	42375-3124	30	42375-3142
13	42375-3125	31	42375-3143
14	42375-3126	32	42375-3144
15	42375-3127	33	42375-3145
16	42375-3128	34	42375-3146
17	42375-3129	35	42375-3147
18	42375-3130	36	42375-3148
19	42375-3131		

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 20 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V. 1).DOC

42375

ENG. NO: 42375-3149 / 3183	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-BEB208
PIN LENGTH: L	.575 / 14.61
MATING LENGTH: M	.350 / 8.89
GOLD POINT: G	.200 / 5.08
PC TAIL LENGTH: P	.135 / 3.43
TIN: T	.200 / 5.08
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-3149	20	42375-3167
03	42375-3150	21	42375-3168
04	42375-3151	22	42375-3169
05	42375-3152	23	42375-3170
06	42375-3153	24	42375-3171
07	42375-3154	25	42375-3172
08	42375-3155	26	42375-3173
09	42375-3156	27	42375-3174
10	42375-3157	28	42375-3175
11	42375-3158	29	42375-3176
12	42375-3159	30	42375-3177
13	42375-3160	31	42375-3178
14	42375-3161	32	42375-3179
15	42375-3162	33	42375-3180
16	42375-3163	34	42375-3181
17	42375-3164	35	42375-3182
18	42375-3165	36	42375-3183
19	42375-3166		

ENG. NO: 42375-3184 / 3218	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-GNB208
PIN LENGTH: L	1.140 / 28.96
MATING LENGTH: M	.913 / 23.20
GOLD POINT: G	.200 / 5.08
PC TAIL LENGTH: P	.137 / 3.48
TIN: T	.200 / 5.08
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0043

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-3184	20	42375-3202
03	42375-3185	21	42375-3203
04	42375-3186	22	42375-3204
05	42375-3187	23	42375-3205
06	42375-3188	24	42375-3206
07	42375-3189	25	42375-3207
08	42375-3190	26	42375-3208
09	42375-3191	27	42375-3209
10	42375-3192	28	42375-3210
11	42375-3193	29	42375-3211
12	42375-3194	30	42375-3212
13	42375-3195	31	42375-3213
14	42375-3196	32	42375-3214
15	42375-3197	33	42375-3215
16	42375-3198	34	42375-3216
17	42375-3199	35	42375-3217
18	42375-3200	36	42375-3218
19	42375-3201		

ENG. NO: 42375-3219 / 3253	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-BPA154
PIN LENGTH: L	.620 / 15.75
MATING LENGTH: M	.280 / 7.11
GOLD POINT: G	NA
PC TAIL LENGTH: P	.250 / 6.35
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-3219	20	42375-3237
03	42375-3220	21	42375-3238
04	42375-3221	22	42375-3239
05	42375-3222	23	42375-3240
06	42375-3223	24	42375-3241
07	42375-3224	25	42375-3242
08	42375-3225	26	42375-3243
09	42375-3226	27	42375-3244
10	42375-3227	28	42375-3245
11	42375-3228	29	42375-3246
12	42375-3229	30	42375-3247
13	42375-3230	31	42375-3248
14	42375-3231	32	42375-3249
15	42375-3232	33	42375-3250
16	42375-3233	34	42375-3251
17	42375-3234	35	42375-3252
18	42375-3235	36	42375-3253
19	42375-3236		

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 21 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: 42375-3254 / 3288	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-DMA154
PIN LENGTH: L	.820 / 20.83
MATING LENGTH: M	.590 / 14.99
GOLD POINT: G	NA
PC TAIL LENGTH: P	.140 / 3.56
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-3254	20	42375-3272
03	42375-3255	21	42375-3273
04	42375-3256	22	42375-3274
05	42375-3257	23	42375-3275
06	42375-3258	24	42375-3276
07	42375-3259	25	42375-3277
08	42375-3260	26	42375-3278
09	42375-3261	27	42375-3279
10	42375-3262	28	42375-3280
11	42375-3263	29	42375-3281
12	42375-3264	30	42375-3282
13	42375-3265	31	42375-3283
14	42375-3266	32	42375-3284
15	42375-3267	33	42375-3285
16	42375-3268	34	42375-3286
17	42375-3269	35	42375-3287
18	42375-3270	36	42375-3288
19	42375-3271		

ENG. NO: 42375-3289 / 3323	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-FNA154
PIN LENGTH: L	1.035 / 26.29
MATING LENGTH: M	.358 / 9.09
GOLD POINT: G	NA
PC TAIL LENGTH: P	.587 / 14.91
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0043

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-3289	20	42375-3307
03	42375-3290	21	42375-3308
04	42375-3291	22	42375-3309
05	42375-3292	23	42375-3310
06	42375-3293	24	42375-3311
07	42375-3294	25	42375-3312
08	42375-3295	26	42375-3313
09	42375-3296	27	42375-3314
10	42375-3297	28	42375-3315
11	42375-3298	29	42375-3316
12	42375-3299	30	42375-3317
13	42375-3300	31	42375-3318
14	42375-3301	32	42375-3319
15	42375-3302	33	42375-3320
16	42375-3303	34	42375-3321
17	42375-3304	35	42375-3322
18	42375-3305	36	42375-3323
19	42375-3306		

ENG. NO: 42375-3324 / 3358	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-CCA154
PIN LENGTH: L	.670 / 17.02
MATING LENGTH: M	.440 / 11.18
GOLD POINT: G	NA
PC TAIL LENGTH: P	.140 / 3.56
TIN: T	OVERALL
CKTS:	2-36
KINKS:	SMES-42003
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-3324	20	42375-3342
03	42375-3325	21	42375-3343
04	42375-3326	22	42375-3344
05	42375-3327	23	42375-3345
06	42375-3328	24	42375-3346
07	42375-3329	25	42375-3347
08	42375-3330	26	42375-3348
09	42375-3331	27	42375-3349
10	42375-3332	28	42375-3350
11	42375-3333	29	42375-3351
12	42375-3334	30	42375-3352
13	42375-3335	31	42375-3353
14	42375-3336	32	42375-3354
15	42375-3337	33	42375-3355
16	42375-3338	34	42375-3356
17	42375-3339	35	42375-3357
18	42375-3340	36	42375-3358
19	42375-3341		

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
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DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: 42375-3359 / 3393	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABB228
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.170 / 4.32
GOLD POINT: G	.100 / 2.54
PC TAIL LENGTH: P	.195 / 4.95
TIN: T	.100 / 2.54
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-3359	20	42375-3377
03	42375-3360	21	42375-3378
04	42375-3361	22	42375-3379
05	42375-3362	23	42375-3380
06	42375-3363	24	42375-3381
07	42375-3364	25	42375-3382
08	42375-3365	26	42375-3383
09	42375-3366	27	42375-3384
10	42375-3367	28	42375-3385
11	42375-3368	29	42375-3386
12	42375-3369	30	42375-3387
13	42375-3370	31	42375-3388
14	42375-3371	32	42375-3389
15	42375-3372	33	42375-3390
16	42375-3373	34	42375-3391
17	42375-3374	35	42375-3392
18	42375-3375	36	42375-3393
19	42375-3376		

ENG. NO: 42375-3394 / 3428	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-EZB208
PIN LENGTH: L	.970/24.64
MATING LENGTH: M	.780/19.81
GOLD POINT: G	.200/5.08
PC TAIL LENGTH: P	.100/ 2.54
TIN: T	.200/5.08
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0043

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-3394	20	42375-3412
03	42375-3395	21	42375-3413
04	42375-3396	22	42375-3414
05	42375-3397	23	42375-3415
06	42375-3398	24	42375-3416
07	42375-3399	25	42375-3417
08	42375-3400	26	42375-3418
09	42375-3401	27	42375-3419
10	42375-3402	28	42375-3420
11	42375-3403	29	42375-3421
12	42375-3404	30	42375-3422
13	42375-3405	31	42375-3423
14	42375-3406	32	42375-3424
15	42375-3407	33	42375-3425
16	42375-3408	34	42374-3426
17	42375-3409	35	42375-3427
18	42375-3410	36	42375-3428
19	42375-3411		

ENG. NO: 42375-3429 / 3463	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ARA154
PIN LENGTH: L	.520/13.21
MATING LENGTH: M	.386/9.80
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.044/1.12
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-3429	20	42375-3447
03	42375-3430	21	42375-3448
04	42375-3431	22	42375-3449
05	42375-3432	23	42375-3450
06	42375-3433	24	42375-3451
07	42375-3434	25	42375-3452
08	42375-3435	26	42375-3453
09	42375-3436	27	42375-3454
10	42375-3437	28	42375-3455
11	42375-3438	29	42375-3456
12	42375-3439	30	42375-3457
13	42375-3440	31	42375-3458
14	42375-3441	32	42375-3459
15	42375-3442	33	42375-3460
16	42375-3443	34	42374-3461
17	42375-3444	35	42375-3462
18	42375-3445	36	42375-3463
19	42375-3446		

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 23 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: 42375-3464 / 3498	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-CJA154
PIN LENGTH: L	.700/17.78
MATING LENGTH: M	.500/12.70
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.110/2.79
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	# 2
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-3464	20	42375-3482
03	42375-3465	21	42375-3483
04	42375-3466	22	42375-3484
05	42375-3467	23	42375-3485
06	42375-3468	24	42375-3486
07	42375-3469	25	42375-3487
08	42375-3470	26	42375-3488
09	42375-3471	27	42375-3489
10	42375-3472	28	42375-3490
11	42375-3473	29	42375-3491
12	42375-3474	30	42375-3492
13	42375-3475	31	42375-3493
14	42375-3476	32	42375-3494
15	42375-3477	33	42375-3495
16	42375-3478	34	42375-3496
17	42375-3479	35	42375-3497
18	42375-3480	36	42375-3498
19	42375-3481		

ENG. NO: 42375-3499/3533	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ETA154
PIN LENGTH: L	.950/24.13
MATING LENGTH: M	.750/19.05
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.110/2.79
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0043

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-3499	20	42375-3517
03	42375-3500	21	42375-3518
04	42375-3501	22	42375-3519
05	42375-3502	23	42375-3520
06	42375-3503	24	42375-3521
07	42375-3504	25	42375-3522
08	42375-3505	26	42375-3523
09	42375-3506	27	42375-3524
10	42375-3507	28	42375-3525
11	42375-3508	29	42375-3526
12	42375-3509	30	42375-3527
13	42375-3510	31	42375-3528
14	42375-3511	32	42375-3529
15	42375-3512	33	42375-3530
16	42375-3513	34	42375-3531
17	42375-3514	35	42375-3532
18	42375-3515	36	42375-3533
19	42375-3516		

ENG. NO: 42375-3534/3568	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AWB208
PIN LENGTH: L	.535/13.59
MATING LENGTH: M	.235/5.97
GOLD POINT: G	.200/5.08
PC TAIL LENGTH: P	.210/5.33
TIN: T	.100/2.54
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02	42375-3534	20	42375-3552
03	42375-3535	21	42375-3553
04	42375-3536	22	42375-3554
05	42375-3537	23	42375-3555
06	42375-3538	24	42375-3556
07	42375-3539	25	42375-3557
08	42375-3540	26	42375-3558
09	42375-3541	27	42375-3559
10	42375-3542	28	42375-3560
11	42375-3543	29	42375-3561
12	42375-3544	30	42375-3562
13	42375-3545	31	42375-3563
14	42375-3546	32	42375-3564
15	42375-3547	33	42375-3565
16	42375-3548	34	42375-3566
17	42375-3549	35	42375-3567
18	42375-3550	36	42375-3568
19	42375-3551		

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 24 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: A-42375-3569/3603	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABB208
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	.100 / 2.54
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	.100 / 2.54
CKTS:	4-36
KINKS:	NO
VOIDED CKTS:	5
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02			20	423753587	42375-3587
03			21	423753588	42375-3588
04			22	423753589	42375-3589
05	423753572	42375-3572	23	423753590	42375-3590
06	423753573	42375-3573	24	423753591	42375-3591
07	423753574	42375-3574	25	423753592	42375-3592
08	423753575	42375-3575	26	423753593	42375-3593
09	423753576	42375-3576	27	423753594	42375-3594
10	423753577	42375-3577	28	423753595	42375-3595
11	423753578	42375-3578	29	423753596	42375-3596
12	423753579	42375-3579	30	423753597	42375-3597
13	423753580	42375-3580	31	423753598	42375-3598
14	423753581	42375-3581	32	423753599	42375-3599
15	423753582	42375-3582	33	423753600	42375-3600
16	423753583	42375-3583	34	423753601	42375-3601
17	423753584	42375-3584	35	423753602	42375-3602
18	423753585	42375-3585	36	423753603	42375-3603
19	423753586	42375-3586			

ENG. NO: A-42375-2974/3008	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-FKB228
PIN LENGTH: L	1.020 / 25.91
MATING LENGTH: M	.805 / 20.45
GOLD POINT: G	.200 / 5.08
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	.200 / 5.08
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0043

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ITEM NUMBER
02			20		
03			21		
04			22		
05	423752977	42375-2977	23		
06			24		
07			25		
08			26		
09			27		
10			28		
11			29		
12			30		
13			31		
14			32		
15			33		
16			34		
17			35		
18			36		
19					

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 25 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: A-42375-3604/3637	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AXA154
PIN LENGTH: L	.540 / 13.72
MATING LENGTH: M	.380 / 9.65
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.070 / 1.78
TIN: T	OVERALL
CKTS:	3-36
KINKS:	NO
VOIDED CKTS:	2
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02			20		
03	42375-3604		21		
04			22		
05			23		
06			24		
07			25		
08			26		
09			27		
10			28		
11			29		
12			30		
13			31		
14			32		
15			33		
16			34		
17			35		
18			36		
19					

ENG. NO: A-42375-3638/3658	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABA154
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	2, 4, 6, 8, 10, 12, 14, 16
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ITEM NUMBER
02			20		
03			21		
04			22		
05			23		
06			24		
07			25		
08			26		
09			27		
10			28		
11			29		
12			30		
13			31		
14			32		
15			33		
16			34		
17	423753639	42375-3639	35		
18			36		
19					

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 26 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: 42375-3659/3693	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AXB208
PIN LENGTH: L	.540 /13.72
MATING LENGTH: M	.250 / 6.35
GOLD POINT: G	.140 / 3.56
PC TAIL LENGTH: P	.200 / 5.08
TIN: T	.135 / 3.43
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02	68300-2000	42375-3659	20		42375-3677
03	68300-2001	42375-3660	21		42375-3678
04		42375-3661	22		42375-3679
05	68300-2006	42375-3662	23		42375-3680
06		42375-3663	24		42375-3681
07		42375-3664	25		42375-3682
08		42375-3665	26		42375-3683
09		42375-3666	27		42375-3684
10		42375-3667	28		42375-3685
11		42375-3668	29		42375-3686
12		42375-3669	30		42375-3687
13		42375-3670	31		42375-3688
14		42375-3671	32		42375-3689
15		42375-3672	33		42375-3690
16		42375-3673	34		42375-3691
17		42375-3674	35		42375-3692
18		42375-3675	36		42375-3693
19		42375-3676			

ENG. NO: 42375-3694/3728	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AXB208
PIN LENGTH: L	.540 / 13.72
MATING LENGTH: M	.250 / 6.35
GOLD POINT: G	.140 / 3.56
PC TAIL LENGTH: P	.200 / 5.08
TIN: T	.135 / 3.43
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	5
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02		42375-3694	20		42375-3712
03		42375-3695	21		42375-3713
04		42375-3696	22		42375-3714
05		42375-3697	23		42375-3715
06		42375-3698	24		42375-3716
07		42375-3699	25		42375-3717
08	68300-2002	42375-3700	26		42375-3718
09		42375-3701	27		42375-3719
10		42375-3702	28		42375-3720
11		42375-3703	29		42375-3721
12		42375-3704	30		42375-3722
13		42375-3705	31		42375-3723
14		42375-3706	32		42375-3724
15		42375-3707	33		42375-3725
16		42375-3708	34		42375-3726
17		42375-3709	35		42375-3727
18		42375-3710	36		42375-3728
19		42375-3711			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 27 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: 42375-3729/3763	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AFB208
PIN LENGTH: L	.475 / 12.07
MATING LENGTH: M	.232 / 5.89
GOLD POINT: G	.150 / 3.81
PC TAIL LENGTH: P	.153 / 3.89
TIN: T	.150 / 3.81
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	5
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	ENG NUMBER	CKTS	MATERIAL NUMBER	ENG NUMBER
02		42375-3729	20		42375-3747
03		42375-3730	21		42375-3748
04		42375-3731	22		42375-3749
05		42375-3732	23		42375-3750
06		42375-3733	24		42375-3751
07		42375-3734	25		42375-3752
08	68300-2007	42375-3735	26		42375-3753
09		42375-3736	27		42375-3754
10		42375-3737	28		42375-3755
11		42375-3738	29		42375-3756
12		42375-3739	30		42375-3757
13		42375-3740	31		42375-3758
14		42375-3741	32		42375-3759
15		42375-3742	33		42375-3760
16		42375-3743	34		42375-3761
17		42375-3744	35		42375-3762
18		42375-3745	36		42375-3763
19		42375-3746			

ENG. NO: 42375-3764/3798	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ETA154
PIN LENGTH: L	.950/24.13
MATING LENGTH: M	.750/19.05
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.110/2.79
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	2
PACKAGING:	BULK PK-40873-0043

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02		20	
03		21	
04		22	
05		23	
06		24	
07		25	
08	42375-3770	26	
09		27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 28 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: 42375-3799/3832	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABA154
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	OVERALL
CKTS:	3-36
KINKS:	NO
VOIDED CKTS:	3
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	CKTS	MATERIAL NUMBER
02		20	
03		21	
04		22	
05	42375-3801	23	
06		24	
07		25	
08		26	
09		27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

ENG. NO: 42375-3733/3867	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABB208
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.250 / 6.35
GOLD POINT: G	.100 / 2.54
PC TAIL LENGTH: P	.115 / 2.92
TIN: T	.100 / 2.54
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	CKTS	MATERIAL NUMBER
02		20	
03		21	
04		22	
05	42375-3836	23	
06		24	
07		25	
08		26	
09		27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

ENG. NO: 42375-3868 / 3902	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-DWA154
PIN LENGTH: L	.850 / 21.59
MATING LENGTH: M	.640 / 16.26
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.120 / 3.05
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02		20	
03		21	
04	42375-3870	22	
05		23	
06	42375-3872	24	
07		25	
08		26	
09		27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 29 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V 1).DOC

42375

ENG. NO: 42375-3903/3932	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-BSA154
PIN LENGTH: L	.630 / 16.00
MATING LENGTH: M	.421 / 10.69
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.119 / 3.02
TIN: T	OVERALL
CKTS:	7-36
KINKS:	NO
VOIDED CKTS:	7
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	CKTS	MATERIAL NUMBER
02		20	
03		21	
04		22	
05		23	
06		24	
07		25	
08	42375-3904	26	
09		27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

ENG. NO: 42375-3933/3964	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-BSA154
PIN LENGTH: L	.630 / 16.00
MATING LENGTH: M	.405/10.29
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.135/3.43
TIN: T	OVERALL
CKTS:	5-36
KINKS:	SMES-42003
VOIDED CKTS:	5
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	CKTS	MATERIAL NUMBER
02		20	
03		21	
04		22	
05		23	
06		24	
07		25	
08		26	
09	42375-3937	27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

ENG. NO: 42375-3965/3995	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-BSA154
PIN LENGTH: L	.630 / 16.00
MATING LENGTH: M	.405/10.29
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.135/3.43
TIN: T	OVERALL
CKTS:	6-36
KINKS:	SMES-42003
VOIDED CKTS:	4, 5, 6
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	CKTS	MATERIAL NUMBER
02		20	
03		21	
04		22	
05		23	
06		24	
07		25	
08		26	
09	42375-3968	27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 30 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V 1).DOC

42375

ENG. NO: A-42375-3996/4030	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AXA154
PIN LENGTH: L	.540 / 13.72
MATING LENGTH: M	.390 / 9.91
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.060 / 1.52
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02		20	
03		21	
04		22	
05		23	
06	42375-4000	24	
07	42375-4001	25	
08		26	
09		27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

ENG. NO: 42375-4031/4059	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABA154
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	OVERALL
CKTS:	8-36
KINKS:	NO
VOIDED CKTS:	2, 4, 6, 8
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	CKTS	MATERIAL NUMBER
02		20	
03		21	
04		22	
05		23	
06		24	
07		25	
08		26	
09	42375-4032	27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

ENG. NO: 42375-4060 / 4094	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-CGA154
PIN LENGTH: L	.690 / 17.53
MATING LENGTH: M	.521 / 13.23
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.079 / 2.01
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	CKTS	MATERIAL NUMBER
02		20	
03		21	
04		22	
05		23	
06	42375-4064	24	
07		25	
08		26	
09		27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 31 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: A-42375-4095/4129	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-DEB228
PIN LENGTH: L	.785 / 19.94
MATING LENGTH: M	.470 / 11.94
GOLD POINT: G	.250 / 6.35
PC TAIL LENGTH: P	.225 / 5.72
TIN: T	.200 / 5.08
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02		20	
03		21	
04		22	
05		23	
06		24	
07		25	
08		26	
09		27	
10	42375-4103	28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18	42375-4111	36	
19			

ENG. NO: A-42375-4130/4161	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ATA154
PIN LENGTH: L	.530/13.46
MATING LENGTH: M	.320/8.13
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.120/3.05
TIN: T	OVERALL
CKTS:	5-36
KINKS:	SMES-42003
VOIDED CKTS:	2, 3, 4
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
		20	
		21	
		22	
05	42375-4130	23	
06		24	
07		25	
08		26	
09		27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

ENG. NO: 42375-4162/4196	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-BSC228
PIN LENGTH: L	.630/16.00
MATING LENGTH: M	.400/10.16
GOLD POINT: G	.345/8.76
PC TAIL LENGTH: P	.140/3.56
TIN: T	.100/2.54
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	CKTS	MATERIAL NUMBER
02		20	
03		21	
04	42375-4164	22	
05	42375-4165	23	
06		24	
07		25	
08		26	
09		27	
10	42375-4170	28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 32 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: A-42375-1622	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-AYB208
PIN LENGTH: L	.545 / 13.84
MATING LENGTH: M	.320 / 8.13
GOLD POINT: G	.140 / 3.56
PC TAIL LENGTH: P	.135 / 3.43
TIN: T	.135 / 3.43
CKTS:	2-36
KINKS:	SMES-42003
VOIDED CKTS:	3
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	CKTS	MATERIAL NUMBER
02		20	
03		21	
04		22	
05		23	
06		24	
07		25	
08		26	
09	42375-1622	27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

ENG. NO: A-42375-4199	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ARB228
PIN LENGTH: L	.520 / 13.21
MATING LENGTH: M	.230 / 5.84
GOLD POINT: G	.140 / 3.56
PC TAIL LENGTH: P	.200 / 5.08
TIN: T	.135 / 3.43
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	CKTS	MATERIAL NUMBER
02	42375-4199	20	
03		21	
04		22	
05		23	
06		24	
07		25	
08		26	
09		27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

ENG. NO: A-42375-4200	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ADB208
PIN LENGTH: L	.465 / 11.81
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	.100 / 2.54
PC TAIL LENGTH: P	.135 / 3.43
TIN: T	.100 / 2.54
CKTS:	2-36
KINKS:	SMES-42003
VOIDED CKTS:	3, 4
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	CKTS	MATERIAL NUMBER
02		20	
03		21	
04		22	
05	42375-4200	23	
06		24	
07		25	
08		26	
09		27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 33 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: 42375-4236	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-CCA118
PIN LENGTH: L	.670 / 17.02
MATING LENGTH: M	.440 / 11.18
GOLD POINT: G	NA
PC TAIL LENGTH: P	.140 / 3.56
TIN: T	OVERALL
CKTS:	2-36
KINKS:	SMES-42003
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02		20	
03		21	
04		22	
05		23	
06	42375-4236	24	
07		25	
08		26	
09		27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

ENG. NO: 42375-4305	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-BDA154
PIN LENGTH: L	.570 / 14.48
MATING LENGTH: M	.339 / 8.61
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.141 / 3.58
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	CKTS	MATERIAL NUMBER
02		20	
03		21	
04		22	
05	42375-4305	23	
06		24	
07		25	
08		26	
09		27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

ENG. NO: 42375-4338/4341	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-BGA154
PIN LENGTH: L	.585 / 14.86
MATING LENGTH: M	.398 / 10.11
GOLD POINT: G	N/A
PC TAIL LENGTH: P	.097 / 2.46
TIN: T	OVERALL
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	CKTS	MATERIAL NUMBER
02		20	
03	42375-4338	21	
04		22	
05		23	
06	42375-4341	24	
07		25	
08		26	
09		27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: UCP2014-3273 DATE: 8/7/2014	KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY	- 34 -

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	MKIPPER	NNGUYEN	FSMITH

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

42375

ENG. NO: 42375-4413	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-ABB208
PIN LENGTH: L	.455 / 11.56
MATING LENGTH: M	.240 / 6.09
GOLD POINT: G	.100 / 2.54
PC TAIL LENGTH: P	.125 / 3.18
TIN: T	.100 / 2.54
CKTS:	6-36
KINKS:	NO
VOIDED CKTS:	2, 4, 6
PACKAGING:	BULK PK-40873-0041

CKTS	ITEM NUMBER	CKTS	ITEM NUMBER
02		20	
03		21	
04		22	
05		23	
06		24	
07	42375-4413	25	
08		26	
09		27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

ENG. NO: 42375-4445	
HEADER NUMBER:	42312-0036
PIN NUMBER:	42663-0364
PLATING:	228
PIN LENGTH: L	.590 / 14.99
MATING LENGTH: M	.380 / 9.65
GOLD POINT: G	.200 / 5.08
PC TAIL LENGTH: P	.120 / 3.05
TIN: T	.135 / 3.43
CKTS:	2-36
KINKS:	NO
VOIDED CKTS:	NONE
PACKAGING:	BULK PK-40873-0041

CKTS	MATERIAL NUMBER	CKTS	MATERIAL NUMBER
02		20	
03		21	
04	42375-4445	22	
05		23	
06		24	
07		25	
08		26	
09		27	
10		28	
11		29	
12		30	
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	
19			

REV:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
T19	EC No.: **UCP2014-3273** DATE: **8/7/2014**	**KK 100 HEADER ASSY FLAT VERTICAL BREAKAWAY**	**- 35 -**

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
SD- 42375-001	**MKIPPER**	**NNGUYEN**	**FSMITH**

TEMPLATE FILENAME: PRODUCT_SPEC[SIZE_A](V.1).DOC

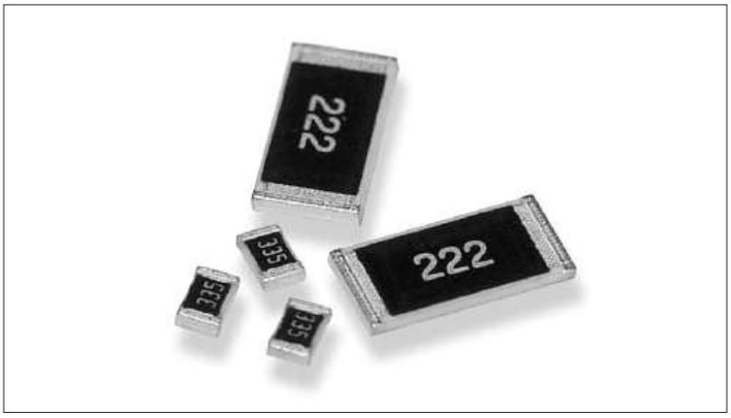
3.- Resistencias.

Thick Film Chip Resistors

Type CRG Series

Key Features

- Thick film resistors with a high power to size ratio,ideally suited to industrial and general purpose use. A range from 1 ohm to 10M and tolerances of 1% and 5%. Also including zero ohm links.
- Suitable for most applications, including high frequency operation, owing to the short lead structure and low capacitance.
- Seven Package Sizes
- Terminal finish: Matte Sn
- MSL Level 2



Precious metal terminations are screen printed onto a ceramic base and fired. The resistive element is screen printed and fired and the passivation layer added. Each resistor is trimmed to tolerance by laser. The pre-scribed tile is broken into strips, the end plating is fired on and the strips broken into individual components. Final termination is made by electroplating.

Characteristics – Electrical

		0201			0402			0603				0805			
Rated Power @ 70 °C (W)		0.05			0.063			0.1				0.125			
Resistance Range	Min	10	1	11	10	1	11	1	101	1	11	1	101	1	11
(Ohms)	Max	1M0	10	1M0	2M0	10	3M3	100	1M0	10	10M	100	1M0	10	10M
Tolerance (%)		1	5	5	1	5	5	1	1	5	5	1	1	5	5
Code letter		F	J	J	F	J	J	F	F	J	J	F	F	J	J
Selection Series		E24	E24	E24	E24	E24	E24	E24	E24	E24	E24	E24	E24	E24	E24
		E96			E96				E96				E96		
Temp. Coefficient (ppm/°C)		±200	±400	±200	±100	±400	±200	±200	±100	±200	±200	±200	±100	±400	±200

		1206				2010				2512			
Rated Power @ 70 °C (W)		0.25				0.5				1			
Resistance Range	Min	1	101	1	11	1	101	1	11	1	101	1	11
Ohms	Max	100	1M0	10	10M	100	1M0	10	10M	100	1M0	10	10M
Tolerance (%)		1	1	5	5	1	1	5	5	1	1	5	5
Code letter		F	F	J	J	F	F	J	J	F	F	J	J
Selection Series		E24	E24	E24	E24	E24	E24	E24	E24	E24	E24	E24	E24
			E96				E96				E96		
Temp. Coefficient (ppm/°C)		±200	±100	±400	±200	±200	±100	±400	±200	±200	±100	±400	±200

	0201	0402	0603	0805	1206	2010	2512
Working Voltage (V)	25	50	50	150	200	200	200
Max. Overload Voltage (V)	50	100	100	300	400	400	400
Operating Temp. Range (°C)	-55 to +125						
Climatic Category (°C)	55/125/56						
Insulation Resistance Dry Min (Mohms)	1000						
Stability (%)	3						
Zerohm (A) Current Max	0.5	1	1	2	2	2	2
Resistance Max	<50 mOhm			<50 mOhm			

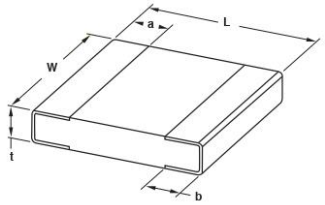
Dimensions are in millimeters and inches unless otherwise specified. Values in brackets are standard equivalents.

Dimensions are shown for reference purposes only. Specifications subject to change.

For email, phone or live chat, go to: **te.com/help**

Type CRG Series

Dimensions



Style	L	W	t	a	b
0201	0.6 ±0.03	0.3 ±0.03	0.23 ±0.03	0.10 ±0.05	0.15 ±0.05
0402	1.0 ±0.1	0.5 ±0.05	0.35 ±0.05	0.2 ±0.1	0.25 ±0.1
0603	1.6 ±0.1	0.8 ±0.15	0.45 ±0.1	0.3 ±0.2	0.3 ±0.1
0805	2.0 ±0.15	1.25 ±0.15	0.55 ±0.1	0.4 ±0.2	0.4 ±0.2
1206	3.1 ±0.15	1.55 ±0.15	0.55 ±0.1	0.45 ±0.2	0.45 ±0.2
2010	5.0 ±0.1	2.5 ±0.15	0.55 ±0.1	0.6 ±0.25	0.5 ±0.2
2512	6.35 ±0.1	3.2 ±0.15	0.55 ±0.1	0.6 ±0.25	0.5 ±0.2

Marking Codes - Case Sizes 0805 to 2512

IEC 4 Digit Marking

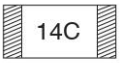
Resistance	100Ω	2.2KΩ	10KΩ	49.9KΩ	100KΩ
Marking Code	1000	2201	1002	4992	1003

Case Sizes 0603

E24 3 Digit Marking - Example: 101=100Ω 102=1KΩ

E24	10	11	12	13	15	16	18	20	22	24	27	30
	33	36	39	43	47	51	56	62	68	75	82	91

E96 3 Digit Marking - Examples: 14C=13K7Ω, 13C=13K3Ω, 68B=4K99Ω, 68X=49.9Ω



0603 E96 Marking Code Table

Code	E96	Code	E96	Code	E96	Code	E96
01	100	25	178	49	316	73	562
02	102	26	182	50	324	74	576
03	105	27	187	51	332	75	590
04	107	28	191	52	340	76	604
05	110	29	196	53	348	77	619
06	113	30	200	54	357	78	634
07	115	31	205	55	365	79	649
08	118	32	210	56	374	80	665
09	121	33	215	57	383	81	681
10	124	34	221	58	392	82	698
11	127	35	226	59	402	83	715
12	130	36	232	60	412	84	732
13	133	37	237	61	422	85	750
14	137	38	243	62	432	86	768
15	140	39	249	63	442	87	787
16	143	40	255	64	453	88	806
17	147	41	261	65	464	89	825
18	150	42	267	66	475	90	845
19	154	43	274	67	487	91	866
20	158	44	280	68	499	92	887
21	162	45	287	69	511	93	909
22	165	46	294	70	523	94	931
23	169	47	301	71	536	95	953
24	174	48	309	72	549	96	976

Code	A	B	C	D	E	F	G	H	X	Y	Z
Multiplier	10^0	10^{-1}	10^2	10^3	10^4	10^5	10^6	10^7	10^{-2}	10^{-2}	10^{-3}

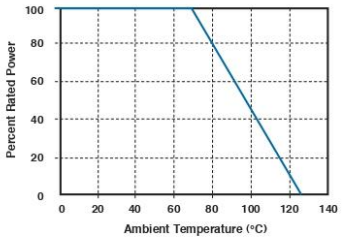
Dimensions are in millimeters and inches unless otherwise specified. Values in brackets are standard equivalents.

Dimensions are shown for reference purposes only. Specifications subject to change.

For email, phone or live chat, go to: **te.com/help**

Type CRG Series

Derating Curve



Mounting

The resistors are suitable for processing on automatic insertion equipment.

Marking

CRG0805, CRG1206, CRG2010, CRG2512
E24 series resistors are marked with a three digit code.
E96 series resistors are marked with a four digit code.
Zerohm components are marked '0'.

CRG0603
E24 5% series are marked with a three digit code.
E24 1% series are marked with a three digit code.
E96 series are marked with the international alphanumeric three character code (available on request).
EXCEPT 10, 11, 13, 15, 20 & 75 decades which are marked as the E24 series.

CRG0201 & CRG0402 series unmarked.

Performance Characteristics

The evaluation of the performance characteristics is carried out with reference to IECQ specifications QC 400 000 and QC 400 100.

TEST REF	Long Term Tests ±(3% + 0.1 ohm)
4.23	Climatic sequence
4.24	Damp heat, steady state
4.25.1	Endurance at 70 °C
4.25.3	Endurance at 125 °C
TEST REF	**Short Term Tests ±(1% + 0.05 ohm)**
4.13	Overload
4.32	Adhesion
4.33	Bond strength of end face plating
4.19	Rapid change of temperature
4.18	Resistance to soldering heat

Storage

Unopened reels should be stored within a temperature range of +5 °C to +25 °C, separated from any dust, chemicals and solvent based materials. Non-adherence to this procedure could effect the solderability of this product.

How to Order

CRG	0603	J	1K0
Common Part	**Size**	**Tolerance**	**Resistance Value**
CRG - Thick Film Chip Resistor	0201 0402 0603 0805 1206 2512	F - ±1% J - ±5%	1 ohm (1 ohm) 1R0 1K ohm (1000 ohms) 1K 100K ohm (100000 ohms) 100K 1M ohm (1000000 ohms) 1M

4.- Potenciómetro.

VISHAY
www.vishay.com

TS53
Vishay Sfernice

5 mm Square Surface Mount Miniature Trimmers Single-Turn Cermet Sealed

FEATURES

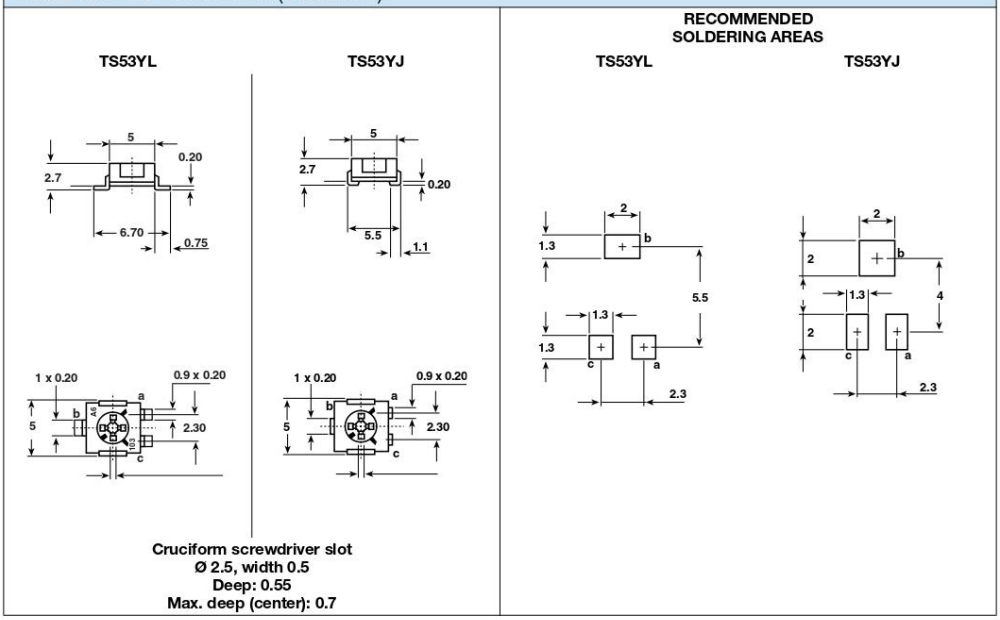
- 0.25 W at 70 °C
- For through hole version see T53Y series
- Wide ohmic range (10 Ω to 1 MΩ)
- Small size for optimum packaging density
- Tests according to CECC 41000 or IEC 60393-1
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

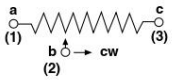
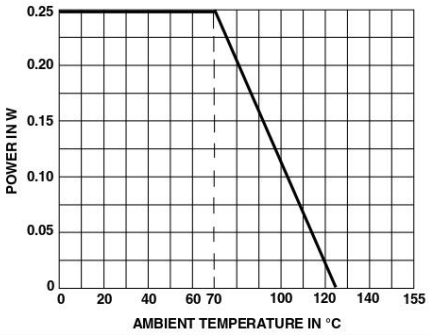
The TS53 trimming potentiometer has been designed for surface mount applications and offers volumetric efficiency (5 mm x 5 mm x 2.7 mm) with high performance and stability.

The TS53 design is suitable for both manual or automatic operation, and can withstand wave, and reflow soldering techniques.

DIMENSIONS in millimeters (± 0.25 mm)



Cruciform screwdriver slot
Ø 2.5, width 0.5
Deep: 0.55
Max. deep (center): 0.7

ELECTRICAL SPECIFICATIONS	
Resistive element	Cermet
Electrical travel	220° ± 15°
Resistance range	10 Ω to 1 MΩ
Standard series	1 - 2 - 5
Tolerance standard	± 20 %
Circuit diagram	
Power rating **linear**	0.25 W at + 70 °C 
Temperature coefficient	See Standard Resistance Element Data table
Limiting element voltage (linear law)	200 V
Contact resistance variation (typical)	1 % or 3 Ω
End resistance (typical)	0.1 % or 3 Ω
Dielectric strength (RMS)	1000 V
Insulation resistance	1 GΩ

MECHANICAL SPECIFICATIONS	
Mechanical travel	270 ° ± 10°
Operating torque (max. Ncm)	1.5
End stop torque (max. Ncm)	3.5
Unit weight (max. g)	0.15
Terminals	Pure Sn (e3)

ENVIRONMENTAL SPECIFICATIONS	
Temperature range	- 55 °C to + 125 °C
Climatic category	55/125/56
Sealing	Sealed container IP67
MSL level	4

SOLDERING RECOMMENDATIONS
Recommended reflow profile 2, see Application Note www.vishay.com/doc?52029
Caution
Reflow soldering must be done within 72 h while stored under a max. temperature of 30 °C, 60 % RH after opening the dry pack envelope.

RECOMMENDED METHOD OF STORAGE

Dry box storage is recommended as soon as the hermetic bag has been opened to prevent moisture absorption. The following conditions should be observed, if dry boxes are not available:

- Storage temperature 10 °C to 30 °C
- Storage humidity ≤ 60 % RH max.

After more than 72 h under these conditions, moisture content will be too high for reflow soldering.
In case of moisture absorption, the devices will recover to the former condition by drying under the following condition:
192 h at 40 °C + 5 °C/- 0 °C and < 5 % RH (dry air/nitrogen) or
96 h at 60 °C + 5 °C and < 5 % RH for all device containers (not suitable for reel) or
24 h at 125 °C + 5 °C (not suitable for reel)

PERFORMANCES

TESTS	CONDITIONS	TYPICAL VALUES AND DRIFTS		
		$\Delta R_T/R_T$ (%)	$\Delta R_{1\text{-}2}/R_{1\text{-}2}$ (%)	OTHER
Electrical endurance	1000 h at rated power 90'/30' - ambient temp. + 70 °C	± 2 %	± 3 %	Contact resistance variation: ΔR < 1 % Rn
Climatic sequence	Phase A dry heat 125 °C Phase B damp heat Phase C cold - 55 °C Phase D damp heat 5 cycles	± 2 %	± 3 %	
Damp heat steady state	Temperature 40 °C - RH 93 % 56 days	± 2 %	± 3 %	Dielectric strength: 1000 V_{RMS} Insulation resistance: > 10^4 MΩ
Charge of temperature	- 55 °C to + 125 °C - 5 cycles	± 1 %		$\Delta V_{1\text{-}2}/\Delta V_{1\text{-}3} \leq \pm 2$ %
Mechanical endurance	100 cycles - rated power	± (3 % + 5 Ω)		
Shock	50 *g* - 11 ms 3 successive shocks in 3 directions	± 1 %		$\Delta V_{1\text{-}2}/\Delta V_{1\text{-}3} \leq \pm 1$ %
Vibration	10 Hz to 55 Hz 0.75 mm or 10 *g* - 6 h	± 1 %		$\Delta V_{1\text{-}2}/\Delta V_{1\text{-}3} \leq \pm 1$ %

STANDARD RESISTANCE ELEMENT DATA

STANDARD RESISTANCE VALUES	LINEAR LAW			TYPICAL TCR - 55 °C + 125 °C
	MAX. POWER AT 70 °C	MAX. WORKING VOLTAGE	MAX. CURRENT THROUGH ELEMENT	
Ω	W	V	mA	ppm/°C
10	0.25	1.58	158	± 100
20	0.25	2.24	112	
50	0.25	3.54	71	
100	0.25	5.00	50	
200	0.25	7.07	35	
500	0.25	11.2	22	
1K	0.25	15.8	16	
2K	0.25	22.4	11	
5K	0.25	35.4	7	
10K	0.25	50.0	5	
20K	0.25	70.7	3.5	
50K	0.25	112	2.2	
100K	0.25	158	1.6	
200K	0.20	200	1.0	
500K	0.08	200	0.4	
1M	0.04	200	0.2	

MARKING

Vishay trademark, ohmic value, manufacturing date

The ohmic value is indicated by a 3 figure code, the first two are significant figures, the third one is the multiplier.
Example: 100 = 10 Ω
101 = 100 Ω
102 = 1000 Ω
503 = 50 000 Ω

PACKAGING

On tape and reel of 500 pieces, code R10 (TR500) and 2000 pieces, code R20 (TR2000)

Cover tape panel strength specifications EIA 481 A and CEI 60286-3.

DRYPACK
Devices are packed in moisture barrier bags to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.

ORDERING INFORMATION (part number)

T	S	5	3	Y	L	5	0	4	M	R	1	0				

MODEL	STYLE	OHMIC VALUE	TOLERANCE	PACKAGING	SPECIAL NUMBER
TS53	**YL** **YJ**	From 10 Ω to 1 MΩ **504** = 500 kΩ	**M** = 20 %	**R10** = Reel 500 pieces On request **R20** = Reel 2000 pieces	(If applicable) Given by Vishay for custom design

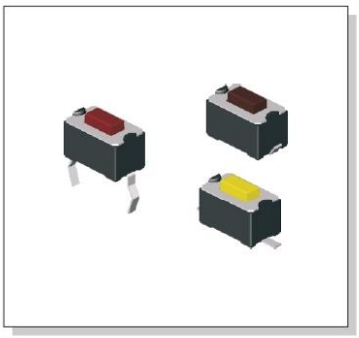
DESCRIPTION (for information only)

TS53	YL	500K	20 %		TR	e3
MODEL	STYLE	VALUE	TOLERANCE	SPECIAL	PACKAGING	LEAD (Pb)-FREE

5.- Pulsador de reset.

DTS-3,DTSM(L)-3 SERIES

3.5x6 Through Hole & SMT Type Tactile Switch



HOW TO ORDER

D T S [ ] 3 [ ] [ ] [ ] [ ]

- [ ]:Through Hole
  M:S.M.T/J-bend outward
  ML:S.M.T/Flat
  MF:S.M.T/Gull-wing
- 3.5x6mm
- Dimension H:
  1=4.3mm
  2=5.0mm
- Operating Force:
  N=Brown, 160gf
  R=Red, 260gf
  S=Salmon, 320gf
  Y=Yellow, 520gf
- Q=Halogen Free >Not Available For Halogen Free
- [ ]=Bag(Through Hole Only)
  B=Tube Package
  T/R=Tape & Reel

TACT SWITCH

SPECIFICATION

MECHANICAL

Operation Force: 520±130gf Yellow(Y)
320±80gf Salmon(S)
260±50gf Red(R)
160±50gf Brown(N)
Stroke: 0.25+0.2/-0.1mm

ENVIRONMENTAL

Operation Temperature Range: -25℃ to +70℃
Storage Temperature Range: -30℃ to +80℃

ELECTRICAL

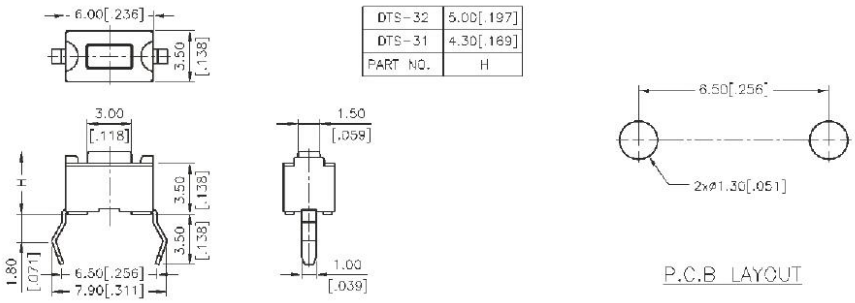
Electrical Life:
50,000 cycles for 160gf
30,000 cycles for 260gf, 320gf, 520gf
Rating: 50mA, 12VDC

PACKAGE

Tube: 135 pcs/tube
DTSM(L)-31: 1800 pcs/reel
DTSM(L)-32: 1600 pcs/reel
Bulk: 1000 pcs/bag

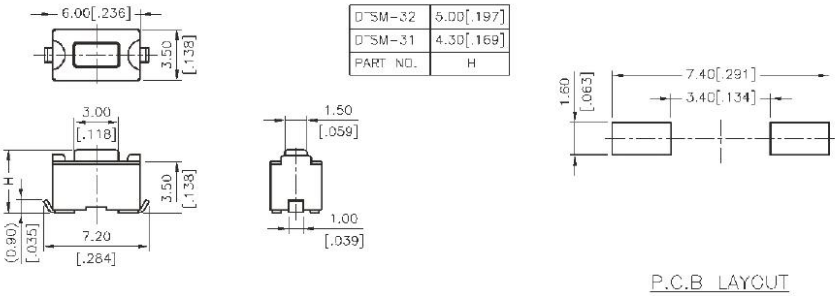
CIRCUIT

DTS-3



DTS-32	5.00[.197]
DTS-31	4.30[.169]
PART NO.	H

DTSM-3



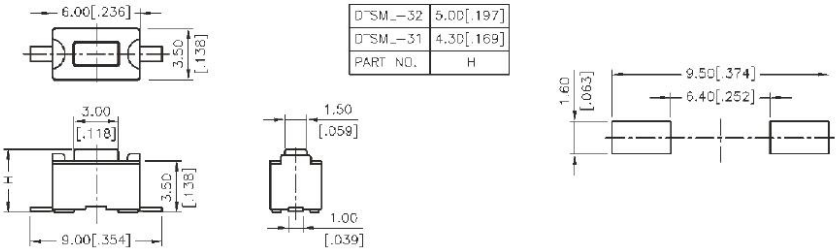
DTSM-32	5.00[.197]
DTSM-31	4.30[.169]
PART NO.	H

APEM

DTS-3,DTSM(L)-3 SERIES

3.5x6 Through Hole & SMT Type Tactile Switch

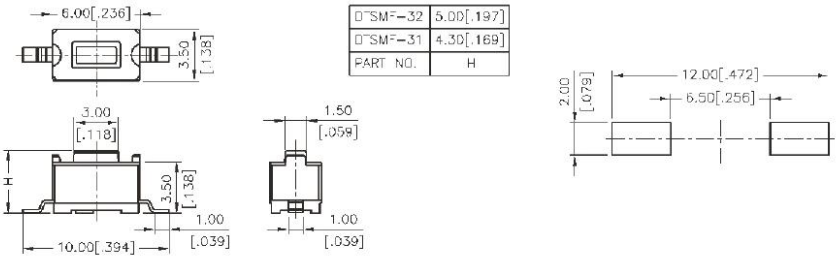
DTSML-3



DTSM-32	5.00[.197]
DTSM-31	4.30[.169]
PART NO.	H

P.C.B LAYOUT

DTSMF-3



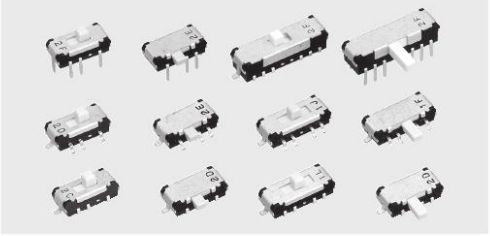
DTSMF-32	5.00[.197]
DTSMF-31	4.30[.169]
PART NO.	H

P.C.B LAYOUT

6.- Interruptor.

SLIDE SWITCHES (SMD) CMS

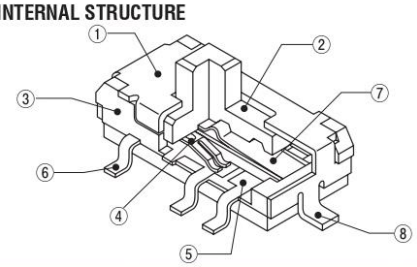
RoHS compliant



■ FEATURES

- RoHS compliant
- Excellent contact stability by twin Gold-plated contact mechanism
- Load life of 30,000 cycles
- Compatible with automatic mounting
- Withstands high soldering temperature

INTERNAL STRUCTURE



	Part name	Material	Flammability
①	Cover	Steel (SPCC), Tin-plated	—
②	Slider	Polyamide	UL94V-0
③	Housing		
④	Slider contact	Copper alloy, Gold-plated	—
⑤	Fixed contact		
⑥	Terminal pin		
⑦	Click spring	Copper alloy	
⑧	Ground terminal	Steel (SPCC), Tin-plated	

■ PART NUMBER DESIGNATION

CMS - 2 2 0 2 T B

Series name

No. of poles
2 : 2 poles
4 : 4 poles

No. of contacts
2 : 2 contacts
3 : 3 contacts
4 : 4 contacts

Setting position
0 : Top setting
1 : Side setting

Shape of terminal
A : J-hook
B : Gull wing
C : Through hole pins

Form of packaging
T : Taping (Reel)
W : Tray packaging (Through hole pins only)
Blank : Bulk in plastic bag

Knob length
2 : 2 mm
4 : 4 mm (2 poles · Side setting only)
6 : 6 mm (4 poles · Side setting only)

※ Please refer to the LIST OF PART NUMBERS when placing orders.

■ LIST OF PART NUMBERS

● 2 poles

Setting position	Shape of terminals	Knob length	Form of packaging	No. of contacts			Pieces in package
				2	3	4	
Top setting	A (J-hook)	2 mm	Taping	CMS-2202TA	CMS-2302TA	CMS-2402TA	900 pcs./reel
			Plastic bag	CMS-2202A	CMS-2302A	CMS-2402A	50 pcs./pack
	B (Gull wing)		Taping	CMS-2202TB	CMS-2302TB	CMS-2402TB	900 pcs./reel
			Plastic bag	CMS-2202B	CMS-2302B	CMS-2402B	50 pcs./pack
	C (Through hole pins)		Tray packaging	CMS-2202WC	CMS-2302WC	CMS-2402WC	50 pcs./tray
			Plastic bag	CMS-2202C	CMS-2302C	CMS-2402C	50 pcs./pack
Side setting	A (J-hook)	2 mm	Taping	CMS-2212TA	CMS-2312TA	CMS-2412TA	900 pcs./reel
			Plastic bag	CMS-2212A	CMS-2312A	CMS-2412A	50 pcs./pack
		4 mm	Taping	CMS-2214TA	CMS-2314TA	CMS-2414TA	900 pcs./reel
			Plastic bag	CMS-2214A	CMS-2314A	CMS-2414A	50 pcs./pack
	B (Gull wing)	2 mm	Taping	CMS-2212TB	CMS-2312TB	CMS-2412TB	900 pcs./reel
			Plastic bag	CMS-2212B	CMS-2312B	CMS-2412B	50 pcs./pack
		4 mm	Taping	CMS-2214TB	CMS-2314TB	CMS-2414TB	900 pcs./reel
			Plastic bag	CMS-2214B	CMS-2314B	CMS-2414B	50 pcs./pack
	Through hole pins	2 mm	Tray packaging	CMS-2212WC	CMS-2312WC	CMS-2412WC	50 pcs./tray
			Plastic bag	CMS-2212C	CMS-2312C	CMS-2412C	50 pcs./pack
		4 mm	Tray packaging	CMS-2214WC	CMS-2314WC	CMS-2414WC	50 pcs./tray
			Plastic bag	CMS-2214C	CMS-2314C	CMS-2414C	50 pcs./pack

● 4 poles

Setting position	Shape of terminals	Knob length	Form of packaging	No. of contacts	Pieces in package
				2	
Top setting	A (J-hook)	2 mm	Taping	CMS-4202TA	500 pcs./reel
			Plastic bag	CMS-4202A	25 pcs./pack
	B (Gull wing)		Taping	CMS-4202TB	500 pcs./reel
			Plastic bag	CMS-4202B	25 pcs./pack
	C (Through hole pins)		Tray packaging	CMS-4202WC	50 pcs./tray
			Plastic bag	CMS-4202C	25 pcs./pack
Side setting	A (J-hook)	6 mm	Taping	CMS-4216TA	500 pcs./reel
			Plastic bag	CMS-4216A	25 pcs./pack
	B (Gull wing)		Taping	CMS-4216TB	500 pcs./reel
			Plastic bag	CMS-4216B	25 pcs./pack
	C (Through hole pins)		Tray packaging	CMS-4216WC	50 pcs./tray
			Plastic bag	CMS-4216C	25 pcs./pack

※ Verify the above part numbers when placing orders.
Taping and tray version can be supplied only in reel or tray unit.

CMS
SLIDE SWITCHES (SMD)

■ STANDARD SPECIFICATIONS

Operating temp. range	— 40 ~ 85 °C
Storage temp. range	
Sealing	Non- Washable
Net weight	0.40 g (CMS-2202) 0.42 g (CMS-2214) 0.45 g (CMS-2302) 0.48 g (CMS-2314) 0.50 g (CMS-2402) 0.54 g (CMS-2414) 0.42 g (CMS-2212) 0.80 g (CMS-4202) 0.48 g (CMS-2312) 0.84 g (CMS-4216) 0.54 g (CMS-2412)

■ ELECTRICAL CHARACTERISTICS

Contact rating Non-switching Switching Minimum	DC50 V 100 mA DC12 V 100 mA DC20 mV 1 μ A
Contact timing	Non-shorting
Contact resistance	70 m Ω maximum
Insulation resistance	100 M Ω minimum (DC500 V)
Dielectric strength	AC500 V, 60 s

■ MECHANICAL CHARACTERISTICS

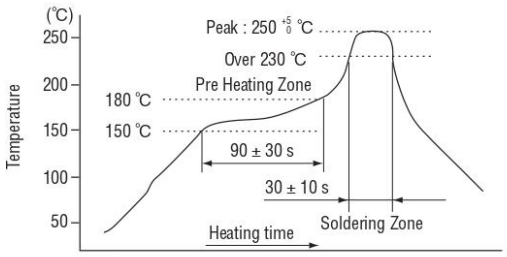
No. of positions	2, 3, 4
Stroke	2 mm
Operating force	1.5 ± 1 N {0.15 ± 0.1 kgf}
Stop strength	30N{3.06 kgf} 15 s (Top setting) 10N{1.02 kgf} 15 s (Side setting)
Solderability	245 ± 3 °C 2 ~ 3 s
Soldering heat	Reflow : 255 °C (Peak temperature) (Please refer to the profile below)
	Flow : 260 ± 3 °C、5~ 6 s
	Manual soldering : 350 ± 10 °C, 3 ~ 4 s
Shear (Adhesion)	50 N {5.09 kgf} 10 s
Substrate bending	Width 90 mm, bend 3 mm, 5 s, 1 time
Pull-off strength	50 N {5.09 kgf} 10 s

{ } : Reference only

■ ENVIRONMENTAL CHARACTERISTICS

Vibration	(Amplitude) 1.5 mmor (Acceleration) 98 m/s², 10-500-10 Hz, 3 directions for 10 cycles each
Shock	490 m/s², 11 ms, sinusoidal wave half cycle, 6 directions for 3 times each
Load life	Continuous load 30000 cycles, DC12 ± 0.5 V, 100 ± 10 mA
Humidity	40 °C, Relative humidity 90 ~ 95 %, 240 h, No load
High temp. exposure	85 °C, 96 h, No load
Low temp. exposure	— 40 °C, 96 h, No load
Thermal shock	— 40 (0.5 h) ~ 85 °C (0.5 h), 5 cycles

〈Reflow profile for soldering heat evaluation〉

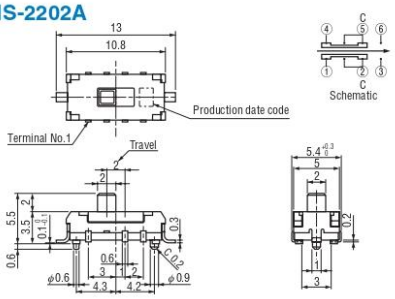


Reflow : two times maximum

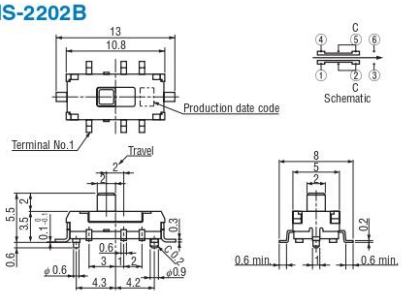
■ OUTLINE DIMENSIONS

Unless otherwise specified, tolerance : ± 0.3 (Unit : mm)

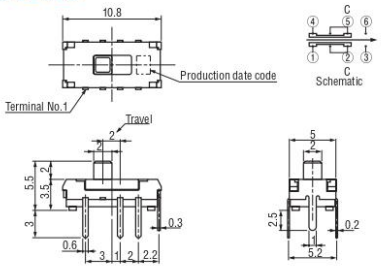
● CMS-2202A



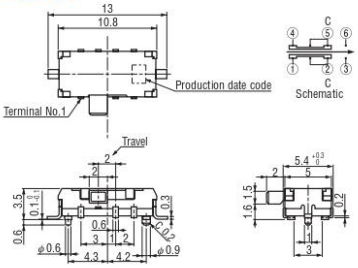
● CMS-2202B



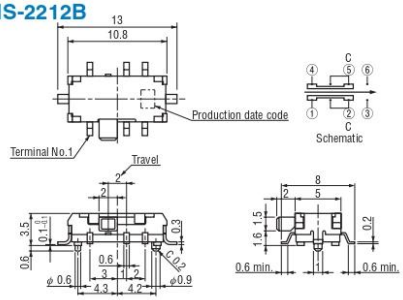
● CMS-2202C



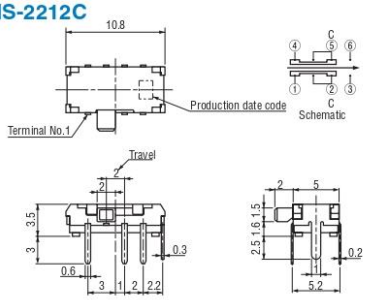
● CMS-2212A



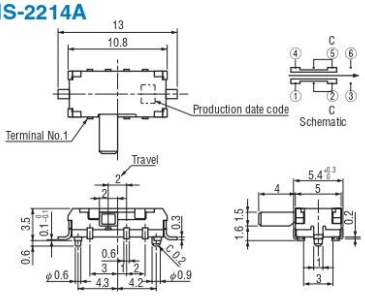
● CMS-2212B



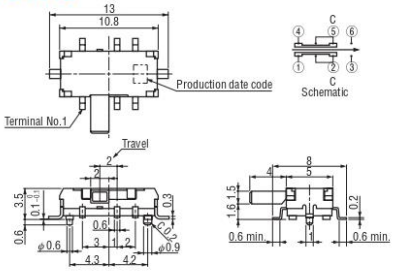
● CMS-2212C



● CMS-2214A



● CMS-2214B

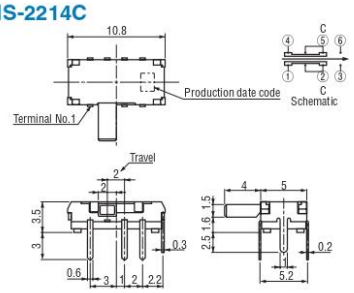


CMS
SLIDE SWITCHES (SMD)

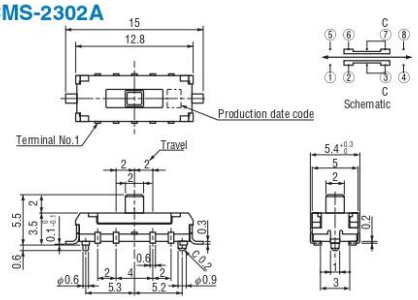
■ OUTLINE DIMENSIONS

Unless otherwise specified, tolerance : ± 0.3 (Unit : mm)

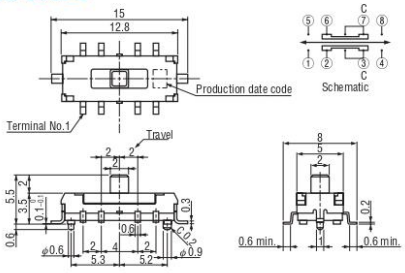
● CMS-2214C



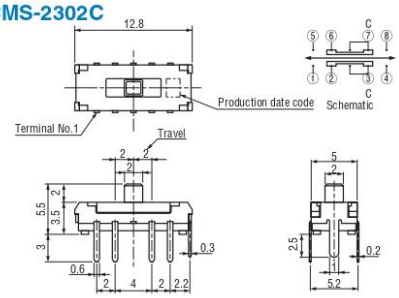
● CMS-2302A



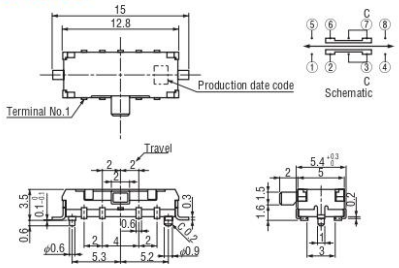
● CMS-2302B



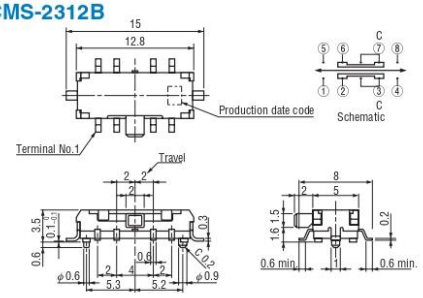
● CMS-2302C



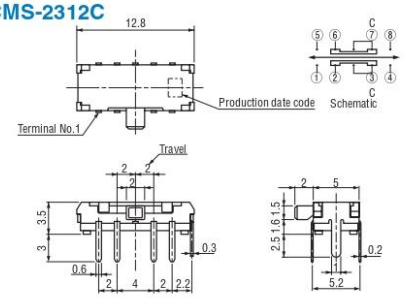
● CMS-2312A



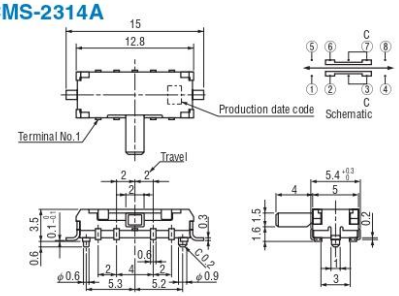
● CMS-2312B



● CMS-2312C



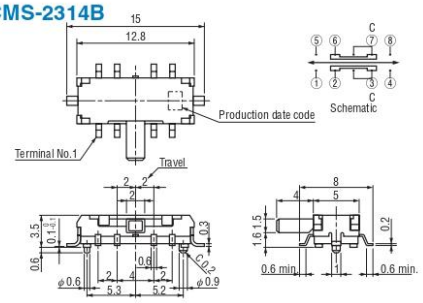
● CMS-2314A



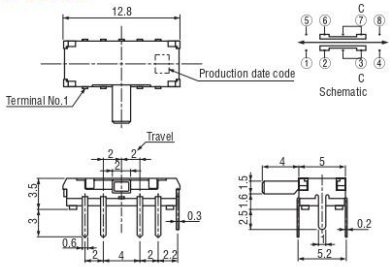
■ OUTLINE DIMENSIONS

Unless otherwise specified, tolerance : ± 0.3 (Unit : mm)

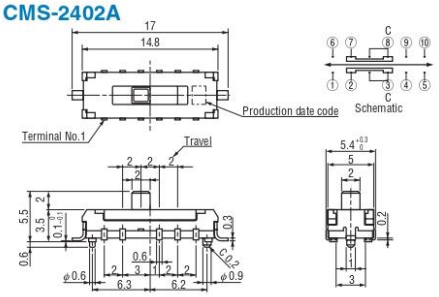
● CMS-2314B



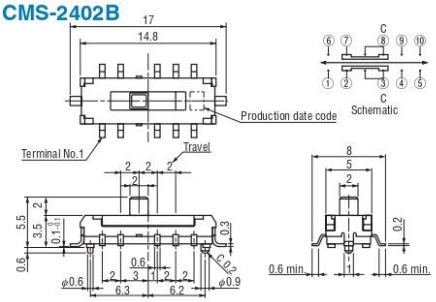
● CMS-2314C



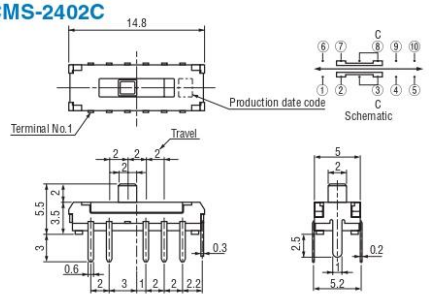
● CMS-2402A



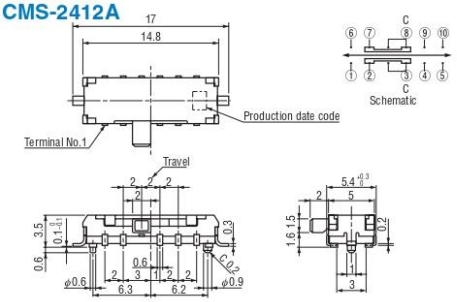
● CMS-2402B



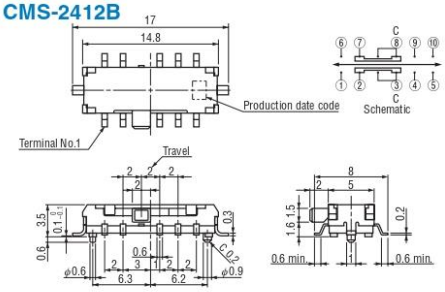
● CMS-2402C



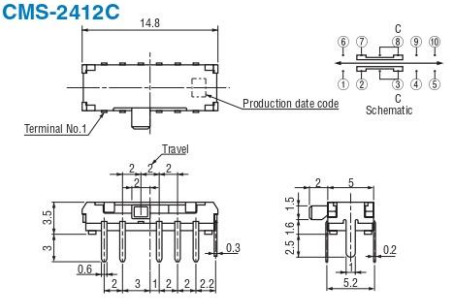
● CMS-2412A



● CMS-2412B



● CMS-2412C

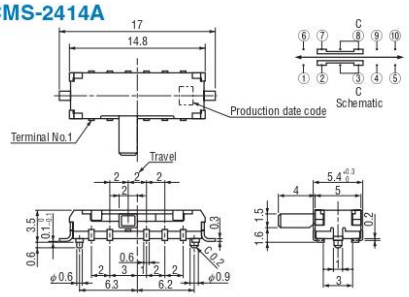


CMS
SLIDE SWITCHES (SMD)

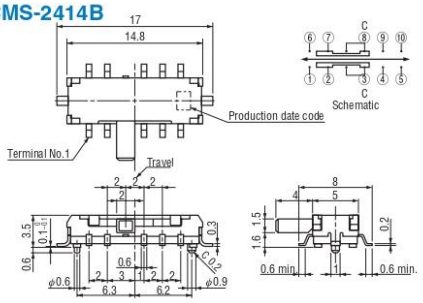
■ OUTLINE DIMENSIONS

Unless otherwise specified, tolerance : ± 0.3 (Unit : mm)

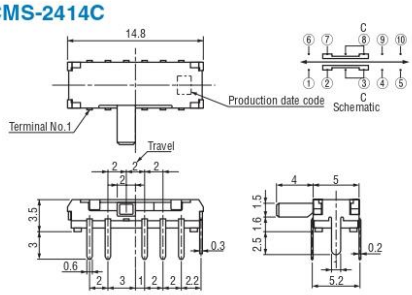
● CMS-2414A



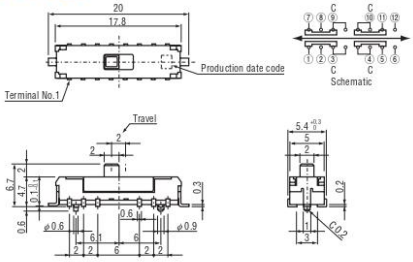
● CMS-2414B



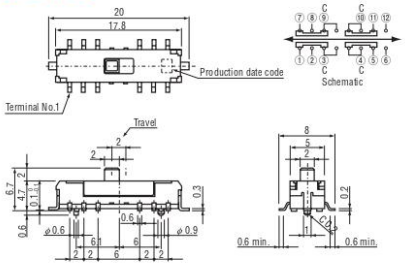
● CMS-2414C



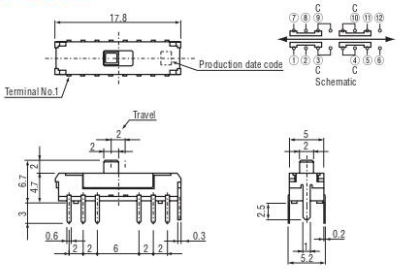
● CMS-4202A



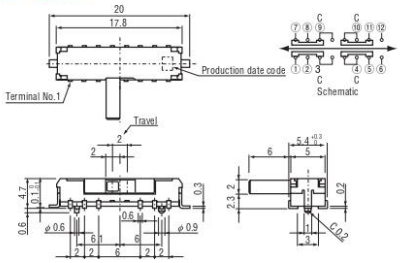
● CMS-4202B



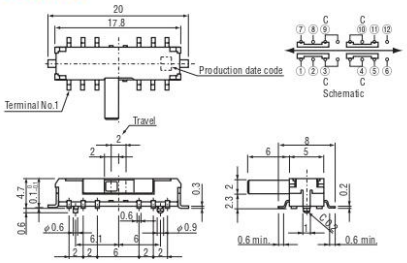
● CMS-4202C



● CMS-4216A



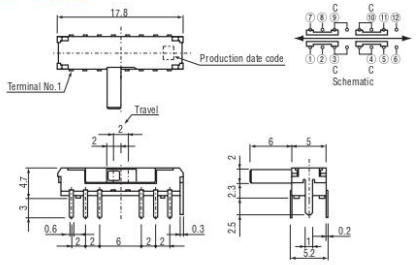
● CMS-4216B



■ OUTLINE DIMENSIONS

Unless otherwise specified, tolerance : ± 0.3 (Unit : mm)

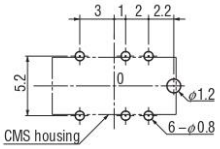
● CMS-4216C



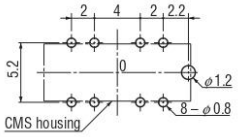
■ SIZE OF P.C.B. PROCESSING

(Unit : mm)

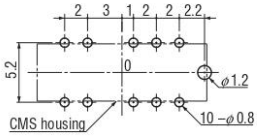
● CMS-22□□C



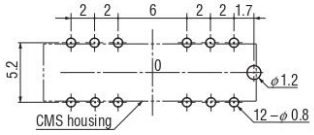
● CMS-23□□C



● CMS-24□□C



● CMS-42□□C

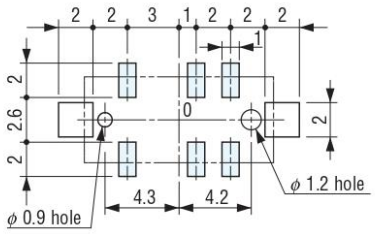


CMS
SLIDE SWITCHES (SMD)

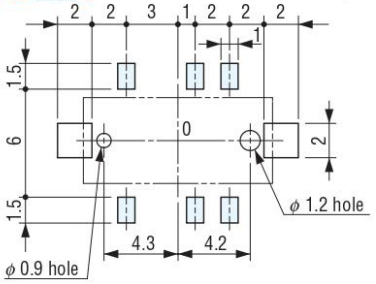
■ RECOMMENDED P.C.B. PAD OUTLINE DIMENSIONS

(Unit : mm)

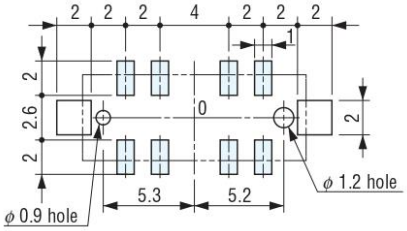
● CMS-22□□A



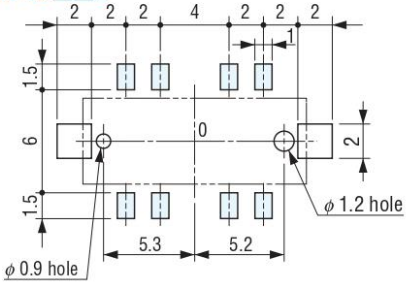
● CMS-22□□B



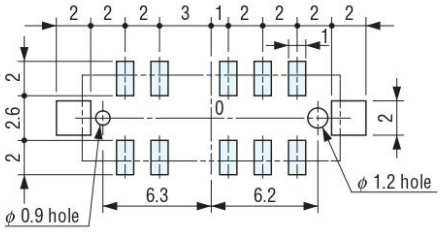
● CMS-23□□A



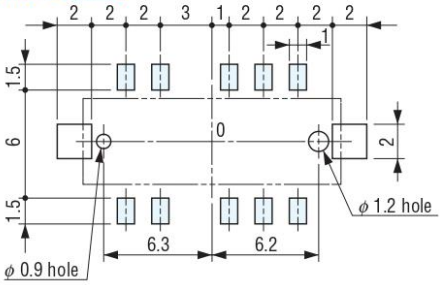
● CMS-23□□B



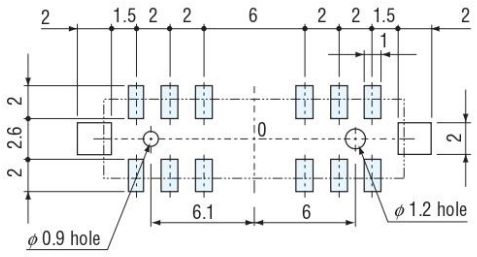
● CMS-24□□A



● CMS-24□□B

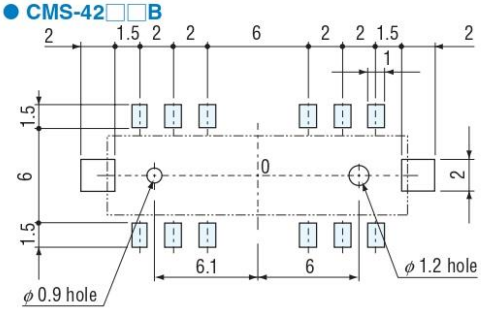


● CMS-42□□A



Note) The zero point is the center of mounting.

● CMS-42□□B



■ PACKAGING SPECIFICATIONS

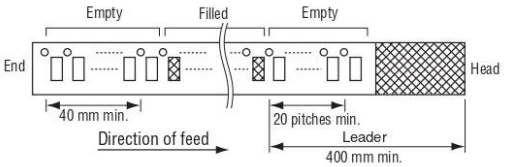
<Taping packaging specifications>

● CMS-2 □□□□ type is packaged in 900 pcs. per reel. Orders will be accepted for units of 900 pcs., i.e., 900, 1800, 2700 pcs., etc. CMS-4 type is packaged in packaged in 500 pcs. per reel. Orders will be accepted for units of 500 pcs.

● Taping version is boxed with one reel.

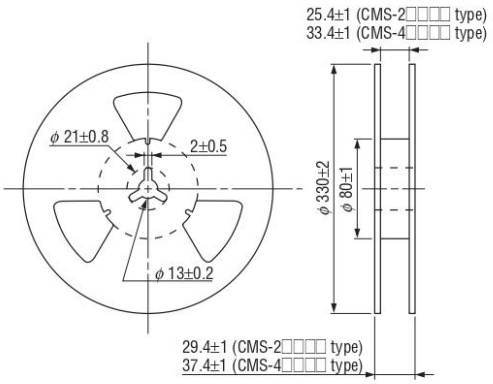
Maximum number of consecutive missing pieces=2
Leader length and reel dimension are shown in the diagrams below:

● Embossed tape dimensions



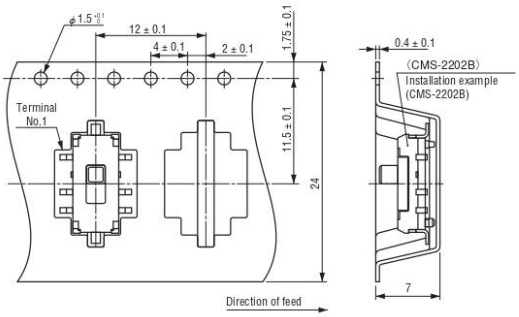
● Reel dimensions

(Unit: mm)
(Conforms to JIS C 0806)
(In accordance with EIAJ ET-7200A)



● CMS-2202TA, TB

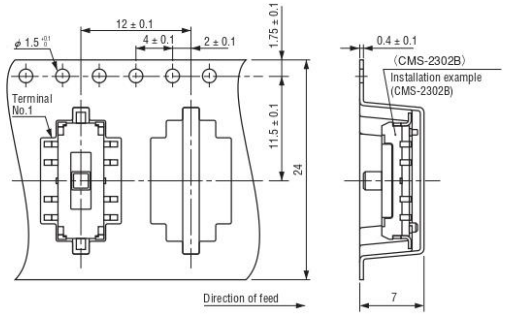
(Unit : mm)
(Conforms to JIS C 0806)



CMS
SLIDE SWITCHES (SMD)

● CMS-2302TA, TB

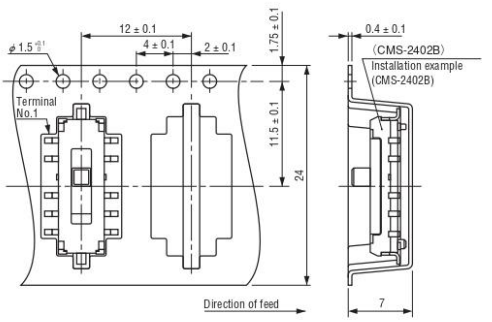
(Conforms to JIS C 0806)



● CMS-2402TA, TB

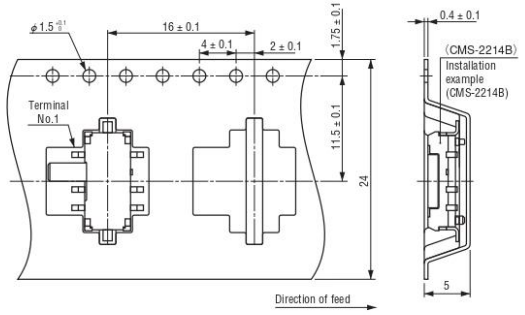
(Unit : mm)

(Conforms to JIS C 0806)



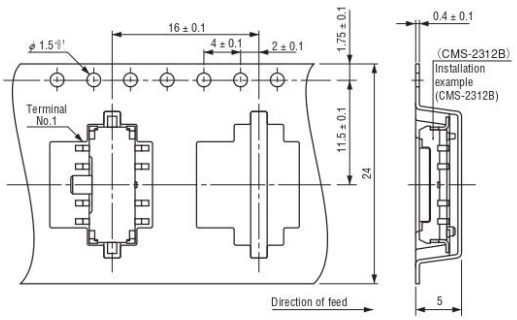
● CMS-2212 • 2214TA, TB

(Conforms to JIS C 0806)



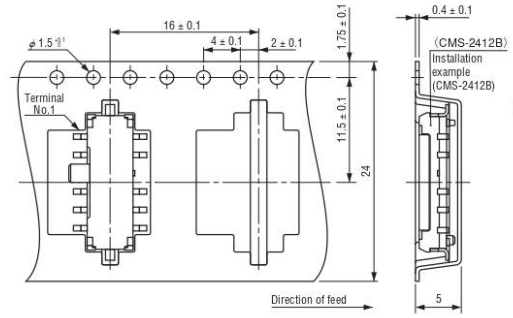
● CMS-2312 • 2314TA, TB

(Conforms to JIS C 0806)



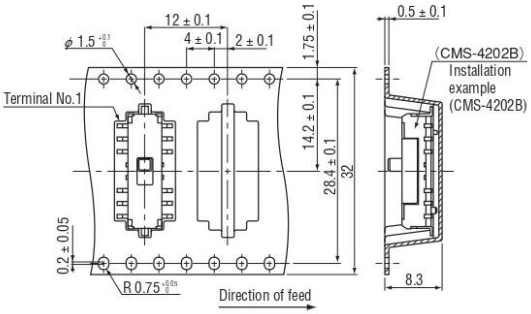
● CMS-2412 • 2414TA, TB

(Conforms to JIS C 0806)



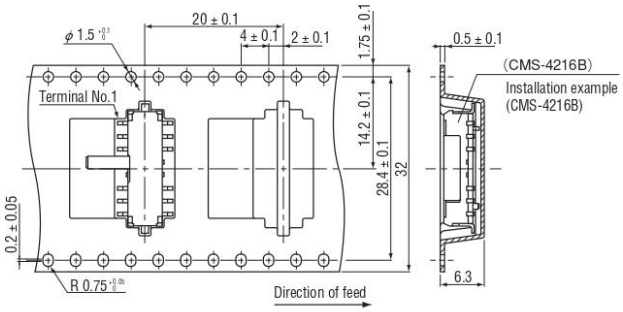
● CMS-4202TA, TB

(Conforms to JIS C 0806)



● CMS-4216TA, TB

(Unit : mm)
(Conforms to JIS C 0806)



<Tray packaging specifications>

- Tray version is packaged in 50 pcs. per tray. Orders will be accepted for units of 50 pcs., i. e., 50, 100, 150 pcs. etc.
- Tray version is boxed with 10 trays.

<Bulk pack specifications>

- The smallest unit of bulk pack in a plastic bag is 10 pcs. per pack.
  Orders will be accepted for unit of minimum 10 pcs., i.e., 10, 20, 30 pcs., etc.
- Boxing of bulk in plastic bag is performed with 50 pcs. (standard 100 pcs. / CMS-2 □□□□ , 50 pcs. / CMS-4 □□□□) per box.

7.- 74LS390

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS185C

CD74HC390, CD54HCT390, CD74HCT390

High-Speed CMOS Logic Dual Decade Ripple Counter

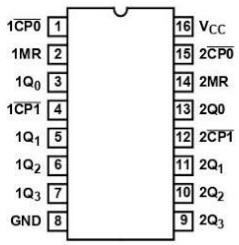
September 1997 - Revised October 2003

Features

- Two BCD Decade or Bi-Quinary Counters
- One Package Can Be Configured to Divide-by-2, 4, 5,10, 20, 25, 50 or 100
- Two Master Reset Inputs to Clear Each Decade Counter Individually
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
  - CMOS Input Compatibility, $I_I \le 1\mu A$ at V_{OL}, V_{OH}

Pinout

CD54HCT390
(CERDIP)
CD74HC390, CD74HCT390
(PDIP, SOIC)
TOP VIEW



Description

The CD74HC390 and 'HCT390 dual 4-bit decade ripple counters are high-speed silicon-gate CMOS devices and are pin compatible with low-power Schottky TTL (LSTTL). These devices are divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD decade or bi-quinary configuration, since they share a common master reset (nMR). If the two master reset inputs (1MR and 2MR) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clock inputs (n$\overline{CP0}$ and n$\overline{CP1}$) of each section allow ripple counter or frequency division applications of divide-by-2, 4. 5, 10, 20, 25, 50 or 100. Each section is triggered by the High-to-Low transition of the input pulses (n$\overline{CP0}$ and n$\overline{CP1}$).

For BCD decade operation, the nQ0 output is connected to the n$\overline{CP1}$ input of the divide-by-5 section. For bi-quinary decade operation, the nO3 output is connected to the n$\overline{CP0}$ input and nQ_0 becomes the decade output.

The master reset inputs (1MR and 2MR) are active-High asynchronous inputs to each decade counter which operates on the portion of the counter identified by the "1" and "2" prefixes in the pin configuration. A High level on the nMR input overrides the clock and sets the four outputs Low.

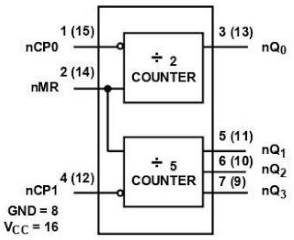
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HCT390F3A	-55 to 125	16 Ld CERDIP
CD74HC390E	-55 to 125	16 Ld PDIP
CD74HC390M	-55 to 125	16 Ld SOIC
CD74HC390MT	-55 to 125	16 Ld SOIC
CD74HC390M96	-55 to 125	16 Ld SOIC
CD74HCT390E	-55 to 125	16 Ld PDIP
CD74HCT390M	-55 to 125	16 Ld SOIC
CD74HCT390MT	-55 to 125	16 Ld SOIC
CD74HCT390M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram



TRUTH TABLE

INPUTS		ACTION
CP	MR	
↑	L	No Change
↓	L	Count
X	H	All Qs Low

H = High Voltage Level, L = Low Voltage Level, X = Don't Care,
↑ = Transition from Low to High Level, ↓ = Transition from High to Low.

BCD COUNT SEQUENCE FOR 1/2 THE 390

COUNT	OUTPUTS			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

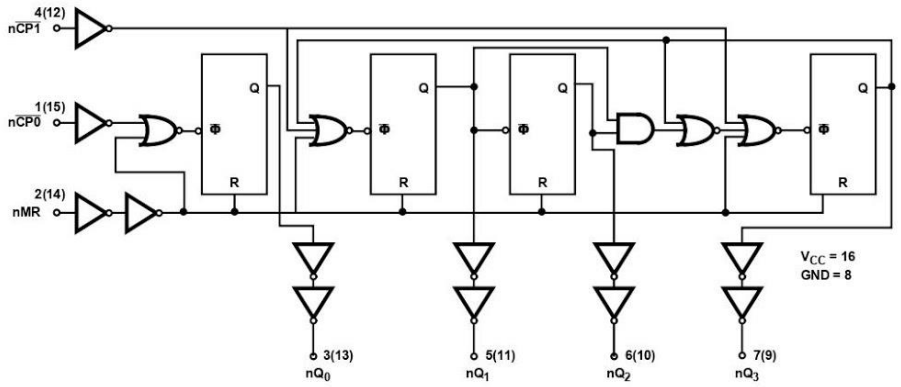
Output nQ0 connected to $n\overline{CP1}$ with counter input on $n\overline{CP0}$.

B-QUINARY COUNT SEQUENCE FOR 1/2 THE 390

COUNT	OUTPUTS			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	H	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

Output nQ3 connected to $n\overline{CP0}$ with counter input on $n\overline{CP1}$.

Logic Diagram



Absolute Maximum Ratings

DC Supply Voltage, V_{CC} ..... -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V ..... ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V ..... ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V ..... ±25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} ..... ±50mA

Operating Conditions

Temperature Range (T_A) ..... -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types ..... 2V to 6V
HCT Types ..... 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O ..... 0V to V_{CC}
Input Rise and Fall Time
2V ..... 1000ns (Max)
4.5V ..... 500ns (Max)
6V ..... 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
E (PDIP) Package 67
M (SOIC) Package 73
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 2)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
$n\overline{CP0}$	0.45
$n\overline{CP1}$, MR	0.6

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Prerequisite for Switching Specifications

CHARACTERISTIC	SYMBOL	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES										
Maximum Clock Frequency	f_{MAX}	2	6	-	-	5	-	4	-	MHz
		4.5	30	-	-	24	-	20	-	MHz
		6	35	-	-	28	-	24	-	MHz
Clock Pulse Width, $n\overline{CP0}$, $n\overline{CP1}$	t_W	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns

Prerequisite for Switching Specifications (Continued)

CHARACTERISTIC	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Reset Removal Time	t_{REM}	2	70	-	-	90	-	105	-	ns
		4.5	14	-	-	18	-	21	-	ns
		6	12	-	-	15	-	18	-	ns
Reset Pulse Width	t_W	2	50	-	-	65	-	75	-	ns
		4.5	10	-	-	13	-	15	-	ns
		6	9	-	-	11	-	13	-	ns
HCT TYPES										
Maximum Clock Frequency	f_{MAX}	4.5	27	-	-	22	-	18	-	MHz
Clock Pulse Width, $n\overline{CP0}$, $n\overline{CP1}$	t_W	4.5	19	-	-	24	-	29	-	ns
Reset Removal Time	t_{REM}	4.5	15	-	-	19	-	22	-	ns
Reset Pulse Width	t_W	4.5	13	-	-	16	-	20	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay (Figure 1) $n\overline{CP0}$ to nQ_0	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
		C_L =15pF	5	-	14	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	30	-	37	-	45	ns
$n\overline{CP1}$ to nQ_1	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	185	-	230	-	280	ns
			4.5	-	-	37	-	46	-	56	ns
			6	-	-	31	-	39	-	48	ns
$n\overline{CP1}$ to nQ_2	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	245	-	305	-	370	ns
			4.5	-	-	49	-	61	-	74	ns
			6	-	-	42	-	52	-	63	ns
$n\overline{CP1}$ to nQ_3	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	180	-	225	-	270	ns
			4.5	-	-	36	-	45	-	54	ns
			5	-	15	-	-	-	-	-	ns
			6	-	-	31	-	38	-	46	ns
$n\overline{CP0}$ to nQ3 (nQ_0 connected to $n\overline{CP1}$)	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	365	-	455	-	550	ns
			4.5	-	-	73	-	91	-	110	ns
			6	-	-	62	-	77	-	94	ns
MR to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	190	-	240	-	285	ns
			4.5	-	-	38	-	48	-	57	ns
		C_L =15pF	5	-	16	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	32	-	41	-	48	ns

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Output Transition Time (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_{IN}	C_L = 50pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	C_L =15pF	5	-	28	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay (Figure 1)	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	40	-	50	-	60	ns
$n\overline{CP0}$ to nQ_0		C_L =15pF	5	-	17	-	-	-	-	-	ns
$n\overline{CP1}$ to nQ_1	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	43	-	51	-	65	ns
$n\overline{CP1}$ to nQ_2	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	55	-	69	-	83	ns
$n\overline{CP1}$ to nQ_3	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	42	-	53	-	63	ns
		C_L =15pF	5	-	18	-	-	-	-	-	ns
$n\overline{CP0}$ to nQ2 (nQ_0 connected to $n\overline{CP1}$)	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	84	-	105	-	126	ns
MR to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	42	-	53	-	63	ns
		C_L =15pF	5	-	18	-	-	-	-	-	ns
Output Transition	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_{IN}	C_L =15pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	C_L =15pF	5	-	32	-	-	-	-	-	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per multiplexer.
4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

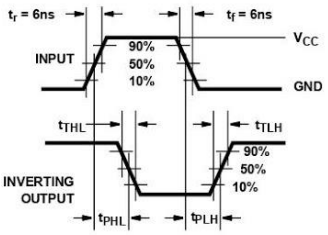


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

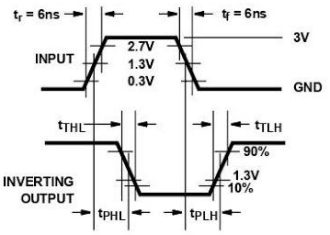


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

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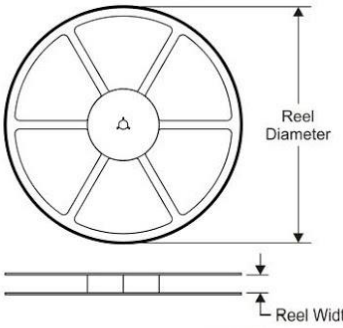
PACKAGE MATERIALS INFORMATION

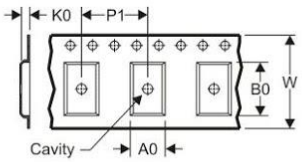
19-Mar-2008

TAPE AND REEL INFORMATION

REEL DIMENSIONS

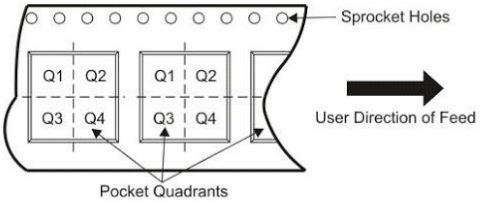


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC390M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT390M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

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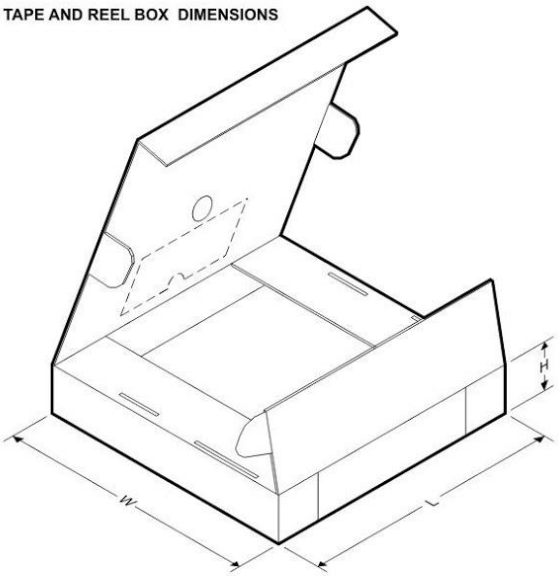
PACKAGE MATERIALS INFORMATION

19-Mar-2008

TAPE AND REEL BOX DIMENSIONS



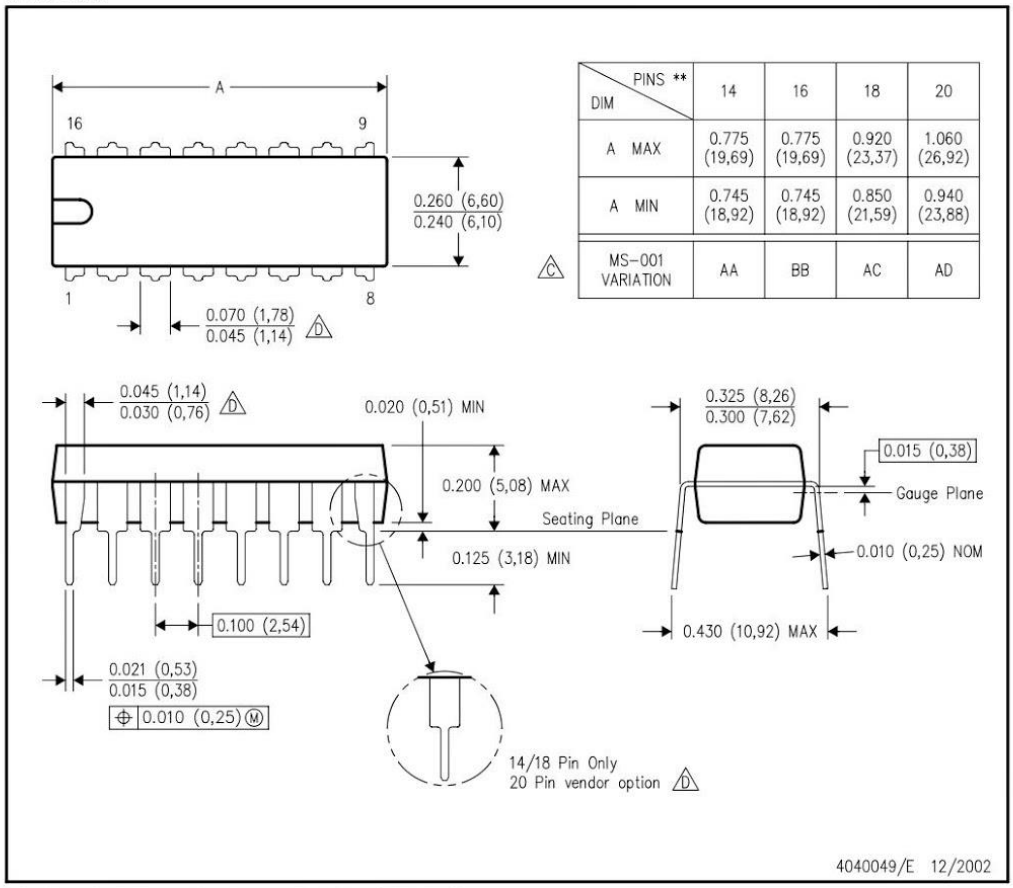
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC390M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT390M96	SOIC	D	16	2500	333.2	345.9	28.6

MECHANICAL DATA

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

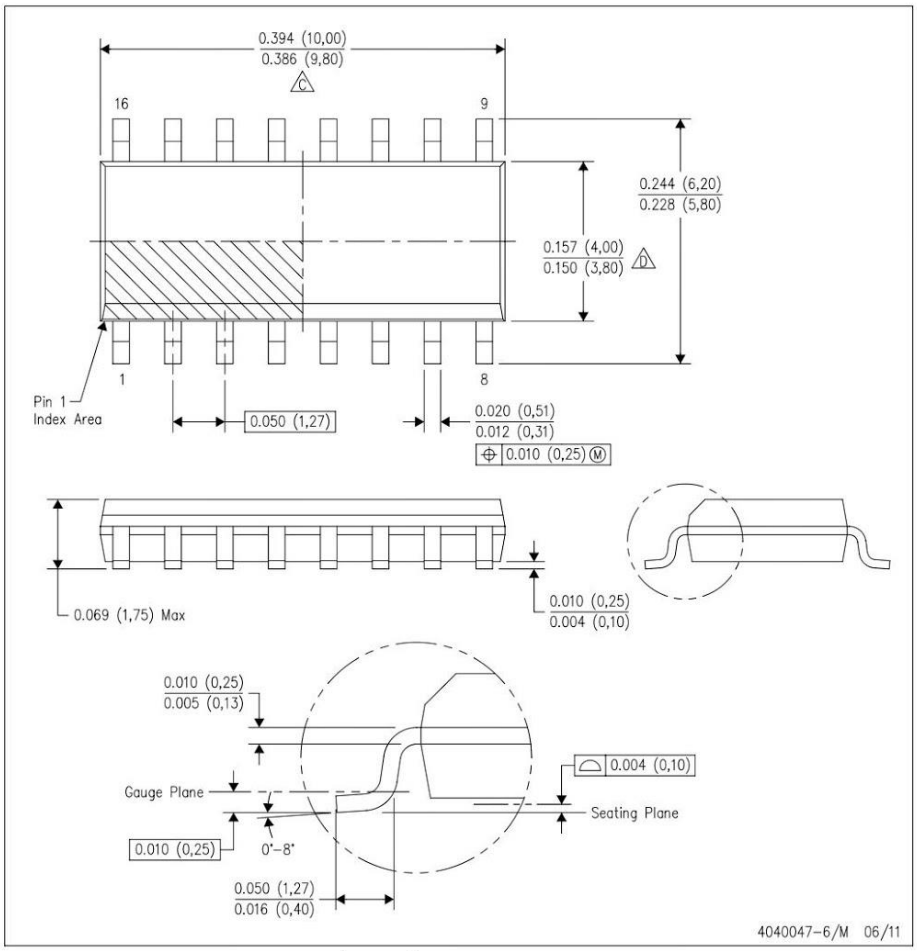


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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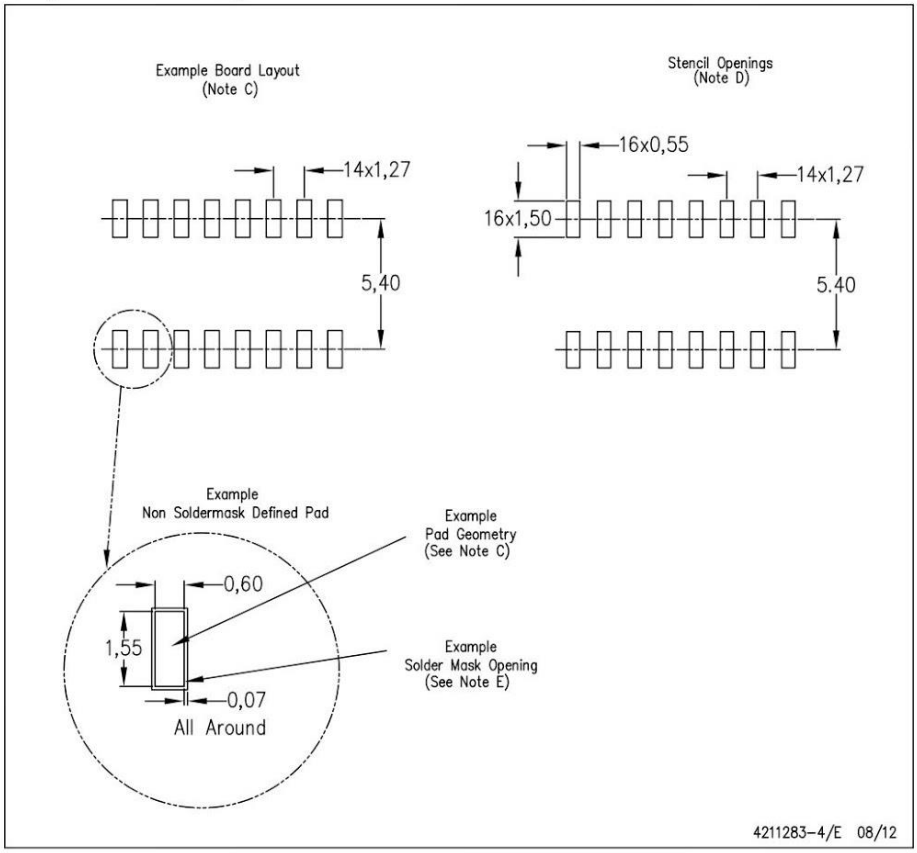
LAND PATTERN DATA

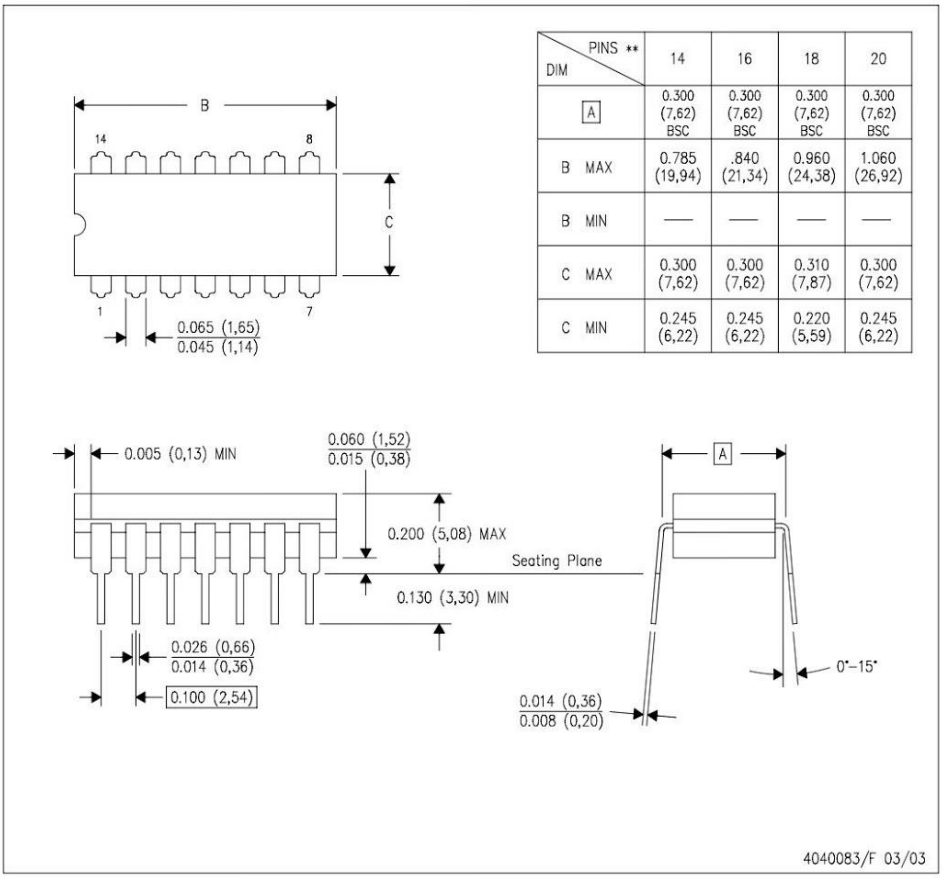
D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

8.- 74LS374

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS183C

February 1998 - Revised May 2004

CD54/74HC374, CD54/74HCT374, CD54/74HC574, CD54/74HCT574

High-Speed CMOS Logic Octal D-Type Flip-Flop, 3-State Positive-Edge Triggered

Features

- Buffered Inputs
- Common Three-State Output Enable Control
- Three-State Outputs
- Bus Line Driving Capability
- Typical Propagation Delay (Clock to Q) = 15ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2-V to 6-V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
  - 4.5-V to 5.5-V Operation
  - Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
  - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

Description

The 'HC374, 'HCT374, 'HC574, and 'HCT574 are octal D-type flip-flops with 3-state outputs and the capability to drive 15 LSTTL loads. The eight edge-triggered flip-flops enter data into their registers on the LOW to HIGH transition of clock (CP). The output enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state. The 374 and 574 are identical in function and differ only in their pinout arrangements.

Ordering Information

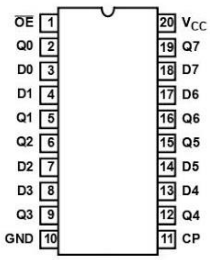
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC374F3A	-55 to 125	20 Ld CERDIP
CD54HC574F3A	-55 to 125	20 Ld CERDIP
CD54HCT374F3A	-55 to 125	20 Ld CERDIP
CD54HCT574F3A	-55 to 125	20 Ld CERDIP
CD74HC374E	-55 to 125	20 Ld PDIP
CD74HC374M	-55 to 125	20 Ld SOIC
CD74HC374M96	-55 to 125	20 Ld SOIC
CD74HC574E	-55 to 125	20 Ld PDIP
CD74HC574M	-55 to 125	20 Ld SOIC
CD74HC574M96	-55 to 125	20 Ld SOIC
CD74HCT374E	-55 to 125	20 Ld PDIP
CD74HCT374M	-55 to 125	20 Ld SOIC
CD74HCT374M96	-55 to 125	20 Ld SOIC
CD74HCT574E	-55 to 125	20 Ld PDIP
CD74HCT574M	-55 to 125	20 Ld SOIC
CD74HCT574M96	-55 to 125	20 Ld SOIC
CD74HCT574PWR	-55 to 125	20 Ld TSSOP

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel.

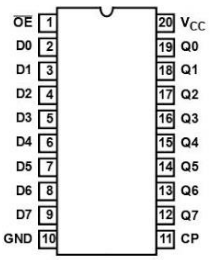
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Pinouts

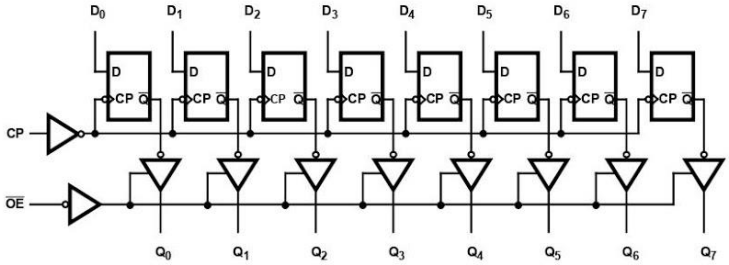
CD54HC374, CD54HCT374
(CERDIP)
CD74HC374, CD74HCT374
(PDIP, SOIC)
TOP VIEW



CD54HC574, CD54HCT574
(CERDIP)
CD74HC574
(PDIP, SOIC)
CD74HCT574
(PDIP, SOIC, TSSOP)
TOP VIEW



Functional Diagram



TRUTH TABLE

INPUTS			OUTPUT
$\overline{OE}$	CP	Dn	Qn
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z

H = High Level (Steady State)
L = Low Level (Steady State)
X= Don't Care
↑= Transition from Low to High Level
Q0= The level of Q before the indicated steady-state input conditions were established
Z = High Impedance State

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Drain Current, per Output, I_O
For -0.5V < V_O < V_{CC} + 0.5V . . . . . ±35mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V . . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 1) . . . . . θ_{JA} (°C/W)
E (PDIP) Package 69
M (SOIC) Package 58
PW (TSSOP) Package 83
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating, and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA
Three- State Leakage Current	V_{IL} or V_{IH}	$V_O = V_{CC}$ or GND	-	6	-	-	±0.5	-	±5.0	-	±10	µA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	0	5.5	-		±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Three- State Leakage Current	V_{IL} or V_{IH}	$V_O = V_{CC}$ or GND	-	6	-	-	±0.5	-	±5.0	-	±10	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 2)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

2. For dual-supply systems, theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS	
	HCT374	HCT574
D0 - D7	0.3	0.4
CP	0.9	0.75
$\overline{OE}$	1.3	0.6

NOTE: Unit Load is ΔI_{CC} limit specific in DC Electrical Specifications Table, e.g., 360µA max. at 25°C.

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
Maximum Clock Frequency	f_{MAX}	2	6	-	-	5	-	-	4	-	-	MHz
		4.5	30	-	-	25	-	-	20	-	-	MHz
		6	35	-	-	29	-	-	23	-	-	MHz
Clock Pulse Width	t_W	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
Setup Time Data to Clock	t_{SU}	2	60	-	-	75	-	-	90	-	-	ns
		4.5	12	-	-	15	-	-	18	-	-	ns
		6	10	-	-	13	-	-	15	-	-	ns
Hold Time Data to Clock	t_H	2	5	-	-	5	-	-	5	-	-	ns
		4.5	5	-	-	5	-	-	5	-	-	ns
		6	5	-	-	5	-	-	5	-	-	ns
HCT TYPES												
Maximum Clock Frequency	f_{MAX}	4.5	30	-	-	25	-	-	20	-	-	MHz
Clock Pulse Width	t_W	4.5	16	-	-	20	-	-	24	-	-	ns
Setup Time Data to Clock	t_{SU}	4.5	12	-	-	15	-	-	18	-	-	ns
Hold Time Data to Clock	t_H	4.5	5	-	-	5	-	-	5	-	-	ns

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay Clock to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	165	-	205	-	250	ns
			4.5	-	-	33	-	41	-	50	ns
		C_L = 15pF	5	-	15	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	28	-	35	-	43	ns
Output Disable to Q	t_{PLZ}, t_{PHZ}	C_L = 50pF	2	-	-	135	-	170	-	205	ns
			4.5	-	-	27	-	34	-	41	ns
		C_L = 15pF	5	-	11	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	23	-	29	-	35	ns

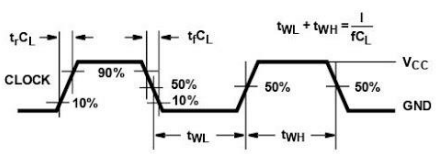
Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Output Enable to Q	t_{PZL}, t_{PZH}	C_L = 50pF	2	-	-	150	-	190	-	225	ns
			4.5	-	-	30	-	38	-	45	ns
		C_L = 15pF	5	-	12	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	26	-	33	-	38	ns
Maximum Clock Frequency	f_{MAX}	C_L = 15pF	5	-	60	-	-	-	-	-	MHz
Output Transition Time	t_{THL}, t_{TLH}	C_L = 50pF	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
			6	-	-	10	-	13	-	15	ns
Input Capacitance	C_I	C_L = 50pF	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	C_O	-	-	20	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	C_L = 15pF	5	-	39	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay Clock to Output	t_{PHL}, t_{PLH}	C_L = 50pF	4.5	-	-	33	-	41	-	50	ns
		C_L = 15pF	5	-	15	-	-	-	-	-	ns
Output Disable to Q	t_{PLZ}, t_{PHZ}	C_L = 50pF	4.5	-	-	28	-	35	-	42	ns
		C_L = 15pF	5	-	11	-	-	-	-	-	ns
Output Enable to Q	t_{PZL}, t_{PZH}	C_L = 50pF	4.5	-	-	30	-	38	-	45	ns
		C_L = 15pF	5	-	12	-	-	-	-	-	ns
Maximum Clock Frequency	f_{MAX}	C_L = 15pF	5	-	60	-	-	-	-	-	MHz
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	12	-	15	-	18	ns
Input Capacitance	C_I	C_L = 50pF	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	C_O	-	-	20	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	C_L = 15pF	5	-	47	-	-	-	-	-	pF

NOTES:

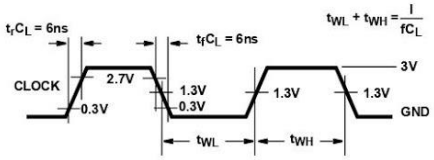
3. C_{PD} is used to determine the dynamic power consumption, per package.
4. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma V_{CC}^2 f_O C_L$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

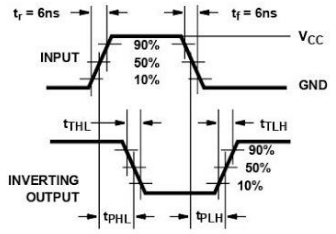


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

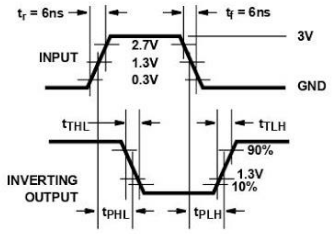


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

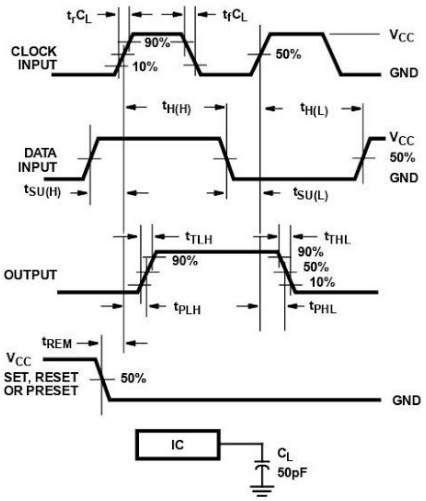


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

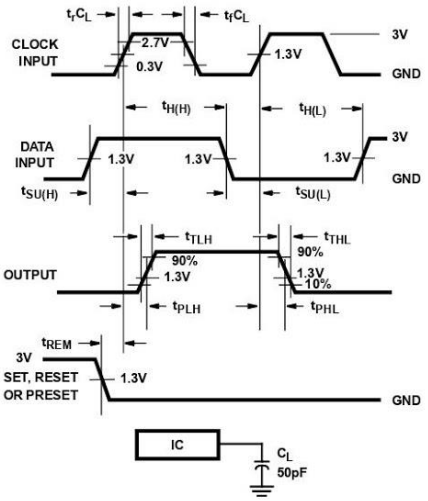


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Test Circuits and Waveforms (Continued)

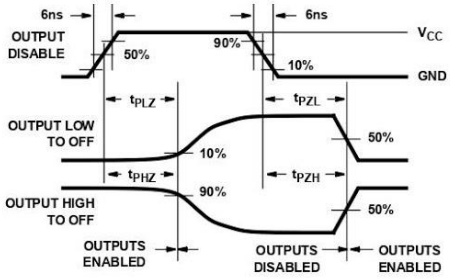


FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

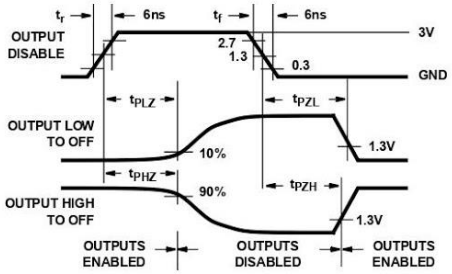
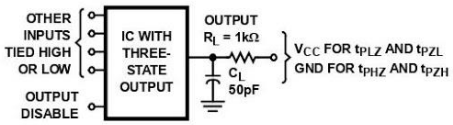


FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

TEXAS INSTRUMENTS

PACKAGE MATERIALS INFORMATION

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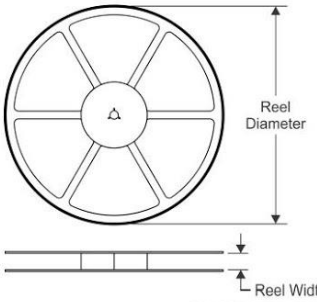
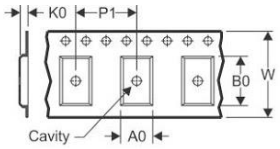
TAPE AND REEL INFORMATION

REEL DIMENSIONS

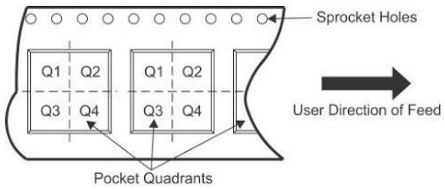


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC374M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HC574M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT374M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT574M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT574PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TEXAS INSTRUMENTS

PACKAGE MATERIALS INFORMATION

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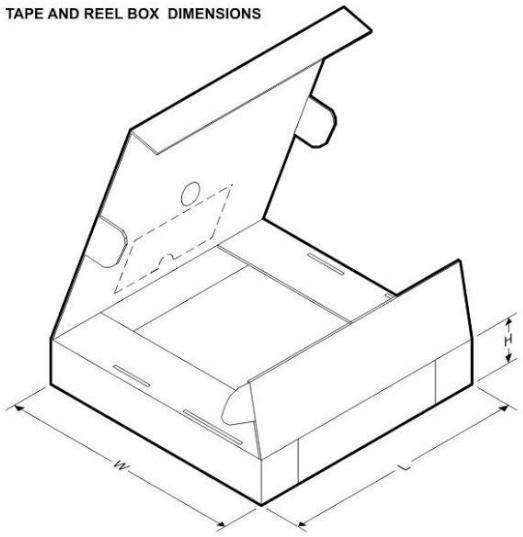
TAPE AND REEL BOX DIMENSIONS



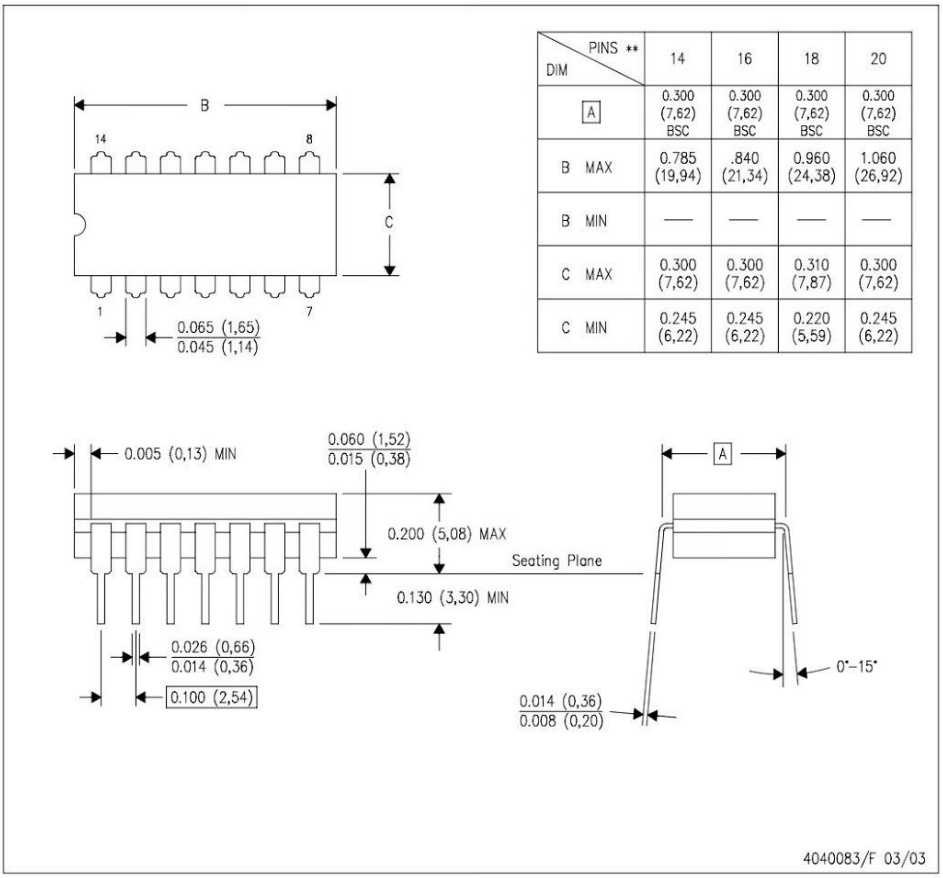
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC374M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HC574M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT374M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT574M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT574PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE

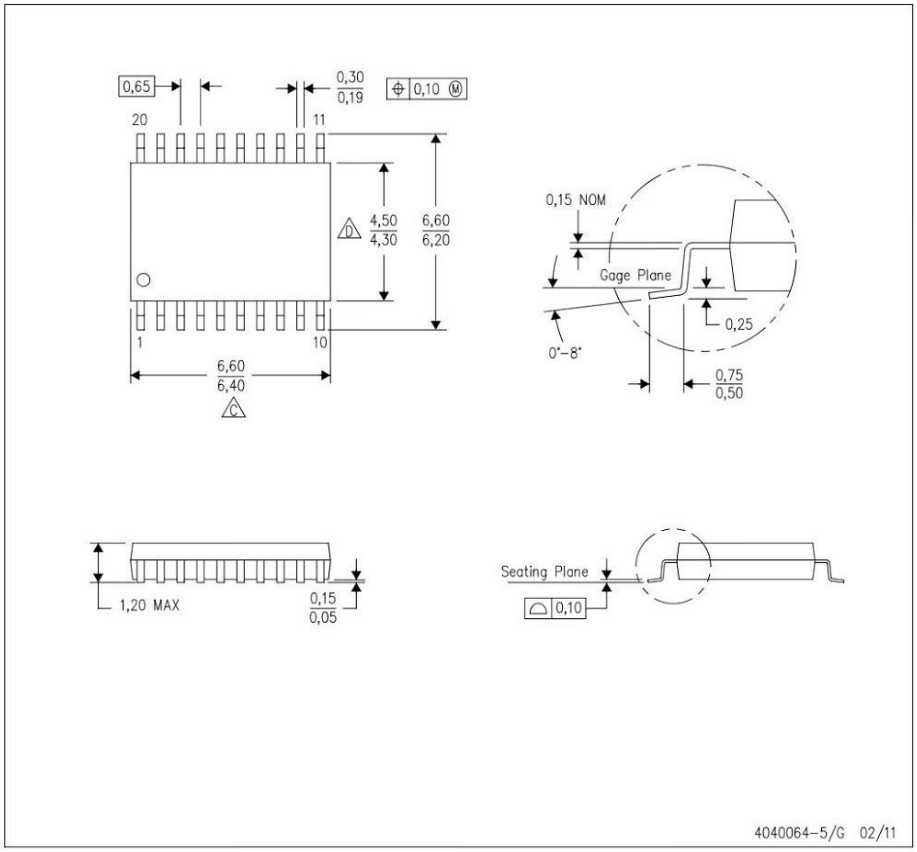


DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MECHANICAL DATA

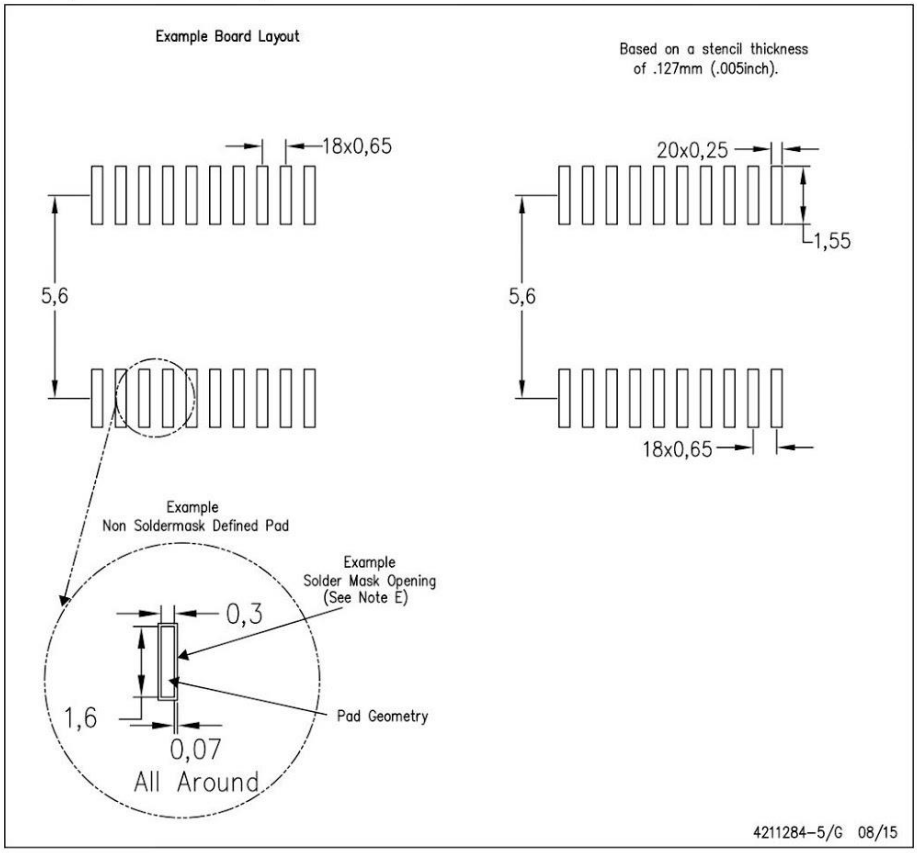
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

LAND PATTERN DATA

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE

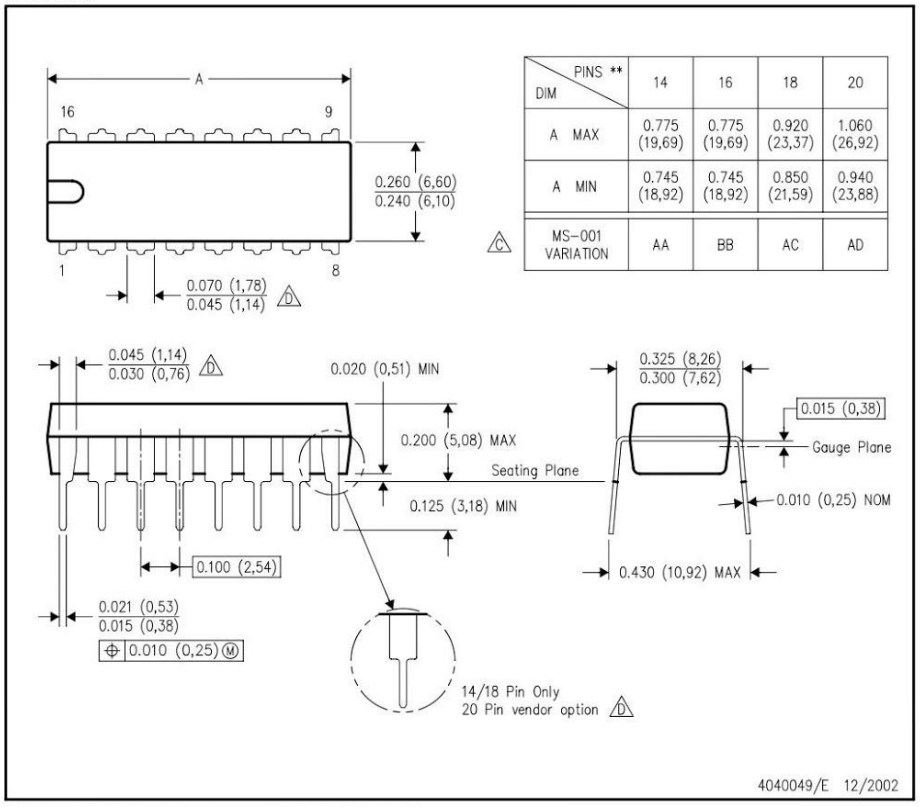


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD

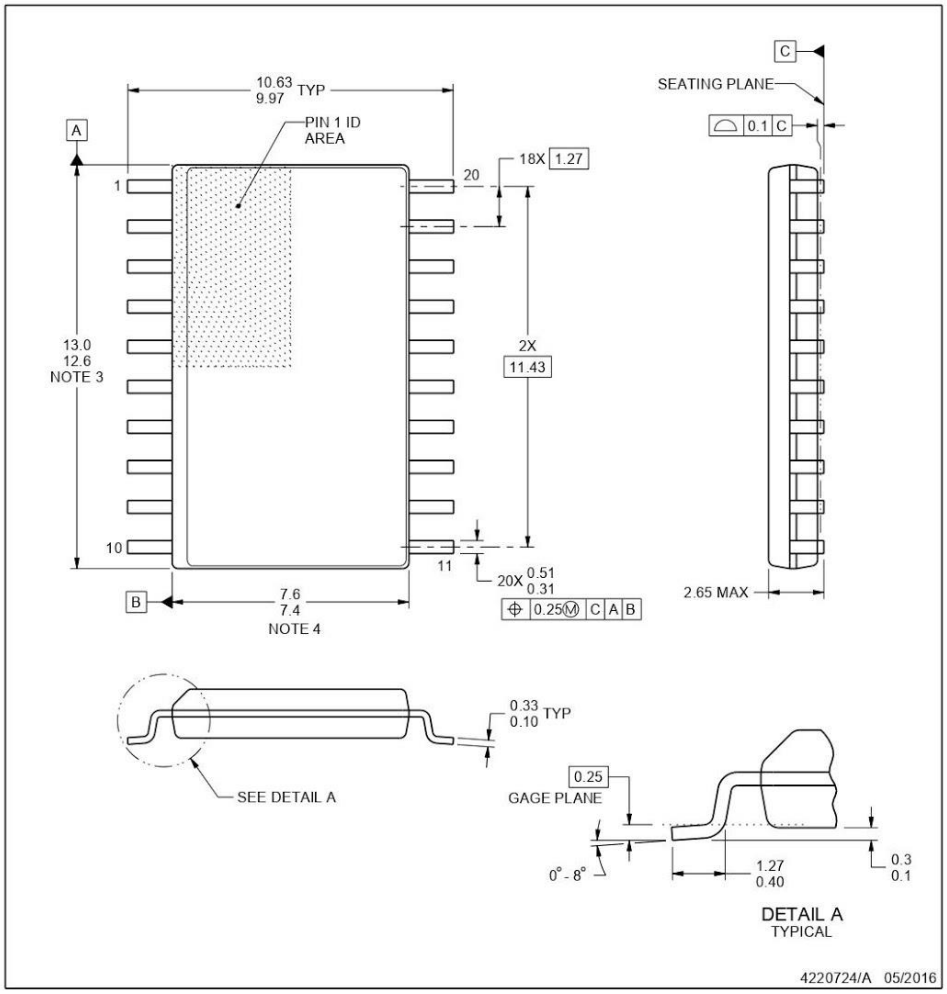
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



NOTES:

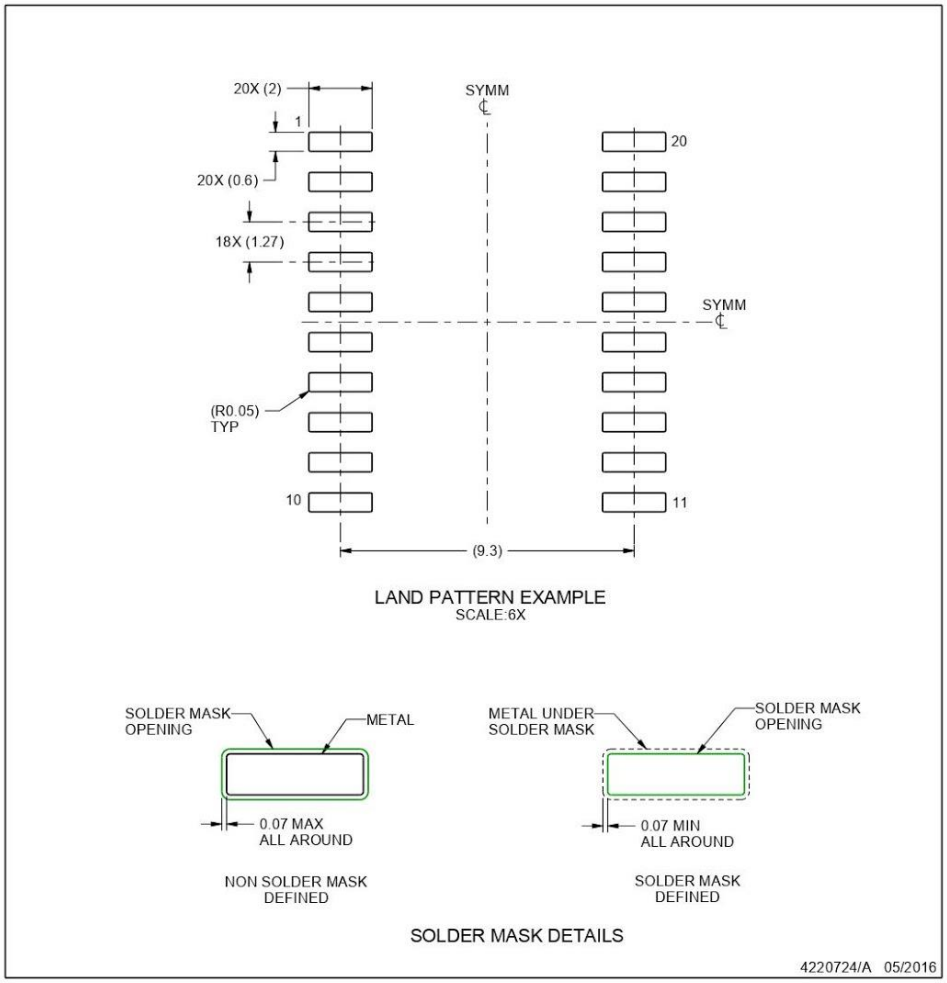
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

DW0020A — **SOIC - 2.65 mm max height**

SOIC



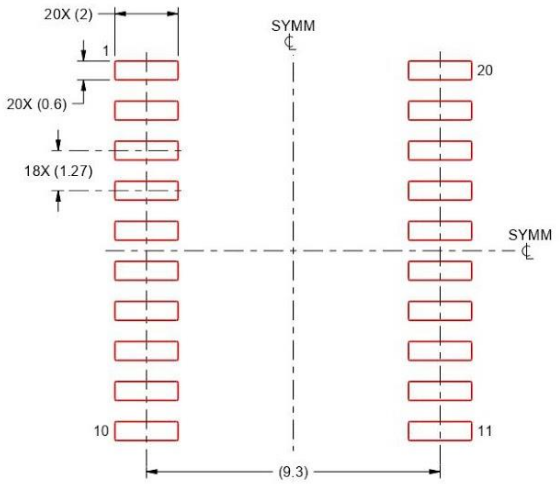
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A — **SOIC - 2.65 mm max height**

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

9.- 74LS47

FAIRCHILD SEMICONDUCTOR™

October 1988
Revised March 2000

DM74LS47
BCD to 7-Segment Decoder/Driver with Open-Collector Outputs

General Description

The DM74LS47 accepts four lines of BCD (8421) input data, generates their complements internally and decodes the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 24 mA in the ON (LOW) state and withstand 15V in the OFF (HIGH) state with a maximum leakage current of 250 μA. Auxiliary inputs provided blanking, lamp test and cascadable zero-suppression functions.

Features

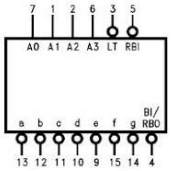
- Open-collector outputs
- Drive indicator segments directly
- Cascadable zero-suppression capability
- Lamp test input

Ordering Code:

Order Number	Package Number	Package Description
DM74LS47M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS47N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

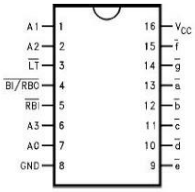
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Connection Diagram



Pin Descriptions

Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI/RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
$\overline{a}$ –$\overline{g}$	Segment Outputs (Active LOW) (Note 1)

Note 1: OC—Open Collector

 DS009817 www.fairchildsemi.com

Truth Table

Decimal or Function	Inputs							Outputs							Note
	$\overline{LT}$	$\overline{RBI}$	A3	A2	A1	A0	$\overline{BI}/\overline{RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(Note 2)
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	(Note 2)
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(Note 3)
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(Note 4)
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(Note 5)

Note 2: $\overline{BI}/\overline{RBO}$ is wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking or a decimal 0 is not desired. X = input may be HIGH or LOW.

Note 3: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.

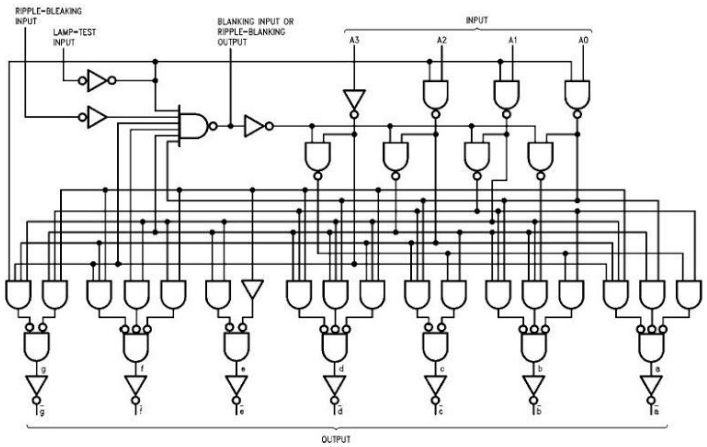
Note 4: When ripple-blanking input ($\overline{RBI}$) and inputs A0, A1, A2 and A3 are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

Note 5: When the blanking input/ripple-blanking output ($\overline{BI}/\overline{RBO}$) is OPEN or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

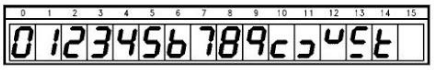
Functional Description

The DM74LS47 decodes the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the $\overline{RBI}$ blanks the display and causes a multi-digit display. For example, by grounding the $\overline{RBI}$ of the highest order decoder and connecting its $\overline{BI}/\overline{RBO}$ to $\overline{RBI}$ of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding $\overline{RBI}$ of the lowest order decoder and connecting its $\overline{BI}/\overline{RBO}$ to $\overline{RBI}$ of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, i.e.: by driving $\overline{RBI}$ of a intermediate decoder from an OR gate whose inputs are $\overline{BI}/\overline{RBO}$ of the next highest and lowest order decoders. $\overline{BI}/\overline{RBO}$ also serves as an unconditional blanking input. The internal NAND gate that generates the $\overline{RBO}$ signal has a resistive pull-up, as opposed to a totem pole, and thus $\overline{BI}/\overline{RBO}$ can be forced LOW by external means, using wired-collector logic. A LOW signal thus applied to $\overline{BI}/\overline{RBO}$ turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to $\overline{LT}$ turns on all segment outputs, provided that $\overline{BI}/\overline{RBO}$ is not forced LOW.

Logic Diagram



Numerical Designations—Resultant Displays



Absolute Maximum Ratings (Note 6)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 6: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current $\overline{a}$ – $\overline{g}$ @ 15V = V_{OH} (Note 7)			−250	µA
I_{OH}	HIGH Level Output Current $\overline{BI}$ /$\overline{RBO}$			−50	µA
I_{OL}	LOW Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Note 7: OFF-State at $\overline{a}$–$\overline{g}$.

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 8)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, $\overline{BI}$ /$\overline{RBO}$	2.7	3.4		V
I_{OFF}	Output HIGH Current Segment Outputs	V_{CC} = 5.5V, V_O = 15V $\overline{a}$ – $\overline{g}$			250	µA
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, $\overline{a}$ – $\overline{g}$		0.35	0.5	V
		I_{OL} = 3.2 mA, $\overline{BI}$ /$\overline{RBO}$			0.5	
		I_{OL} = 12 mA, $\overline{a}$ –$\overline{g}$		0.25	0.4	
		I_{OL} = 1.6 mA, $\overline{BI}$ /$\overline{RBO}$			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			100	µA
		V_{CC} = Max, V_I = 10V				
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 9), I_{OS} at $\overline{BI}$/$\overline{RBO}$	−0.3		−2.0	mA
I_{CC}	Supply Current	V_{CC} = Max			13	mA

Note 8: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 9: Not more than one output should be shorted at a time, and the duration should not exceed one second.

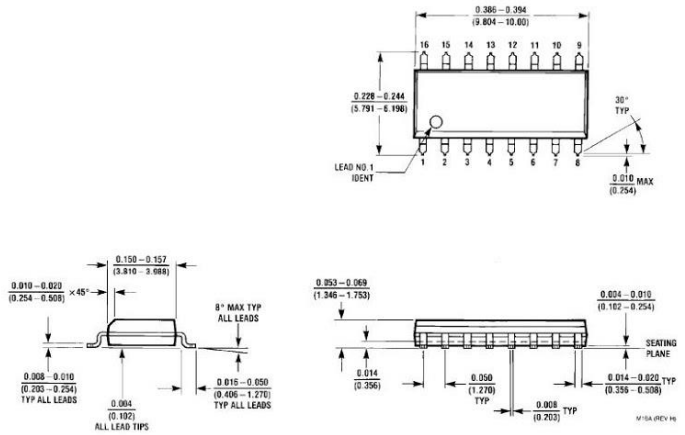
Switching Characteristics

at V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	Conditions	R_L = 665Ω, C_L = 15 pF Min	R_L = 665Ω, C_L = 15 pF Max	Units
t_{PLH}	Propagation Delay			100	ns
t_{PHL}	An to $\overline{a}$ –$\overline{g}$			100	
t_{PLH}	Propagation Delay			100	ns
t_{PHL}	$\overline{RBI}$ to $\overline{a}$ –$\overline{g}$ (Note 10)			100	

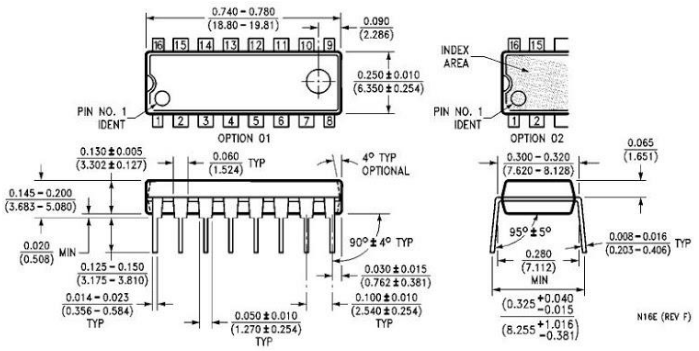
Note 10: $\overline{LT}$ = HIGH, A0–A3 = LOW

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

10.- 74LS393

74HC393; 74HCT393

Dual 4-bit binary ripple counter

Rev. 6 — 3 December 2015 Product data sheet

1. General description

The 74HC393; 7474HCT393 is a dual 4-stage binary ripple counter. Each counter features a clock input (n$\overline{CP}$), an overriding asynchronous master reset input (nMR) and 4 buffered parallel outputs (nQ0 to nQ3). The counter advances on the HIGH-to-LOW transition of n$\overline{CP}$. A HIGH on nMR clears the counter stages and forces the outputs LOW, independent of the state of n$\overline{CP}$. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Input levels:
  - For 74HC393: CMOS level
  - For 74HCT393: TTL level
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V.
- Two 4-bit binary counters with individual clocks
- Divide by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC393D	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT393D				
74HC393DB	−40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT393DB				
74HC393PW	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT393PW				
74HC393BQ	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74HCT393BQ				

nexperia

4. Functional diagram

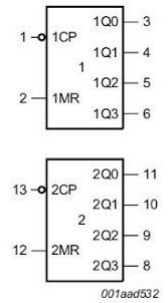


Fig 1. Logic symbol

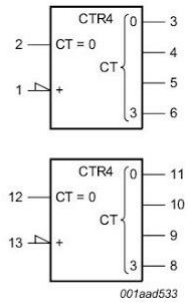


Fig 2. IEC logic symbol

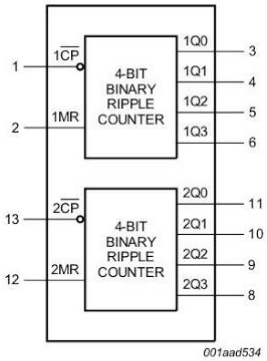


Fig 3. Functional diagram

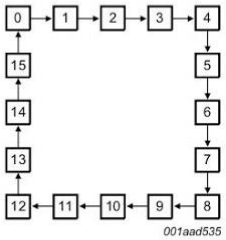


Fig 4. State diagram

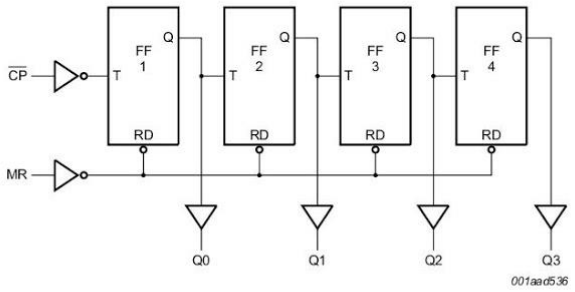


Fig 5. Logic diagram (one counter)

5. Pinning information

5.1 Pinning

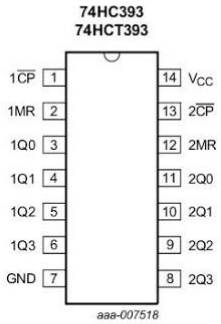


Fig 6. Pin configuration SO14

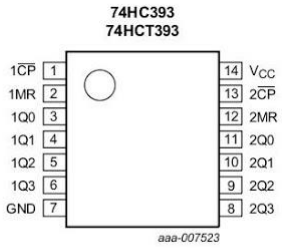
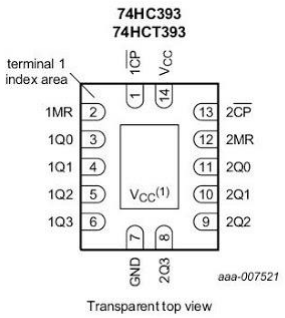


Fig 7. Pin configuration SSOP14 and TSSOP14



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to V_{CC}.

Fig 8. Pin configuration DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{CP}$	1	clock input (HIGH-to-LOW, edge-triggered)
1MR	2	asynchronous master reset input (active HIGH)
1Q0	3	flip-flop output
1Q1	4	flip-flop output
1Q2	5	flip-flop output
1Q3	6	flip-flop output
GND	7	ground (0 V)
2Q3	8	flip-flop output
2Q2	9	flip-flop output
2Q1	10	flip-flop output
2Q0	11	flip-flop output
2MR	12	asynchronous master reset input (active HIGH)
$2\overline{CP}$	13	clock input (HIGH-to-LOW, edge-triggered)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Count sequence for one counter [1]

Count	Output			
	nQ0	nQ1	nQ2	nQ3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

[1] H = HIGH voltage level; L = LOW voltage level.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	±50	mA
I_{GND}	ground current		-	±50	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	SO14, (T)SSOP14 and DHVQFN14 package [1]	-	500	mW

[1] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC393			74HCT393			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC393										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±0.1	-	±0.1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA

Table 6. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT393										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = −20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −6 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI_{CC}	additional supply current	V_I = V_{CC} − 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A								
		per input pin; $n\overline{CP}$	-	40	144	-	180	-	196	μA
		per input pin; nMR	-	100	360	-	450	-	490	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC393										
t_{pd}	propagation delay	$n\overline{CP}$ to nQ0; see Figure 9 [1]								
		V_{CC} = 2.0 V	-	41	125	-	155	-	190	ns
		V_{CC} = 4.5 V	-	15	25	-	31	-	38	ns
		V_{CC} = 5 V; C_L = 15 pF	-	12	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	12	21	-	26	-	32	ns
		nQx to nQ(x+1); see Figure 9 [1]								
		V_{CC} = 2.0 V	-	14	45	-	55	-	70	ns
		V_{CC} = 4.5 V	-	5	9	-	11	-	14	ns
		V_{CC} = 5 V; C_L = 15 pF	-	5	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	4	8	-	9	-	12	ns
t_{PHL}	HIGH to LOW propagation delay	nMR to nQx; see Figure 10								
		V_{CC} = 2.0 V	-	39	140	-	175	-	210	ns
		V_{CC} = 4.5 V	-	14	28	-	35	-	42	ns
		V_{CC} = 5 V; C_L = 15 pF	-	11	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	11	24	-	30	-	36	ns
t_t	transition time	Qn; see Figure 9 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	$n\overline{CP}$ HIGH or LOW; see Figure 9								
		V_{CC} = 2.0 V	80	17	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	5	-	17	-	20	-	ns
		nMR HIGH; see Figure 10								
		V_{CC} = 2.0 V	80	19	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t_{rec}	recovery time	nMR to $n\overline{CP}$; see Figure 10								
		V_{CC} = 2.0 V	5	3	-	5	-	5	-	ns
		V_{CC} = 4.5 V	5	1	-	5	-	5	-	ns
		V_{CC} = 6.0 V	5	1	-	5	-	5	-	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$f_{clk(max)}$	maximum clock frequency	see Figure 9								
		V_{CC} = 2.0 V	6	30	-	5	-	4	-	MHz
		V_{CC} = 4.5 V	30	90	-	24	-	20	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	99	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	35	107	-	28		24	-	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} [3]	-	23	-	-	-	-	-	pF
74HCT393										
t_{pd}	propagation delay	$n\overline{CP}$ to nQ0; see Figure 9 [1]								
		V_{CC} = 4.5 V	-	15	25	-	31	-	38	ns
		V_{CC} = 5 V; C_L = 15 pF	-	20	-	-	-	-	-	ns
		nQx to nQ(x+1); see Figure 9 [1]								
		V_{CC} = 4.5 V	-	6	10	-	13	-	15	ns
		V_{CC} = 5 V; C_L = 15 pF	-	6	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	nMR to nQx; see Figure 10								
		V_{CC} = 4.5 V	-	18	32	-	40	-	48	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	-	-	-	-	ns
t_t	transition time	Qn; see Figure 9 [2]								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t_W	pulse width	$n\overline{CP}$ HIGH or LOW; see Figure 9								
		V_{CC} = 4.5 V	19	11	-	24	-	29	-	ns
		nMR HIGH; see Figure 10								
		V_{CC} = 4.5 V	16	6	-	20	-	24	-	ns
t_{rec}	recovery time	nMR to $n\overline{CP}$; see Figure 10								
		V_{CC} = 4.5 V	5	0	-	5	-	5	-	ns
$f_{clk(max)}$	maximum clock frequency	see Figure 9								
		V_{CC} = 4.5 V	27	48	-	22	-	18	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	53	-	-	-	-	-	MHz

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 11.

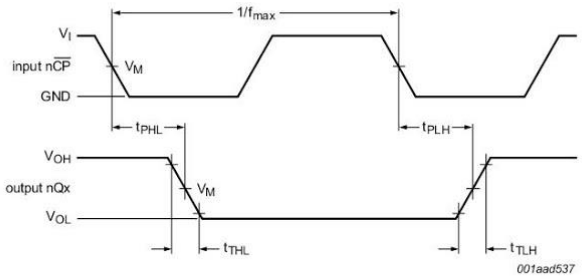
Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} − 1.5 V [3]	-	25	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1 Waveforms

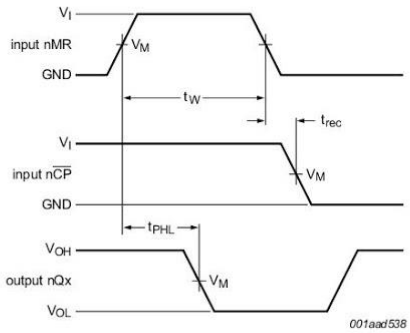


Measurement points are given in Table 8.

Fig 9. Propagation delays clock (nCP) to output (nQx), the output transition times and the maximum clock frequency

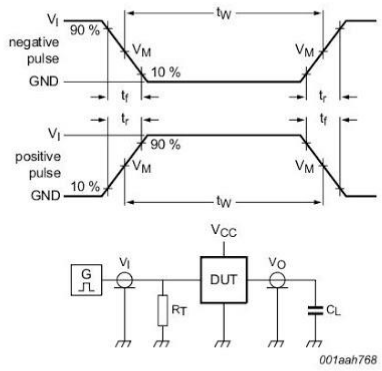
Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC393	$0.5V_{CC}$	$0.5V_{CC}$
74HCT393	1.3 V	1.3 V



Measurement points are given in Table 8.

Fig 10. Propagation delays clock ($n\overline{CP}$) to output (nQx), pulse width master reset (nMR), and recovery time master reset (nMR) to clock ($n\overline{CP}$)



Test data is given in Table 9.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

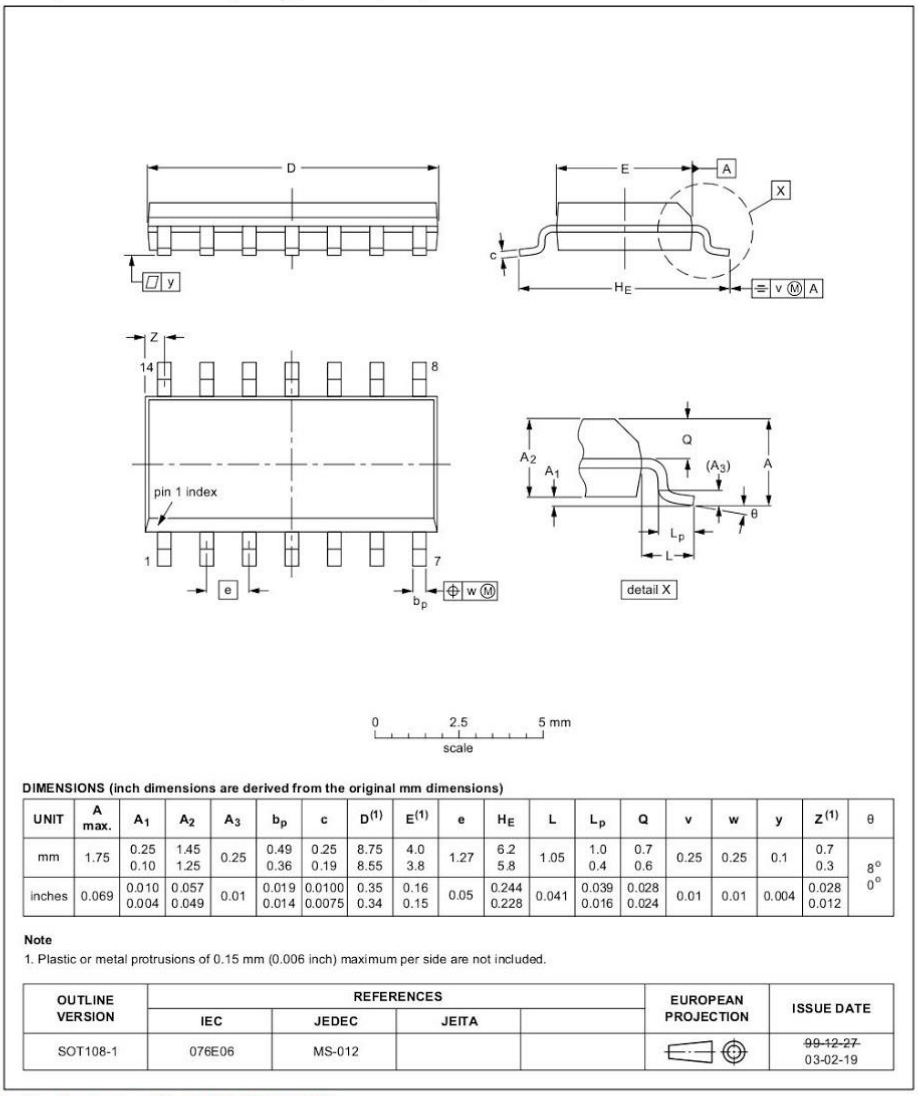
Fig 11. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC393	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT393	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

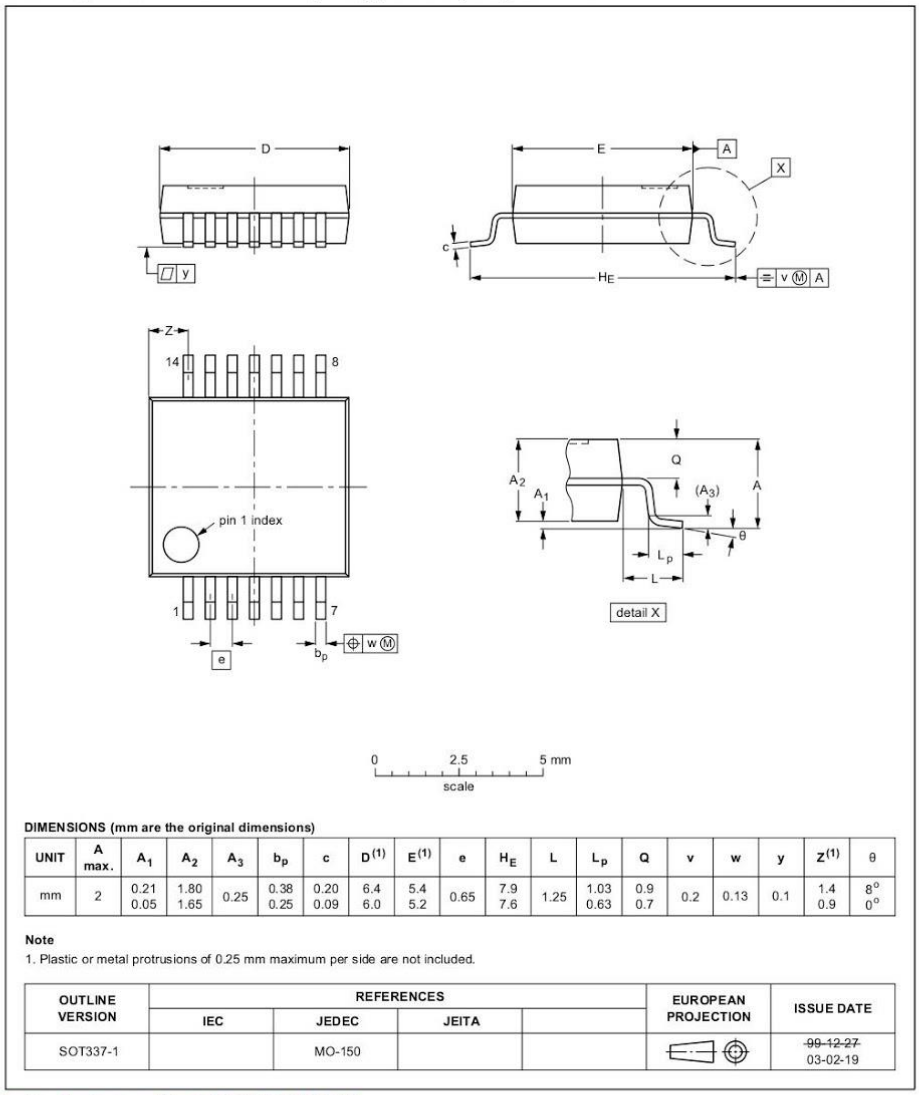
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^{o} 0^{o}

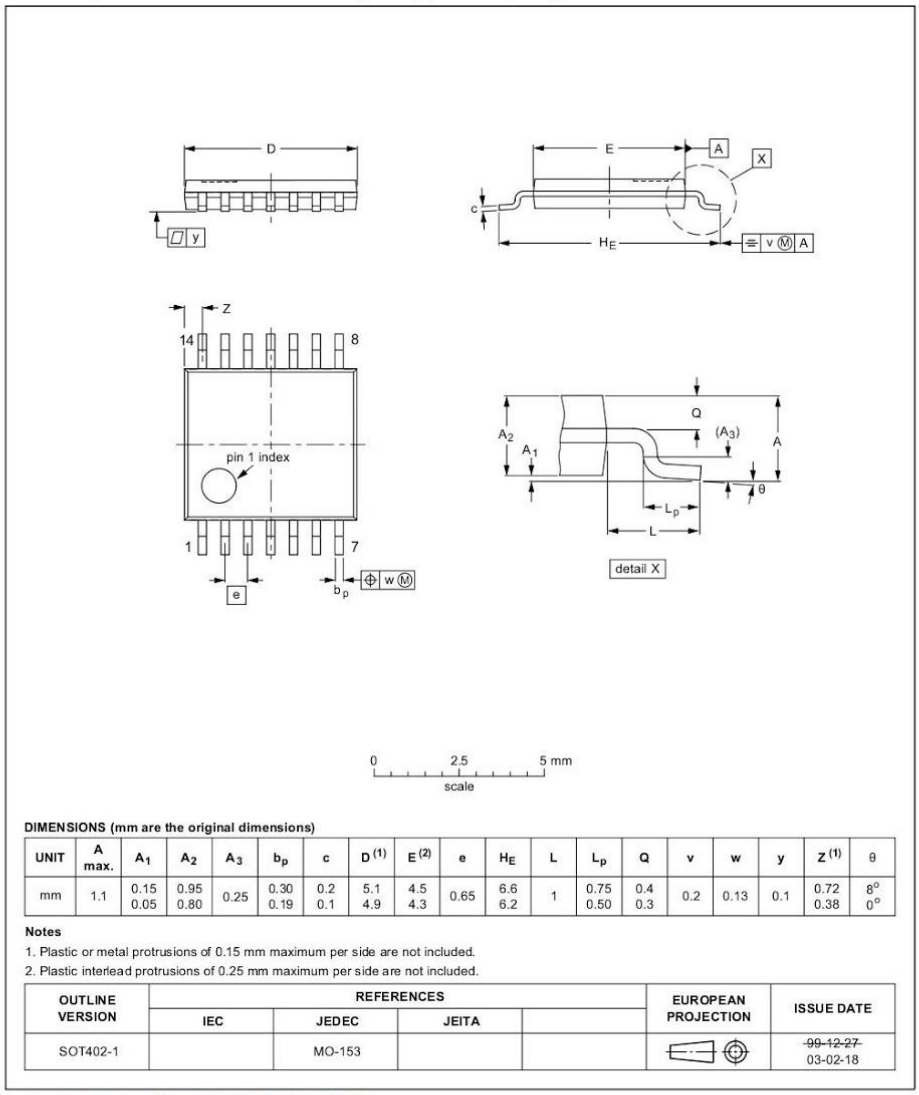
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

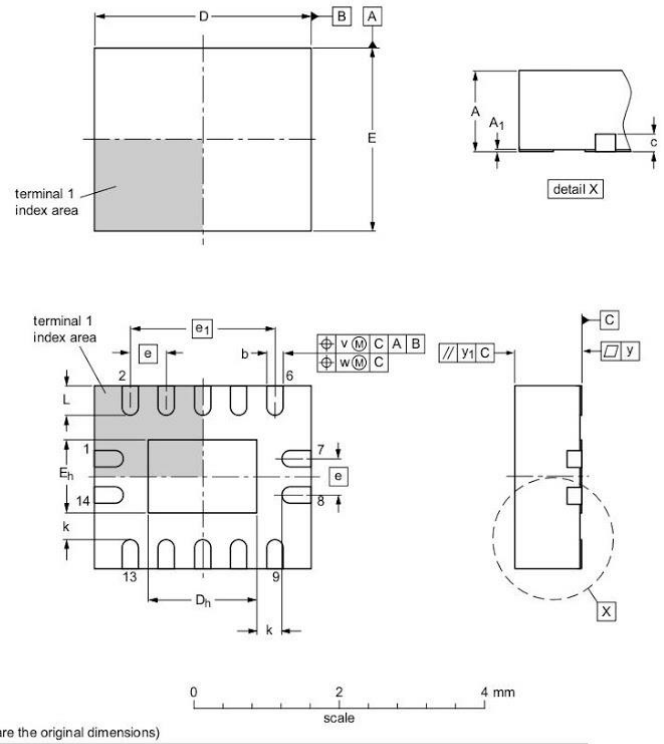
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 14. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	k	L	v	w	y	y_1
	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig 15. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT393 v.6	20151203	Product data sheet	-	74HC_HCT393 v.5
Modifications:	• Type numbers 74HC393N and 74HCT393N (SOT27-1) removed.			
74HC_HCT393 v.5	20140401	Product data sheet	-	74HC_HCT393 v.4
Modifications:	• The conditions for C_{PD} have been corrected (errata).			
74HC_HCT393 v.4	20130516	Product data sheet	-	74HC_HCT393 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT393 v.3	20050906	Product data sheet	-	74HC_HCT393_CNV v.2
74HC_HCT393_CNV v.2	19901201	Product specification	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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15. Contact information

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11.- 74LS157

SDLS058

SN54157, SN54LS157, SN54LS158, SN54S157, SN54S158, SN74157, SN74LS157, SN74LS158, SN74S157, SN74S158
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

MARCH 1974 – REVISED MARCH 1988

- Buffered Inputs and Outputs
- Three Speed/Power Ranges Available

TYPES	TYPICAL AVERAGE PROPAGATION TIME	TYPICAL POWER DISSIPATION
'157	9 ns	150 mW
'LS157	9 ns	49 mW
'S157	5 ns	250 mW
'LS158	7 ns	24 mW
'S158	4 ns	195 mW

applications

- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables (One Variable Is Common)
- Source Programmable Counters

description

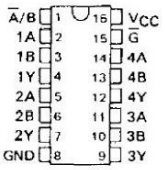
These monolithic data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The '157, 'LS157, and 'S157 present true data whereas the 'LS158 and 'S158 present inverted data to minimize propagation delay time.

FUNCTION TABLE

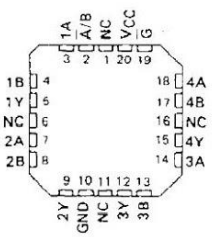
INPUTS				OUTPUT Y	
STROBE $\overline{G}$	SELECT $\overline{A}$/B	A	B	'157, 'LS157, 'S157	'LS158 'S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant

SN54157, SN54LS157, SN54S157, SN54LS158, SN54S158 . . . J OR W PACKAGE
SN74157 . . . N PACKAGE
SN74LS157, SN74S157, SN74LS158, SN74S158 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS157, SN54S157, SN54LS158, SN54S158 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

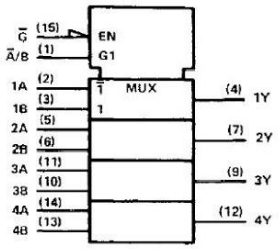
Supply voltage, V_{CC} (See Note 1) . . . . . 7 V
Input voltage: '157, 'S158 . . . . . 5.5 V
'LS157, 'LS158 . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

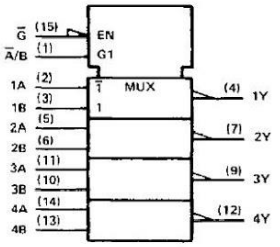
SN54157, SN54LS157, SN54LS158, SN54S157, SN54S158,
SN74157, SN74LS157, SN74LS158, SN74S157, SN74S158
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

logic symbols†

'157, 'LS157, 'S157



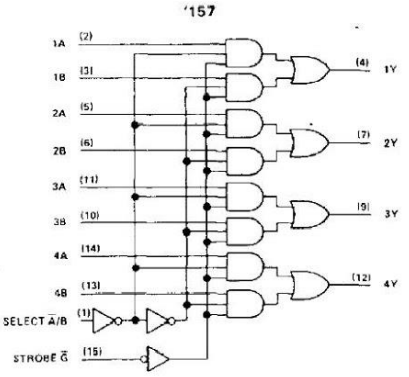
'158, 'LS158, 'S158



† These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

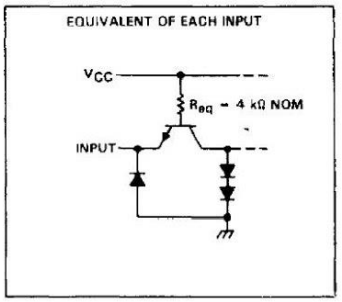
'157



schematics of inputs and outputs

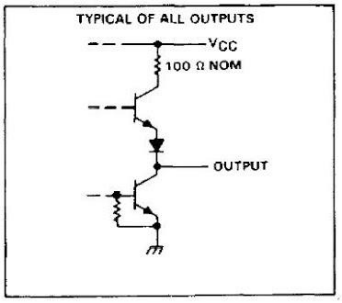
'157

EQUIVALENT OF EACH INPUT



'157

TYPICAL OF ALL OUTPUTS



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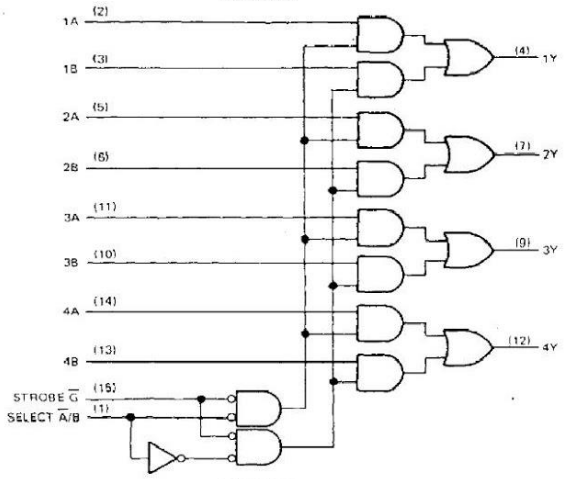
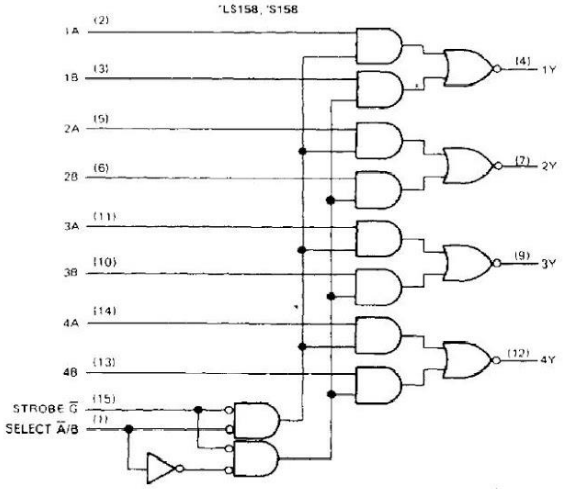
SN54LS157, SN54LS158, SN54S157, SN54S158,
SN74LS157, SN74LS158, SN74S157, SN74S158
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

logic diagrams (positive logic)

'LS157, 'S157



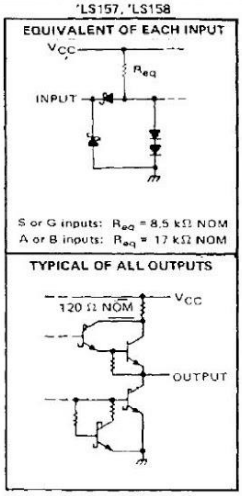
'LS158, 'S158



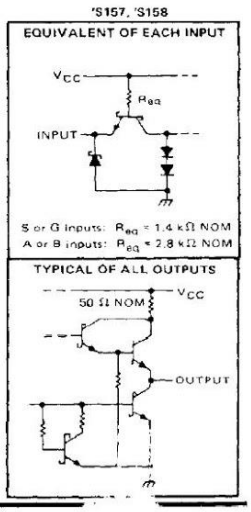
Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs

'LS157, 'LS158



'S157, 'S158



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SN54157, SN74157
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54157			SN74157			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54157			SN74157			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		30	48		30	48	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	C_L = 15 pF, R_L = 400 Ω, See Note 3		9	14	ns
t_{PHL}				9	14	
t_{PLH}	Strobe $\overline{G}$			13	20	ns
t_{PHL}				14	21	
t_{PLH}	Select $\overline{A}$/B			15	23	ns
t_{PHL}				18	27	

¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−400			−400	μA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA					−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −400 μA			2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 4 mA			0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA						0.35	0.5	
I_I	Input current at maximum input voltage	$\overline{A}/B$ or $\overline{G}$	V_{CC} = MAX, V_I = 7 V					0.2			0.2	mA
		A or B						0.1			0.1	
I_{IH}	High-level input current	$\overline{A}/B$ or $\overline{G}$	V_{CC} = MAX, V_I = 2.7 V					40			40	μA
		A or B						20			20	
I_{IL}	Low-level input current	$\overline{A}/B$ or $\overline{G}$	V_{CC} = MAX, V_I = 0.4 V					−0.8			−0.8	mA
		A or B						−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2		'LS157		9.7	16		9.7	16	mA
					'LS158		4.8	8		4.8	8	
			V_{CC} = MAX, All A inputs at 4.5 V, All other inputs at 0 V		'LS158		6.5	11		6.5	11	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS	'LS157			'LS158			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data	C_L = 15 pF, R_L = 2 kΩ, See Note 3		9	14		7	12	ns
t_{PHL}				9	14		10	15	
t_{PLH}	Strobe $\overline{G}$			13	20		11	17	ns
t_{PHL}				14	21		18	24	
t_{PLH}	Select $\overline{A}/B$			15	23		13	20	ns
t_{PHL}				18	27		16	24	

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 3: Load circuits and voltage diagrams are shown in Section 1.

SN54S157, SN54S158, SN74S157, SN74S158
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

	SN54S157 SN54S158			SN74S157 SN74S158			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S157 SN74S157			SN54S158 SN74S158			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	Series 54S	2.5	3.4		2.5	3.4		V
				Series 74S	2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	$\overline{A}/B$ or $\overline{G}$	V_{CC} = MAX, V_I = 2.7 V				100			100	µA
		A or B					50			50	
I_{IL}	Low-level input current	$\overline{A}/B$ or $\overline{G}$	V_{CC} = MAX, V_I = 0.5 V				−4			−4	mA
		A or B					−2			−2	
I_{OS}	Short-circuit ouput current§		V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, All inputs at 4.5 V, See Note 2			50	78		39	61	mA
			V_{CC} = MAX, A inputs at 4.5 V, B,G,S, inputs at 0 V, See Note 2							81	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
Note 2: I_{CC} is measured with all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS	SN54S157 SN74S157			SN54S158 SN74S158			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data	C_L = 15 pF, R_L = 280 Ω, See Note 3		5	7.5		4	6	ns
t_{PHL}				4.5	6.5		4	6	
t_{PLH}	Strobe $\overline{G}$			8.5	12.5		6.5	11.5	ns
t_{PHL}				7.5	12		7	12	
t_{PLH}	Select $\overline{A}/B$			9.5	15		8	12	ns
t_{PHL}				9.5	15		8	12	

¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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PACKAGE MATERIALS INFORMATION

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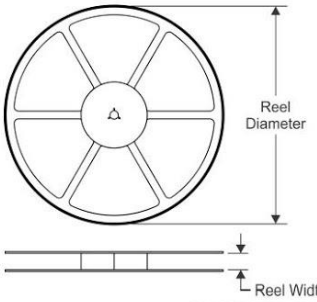
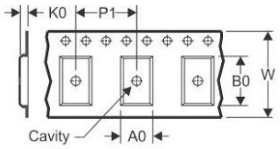
8-Apr-2013

TAPE AND REEL INFORMATION

REEL DIMENSIONS

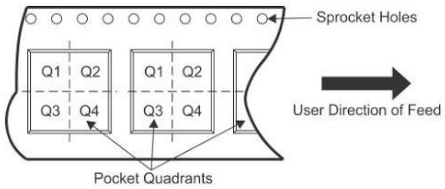


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS157DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS158DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS158NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TEXAS INSTRUMENTS

PACKAGE MATERIALS INFORMATION

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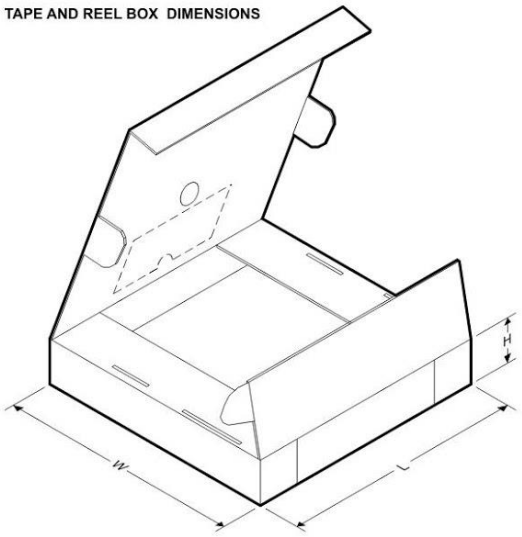
TAPE AND REEL BOX DIMENSIONS



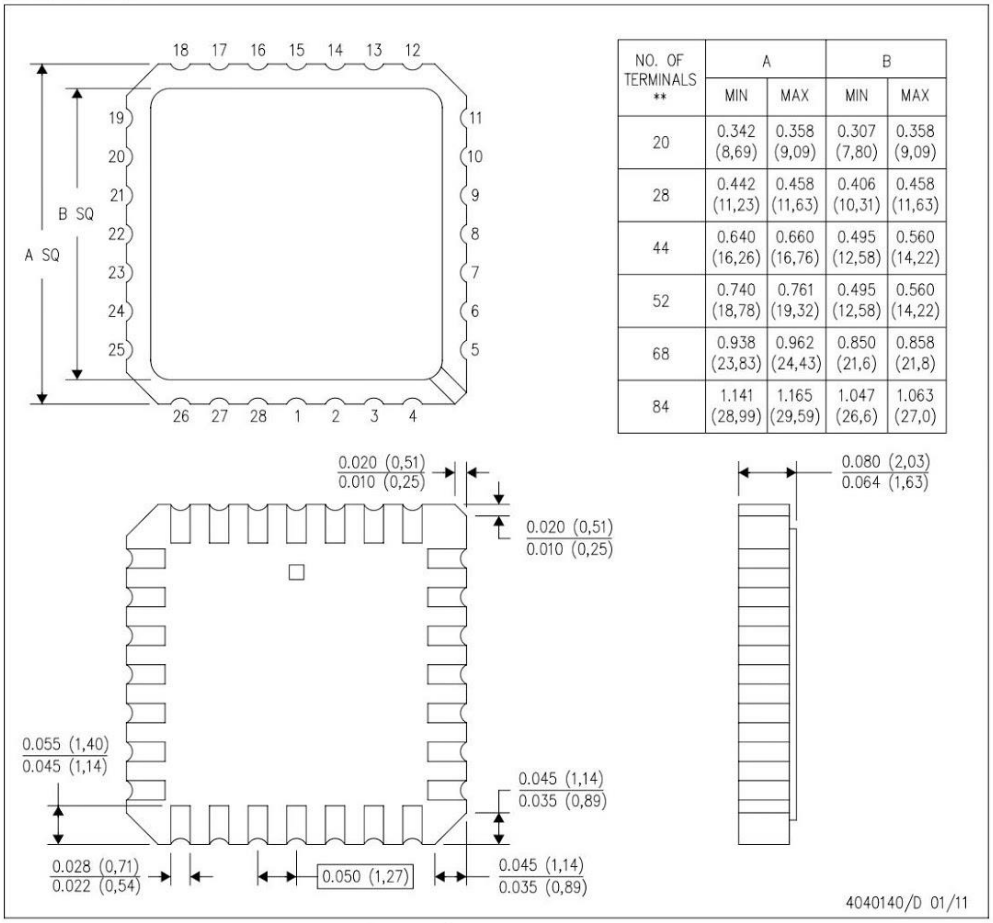
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS157DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS158DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS158NSR	SO	NS	16	2000	367.0	367.0	38.0

MECHANICAL DATA

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

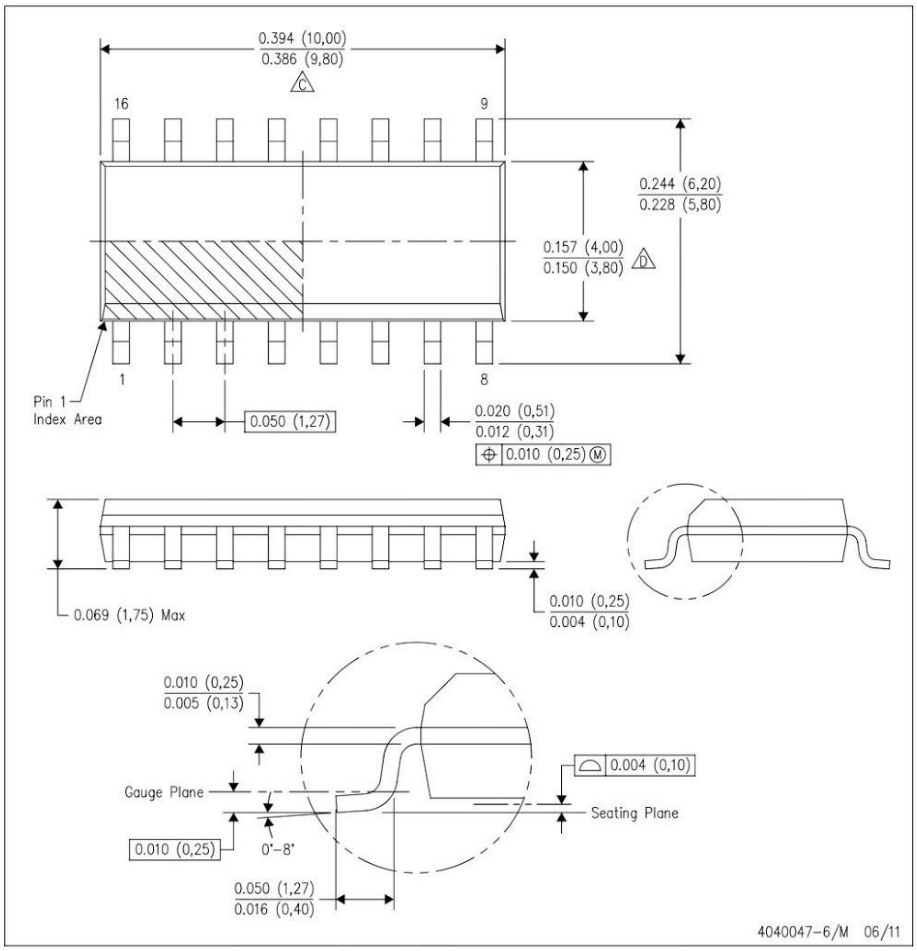


NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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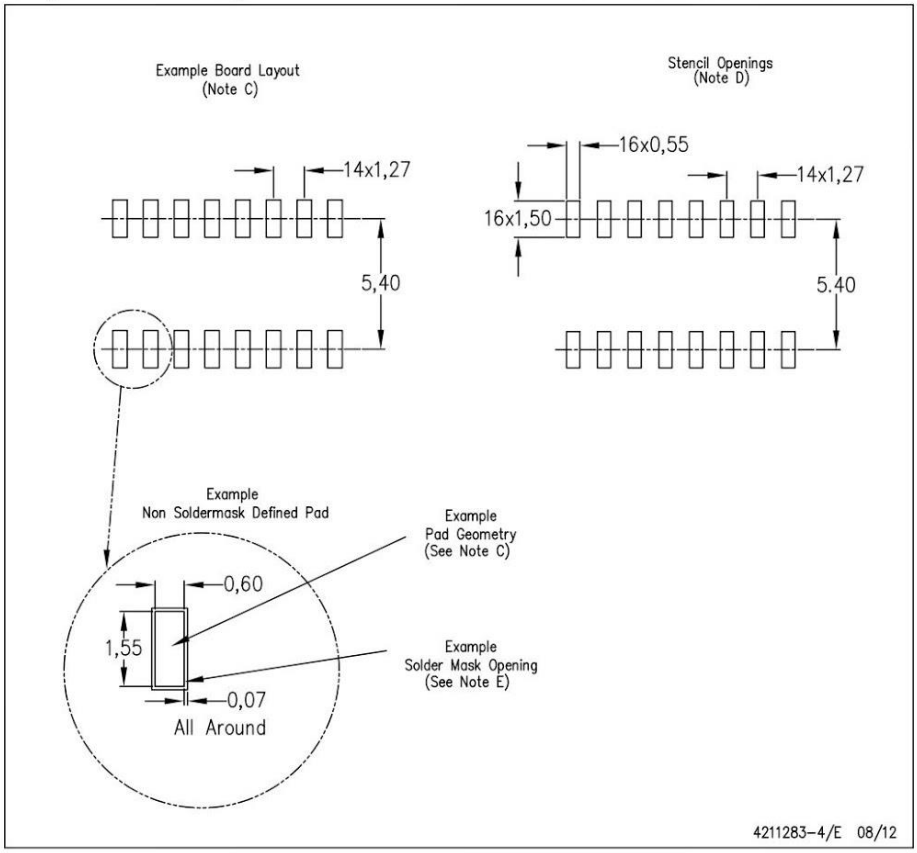
LAND PATTERN DATA

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

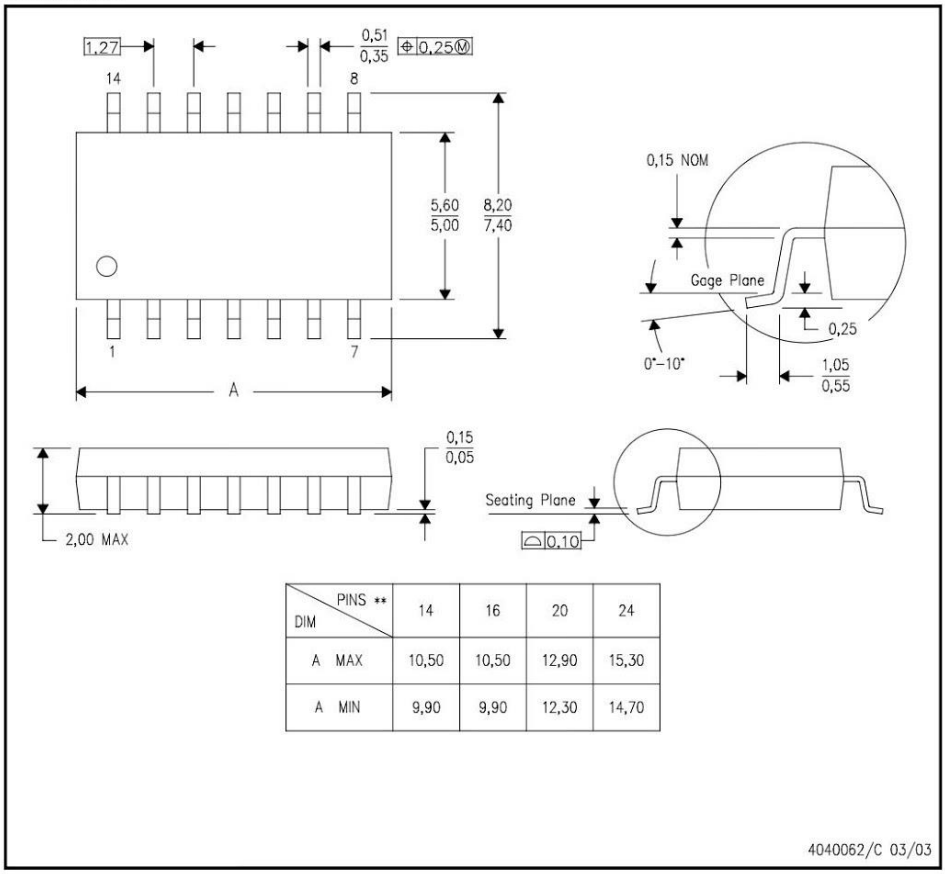


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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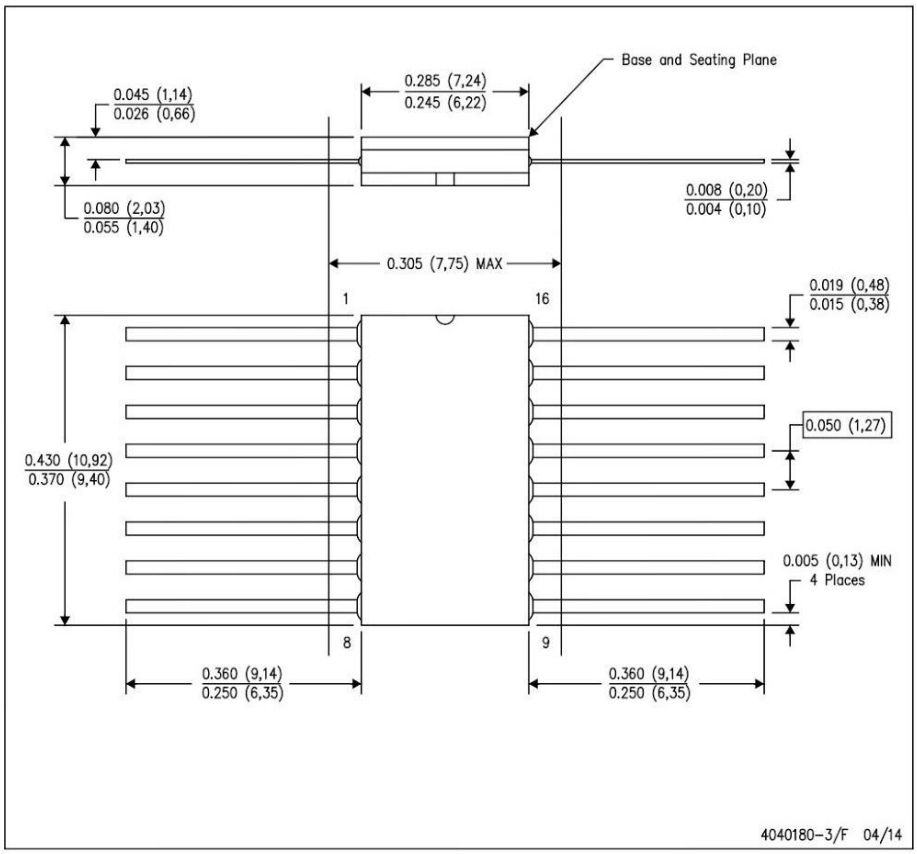
MECHANICAL DATA

W (R–GDFP–F16) CERAMIC DUAL FLATPACK

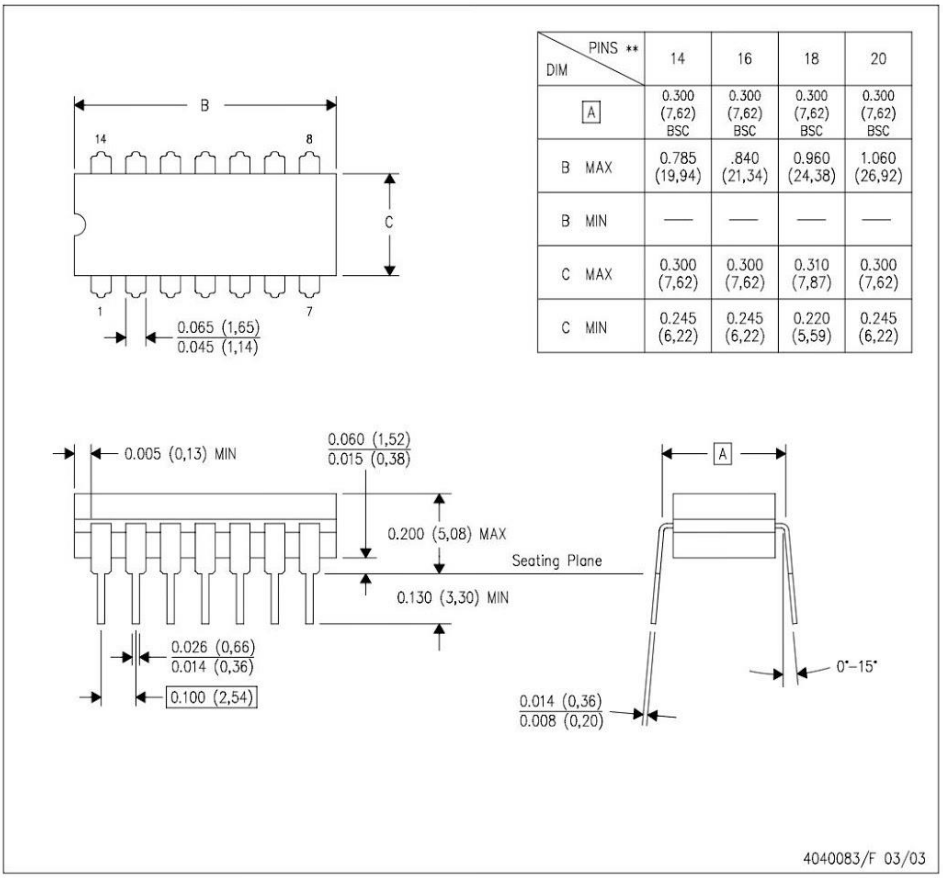


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



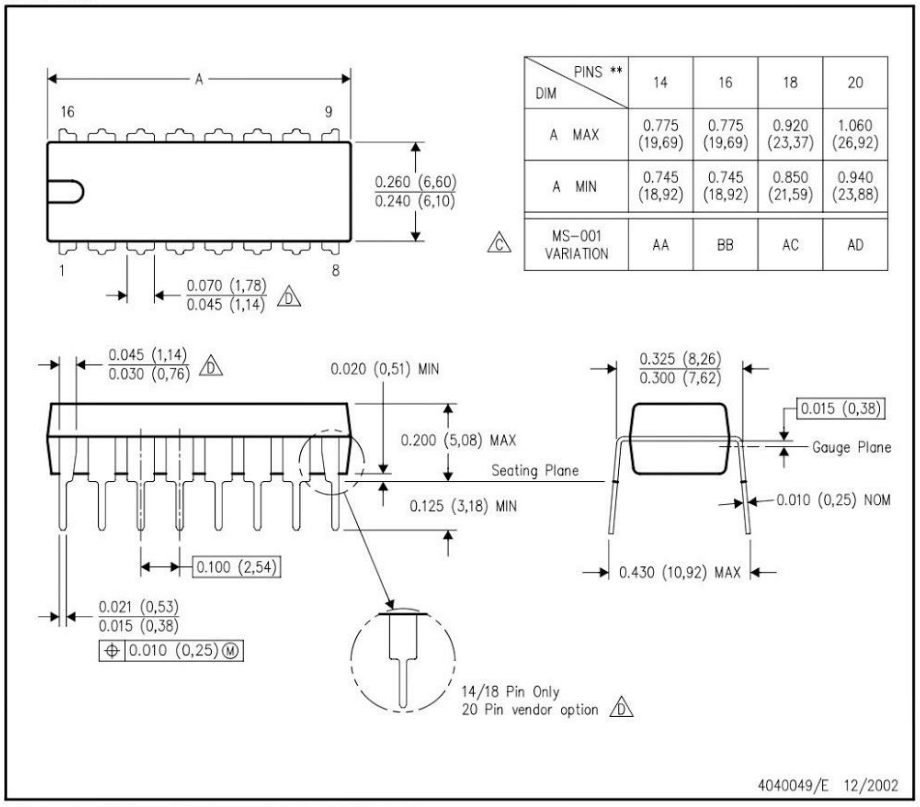
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MECHANICAL DATA

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS INSTRUMENTS
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12.- DAC0808

National Semiconductor

May 1999

DAC0808
8-Bit D/A Converter

General Description

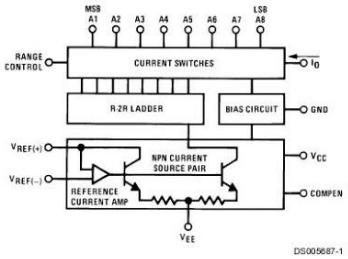
The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 $I_{REF}/256$. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 µA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 is independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

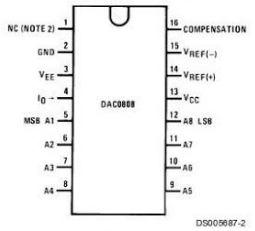
Features

- Relative accuracy: ±0.19% error maximum
- Full scale current match: ±1 LSB typ
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/µs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

Block and Connection Diagrams



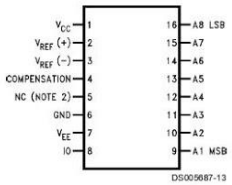
Dual-In-Line Package



Top View
Order Number DAC0808
See NS Package M16A or N16A

Block and Connection Diagrams (Continued)

Small-Outline Package



Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	N PACKAGE (N16A) (Note 1)		SO PACKAGE (M16A)
8-bit	0°C≤T_A≤+75°C	DAC0808LCN	MC1408P8	DAC0808LCM

Note 1: Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage	
V_{CC}	+18 V_{DC}
V_{EE}	−18 V_{DC}
Digital Input Voltage, V5–V12	−10 V_{DC} to +18 V_{DC}
Applied Output Voltage, V_O	−11 V_{DC} to +18 V_{DC}
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Note 4)	1000 mW
ESD Susceptibility (Note 5)	TBD
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC0808	$0 \le T_A \le +75°C$

Electrical Characteristics

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, V_{REF}/R14 = 2 mA, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	(*Figure 4*)				%
	DAC0808LC (LM1408-8)				**±0.19**	%
	Settling Time to Within ½ LSB (Includes t_{PLH})	T_A=25°C (Note 7), (*Figure 5*)		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C, (*Figure 5*)		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	(*Figure 3*)				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	(*Figure 3*)				
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	(*Figure 3*)		−1	−3	μA
	Output Current Range	(*Figure 3*)				
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	Output Current	V_{REF} = 2.000V, R14 = 1000Ω,				
		(*Figure 3*)	1.9	1.99	2.1	mA
	Output Current, All Bits Low	(*Figure 3*)		0	4	μA
	Output Voltage Compliance (Note 3)	$E_r \le 0.19\%$, T_A = 25°C				
	V_{EE}=−5V, I_{REF}=1 mA				−0.55, +0.4	V_{DC}
	V_{EE} Below −10V				−5.0, +0.4	V_{DC}
SRI_{REF}	Reference Current Slew Rate	(*Figure 6*)	4	8		mA/μs
	Output Current Power Supply Sensitivity	$-5V \le V_{EE} \le -16.5V$		0.05	2.7	μA/V
	Power Supply Current (All Bits Low)	(*Figure 3*)				
I_{CC}				2.3	22	mA
I_{EE}				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25°C, (*Figure 3*)				
V_{CC}			4.5	5.0	5.5	V_{DC}
V_{EE}			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					

Electrical Characteristics (Continued)

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, V_{REF}/R14 = 2 mA, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 3: Range control is not required.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maixmum Ratings, whichever is lower. For this device, T_{JMAX} = 125°C, and the typical junction-to-ambient thermal resistance of the dual-in-line J package when the board mounted is 100°C/W. For the dual-in-line N package, this number increases to 175°C/W and for the small outline M package this number is 100°C/W.

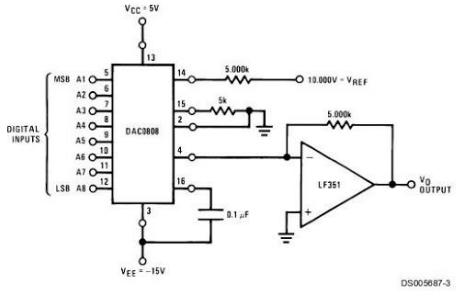
Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: All current switches are tested to guarantee at least 50% of rated current.

Note 7: All bits switched.

Note 8: Pin-out numbers for the DAL080X represent the dual-in-line package. The small outline package pinout differs from the dual-in-line package.

Typical Application



$$V_O = 10V\left(\frac{A1}{2} + \frac{A2}{4} + \ldots \frac{A8}{256}\right)$$

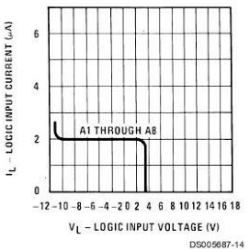
DS005687-23

DS005687-3

FIGURE 1. +10V Output Digital to Analog Converter (Note 8)

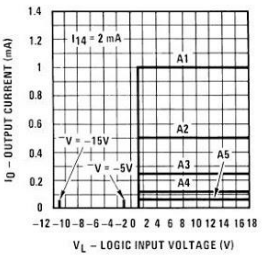
Typical Performance Characteristics V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, unless otherwise noted

Logic Input Current vs Input Voltage



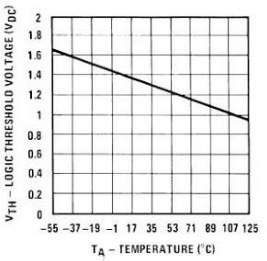
DS005687-14

Bit Transfer Characteristics



DS005687-15

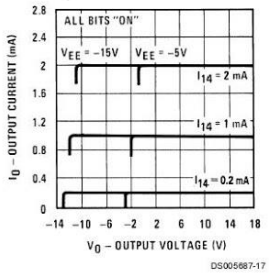
Logic Threshold Voltage vs Temperature



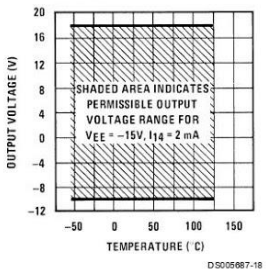
DS005687-16

Typical Performance Characteristics V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, unless otherwise noted (Continued)

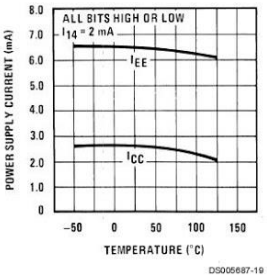
Output Current vs Output Voltage (Output Voltage Compliance)



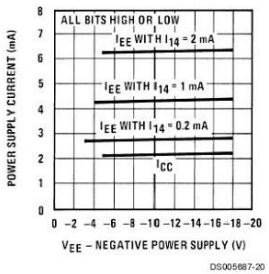
Output Voltage Compliance vs Temperature



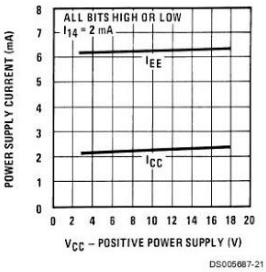
Typical Power Supply Current vs Temperature



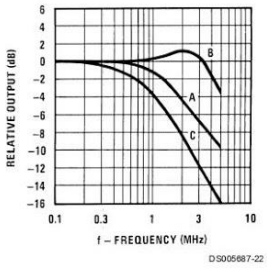
Typical Power Supply Current vs V_{EE}



Typical Power Supply Current vs V_{CC}



Reference Input Frequency Response



Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}, R_L = 50Ω, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1V above ground.

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp, R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

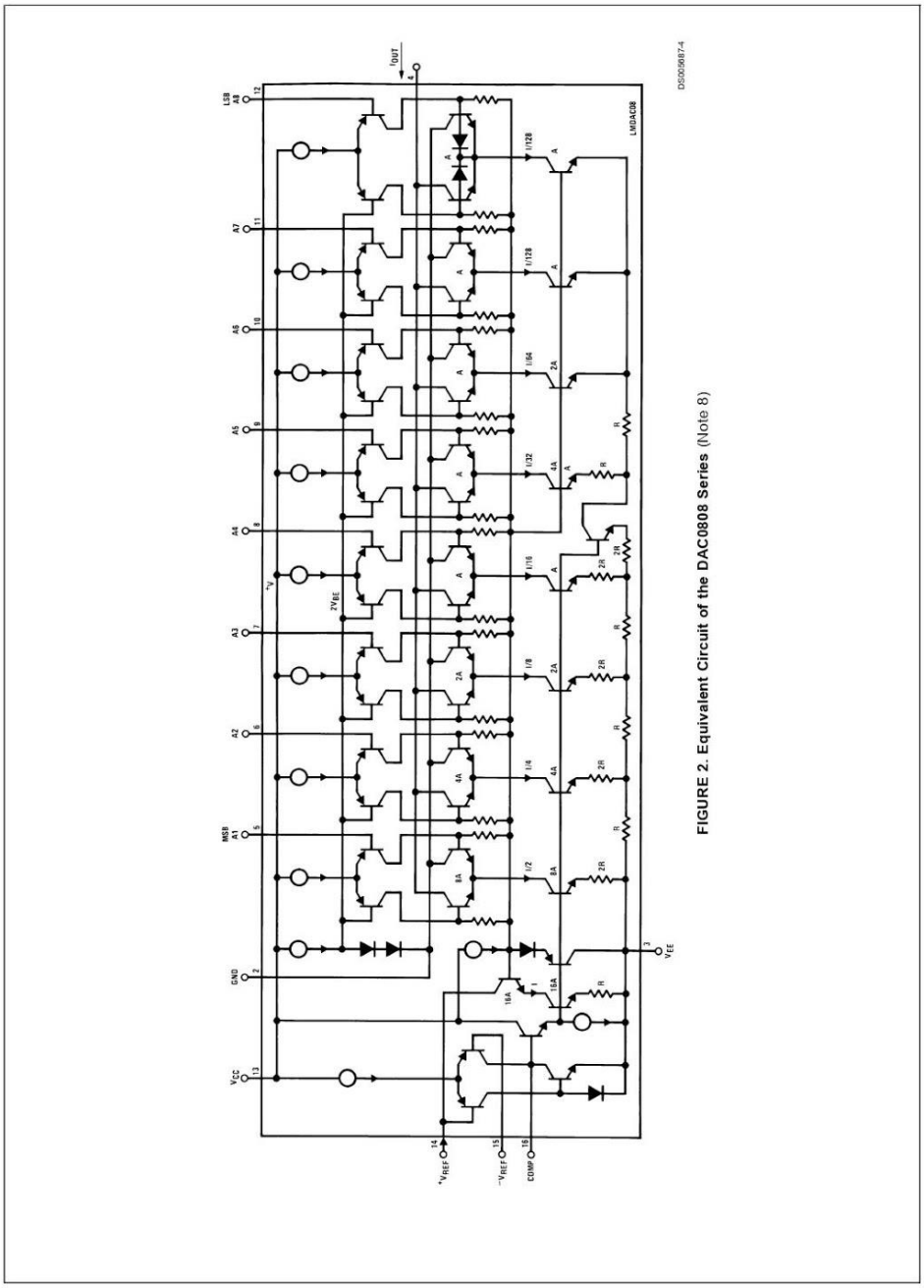
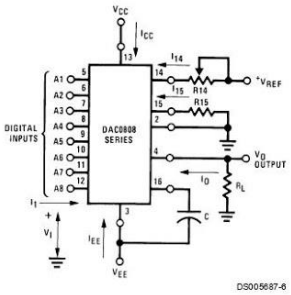


FIGURE 2. Equivalent Circuit of the DAC0808 Series (Note 8)

Test Circuits



V_I and I_1 apply to inputs A1–A8.
The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right)$$

$$\text{where } K \cong \frac{V_{REF}}{R14}$$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

FIGURE 3. Notation Definitions Test Circuit (Note 8)

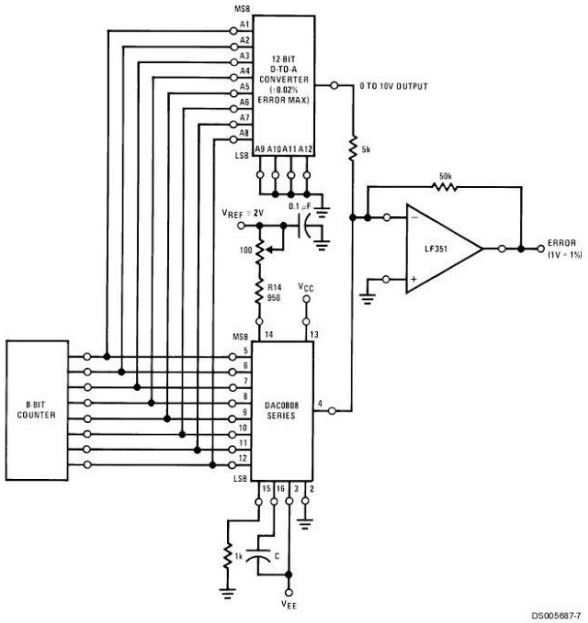


FIGURE 4. Relative Accuracy Test Circuit (Note 8)

Test Circuits (Continued)

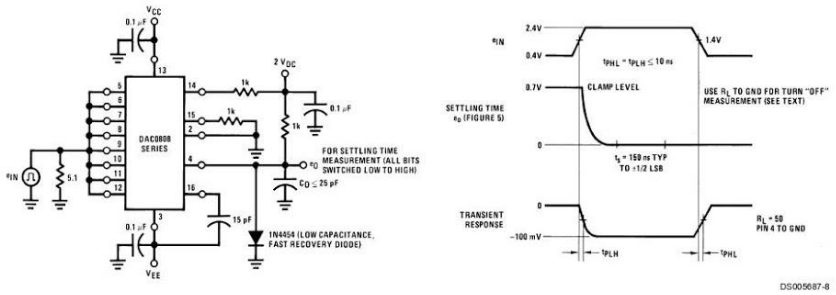


FIGURE 5. Transient Response and Settling Time (Note 8)

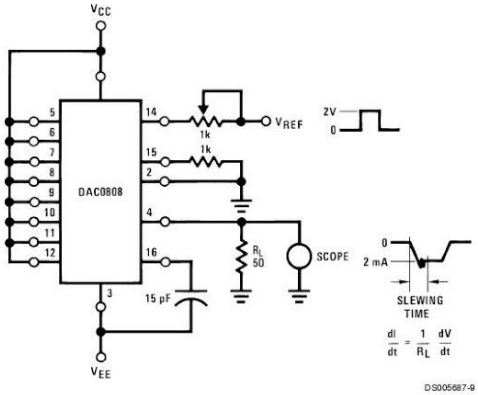


FIGURE 6. Reference Current Slew Rate Measurement (Note 8)

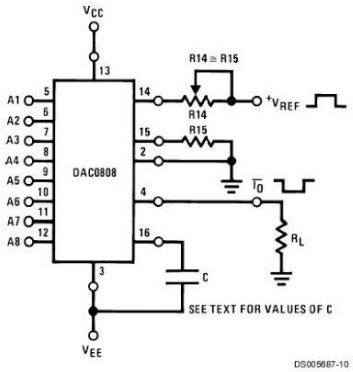


FIGURE 7. Positive V_{REF} (Note 8)

Test Circuits (Continued)

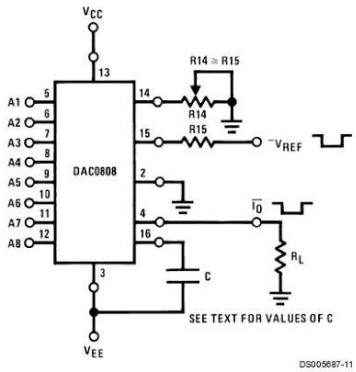


FIGURE 8. Negative V_{REF} (Note 8)

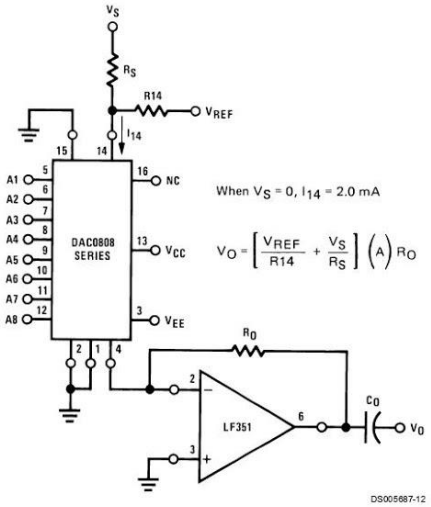


FIGURE 9. Programmable Gain Amplifier or Digital Attenuator Circuit (Note 8)

Application Hints

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input currrent, I_{14}, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 7*. The reference voltage source supplies the full current I_{14}.

For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 kΩ, minimum capacitor values are 15, 37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 8*. A high input impedance is the main

Application Hints (Continued)

advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 µF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.55 to 0.4V when V_{EE} = −5V due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to −5V where the negative supply voltage is more negative than −10V. Using a full-scale current of 1.992 mA and load resistor of 2.5 kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but a 2.5 kΩ load increases worst-case settling time to 1.2 µs (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than −8V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within ±½ LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 µA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in *Figure 4*. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA. Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±½ of one part in 65,536 or ±0.00076%, which is much more accurate than the ±0.019% specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 µA to 4 mA, the additional error contributions are less than 1.6 µA. This is well within 8-bit accuracy when referred to full-scale.

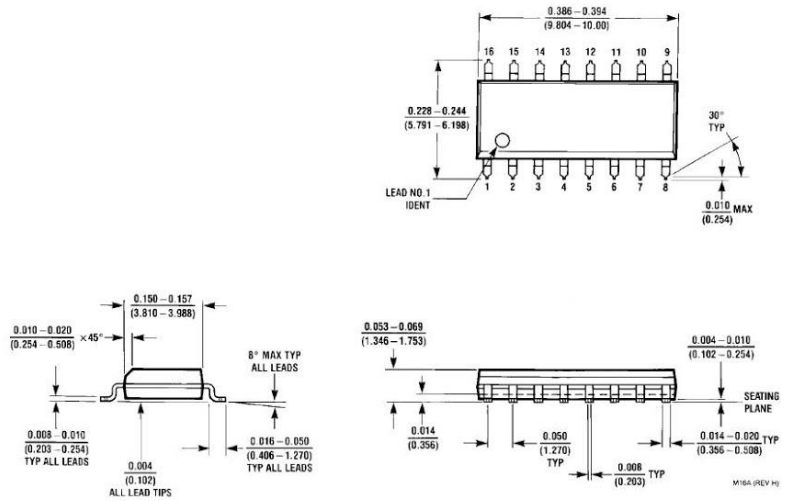
A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

SETTLING TIME

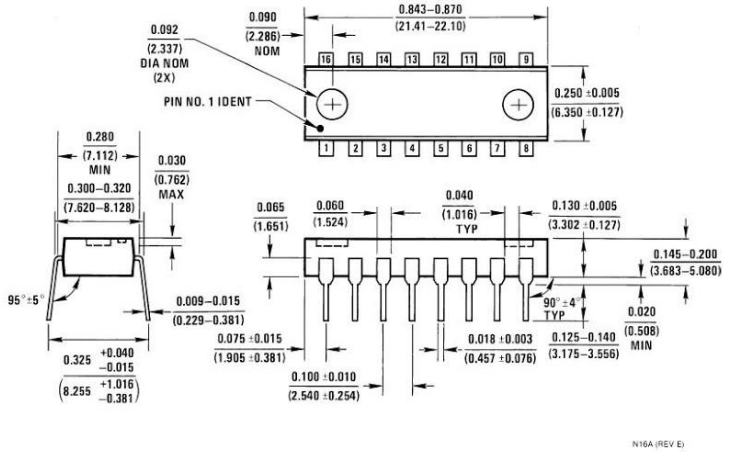
The worst-case switching condition occurs when all bits are switched ON, which corresponds to a low-to-high transition for all bits. This time is typically 150 ns for settling to within ±½ LSB, for 8-bit accuracy, and 100 ns to ½ LSB for 7 and 6-bit accuracy. The turn OFF is typically under 100 ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25$ pF.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 µF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

Physical Dimensions inches (millimeters) unless otherwise noted



Small Outline Package
Order Number DAC0808LCM
NS Package Number M16A



Dual-In-Line Package
Order Number DAC0808
NS Package Number N16A

13.- LM311

FAIRCHILD
SEMICONDUCTOR®

www.fairchildsemi.com

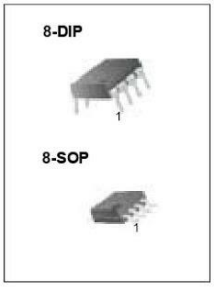
LM311
Single Comparator

Features

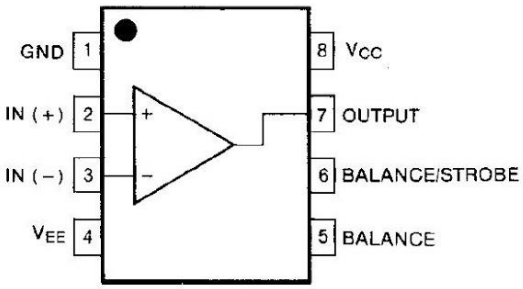
- Low input bias current : 250nA (Max)
- Low input offset current : 50nA (Max)
- Differential Input Voltage : ±30V
- Power supply voltage : single 5.0V supply to ±15V.
- Offset voltage null capability.
- Strobe capability.

Description

The LM311 series is a monolithic, low input current voltage comparator. The device is also designed to operate from dual or single supply voltage.

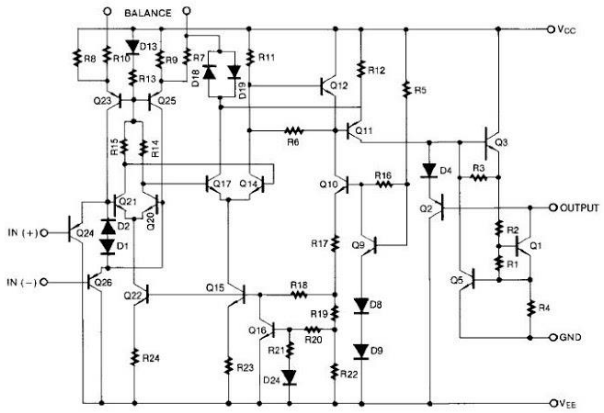


Internal Block Diagram



Rev. 1.0.1

Schematic Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Total Supply Voltage	V_{CC}	36	V
Output to Negative Supply Voltage LM311	V_O - V_{EE}	40	V
Ground to Negative voltage	V_{EE}	-30	V
Differential Input Voltage	$V_{I(DIFF)}$	30	V
Input Voltage	V_I	±15	V
Output Short Circuit Duration	-	10	sec
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_{OPR}	0 ~ +70	°C
Storage Temperature Range	T_{STG}	- 65 ~ +150	°C

Electrical Characteristics

(V_{CC} = 15V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Offset Voltage	V_{IO}	$R_S \leq 50K\Omega$		-	1.0	7.5	mV
			Note 1	-	-	10	
Input Offset Current	I_{IO}			-	6	50	nA
			Note 1	-	-	70	
Input Bias Current	I_{BIAS}			-	100	250	nA
			Note 1	-	-	300	
Voltage Gain	G_V	-		40	200	-	V/mV
Response Time	T_{RES}		Note 2	-	200	-	ns
Saturation Voltage	V_{SAT}	I_O =50mA, $V_I \leq$ -10mV		-	0.75	1.5	V
		$V_{CC} \geq$ 4.5V, V_{EE} =0V I_O =8mA, $V_I \leq$ -10mV,	Note 1	-	0.23	0.4	
Strobe "ON" Current	$I_{STR(ON)}$	-		-	3	-	mA
Output Leakage Current	I_{SINK}	I_{STR} =3mA, $V_I \geq$ 10mV V_O =15V, V_{CC}=±15V		-	0.2	50	nA
Input Voltage Range	$V_{I(R)}$	Note 1		-14.5 to 13.0	-14.7 to 13.8	-	V
Positive Supply Current	I_{CC}	-		-	3.0	7.5	mA
Negative Supply Current	I_{EE}	-		-	-2.2	-5.0	mA
Strobe Current	I_{STR}	-		-	3	-	mA

Notes :
1. $0 \leq T_A \leq +70°C$
2. The response time specified is for a 100mV input step with 5mV over drive.

Typical Performance Characteristics

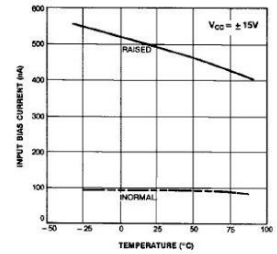


Figure 1. Input Bias Current vs Temperature

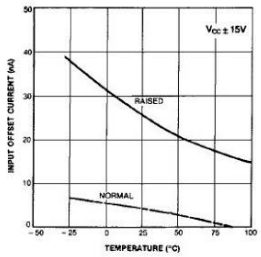


Figure 2. Input Offset Current vs Temperature

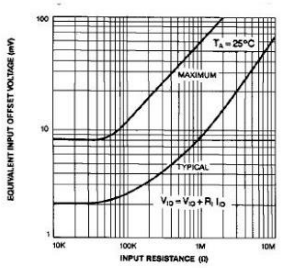


Figure 3. Offset Voltage vs Input Resistance

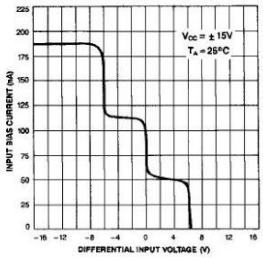


Figure 4. Input Bias Current vs Differential input voltage

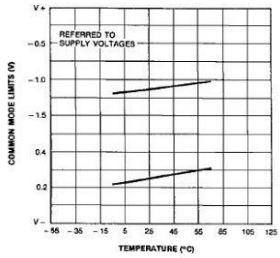


Figure 5. Common Mode Limits vs Temperature

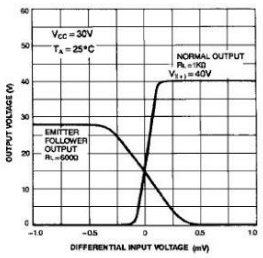


Figure 6. Output Voltage vs Differential input voltage

Typical Performance Characteristics (continued)

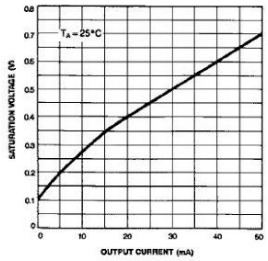


Figure 7. Saturation voltage vs Current

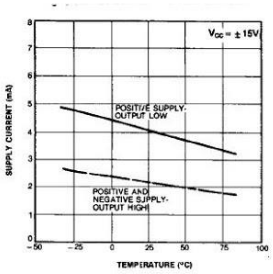


Figure 8. Supply Current vs Temperature

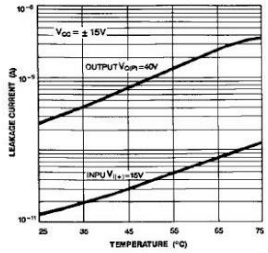


Figure 9. Leakage Current vs Temperature

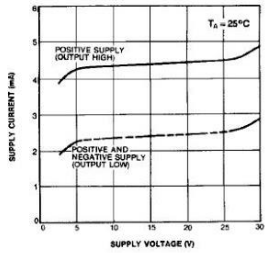


Figure 10. Supply Current vs Supply Voltage

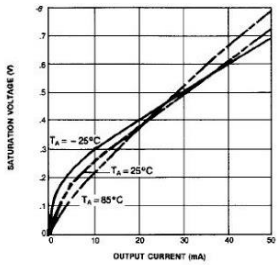


Figure 11. Current Saturation Voltage

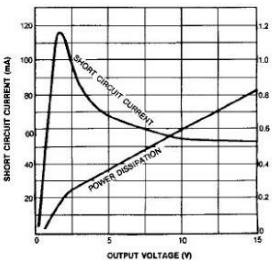
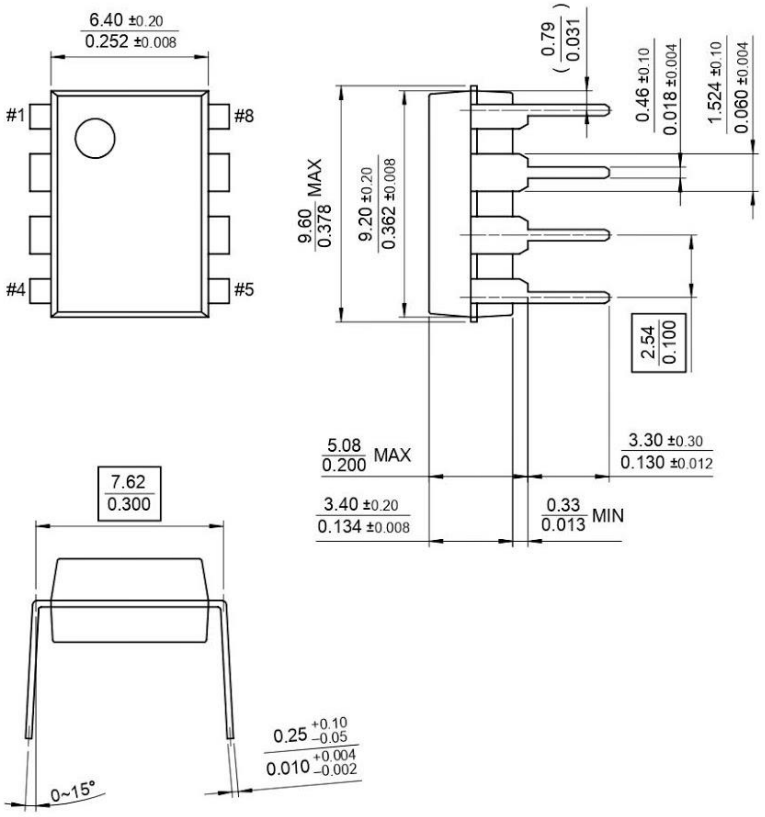


Figure 12. Output Limiting Characterstics

Mechanical Dimensions

Package

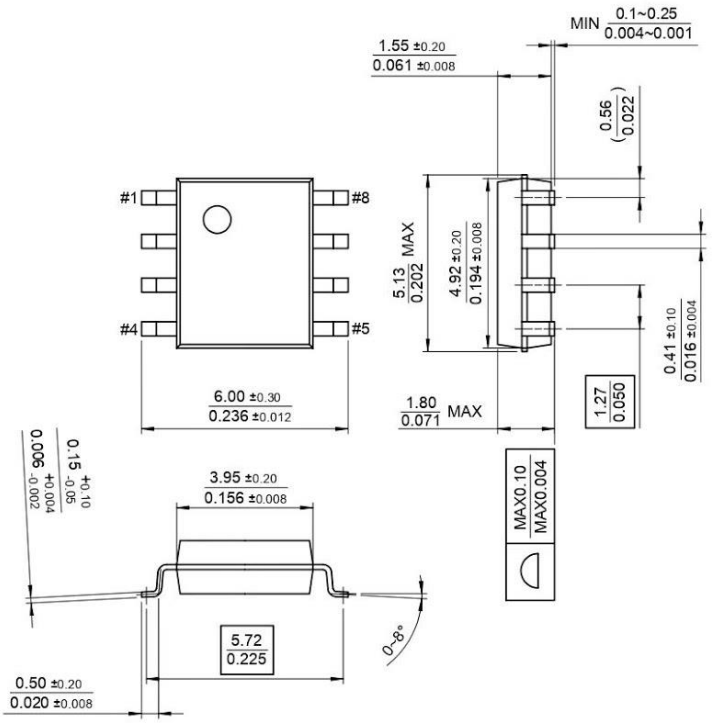
8-DIP



Mechanical Dimensions (Continued)

Package

8-SOP



Ordering Information

Product Number	Package	Operating Temperature
LM311N	8-DIP	0 ~ +70°C
LM311M	8-SOP	

14.- LM741

TEXAS INSTRUMENTS

uA741

SLOS094E – NOVEMBER 1970 – REVISED JANUARY 2015

µA741 General-Purpose Operational Amplifiers

1 Features

- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- No Latch-Up

2 Applications

- DVD Recorders and Players
- Pro Audio Mixers

3 Description

The µA741 device is a general-purpose operational amplifier featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 11.

The µA741C device is characterized for operation from 0°C to 70°C. The µA741M device (obsolete) is characterized for operation over the full military temperature range of –55°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
µA741x	SOIC (8)	4.90 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm
	SO (8)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

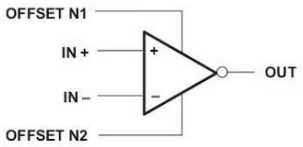


Table of Contents

5 Revision History

Changes from Revision D (February 2014) to Revision E — **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Moved *Typical Characteristics* into *Specifications* section. ... 7

Changes from Revision C (January 2014) to Revision D — **Page**

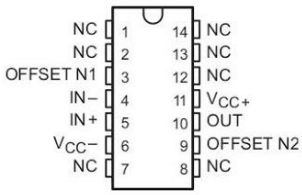
- Fixed *Typical Characteristics* graphs to remove extra lines. ... 7

Changes from Revision B (September 2000) to Revision C — **Page**

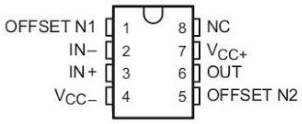
- Updated document to new TI data sheet format - no specification changes. ... 1
- Deleted *Ordering Information* table. ... 1

6 Pin Configurations and Functions

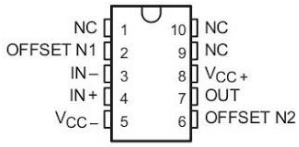
µA741M . . . J PACKAGE
(TOP VIEW)



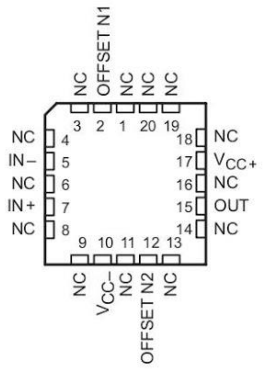
µA741M . . . JG PACKAGE
µA741C, µA741I . . . D, P, OR PW PACKAGE
(TOP VIEW)



µA741M . . . U PACKAGE
(TOP VIEW)



µA741M . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

Pin Functions

NAME	PIN				TYPE	DESCRIPTION
	J	JG, D, P, or PW	U	FK		
IN+	5	3	4	7	I	Noninverting input
IN–	4	2	3	5	I	Inverting input
NC	1, 2, 8, 12, 13, 14	8	1, 9, 10	1,3,4,6,8,9,11,13,14,16,18,19,20	—	Do not connect
OFFSET N1	3	1	2	2	I	External input offset voltage adjustment
OFFSET N2	9	5	6	12	I	External input offset voltage adjustment
OUT	10	6	7	15	O	Output
V_{CC}+	11	7	8	17	—	Positive supply
V_{CC}–	6	4	5	10	—	Negative supply

7 Specifications

7.1 Absolute Maximum Ratings

over virtual junction temperature range (unless otherwise noted)(1)

			µA741C		µA741M		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage(2)		–18	18	–22	22	C
V_{ID}	Differential input voltage(3)		–15	15	–30	30	V
V_I	Input voltage, any input(2)(4)		–15	15	–15	15	V
	Voltage between offset null (either OFFSET N1 or OFFSET N2) and V_{CC-}		–15	15	–0.5	0.5	V
	Duration of output short circuit(5)		Unlimited				
	Continuous total power dissipation		See Table 1				
T_A	Operating free-air temperature range		0	70	–55	125	°C
	Case temperature for 60 seconds	FK package	N/A	N/A		260	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	J, JG, or U package	N/A	N/A		300	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	D, P, or PS package		260	N/A	N/A	°C
T_{stg}	Storage temperature range		–65	150	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+ with respect to IN –.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or either power supply. For the µA741M only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

7.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
V_{CC-}			–5	–15	
T_A	Operating free-air temperature	µA741C	0	70	°C
		µA741M	–55	125	

Table 1. Dissipation Ratings Table

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	TA = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	N/A	N/A	500 mW	500 mW	N/A
PS	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW

7.3 Electrical Characteristics µA741C, µA741M

at specified virtual junction temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	µA741C			µA741M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		1	6		1	5	mV
			Full range			7.5		±15	6	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0	25°C		±15			20	200	mV
I_{IO}	Input offset current	V_O = 0	25°C		20	200			500	nA
			Full range			300			500	
I_{IB}	Input bias current	V_O = 0	25°C		80	500		80	500	nA
			Full range			800			1500	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		±12	±14		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L = 2 kΩ	25°C	±10			±10	±13		
		R_L ≥ 2kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2kΩ	25°C	20	200		50	200		V/mV
		V_O = ±10 V	Full range	15			25			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0, See (2)	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V	25°C		30	150		30	150	µV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	V_O = 0, No load	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	V_O = 0, No load	25°C		50	85		50	85	mW
			Full range			100			100	

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the µA741C is 0°C to 70°C and the µA741M is –55°C to 125°C.
(2) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

7.4 Electrical Characteristics µA741Y

at specified virtual junction temperature, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	µA741Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0		1	5	mV
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0		±15		mV
I_{IO}	Input offset current	V_O = 0		20	200	nA
I_{IB}	Input bias current	V_O = 0		80	500	nA
V_{ICR}	Common-mode input voltage range		±12	±13		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	±12	±14		V
		R_L = 2 kΩ	±10	±13		
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2kΩ	20	200		V/mV
r_i	Input resistance		0.3	2		MΩ
r_o	Output resistance	V_O = 0, See(1)		75		Ω
C_i	Input capacitance			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$	70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V		30	150	µV/V
I_{OS}	Short-circuit output current			±25	±40	mA
I_{CC}	Supply current	V_O = 0, No load		1.7	2.8	mA
P_D	Total power dissipation	V_O = 0, No load		50	85	mW

(1) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

7.5 Switching Characteristics µA741C, µA741M

over operating free-air temperature range, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	µA741C			µA741M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.3			0.3		µs
	Overshoot factor			5%			5%		—
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5			0.5		V/µs

7.6 Switching Characteristics µA741Y

over operating free-air temperature range, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	µA741Y			UNIT
			MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.3		µs
	Overshoot factor			5%		—
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5		V/µs

7.7 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

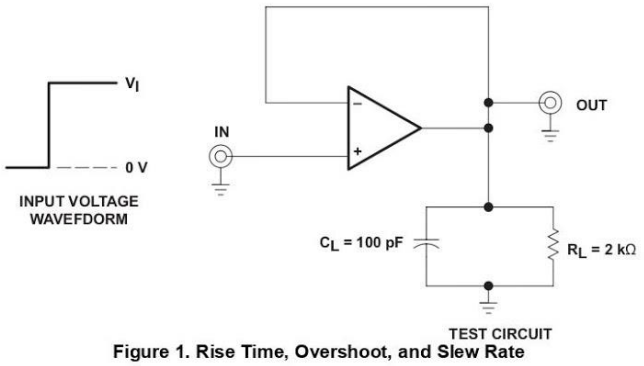


Figure 1. Rise Time, Overshoot, and Slew Rate

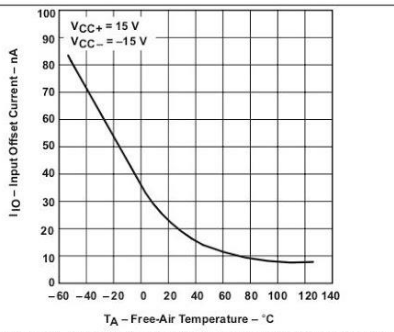


Figure 2. Input Offset Current vs Free-Air Temperature

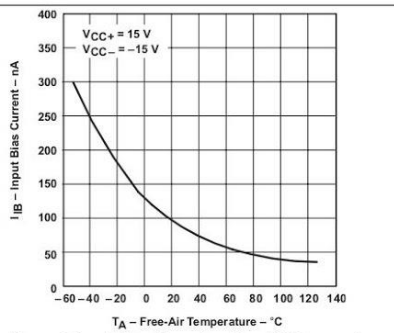


Figure 3. Input Bias Current vs Free-Air Temperature

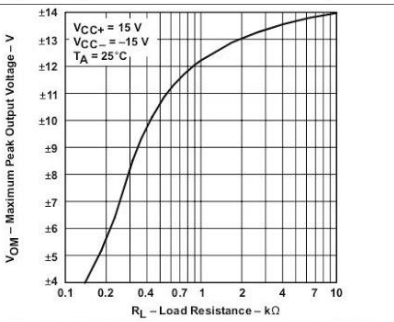


Figure 4. Maximum Output Voltage vs Load Resistance

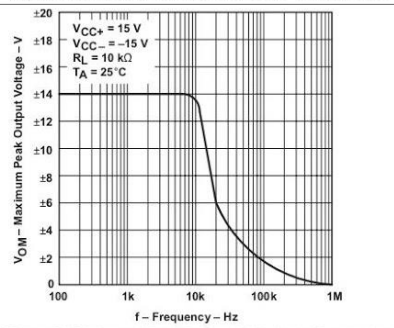


Figure 5. Maximum Peak Output Voltage vs Frequency

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

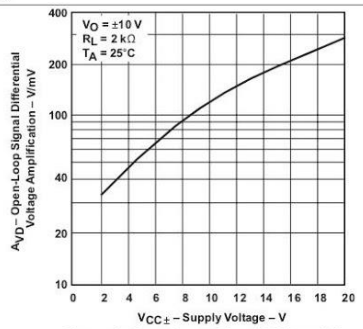


Figure 6. Open-Loop Signal Differential Voltage Amplification vs Supply Voltage

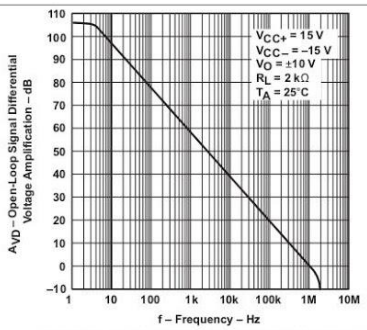


Figure 7. Open-Loop Large-Signal Differential Voltage Amplification vs Frequency

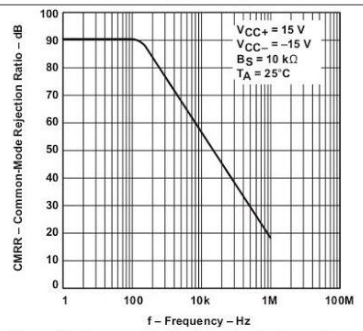


Figure 8. Common-Mode Rejection Ratio vs Frequency

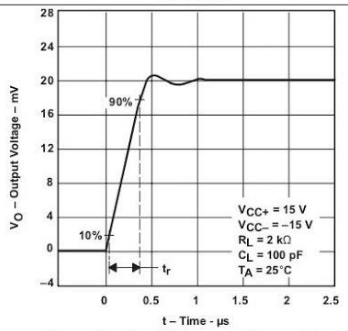


Figure 9. Output Voltage vs Elapsed Time

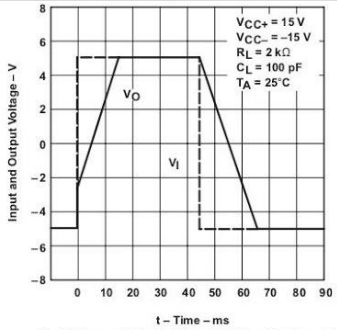


Figure 10. Voltage-Follower Large-Signal Pulse Response

8 Detailed Description

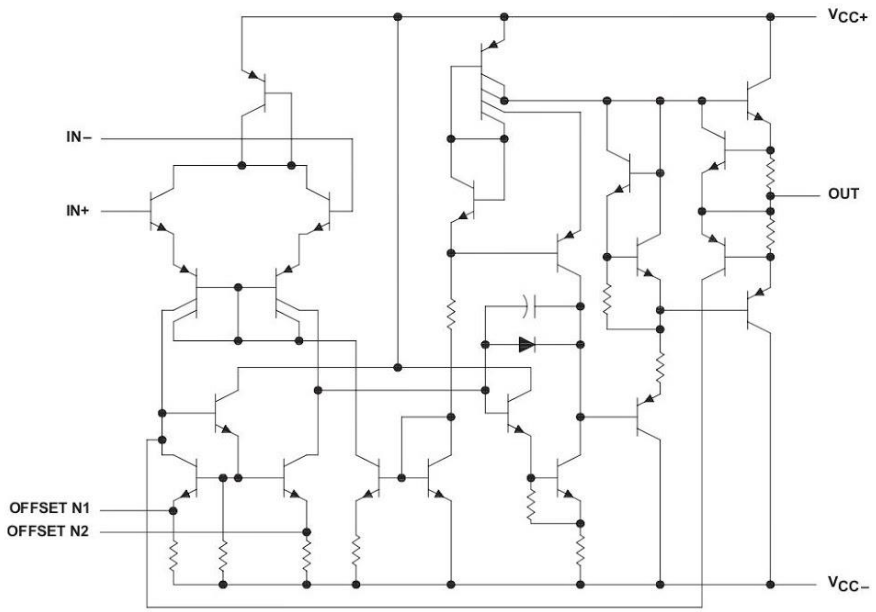
8.1 Overview

The µA741 device is a general-purpose operational amplifier featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 11.

The µA741C device is characterized for operation from 0°C to 70°C. The µA741M device (obsolete) is characterized for operation over the full military temperature range of –55°C to 125°C.

8.2 Functional Block Diagram



Component Count	
Transistors	22
Resistors	11
Diode	1
Capacitor	1

8.3 Feature Description

8.3.1 Offset-Voltage Null Capability

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors, etc. The input offset pins allow the designer to adjust for these mismatches by external circuitry. See the *Application and Implementation* section for more details on design techniques.

8.3.2 Slew Rate

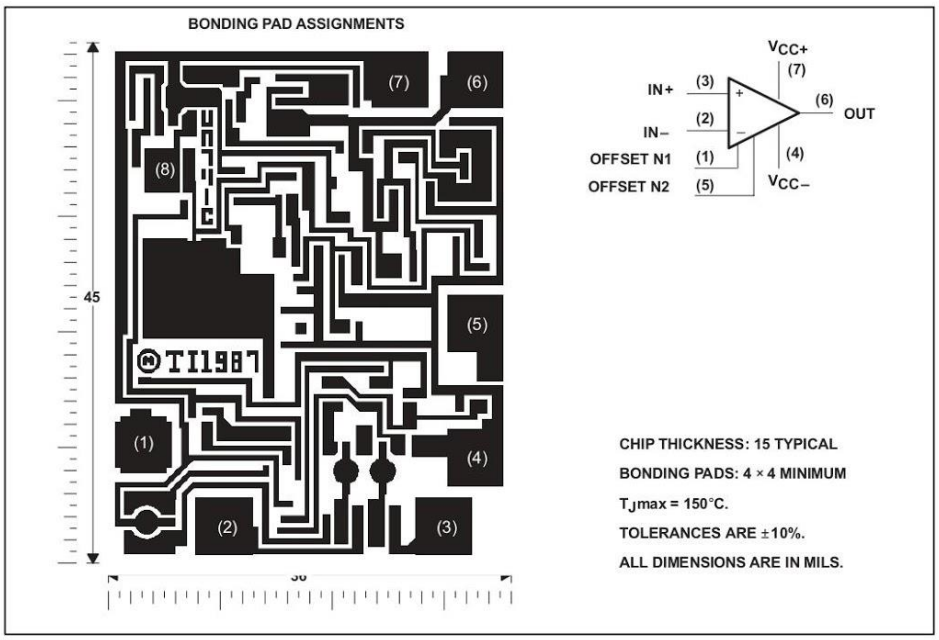
The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The μA741 has a 0.5-V/μs slew rate. Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* graphs.

8.4 Device Functional Modes

The μA741 is powered on when the supply is connected. It can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

8.5 μA741Y Chip Information

This chip, when properly assembled, displays characteristics similar to the μA741C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors, etc. The input offset pins allow the designer to adjust for these mismatches by external circuitry. These input mismatches can be adjusted by putting resistors or a potentiometer between the inputs as shown in Figure 13. A potentiometer can be used to fine tune the circuit during testing or for applications which require precision offset control. More information about designing using the input-offset pins, see the application note *Nulling Input Offset Voltage of Operational Amplifiers*, SLOA045.

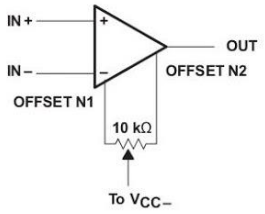


Figure 11. Input Offset Voltage Null Circuit

9.2 Typical Application

The voltage follower configuration of the operational amplifier is used for applications where a weak signal is used to drive a relatively high current load. This circuit is also called a buffer amplifier or unity gain amplifier. The inputs of an operational amplifier have a very high resistance which puts a negligible current load on the voltage source. The output resistance of the operational amplifier is almost negligible, so it can provide as much current as necessary to the output load.

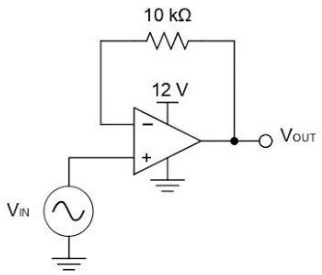


Figure 12. Voltage Follower Schematic

9.2.1 Design Requirements

- Output range of 2 V to 11.5 V
- Input range of 2 V to 11.5 V

Typical Application (continued)

- Resistive feedback to negative input

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Swing

The output voltage of an operational amplifier is limited by its internal circuitry to some level below the supply rails. For this amplifier, the output voltage swing is within ±12 V, which accommodates the input and output voltage requirements.

9.2.2.2 Supply and Input Voltage

For correct operation of the amplifier, neither input must be higher than the recommended positive supply rail voltage or lower than the recommended negative supply rail voltage. The chosen amplifier must be able to operate at the supply voltage that accommodates the inputs. Because the input for this application goes up to 11.5 V, the supply voltage must be 12 V. Using a negative voltage on the lower rail rather than ground allows the amplifier to maintain linearity for inputs below 2 V.

9.2.3 Application Curves for Output Characteristics

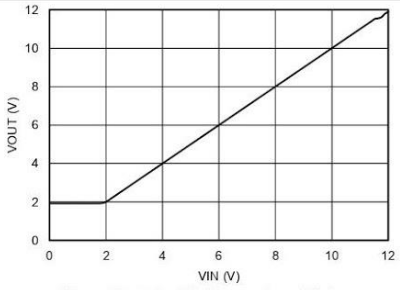


Figure 13. Output Voltage vs Input Voltage

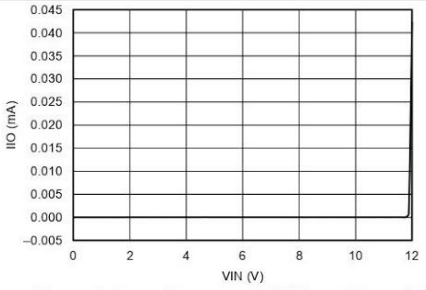


Figure 14. Current Drawn Input of Voltage Follower (I_{IO}) vs Input Voltage

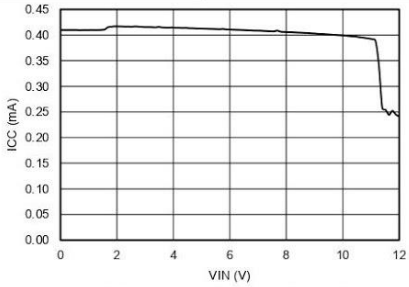


Figure 15. Current Drawn from Supply (I_{CC}) vs Input Voltage

10 Power Supply Recommendations

The µA741 is specified for operation from ±5 to ±15 V; many specifications apply from 0°C to 70°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than ±18 V can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

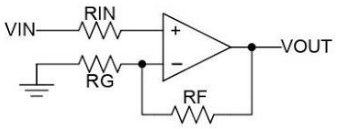


Figure 16. Operational Amplifier Schematic for Noninverting Configuration

Layout Example (continued)

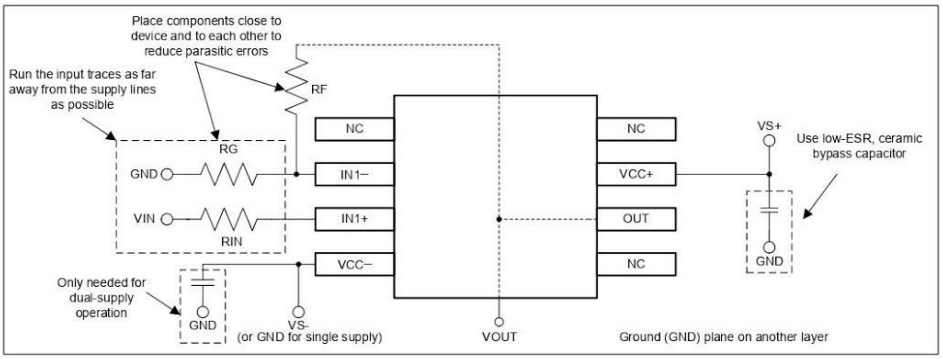


Figure 17. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

TEXAS INSTRUMENTS

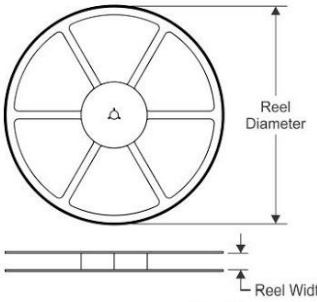
PACKAGE MATERIALS INFORMATION

www.ti.com

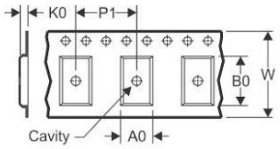
17-Feb-2014

TAPE AND REEL INFORMATION

REEL DIMENSIONS

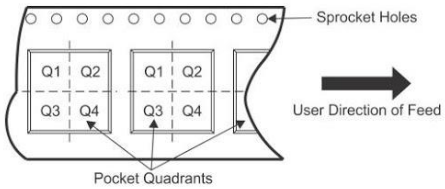


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA741CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA741CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1

TEXAS INSTRUMENTS

PACKAGE MATERIALS INFORMATION

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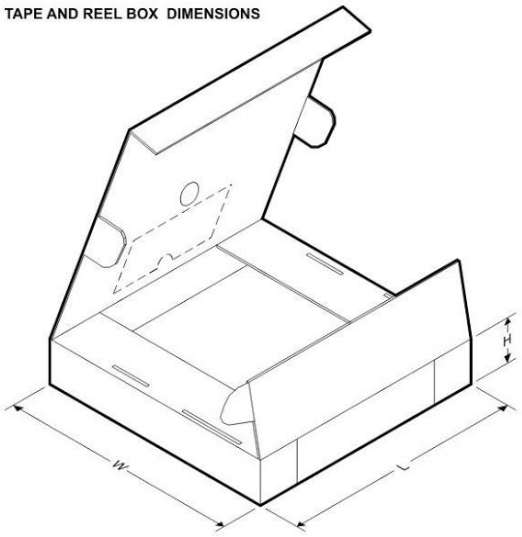
17-Feb-2014

TAPE AND REEL BOX DIMENSIONS



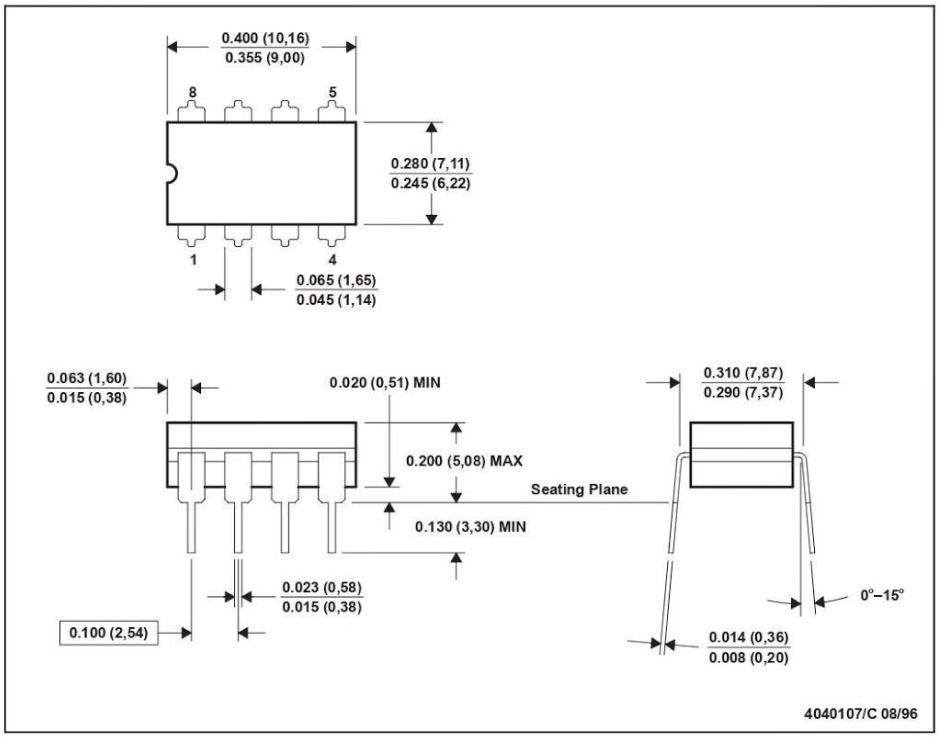
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA741CDR	SOIC	D	8	2500	340.5	338.1	20.6
UA741CPSR	SO	PS	8	2000	367.0	367.0	38.0

MECHANICAL DATA

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**

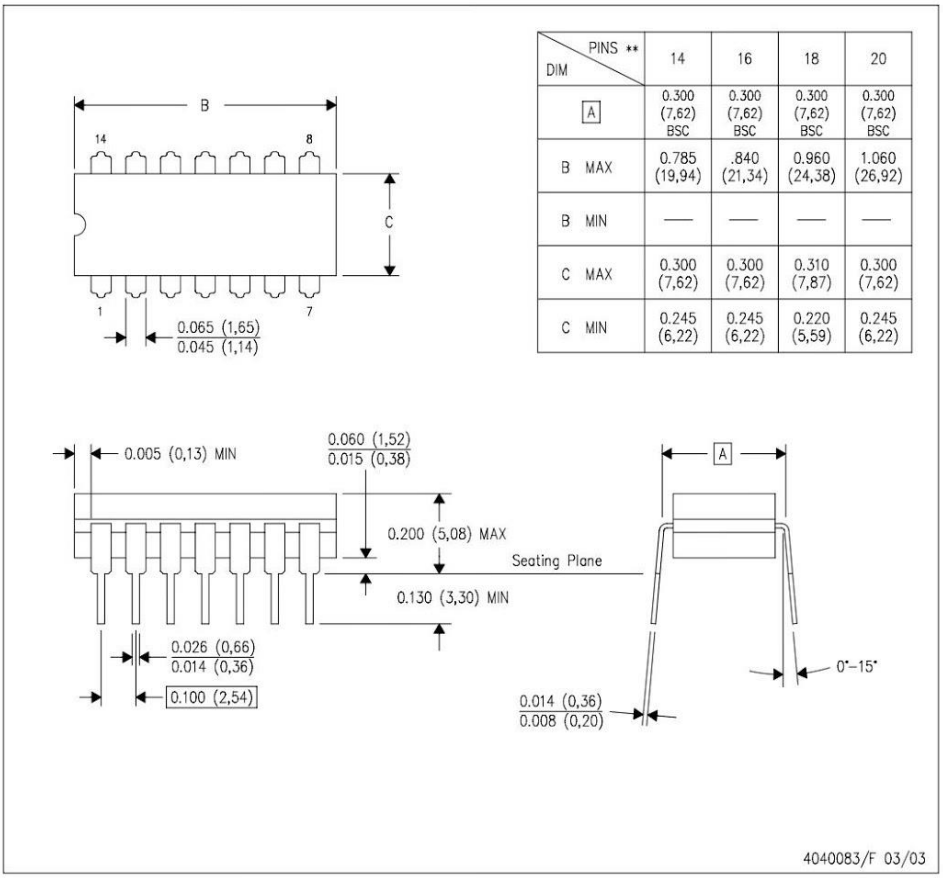


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



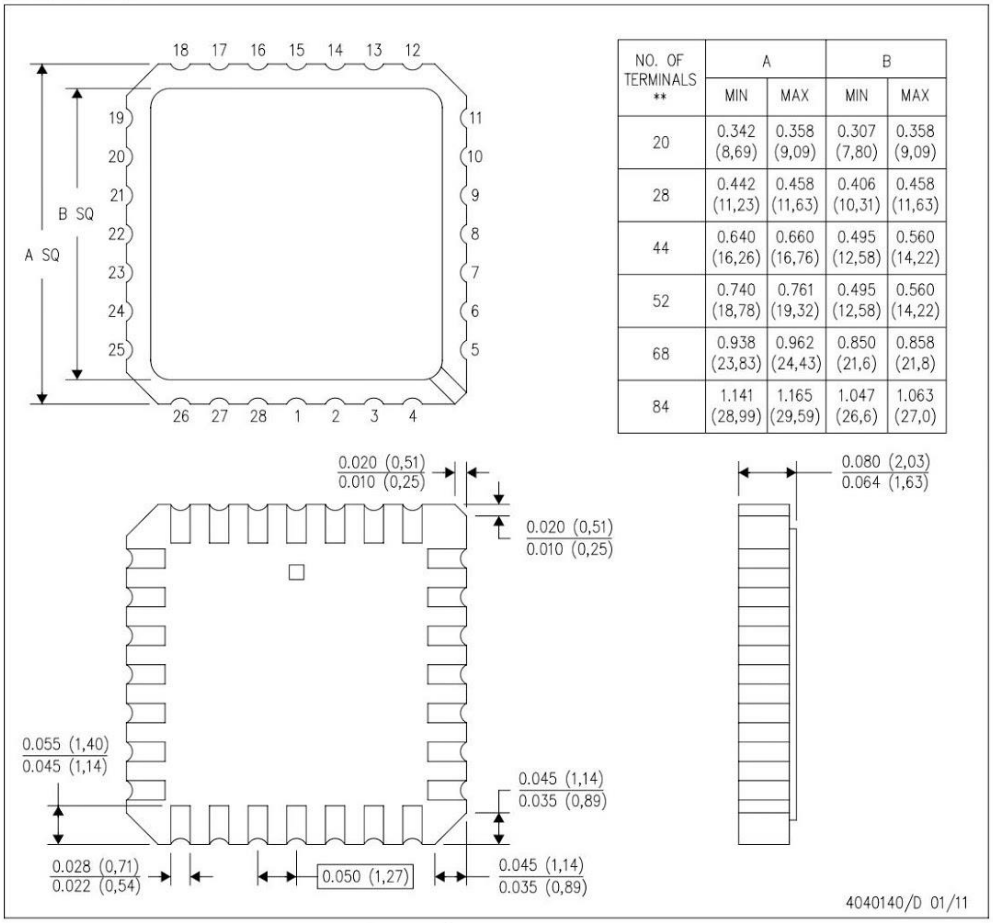
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MECHANICAL DATA

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

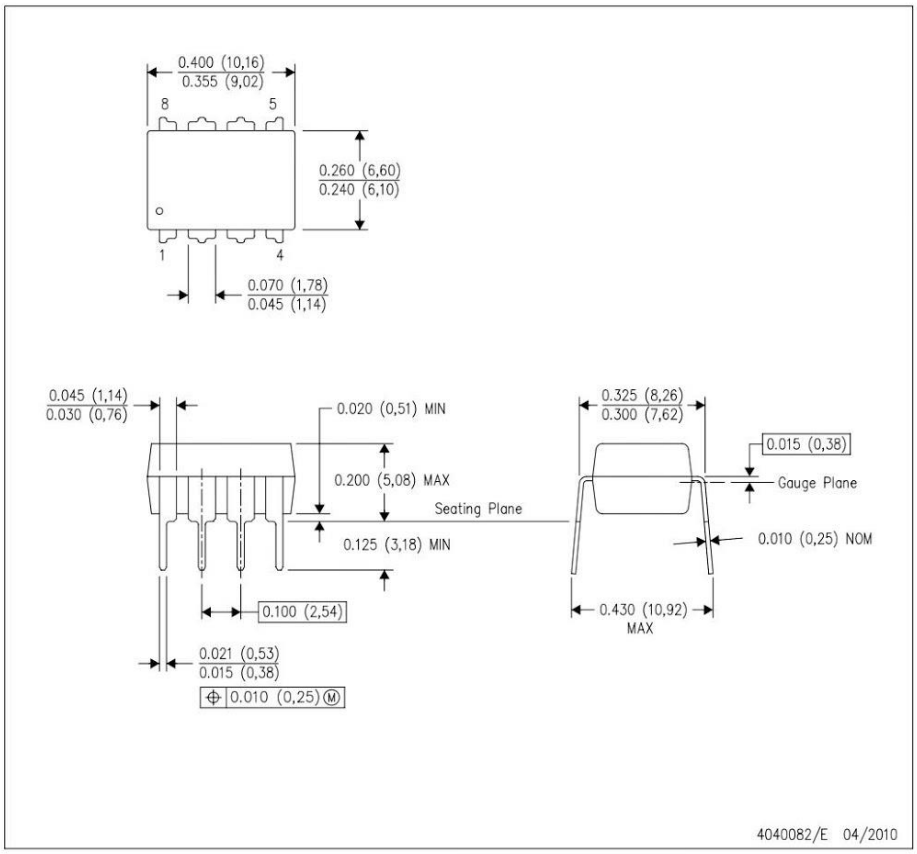


NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

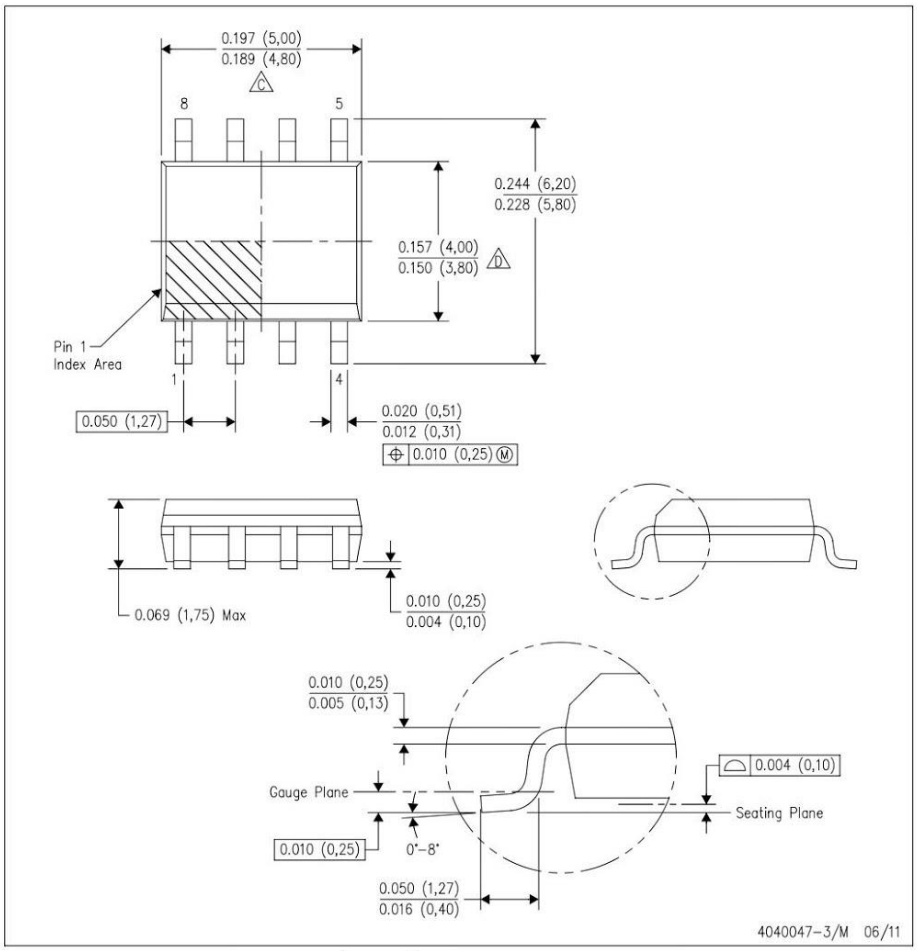
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

MECHANICAL DATA

D (R–PDSO–G8) PLASTIC SMALL OUTLINE

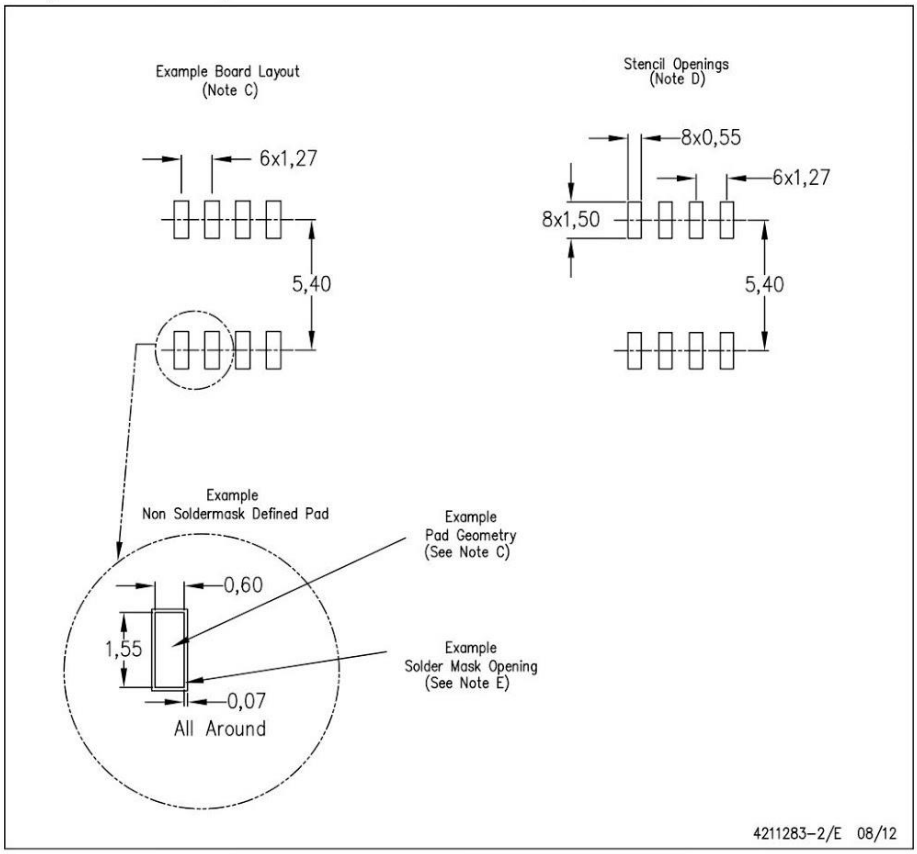


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

TEXAS INSTRUMENTS
www.ti.com

LAND PATTERN DATA

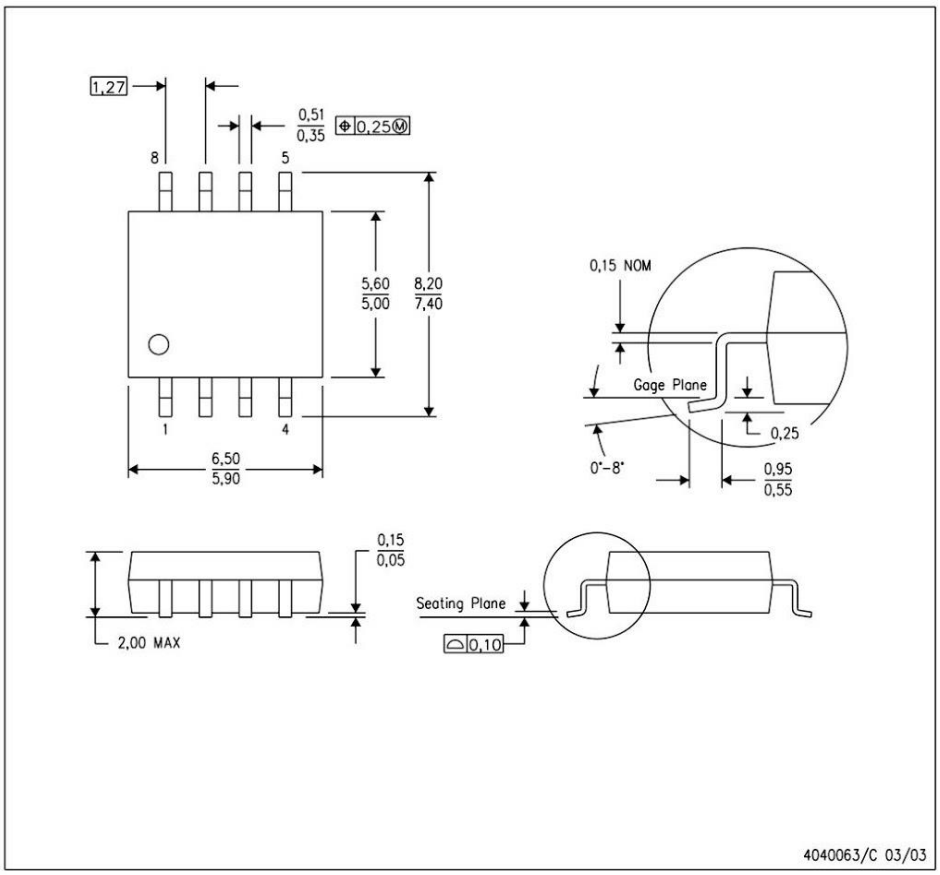
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

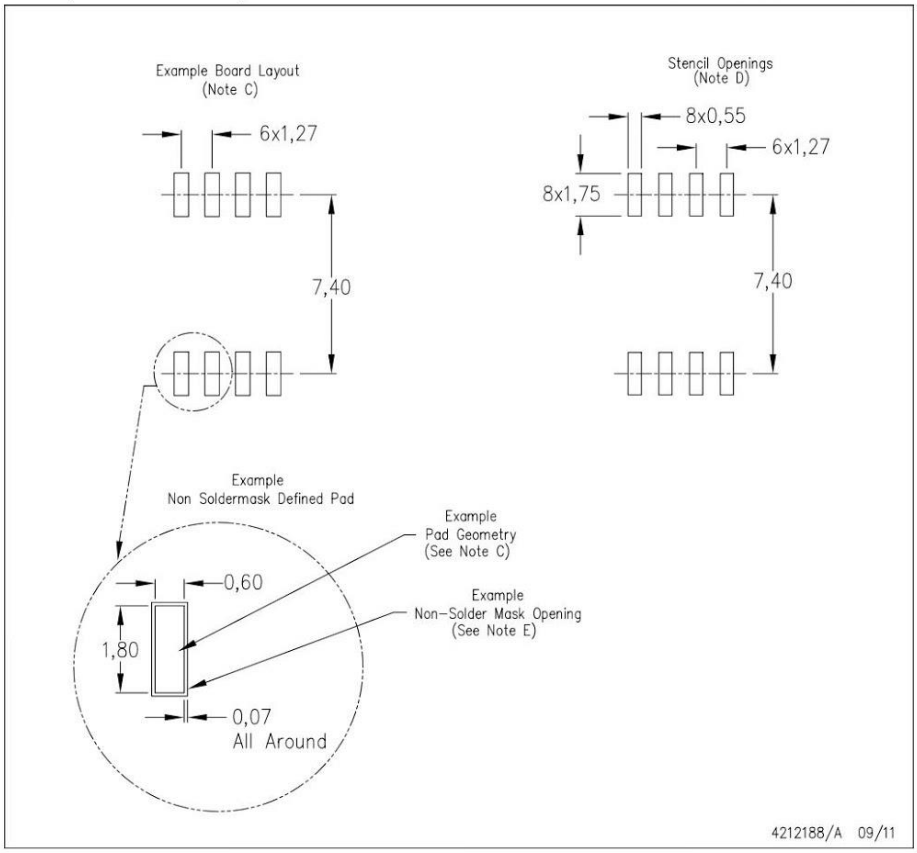
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

LAND PATTERN DATA

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

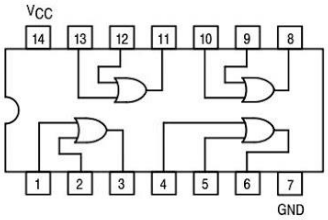
15.- 74LS32

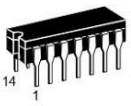
MOTOROLA

QUAD 2-INPUT OR GATE

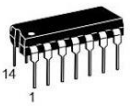
SN54/74LS32

QUAD 2-INPUT OR GATE
LOW POWER SCHOTTKY





J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS32

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

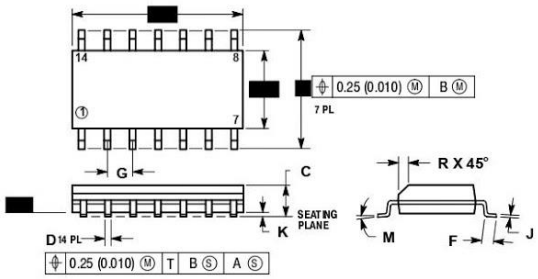
Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				6.2	mA	V_{CC} = MAX	
	Total, Output LOW				9.8			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Turn-Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn-On Delay, Input to Output		14	22	ns	

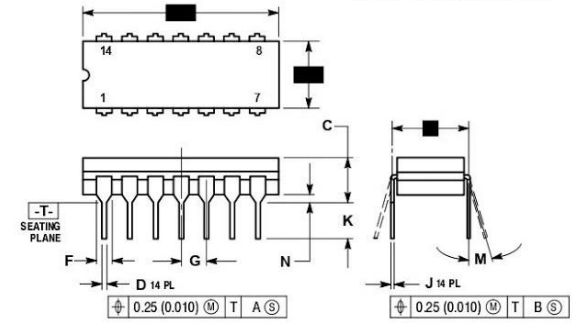
Case 751A-02 D Suffix
14-Pin Plastic
SO-14



NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
6. 751A-01 IS OBSOLETE, NEW STANDARD 751A-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

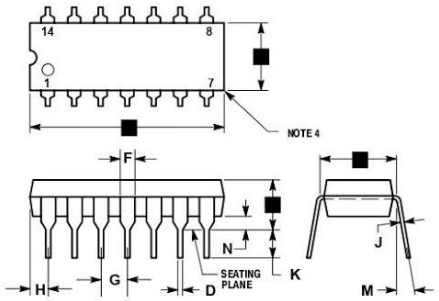
Case 632-08 J Suffix
14-Pin Ceramic Dual In-Line



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. 632-01 THRU-07 OBSOLETE, NEW STANDARD 632-08.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

Case 646-06 N Suffix
14-Pin Plastic



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.
5. 646-05 OBSOLETE, NEW STANDARD 646-06.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

16.- 74LS08

FAIRCHILD
SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS08
Quad 2-Input AND Gates

General Description

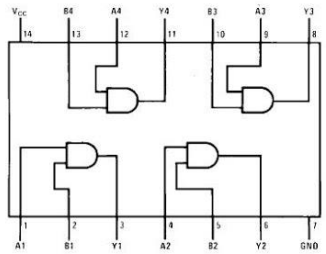
This device contains four independent gates each of which performs the logic AND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS08M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS08SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS08N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Y = AB

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

 DS006347 www.fairchildsemi.com

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		2.4	4.8	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		4.4	8.8	mA

Switching Characteristics

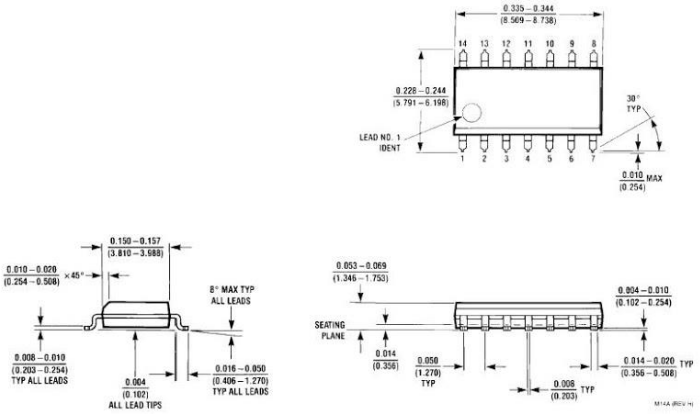
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	5	18	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

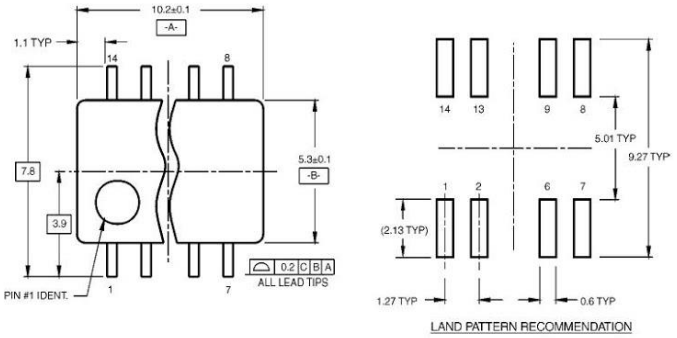
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters) unless otherwise noted

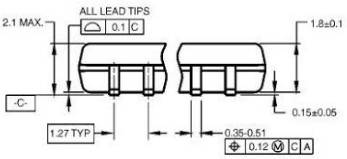


14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

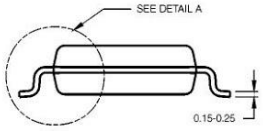
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

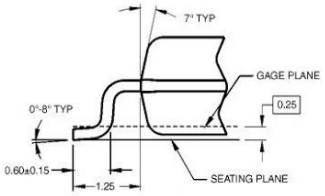


LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS





DETAIL A

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

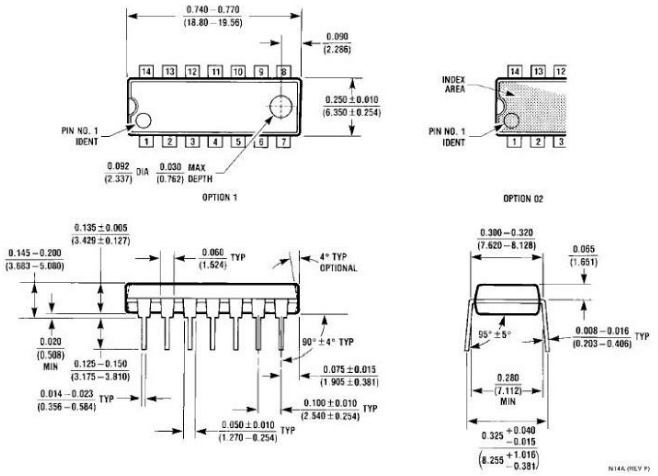
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

17.- DISPLAY 7 SEGMENTOS.

Agilent Technologies

7.6 mm (0.3 inch) Micro Bright Seven Segment Displays

Technical Data

HDSP-740x Series
HDSP-750x Series
HDSP-780x Series
HDSP-A15x Series
HDSP-A40x Series

Features

- **Available with Colon for Clock Display**
- **Compact Package**
  0.300 x 0.500 inches
  Leads on 2.54 mm (0.1 inch) Centers
- **Choice of Colors**
  AlGaAs Red, High Efficiency Red, Yellow, Green, Orange
- **Excellent Appearance**
  Evenly Lighted Segments
  Mitered Corners on Segments
  Surface Color Gives Optimum Contrast
  ± 50° Viewing Angle
- **Design Flexibility**
  Common Anode or Common Cathode
  Right Hand Decimal Point
  ± 1. Overflow Character
- **Categorized for Luminous Intensity**
  Yellow and Green Categorized for Color
  Use of Like Categories Yields a Uniform Display
- **High Light Output**
- **High Peak Current**
- **Excellent for Long Digit String Multiplexing**
- **Intensity and Color Selection Available**
  See Intensity and Color Selected Displays Data Sheet
- **Sunlight Viewable AlGaAs**

Description

The 7.6 mm (0.3 inch) LED seven segment displays are designed for viewing distances up to 3 metres (10 feet). These devices use an industry standard size package and pinout. Both the numeric and

Devices

Orange HDSP-	AlGaAs[1] HDSP-	HER[1] HDSP-	Yellow[1] HDSP-	Green[1] HDSP-	Description	Package Drawing
A401	A151	7501	7401	7801	Common Anode Right Hand Decimal	A
		7502	7402	7802	Common Anode Right Hand Decimal, Colon	B
A403	A153	7503	7403	7803	Common Cathode Right Hand Decimal	C
		7504	7404	7804	Common Cathode Right Hand Decimal, Colon	D
	A157	7507	7407	7807	Common Anode ± 1. Overflow	E
	A158	7508	7408	7808	Common Cathode ± 1. Overflow	F

Note:
1. These displays are recommended for high ambient light operation. Please refer to the HDSP-A10X AlGaAs, HDSP-335X HER, HDSP-A80X Yellow, and HDSP-A90X Green data sheet for low current operation.

± 1. overflow devices feature a right hand decimal point. All devices are available as either common anode or common cathode.

These displays are ideal for most applications. Pin for pin equivalent displays are also available in a low current design. The low current displays are ideal for portable applications. For additional information see the Low Current Seven Segment Displays.

Part Numbering System

5082 -X X X X-X X X X X
HDSP-X X X X-X X X X X

Mechanical Options[1]
00: No Mechanical Option

Color Bin Options[1,2]
0: No Color Bin Limitation
3: Color Bins 3- and 3+ only (applicable for Yellow devices only)
Z: Color Bins 2- and 3+ only (applicable for Yellow devices only)

Maximum Intensity Bin[1,2]
0: No Maximum Intensity Bin Limitation

Minimum Intensity Bin[1,2]
0: No Minimum Intensity Bin Limitation

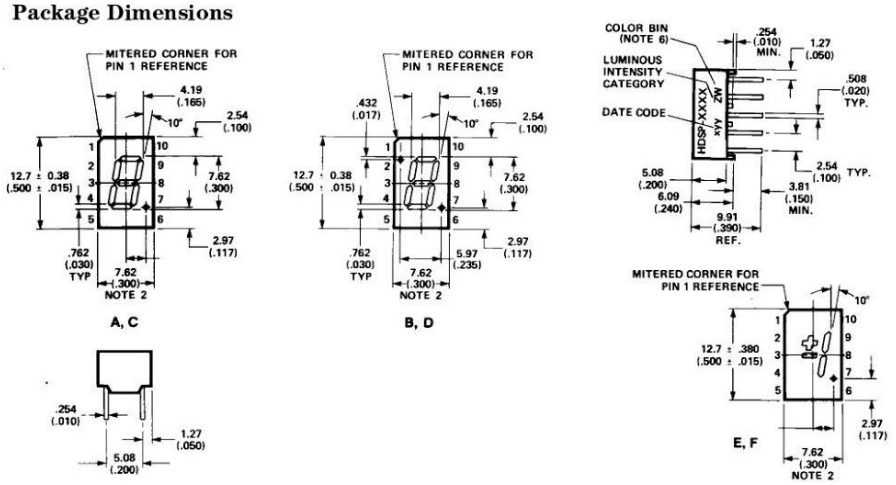
Device Configuration/Color[1]
1: Common Anode
2: Common Anode
3: Common Cathode
4: Common Cathode

Device Specific Configuration[1]
Refer to Respective Datasheet

Package[1]
A: 7.6 mm (0.3 inch) Single Digit Seven Segment Display

Notes:
1. For codes not listed in the figure above, please refer to the respective datasheet or contact your nearest Agilent representative for details.
2. Bin options refer to shippable bins for a part number. Color and Intensity Bins are typically restricted to 1 bin per tube (exceptions may apply). Please refer to respective datasheet for specific bin limit information.

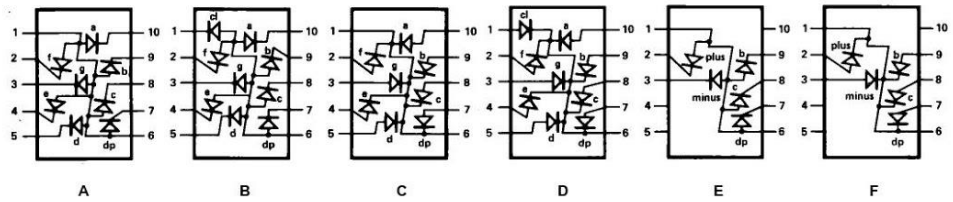
Package Dimensions



NOTES:
1. ALL DIMENSIONS IN MILLIMETRES (INCHES).
2. MAXIMUM.
3. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
4. REDUNDANT ANODES.
5. REDUNDANT CATHODES.
6. FOR HDSP-7400/-7800 SERIES PRODUCT ONLY.

	FUNCTION					
PIN	A	B	C	D	E	F
1	ANODE[4]	CATHODE COLON	CATHODE[5]	ANODE COLON	ANODE[4]	CATHODE[5]
2	CATHODE f	CATHODE f	ANODE f	ANODE f	CATHODE PLUS	ANODE PLUS
3	CATHODE g	CATHODE g	ANODE g	ANODE g	CATHODE MINUS	ANODE MINUS
4	CATHODE e	CATHODE e	ANODE e	ANODE e	NC	NC
5	CATHODE d	CATHODE d	ANODE d	ANODE d	NC	NC
6	ANODE[4]	ANODE	CATHODE[5]	CATHODE	ANODE[4]	CATHODE[5]
7	CATHODE DP	CATHODE DP	ANODE DP	ANODE DP	CATHODE DP	ANODE DP
8	CATHODE c	CATHODE c	ANODE c	ANODE c	CATHODE c	ANODE c
9	CATHODE b	CATHODE b	ANODE b	ANODE b	CATHODE b	ANODE b
10	CATHODE a	CATHODE a	ANODE a	ANODE a	NC	NC

Internal Circuit Diagram



Absolute Maximum Ratings

Description	AlGaAs Red HDSP-A150 Series	HER/Orange HDSP-7500/-A40X Series	Yellow HDSP-7400 Series	Green HDSP-7800 Series	Units
Average Power per Segment or DP	96	105	80	105	mW
Peak Forward Current per Segment or DP	160[1]	90[3]	60[5]	90[7]	mA
DC Forward Current per Segment or DP	40[2]	30[4]	20[6]	30[8]	mA
Operating Temperature Range	–20 to +100[9]	–40 to +100			°C
Storage Temperature Range	–55 to +100				°C
Reverse Voltage per Segment or DP	3.0				V
Lead Solder Temperature for 3 Seconds (1.59 mm [0.063 in.] below seating plane)	260				°C

Notes:
1. See Figure 1 to establish pulsed conditions.
2. Derate above 46°C at 0.54 mA/°C.
3. See Figure 6 to establish pulsed conditions.
4. Derate above 53°C at 0.45 mA/°C.
5. See Figure 7 to establish pulsed conditions.
6. Derate above 81°C at 0.52 mA/°C.
7. See Figure 8 to establish pulsed conditions.
8. Derate above 39°C at 0.37 mA/°C.
9. For operation below –20°C, contact your local Agilent components sales office or an authorized distributor.

Electrical/Optical Characteristics at T_A = 25°C

AlGaAs Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A15x	Luminous Intensity/Segment[1,2,5] (Digit Average)	I_V	6.9	14.0		mcd	I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		1.8		V	I_F = 20 mA
				2.0	3.0	V	I_F = 100 mA
	Peak Wavelength	λ_{PEAK}		645		nm	
	Dominant Wavelength[3]	λ_d		637		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	15.0		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		255		°C/W/Seg	

High Efficiency Red

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
750x	Luminous Intensity/Segment[1,2,6] (Digit Average)	I_V	360	980		µcd	I_F = 5 mA
				5390			I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.0	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		635		nm	
	Dominant Wavelength[3]	λ_d		626		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$		200		°C/W/Seg	

Orange

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
A40x	Luminous Intensity/Segment[1,2,6] (Digit Average)	I_V		0.70		mcd	I_F = 5 mA
	Forward Voltage/Segment or DP	V_F		2.0	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		600		nm	
	Dominant Wavelength[3]	λ_d		603		nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	30		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$		200		°C/W/Seg	

Yellow

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
740x	Luminous Intensity/Segment[1,2,7] (Digit Average)	I_V	225	480		µcd	I_F = 5 mA
				2740			I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.2	2.5	V	I_F = 20 mA
	Peak Wavelength	λ_{PEAK}		583		nm	
	Dominant Wavelength[3,9]	λ_d	581.5	586	592.5	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50.0		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W/Seg	

High Performance Green

Device Series HDSP-	Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
780x	Luminous Intensity/Segment[1,2,8] (Digit Average)	I_V	860	3000		µcd	I_F = 10 mA
				6800			I_F = 20 mA
	Forward Voltage/Segment or DP	V_F		2.1	2.5	V	I_F = 10 mA
	Peak Wavelength	λ_{PEAK}		566		nm	
	Dominant Wavelength[3,9]	λ_d		571	577	nm	
	Reverse Voltage/Segment or DP[4]	V_R	3.0	50.0		V	I_R = 100 µA
	Temperature Coefficient of V_F/Segment or DP	ΔV_F/°C		-2		mV/°C	
	Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$		200		°C/W/Seg	

Notes:
1. Case temperature of device immediately prior to the intensity measurement is 25°C.
2. The digits are categorized for luminous intensity. The intensity category is designated by a letter on the side of the package.
3. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
4. Typical specification for reference only. Do not exceed absolute maximum ratings.
5. For low current operation the AlGaAs HDSP-A101 series displays are recommended.
6. For low current operation the HER HDSP-7511 series displays are recommended.
7. For low current operation the Yellow HDSP-A801 series displays are recommended.
8. For low current operation the Green HDSP-A901 series displays are recommended.
9. The yellow (HDSP-7400) and Green (HDSP-7800) displays are categorized for dominant wavelength. The category is designated by a number adjacent to the luminous intensity category letter.

AlGaAs Red

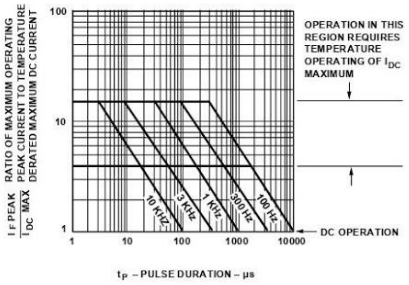


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration – AlGaAs Red.

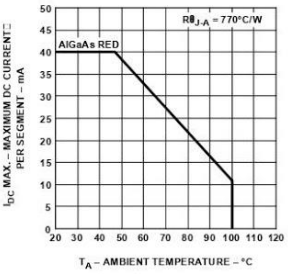


Figure 2. Maximum Allowable DC Current per Segment as a Function of Ambient Temperature.

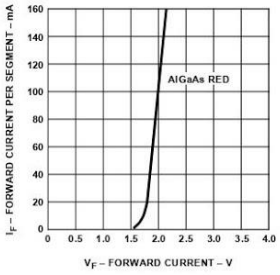


Figure 3. Forward Current vs. Forward Voltage.

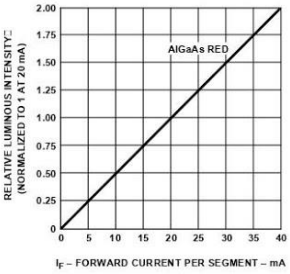


Figure 4. Relative Luminous Intensity vs. DC Forward Current.

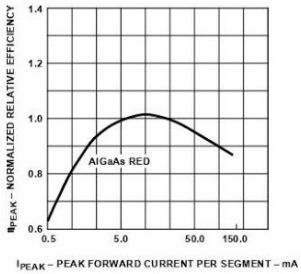


Figure 5. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

HER, Yellow, Green, Orange

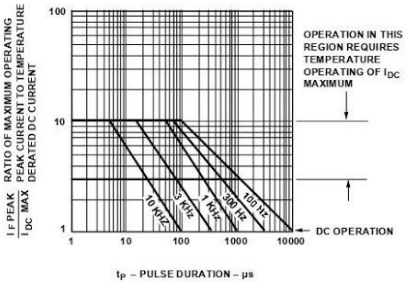


Figure 6. Maximum Tolerable Peak Current vs. Pulse Duration – HER, Orange.

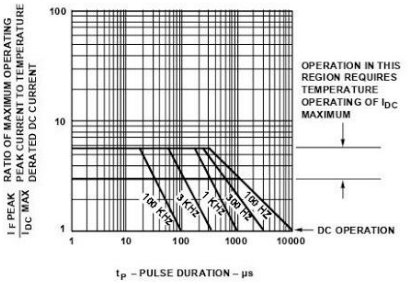


Figure 7. Maximum Tolerable Peak Current vs. Pulse Duration – Yellow.

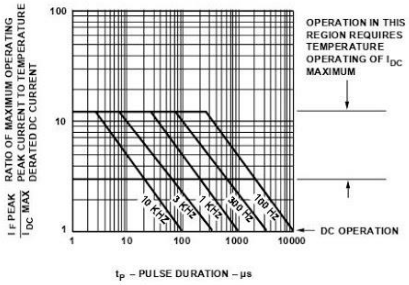


Figure 8. Allowable Peak Current vs. Pulse Duration – Green.

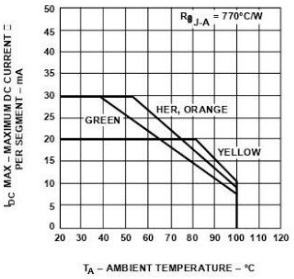


Figure 9. Maximum Allowable DC Current per Segment as a Function of Ambient Temperature.

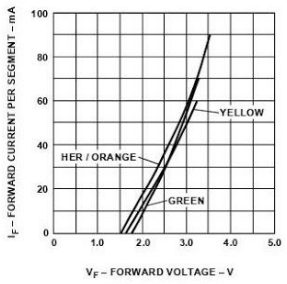


Figure 10. Forward Current vs. Forward Voltage Characteristics.

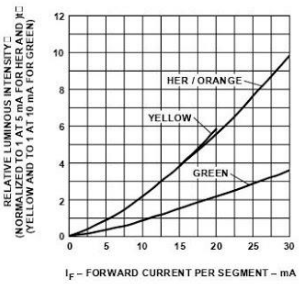


Figure 11. Relative Luminous Intensity vs. DC Forward Current.

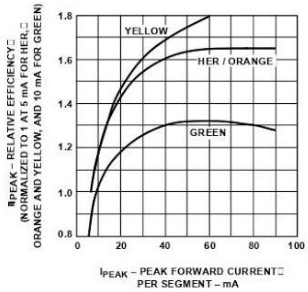


Figure 12. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

Intensity Bin Limits (mcd)

AlGaAs Red

HDSP-A15x		
IV Bin Category	**Min.**	**Max.**
M	7.07	13.00
N	10.60	19.40
O	15.90	29.20
P	23.90	43.80
Q	35.80	65.60

HER

HDSP-750x		
IV Bin Category	**Min.**	**Max.**
B	0.342	0.630
C	0.516	0.946
D	0.774	1.418
E	1.160	2.127
F	1.740	3.190
G	2.610	4.785
H	3.915	7.177

Orange

HDSP-A40X		
IV Bin Category	**Min.**	**Max.**
A	0.284	0.433
B	0.354	0.541
C	0.443	0.677
D	0.554	0.846
E	0.692	1.057
F	0.856	1.322
G	1.082	1.652
H	1.352	2.066
I	1.692	2.581
J	2.114	3.227
K	2.641	4.034
L	3.300	5.042
M	4.127	6.303
N	5.157	7.878

Yellow

HDSP-740x		
IV Bin Category	**Min.**	**Max.**
B	0.229	0.387
C	0.317	0.582
D	0.476	0.872
E	0.714	1.311
F	1.073	1.967
G	1.609	2.950
H	2.413	4.425

Green

HDSP-780x		
IV Bin Category	**Min.**	**Max.**
H	0.86	1.58
I	1.29	2.37
J	1.94	3.55
K	2.90	5.33
L	4.37	8.01

Color Categories

Color	Bin	Dominant Wavelength (nm)	
		Min.	Max.
Yellow	1	581.50	585.00
	3	584.00	587.50
	2	586.50	590.00
	4	589.00	592.50
Green	2	573.00	577.00
	3	570.00	574.00
	4	567.00	571.00
	5	564.00	568.00

Note:
All categories are established for classification of products. Products may not be available in all categories. Please contact your Agilent representatives for further clarification/information.

Contrast Enhancement

For information on contrast enhancement, please see Application Note 1015.

Soldering/Cleaning

Cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloro-ethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the package of plastic LED parts.

For further information on soldering LEDs, please refer to Application Note 1027.

18.- LM7805

FAIRCHILD
SEMICONDUCTOR®

www.fairchildsemi.com

MC78XX/LM78XX/MC78XXA

3-Terminal 1A Positive Voltage Regulator

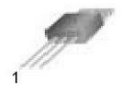
Features

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

Description

The MC78XX/LM78XX/MC78XXA series of three terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

TO-220



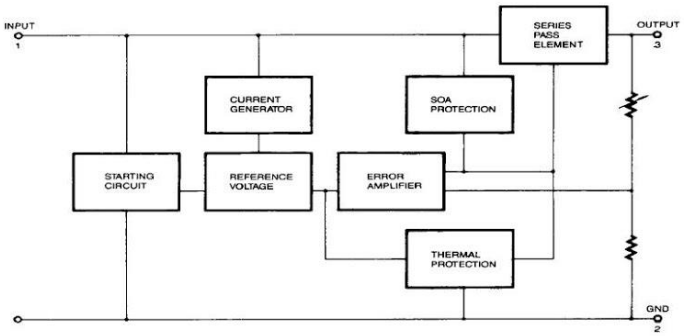
1

D-PAK

1

1. Input 2. GND 3. Output

Internal Block Digram



Rev. 1.0.1

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input Voltage (for V_O = 5V to 18V) (for V_O = 24V)	V_I V_I	35 40	V V
Thermal Resistance Junction-Cases (TO-220)	$R_{\theta JC}$	5	°C/W
Thermal Resistance Junction-Air (TO-220)	$R_{\theta JA}$	65	°C/W
Operating Temperature Range	T_{OPR}	0 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Electrical Characteristics (MC7805/LM7805)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I = 10V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7805/LM7805			Unit
				Min.	Typ.	Max.	
Output Voltage	V_O	T_J =+25 °C		4.8	5.0	5.2	V
		5.0mA ≤ I_O ≤ 1.0A, P_O ≤ 15W V_I = 7V to 20V		4.75	5.0	5.25	
Line Regulation (Note1)	Regline	T_J=+25 °C	V_O = 7V to 25V	-	4.0	100	mV
			V_I = 8V to 12V	-	1.6	50	
Load Regulation (Note1)	Regload	T_J=+25 °C	I_O = 5.0mA to1.5A	-	9	100	mV
			I_O =250mA to 750mA	-	4	50	
Quiescent Current	I_Q	T_J =+25 °C		-	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A		-	0.03	0.5	mA
		V_I= 7V to 25V		-	0.3	1.3	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O= 5mA		-	-0.8	-	mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A=+25 °C		-	42	-	μV/Vo
Ripple Rejection	RR	f = 120Hz V_O = 8V to 18V		62	73	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25 °C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	15	-	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A =+25 °C		-	230	-	mA
Peak Current	I_{PK}	T_J =+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7805A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O =1A, V_I = 10V, C_I=0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Output Voltage	V_O	T_J =+25 °C		4.9	5	5.1	V
		I_O = 5mA to 1A, P_O ≤ 15W V_I = 7.5V to 20V		4.8	5	5.2	
Line Regulation (Note1)	Regline	V_I = 7.5V to 25V I_O = 500mA		-	5	50	mV
		V_I = 8V to 12V		-	3	50	
		T_J =+25 °C	V_I= 7.3V to 20V	-	5	50	
			V_I= 8V to 12V	-	1.5	25	
Load Regulation (Note1)	Regload	T_J =+25 °C I_O = 5mA to 1.5A		-	9	100	mV
		I_O = 5mA to 1A		-	9	100	
		I_O = 250mA to 750mA		-	4	50	
Quiescent Current	I_Q	T_J =+25 °C		-	5.0	6	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		-	-	0.5	mA
		V_I = 8 V to 25V, I_O = 500mA		-	-	0.8	
		V_I = 7.5V to 20V, T_J =+25 °C		-	-	0.8	
Output Voltage Drift	$\Delta V/\Delta T$	Io = 5mA		-	-0.8	-	mV/ °C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_A =+25 °C		-	10	-	μV/Vo
Ripple Rejection	RR	f = 120Hz, I_O = 500mA V_I = 8V to 18V		-	68	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25 °C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	17	-	mΩ
Short Circuit Current	I_{SC}	V_I= 35V, T_A =+25 °C		-	250	-	mA
Peak Current	I_{PK}	T_J= +25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Typical Perfomance Characteristics

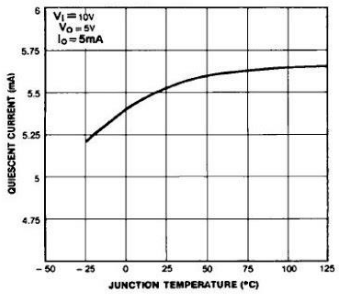


Figure 1. Quiescent Current

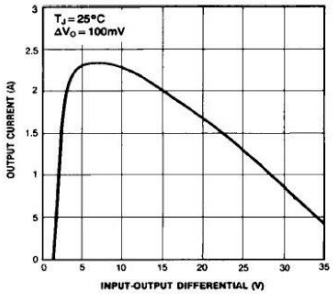


Figure 2. Peak Output Current

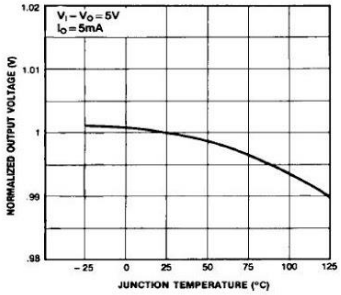


Figure 3. Output Voltage

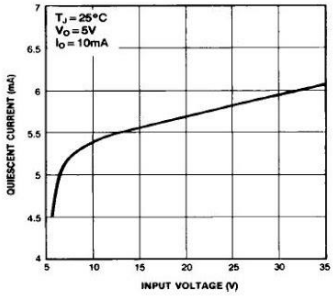


Figure 4. Quiescent Current

Typical Applications

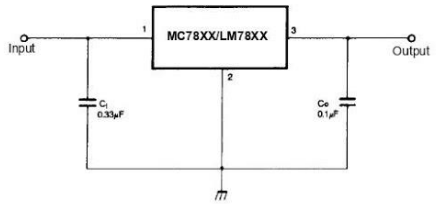


Figure 5. DC Parameters

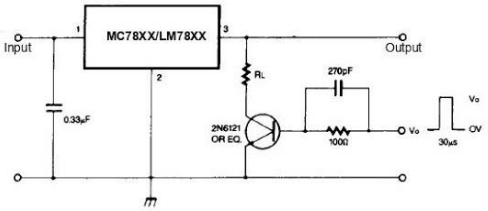


Figure 6. Load Regulation

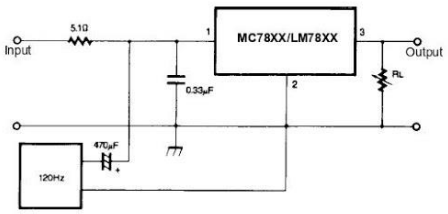


Figure 7. Ripple Rejection

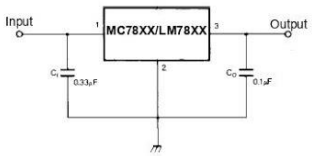
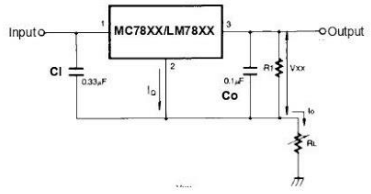


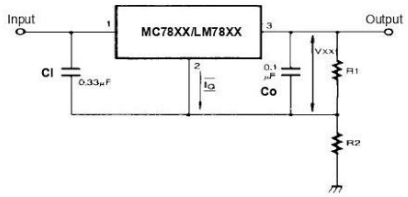
Figure 8. Fixed Output Regulator



$$I_O = \frac{V_{XX}}{R_1} + I_Q$$

Figure 9. Constant Current Regulator

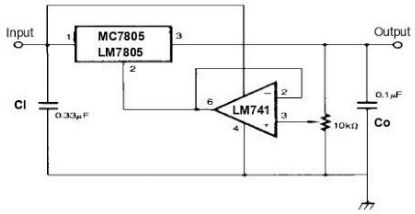
Notes:
(1) To specify an output voltage. substitute voltage value for "XX." A common ground is required between the input and the Output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.
(2) C_I is required if regulator is located an appreciable distance from power Supply filter.
(3) C_O improves stability and transient response.



$$I_{RI} \geq 5I_Q$$

$$V_O = V_{XX}(1+R_2/R_1)+I_QR_2$$

Figure 10. Circuit for Increasing Output Voltage



$$I_{RI} \geq 5\ I_Q$$

$$V_O = V_{XX}(1+R_2/R_1)+I_QR_2$$

Figure 11. Adjustable Output Regulator (7 to 30V)

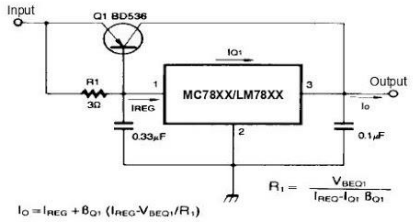


Figure 12. High Current Voltage Regulator

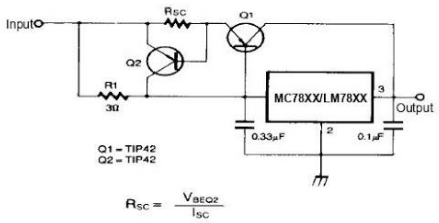


Figure 13. High Output Current with Short Circuit Protection

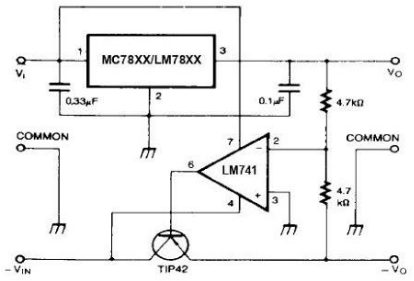


Figure 14. Tracking Voltage Regulator

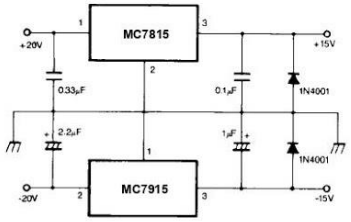


Figure 15. Split Power Supply (±15V-1A)

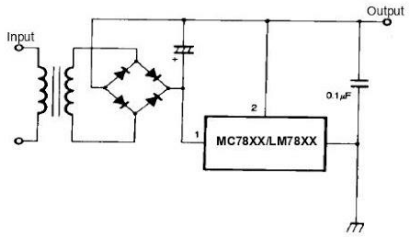


Figure 16. Negative Output Voltage Circuit

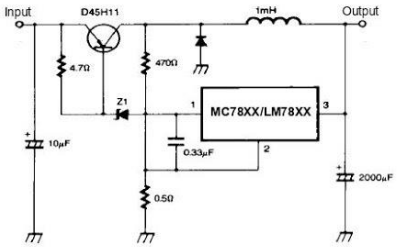
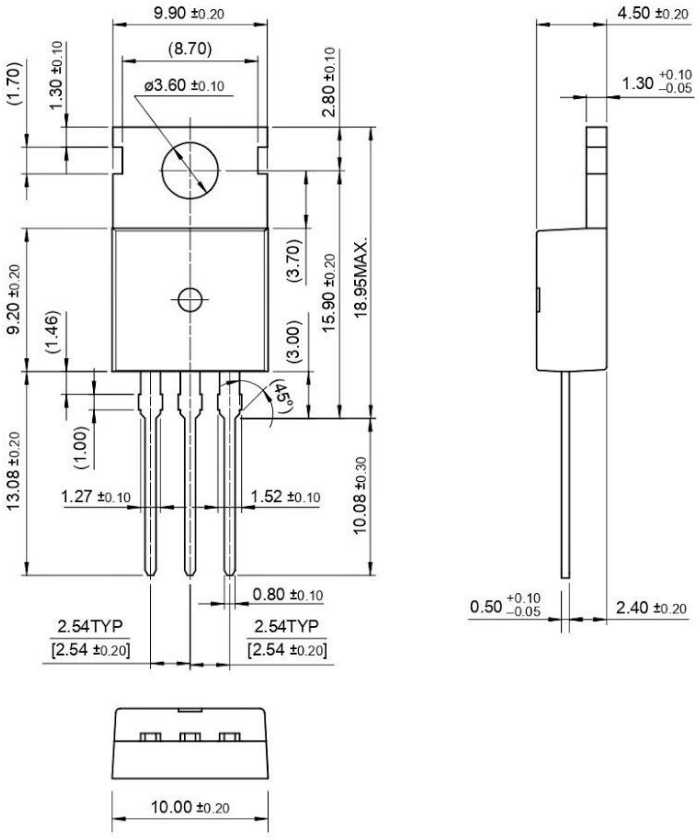


Figure 17. Switching Regulator

Mechanical Dimensions

Package

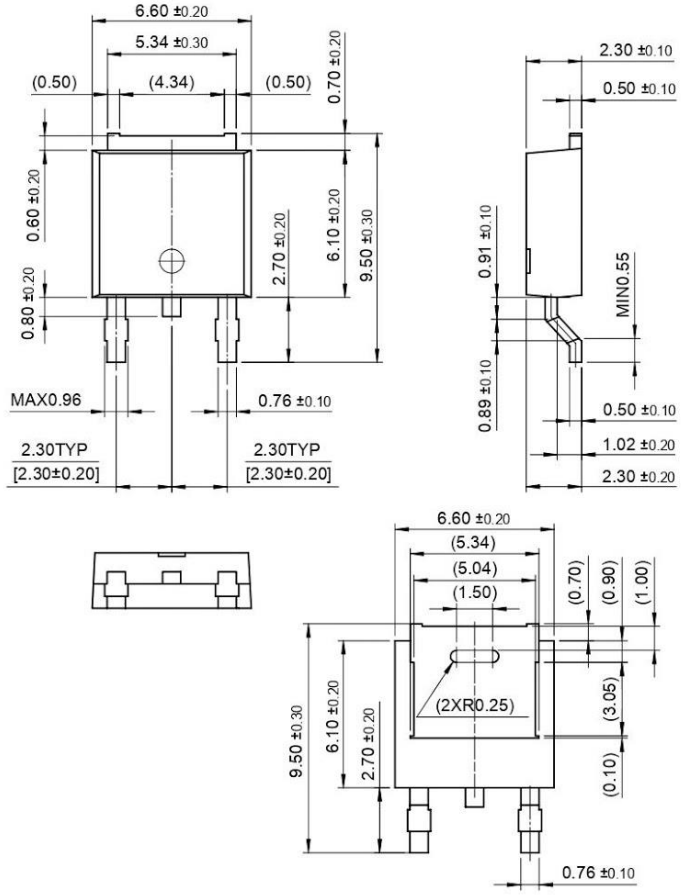
TO-220



Mechancal Dimensions (Continued)

Package

D-PAK



Ordering Information

Product Number	Output Voltage Tolerance	Package	Operating Temperature
LM7805CT	±4%	TO-220	0 ~ + 125°C

Product Number	Output Voltage Tolerance	Package	Operating Temperature
MC7805CT	±4%	TO-220	0 ~ + 125°C
MC7806CT			
MC7808CT			
MC7809CT			
MC7810CT			
MC7812CT			
MC7815CT			
MC7818CT			
MC7824CT			
MC7805CDT		D-PAK	
MC7806CDT			
MC7808CDT			
MC7809CDT			
MC7810CDT			
MC7812CDT			
MC7805ACT	±2%	TO-220	
MC7806ACT			
MC7808ACT			
MC7809ACT			
MC7810ACT			
MC7812ACT			
MC7815ACT			
MC7818ACT			
MC7824ACT			