Sistema de transmisión OOK basado en lámparas LED de iluminación

TRABAJO FIN DE GRADO

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Titulación: Grado en Ingeniería Electrónica Industrial y Automática

Contenido

CAPÍTULO 1

1. Introducción

En el presente texto se aborda el Trabajo Fin de Grado (TFG) correspondiente al Grado en Ingeniería Electrónica Industrial y Automática de la Universidad de La Laguna. A lo largo del documento se desarrolla el diseño e implementación de un dispositivo transmisor y receptor que transmite señales digitales utilizando como medio de transmisión la luz visible. Se trata de un sistema que se enmarca en el campo de las Comunicaciones por Luz Visible o VLC (Visible Light Communication), en donde se transmite información a través de radiación electromagnética de longitud de onda entre 375 – 780 nm (espectro visible por el ojo humano).

Históricamente, la transmisión mediante señales ópticas ha sido ampliamente utilizada, inicialmente con mensajes simples como las reflexiones de la luz en superficies brillantes, hasta mensajes más complejos, como actualmente se hace a través de la fibra óptica, pasando por faros, señales entre barcos, semáforos, etc. En definitiva, estos sistemas están presentes en la vida diaria de gran parte de la población. Una de las ventajas de este tipo de tecnología radica en que es posible aprovechar elementos que se encuentran bastante extendidos (faros de vehículos, semáforos, lámparas de interior, televisores, carteles luminosos comerciales...) y utilizarlos para transmitir mensajes a unidades móviles (telefonía, vehículos...) [1].

En el mundo actualmente, gran parte de la energía eléctrica producida se emplea en la iluminación. El gran avance de las comunicaciones por luz visible se debe a la aparición de los primeros diodos LED (Light Emitting Diode) de bajo consumo y con una buena capacidad de conmutación, de hecho, hoy en día están presentes en semáforos, alumbrado público, carteles publicitarios, luces de vehículos, etc. En general, el esfuerzo de los investigadores se ha centrado principalmente en conseguir que las lámparas o bombillas LED, además de cumplir su función principal de iluminar, también permitan transmitir información. Con el paso de los años, el interés por la tecnología VLC se ha intensificado, de hecho, los sistemas que se diseñan y proponen permiten, cada vez, alcanzar mayores velocidades de transmisión llegando al orden de Gigabits por segundo [1].

1.1. Objetivo

Este trabajo fin de grado consiste en el desarrollo de un sistema de transmisión digital que utiliza como medio de transmisión la luz visible, caracterizado por emplear un esquema de modulación OOK (On-Off Keying) y las actuales lámparas LED de iluminación comerciales como dispositivo emisor. Además de diseñar e implementar el modulador y demodulador OOK, se aborda el diseño e implementación del receptor óptico que constituye la etapa de entrada del sistema receptor. En la Figura 1.1 se puede observar el diagrama de bloques del sistema de comunicación desarrollado, en el que se pueden distinguir, como en cualquier sistema de comunicación, el transmisor, el canal o medio de transmisión y el receptor.

En el sistema desarrollado, el transmisor está compuesto por un codificador tipo Manchester o bifase-L, el modulador en banda base y el emisor óptico, compuesto por el circuito excitador y la fuente óptica. La función del codificador Manchester es la de realizar una aleatorización de los datos suministrados por la fuente binaria con la finalidad de evitar la aparición de largas cadenas de un mismo símbolo binario. La función del modulador en banda base reside en transformar los bits que se desean transmitir en señales con un formato adecuado para ser transmitidas por el canal de comunicaciones, en este caso siguiendo un esquema de modulación OOK. Por último, la del emisor óptico, basado en la utilización de una lámpara LED como fuente óptica, es la de llevar a cabo la conversión electro-óptica necesaria para adaptar la señal a transmitir a las características del canal visible. En lo que se refiere al receptor, éste está formado por el receptor óptico, que incluye el sensor de radiación visible y una etapa de amplificación/acondicionamiento de señal, el demodulador en banda base y el decodificador Manchester. Como sensor de radiación, encargado de llevar a cabo la conversión óptico- eléctrica, se ha empleado el fotodiodo S3071 del fabricante Hamamatsu. La función del demodulador en banda base es realizar el proceso inverso del modulador, es decir, a partir de la señal OOK resultante de la conversión óptico-eléctrica realizada por el receptor óptico, obtener los bits o secuencia de bits que en formato Manchester han sido recibidos desde el sistema transmisor. Por último, el decodificador Manchester tiene como misión recuperar los bits de información transmitidos a partir de la secuencia de datos binarios proporcionados por el demodulador. Por último, indicar que la sincronización entre el transmisor y el receptor está basada en el protocolo de comunicación serial asíncrono RS-232, la programación de los bloques de transmisión y recepción se ha realizado en VHDL (Very High-Speed Integrated Circuit Hardware Description Language), con el software ISE Design Suite 14.7, y la implementación se ha llevado a cabo en la placa de desarrollo Nexys A7 Artix.

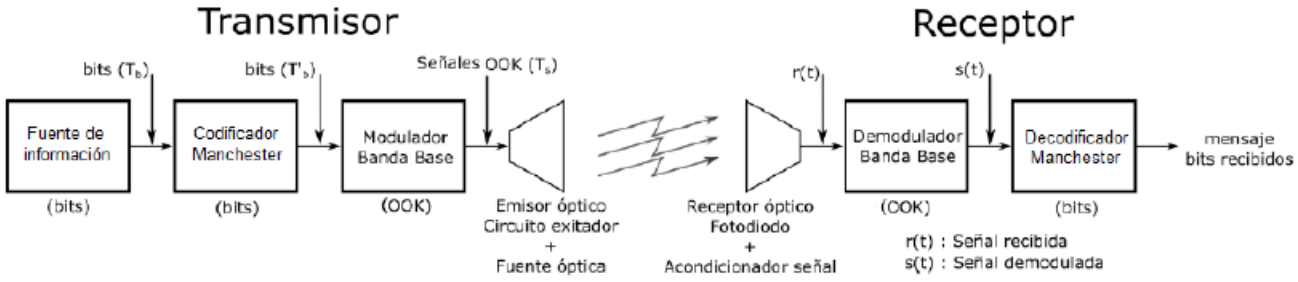

Figura 1.1: Sistema óptico de transmisión OOK.

1.2. Abstract

A field-programmable gate array is used as the controller of a system that is going to be in charge of sending data through visible light. The transmission will be carried out with an LED lamp and the data will be modulated in On Off Keying, encoded in Manchester and finally a packet will be formed using the RS-232 protocol. For all this, a transmission module has been designed together with the relevant electronic circuits. On the other hand, the transmitted data will be received by a photodiode and whose signal will be appropriately conditioned so that it can be detected by the reception stage that will be in charge of decoding the transmitted signal and obtaining the original signal.

For the transmission stage, it was necessary to design an electronic circuit that essentially consists of a buffer to be able to raise the 3.3V voltage from the Nexys development board to 5V, which is the supply voltage of the LED lamp.

On the other hand, for the reception circuit, a TL082 operating amplifier is used in negative feedback that allows us to condition the signal from the sensor, being a photodiode in our case, to the reception pin that of the receiver module for the decoding of the signal.

1.3. Estructura de la Memoria

El presente documento se desarrolla en los siguientes capítulos en los cuales se recogen las dificultades y soluciones encontradas y aportadas para cumplir con el objetivo propuesto.

- Capítulo 1. Se propone el objetivo a conseguir y un breve resumen de la estrategia seguida para lograrlo.
- Capítulo 2. Fundamentos teóricos. Conceptos teóricos que se han tenido en cuenta a la hora de desarrollar el presente trabajo.
- Capítulo 3. Descripción del sistema. Se realiza un extenso recorrido a través del hardware y software empleados en la transmisión y recepción de los datos, así como su tratamiento.
- Capítulo 4. Resultados. Se exponen los resultados obtenidos.
- Capítulo 5. Presupuesto. Coste económico para la compra de materiales y mano de obra.
- Capítulo 6. A vista de los resultados se obtienen las conclusiones del Trabajo Fin de Grado.
- Capítulo 7. Bibliografía.
- Capítulo 8. Anexos.

CAPÍTULO 2

2. Fundamentos Teóricos

En este capítulo se abordan algunos de los aspectos teóricos implicados en el desarrollo del presente trabajo. En concreto, se describen conceptos relacionados con los sistemas de comunicaciones por luz visible (VLC), el estándar IEEE 802.15.7, la modulación OOK, la codificación Manchester, el estándar RS-232 y los receptores ópticos.

2.1. Sistema de comunicación mediante luz visible (VLC)

Los sistemas de comunicación por luz visible o sistemas VLC se basan en una tecnología que permite la transmisión de información en el espectro visible mediante la modulación de la intensidad de la luz transmitida (Figura 2.1). El gran desarrollo de los diodos LED han favorecido que esta tecnología haya sido investigada en mayor profundidad en las últimas décadas.

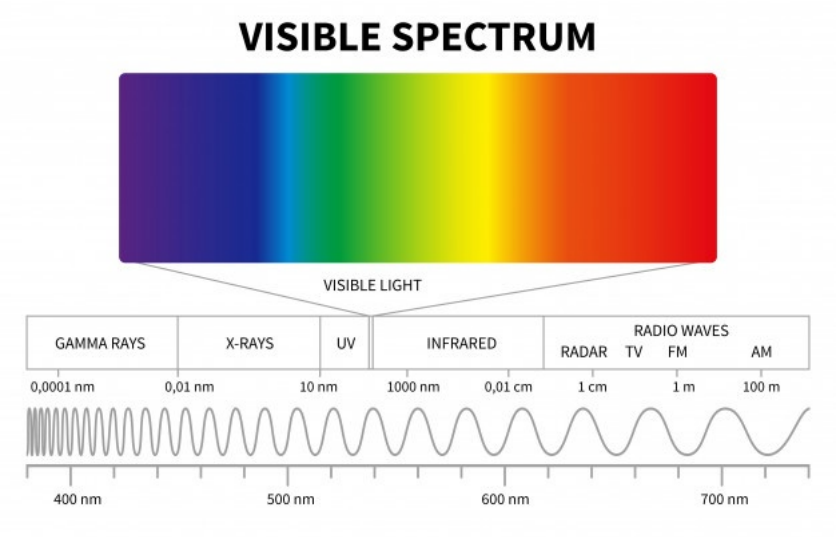

Figura 2.1: Espectro de frecuencias visible por el ojo humano.

Otro de los objetivos de los sistemas VLC, además de la de transmitir información, es que las lámparas LED sigan realizando su función principal de iluminar. En este sentido, los principales problemas que se pueden encontrar son: el parpadeo (flicker) y el control de la atenuación o regulación de la intensidad lumínica de la lámpara (dimming). Las altas frecuencias utilizadas durante la transmisión permiten que el usuario no perciba el parpadeo del LED y, por lo tanto, no se vea afectada su función principal, la de iluminar. Al tratarse de un sistema que utiliza la luz para transmitir información, la velocidad puede llegar a ser bastante alta, sin embargo, existen otras restricciones tecnológicas que limitan la máxima velocidad alcanzable, como puede ser la electrónica del receptor, el medio de transmisión y la distancia [2].

En este trabajo, se utiliza una tasa de bit de **100 kbps**, ya que se ha comprobado que la lámpara LED utilizada y el receptor diseñado no son capaces de responder a frecuencias superiores a 200 kHz. Además, a la hora de diseñar un sistema de transmisión de información basado en VLC, se puede optar por realizar una transmisión basada en un enlace con línea de visión directa (LOS, Line Of Sight) o en un enlace en difusión. Por su simplicidad, en este trabajo se ha optado por implementar un sistema VLC del tipo LOS, es decir, con visión directa entre el emisor y el receptor.

La Figura 2.2 muestra un ejemplo práctico del emisor óptico (circuito excitador y fuente óptica) de un sistema de comunicación VLC que utiliza como fuente óptica un diodo LED, mientras que en la Figura 2.3 se puede observar un ejemplo de la relación entre el flujo luminoso y la intensidad que circula por el diodo LED.

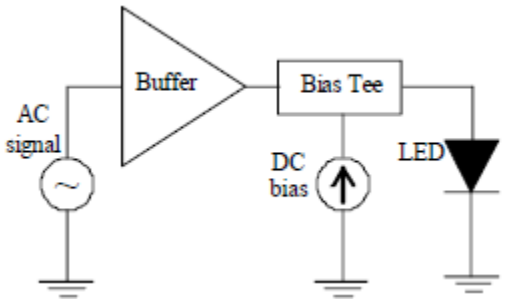

Figura 2.2: Circuito controlador típico para modular la salida óptica de un LED.

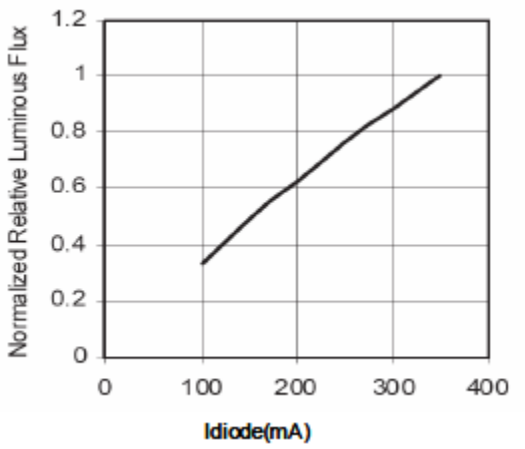

Figura 2.3: Flujo luminoso relativo en función de la corriente.

Las figuras 2.2 y 2.3 muestran un ejemplo práctico de sistemas de comunicaciones VLC con LED. En la figura 2.2 se muestra un circuito típico para obtener datos de iluminación y transmisión de la lámpara LED, mientras que en la figura 2.3 podemos observar un ejemplo de la forma de la curva entre flujo luminoso y la intensidad que circula por el diodo

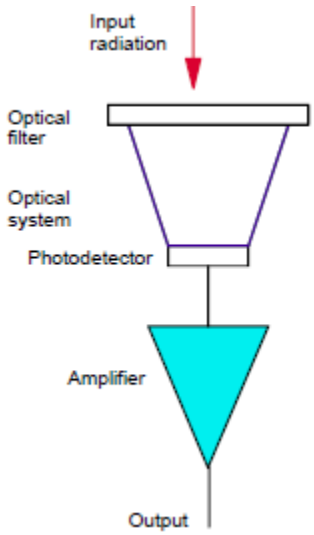

Figura 2.4: Esquema generalde un receptor óptico.

En la Figura 2.4 se visualiza el esquema general del receptor óptico (fotodiodo y acondicionamiento de señal), en donde el fotodetector se encarga de realizar la conversión fotoeléctrica y la etapa de amplificación de la señal eléctrica proporcionada por el fotodetector.

2.2. Estándar IEEE 802.15.7

El uso del canal visible no sólo ofrece un amplio ancho de banda sin regular y una alternativa a las bandas de radiofrecuencia ya muy saturadas, sino que además permite usar las infraestructuras ya existentes en todas las viviendas u oficinas. Este hecho suscitó un gran interés por parte de las universidades, empresas y organizaciones de todo el mundo en orientar parte de sus esfuerzos en el estudio y desarrollo de este tipo de sistemas. Una vez reconocido el potencial que podía tener la tecnología VLC, en el año 2011 se publica el estándar IEEE 802.15.7, el cual pretendía regular, mediante la definición de las especificaciones de las capas MAC y PHY, el uso de la tecnología VLC en redes de área personal inalámbricas o WPAN [3]. Este estándar ha sido sometido a diferentes actualizaciones por el grupo de trabajo encargado de dicho estándar mediante diferentes acciones en colaboración con otros grupos de trabajo, asociaciones, instituciones y universidades.

En el documento se preocupan por varios retos que deben superar este tipo de comunicaciones. Uno de ellos es el de llegar a un acuerdo sobre que es el parpadeo y como mitigarlo. Citando directamente del estándar, se define el parpadeo como a la fluctuación del brillo de la luz. Para evitar estos cambios se define un tiempo máximo de parpadeo o MFTP (Maximum Flickering Time Period), cuyo efecto no se manifiesta a partir de frecuencias superiores a 200 Hz. Otros de los puntos importantes que se tratan es la diferencia existente entre la luz percibida y la medida debida a la dilatación de la pupila (ecuación 1), cuya relación se representa gráficamente en la Figura 2.5.

$$LuzPercibida = 100 \cdot \sqrt{\frac{LuzMedida}{100}} \tag{1}$$

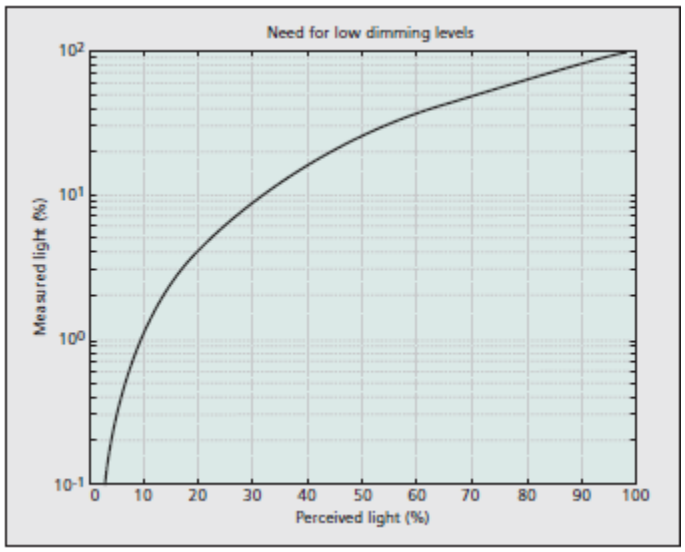

Figura 2.5: Relación entre la luz medida y percibida por el ojo humano.

Respecto a los esquemas de modulación y codificación, el estándar IEEE 802.15.7 ha optado por tres posibles implementaciones del nivel PHY, soportando topologías tanto peer- to-peer como en estrella, con tasas de transmisión desde 11,67 kbps hasta 96 Mbps tanto en interiores como en exteriores. Las velocidades más bajas están asociadas a la utilización de esquemas VOOK (Variable OOK) que, ofrece un control de luminosidad ajustable o dimming a la vez que evita los problemas de parpadeo o flickering mediante el uso de una codificación tipo Machester o codificaciones de bloque. Esta técnica se basa en utilizar una modulación OOK con un ciclo de trabajo muy reducido y añadir a continuación pulsos hasta lograr el nivel de dimming deseado. La segunda implementación, asociada a la consecución de las velocidades de transmisión medias, se basa en el empleo de un esquema de modulación VPPM (Variable PPM), el cual consiste en combinar una modulación 2-PPM con técnicas PWM (Pulse Width Modulation). La tercera propuesta del estándar y más novedosa, es la conocida como CSK (Color Shift keying), la cual respalda la consecución de tasas hasta 96 Mbps, y consiste básicamente en crear una constelación dividiendo el espectro de color, definido por la norma CIE1931, en siete bandas donde se especifican las longitudes de onda utilizadas para transmitir símbolos de tres bits.

Como se ha comentado con anterioridad, en este trabajo se aborda el desarrollo de un sistema de comunicación VLC, caracterizado por emplear un esquema de modulación OOK y una lámpara LED de iluminación como dispositivo emisor. Se trata de un sistema basado en uno de los modos de operación que el estándar IEEE 802.15.7 propone en una de sus tres posibles implementaciones del nivel PHY (Figura 2.6), en el que, además de hacer uso de la modulación OOK, se propone la utilización de codificación Manchester para aleatorizar los

datos suministrados por la fuente binaria para evitar la aparición de largas cadenas de un mismo símbolo binario, lo que supondría por momentos el apagado de la lámpara LED de iluminación.

Modulation	RLL code	Optical clock rate	FEC		Data rate
			Outer code (RS)	Inner code (CC)	
OOK	Manchester	200 kHz	(15,7)	1/4	11.67 kb/s
			(15,11)	1/3	24.44 kb/s
			(15,11)	2/3	48.89 kb/s
			(15,11)	None	73.3 kb/s
			None	None	100 kb/s

Figura 2.6: Modos de operación

2.3. Modulación OOK (On-Off Keying)

En el diseño del sistema VLC desarrollado en este trabajo se utiliza el esquema de modulación en amplitud en banda base OOK (On-Off Keying), que en español se traduciría como modulación encendido-apagado. El término "keying" viene del código morse, donde la transmisión se activaba o desactivaba a mano, y al interruptor que se utilizaba para ello se denominaba "key". La modulación OOK en banda base consiste en encender o apagar la lámpara LED dependiendo de si el dato o el bit a transmitir es un 1 o un 0 lógico, es decir al encendido y apagado se le asocia una forma de pulso determinada que a su vez corresponde a cada uno de los dos dígitos binarios posibles. En la Figura 2.7 se muestra un ejemplo de modulación OOK, donde al 1 lógico se le asocia la presencia de un pulso de duración el tiempo de bit (encendido) y al 0 lógico la ausencia de dicho pulso (apagado). Como se puede observar, en este tipo de modulación OOK con pulsos del tipo NRZ (Non Return to Zero), el tiempo de bit es similar al tiempo de símbolo.

Figura 2.7: Esquema modulación OOK.

2.4. Codificación Manchester

La codificación Manchester o bifase-L, se basa en emplear formas de pulso para el 1 y el 0 lógico en el que a la mitad del tiempo de bit se produce una transición entre los dos posibles niveles de señal. En la Figura 2.8 se muestra un ejemplo de codificación donde al 1 lógico se le asocia una transición desde el nivel de señal alto al bajo a la mitad del bit, y al 0 lógico, una transición de nivel de bajo al alto.

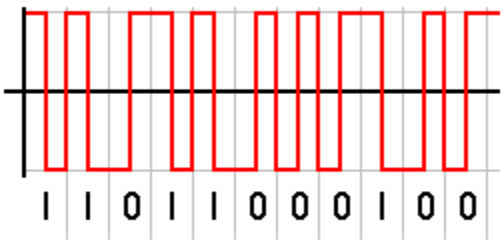

Figura 2.8: Ejemplo de codificación Manchester.

La codificación Manchester es una codificación de línea que posee características intrínsecas de reloj, lo que permitiría realizar una sincronización de símbolo o de bit con facilidad. Sin embargo, en este trabajo se emplea dicha codificación, también propuesta por el estándar IEEE 802.15.7, como código de aleatorización de los datos suministrados por la fuente binaria con la finalidad de evitar la aparición de largas cadenas de un mismo símbolo binario. La principal desventaja de este tipo de codificación es que demanda del doble de ancho de banda que requiere la modulación en banda base o codificación OOK. Desde un punto de vista práctico, la Tabla 2.1 muestra cómo realizar la codificación Manchester a partir de los datos procedentes de un esquema de modulación OOK en banda base.

Valor lógico	Código Manchester
0	01
1	10

Tabla 2.1: Codificación Manchester.

2.5. Protocolo RS-232

El protocolo RS-232 es un protocolo de comunicación serial asíncrono que surge en el año 1969 orientado a realizar comunicaciones punto a punto a distancias cortas (Figura 2.9).

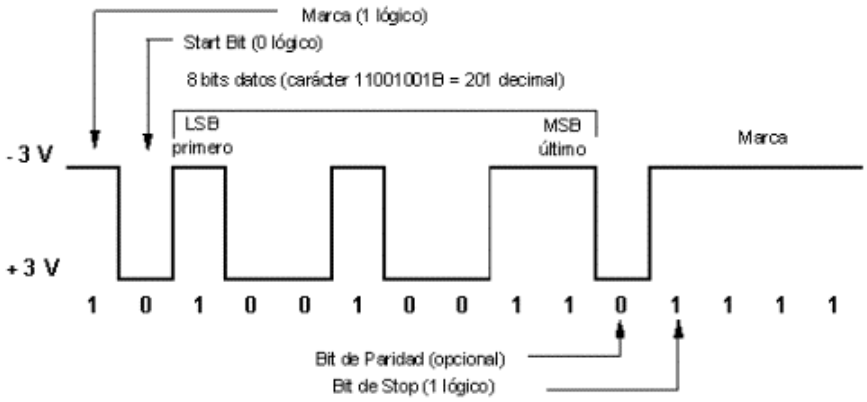

Figura 2.9: Protocolo RS-232.

En este protocolo, a cada conjunto de datos de 8 bits se le añade un bit de inicio (un cero) al principio de la trama, un bit de paridad que es opcional y un bit en alto de stop. Este protocolo permite realizar una comunicación asíncrona, donde el receptor puede detectar el comienzo del mensaje o información mediante la detección de un cambio de 1 a 0 en la recepción de los datos (bit de inicio). Una vez transmitido los 8 bits de datos y el bit de paridad, la señal se queda en alta (bit de stop), el receptor deberá permanecer en espera hasta que se vuelva a producir una transición de nivel alto a bajo, lo que indicaría la recepción del bit de inicio de un nuevo mensaje.

2.6. Receptores ópticos

Un receptor óptico básico consta de un dispositivo sensor de radiación y una etapa adicional de amplificación o acondicionamiento de señal. El dispositivo sensor o fotodetector puede ser del tipo fotoconductivo o fotovoltaico y se encarga de realizar la conversión de potencia luminosa a corriente eléctrica o tensión. En este trabajo se ha empleado como dispositivo sensor o fotodetector un fotodiodo actuando en modo fotoconductivo. Los fotodiodos son un tipo de diodos que, polarizados en inversa, convierten la luz que incide sobre ellos en corriente eléctrica (Figura 2.10).

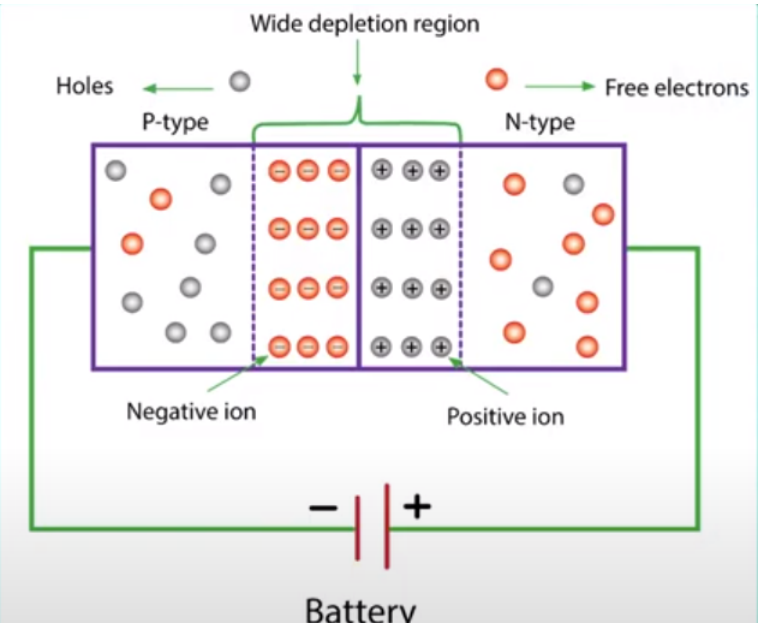

Figura 2.10: Unión P-N polarizada en inversa

Si el haz de luz incidente tiene la suficiente energía, los electrones que llenaban la capa de valencia promocionarán a la capa de conducción. Como resultado se obtiene un electrón libre y un hueco libre, que se aceleran debido al campo eléctrico, generando así una intensidad de corriente eléctrica a través del dispositivo.

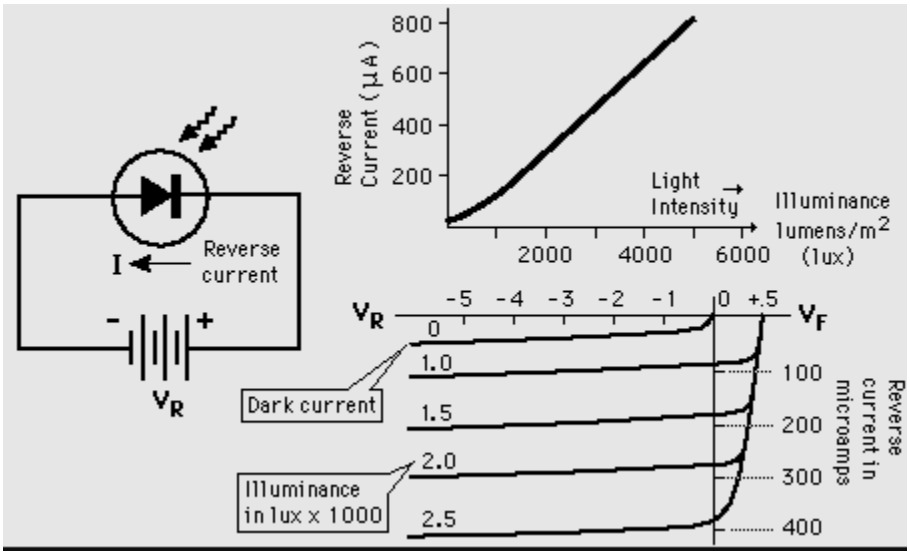

Figura 2.11: Curvas características de un fotodiodo.

En la Figura 2.11 se muestran las curvas características de un fotodiodo junto a la relación entre la intensidad de corriente generada frente a la intensidad lumínica. Esta al ser prácticamente lineal convierte a los fotodiodos en elementos muy útiles en diversas aplicaciones. Respecto a la etapa adicional de amplificación situada tras el fotodetector, las topologías existentes se pueden agrupar de acuerdo con la siguiente clasificación [4]: Amplificadores de alta impedancia: se caracterizan por presentar la mejor sensibilidad e inmunidad frente al ruido. Por el contrario, precisan de una ecualización posterior debido a que integran la señal que reciben y presentan un margen dinámico pequeño. Son útiles cuando el parámetro restrictivo es el ruido ambiente.

Amplificadores de baja impedancia: presentan un elevado ancho de banda y un amplio margen dinámico, si bien su sensibilidad es deficiente. Se aplican en el diseño de transmisores de alta velocidad y entornos de bajo nivel de ruido.

Amplificadores de transimpedancia (Figura 2.12): constituyen una solución de compromiso para mejorar la sensibilidad manteniendo el ancho de banda y el margen dinámico. Usan un bucle de realimentación que puede ser pasivo, activo o una realimentación óptica. Este es la topología empleada en este trabajo para implementar la etapa de amplificación localizada tras el fotodiodo o fotodetector.

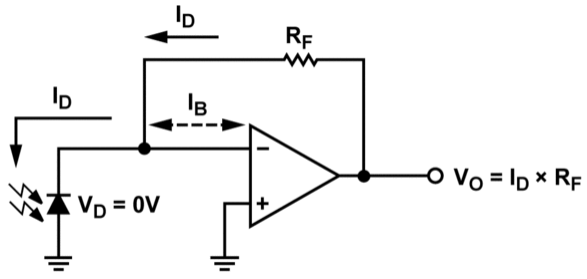

Figura 2.12: Amplificador de transimpedancia.

Amplificadores con circuito resonante: su filosofía de diseño es similar a los sistemas heterodinos convencionales. Se diseñan para mejorar la relación señal-ruido en una banda determinada, para lo que se utiliza un circuito resonante o tanque.

Amplificadores con bobina de entrada: consiste en utilizar una topología como las descritas anteriormente y añadirle a la entrada un elemento inductor (bobina) de tal forma que se aprovechen las características en cuanto a sensibilidad de la etapa amplificadora y se aumente el ancho de banda del sistema. Su utilización se recomienda para sistemas de muy alta velocidad.

Cabe destacar que estas dos últimas topologías presentan elevada inestabilidad y dificultad de sintonización, lo que hace que sean descartadas en muchas aplicaciones.

CAPÍTULO 3

3. Descripción del sistema

En el presente capítulo se desarrollarán los pasos seguidos tanto a nivel de hardware como de software para alcanzar el objetivo propuesto. Se describen los bloques que participan en las diferentes etapas tanto de transmisión como de recepción, así como la electrónica empleada.

En la figura 3.1 se representa el esquema general del sistema empleado. Se empleará la FPGA Nexys A7 Artix-7 la cual cuenta con interruptores que nos permiten elegir la combinación de cuatro bits a transmitir en el mensaje. El bloque transmisor tiene la función de codificar la señal en Manchester, empaquetar los ocho bits según el protocolo RS-232 y modular la señal en OOK. La placa de desarrollo trabaja con niveles de tensión de 0 y 3,3 V mientras que la lámpara LED opera con niveles de 0 a 5 V. Por lo que ha sido necesario diseñar e implementar un circuito electrónico que adapte los niveles de salida de la placa a los de entrada de lámpara.

La luz de la lámpara incide sobre un fotodiodo conectado a un circuito de acondicionamiento de señal que recibe la señal de 11 Bits captada por el fotodiodo. Finalmente, la salida del circuito de recepción se trata en un bloque receptor que se encarga de decodificar la señal y mostrar la señal original emitida.

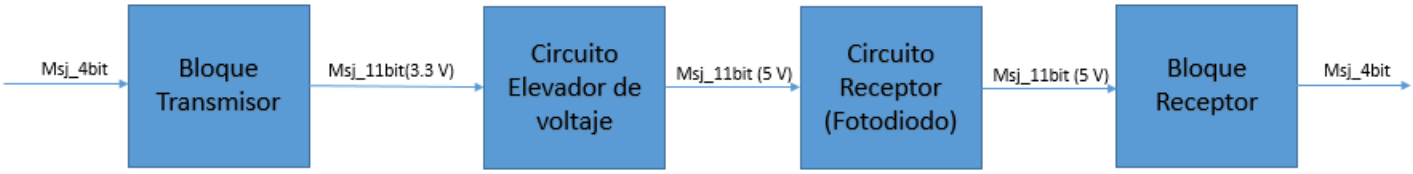

Figura 3.1: Esquema general del sistema.

3.1. Nexys A7 Artix-7 100t FPGA Trainer board

Tanto el módulo de transmisión como el de recepción están gobernados por una Field-Programmable Gate Array, conocida por su siglas en inglés como FPGA. En este trabajo hemos empleado la Nexys A7 Artix-7 100t de la empresa Digilent.

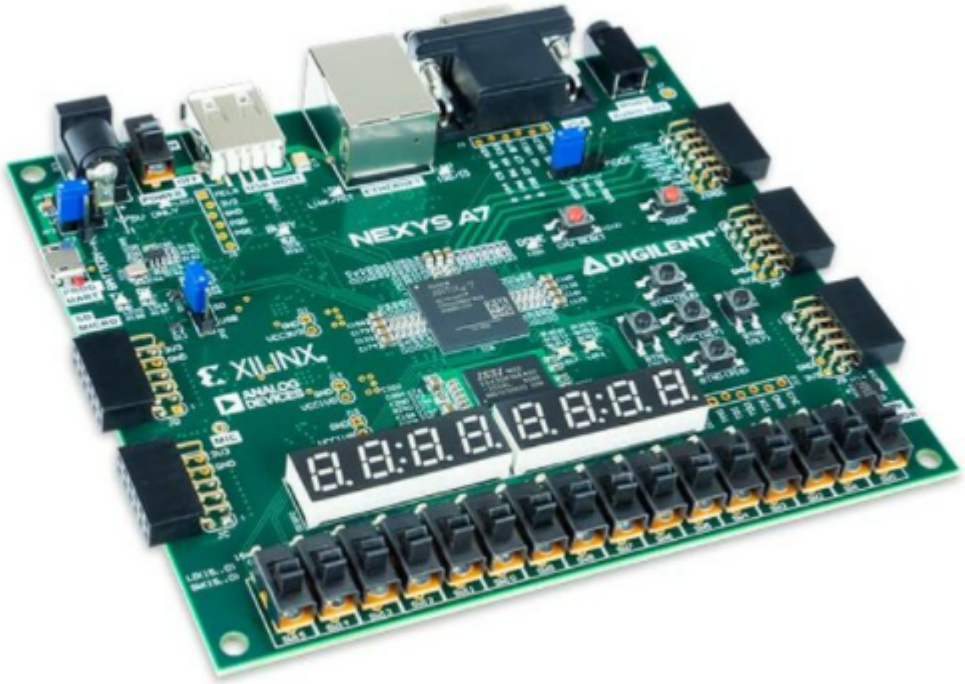

Figura 3.2: Nexys A7 Artiz-7 100t.

	Nexys A7-50T	Nexys A7-100T
FPGA part	XC7A50T-1CSG324C	XC7A100T-1CSG324C
Logic Slices	8,150	15,850
Block RAM (Kbits)	2,700	4,860
DDR2 Memory (MiB)	128	128
Clock Tiles (with PLL)	5	6
DSP Slices	120	240

Figura 3.3: Principales características de las placas Nexys A7.

La Nexys A7 tiene integrado un reloj con una velocidad que excede los 450 MHz. Haciéndola adecuada en relación a las necesidades que se requieren en este trabajo.

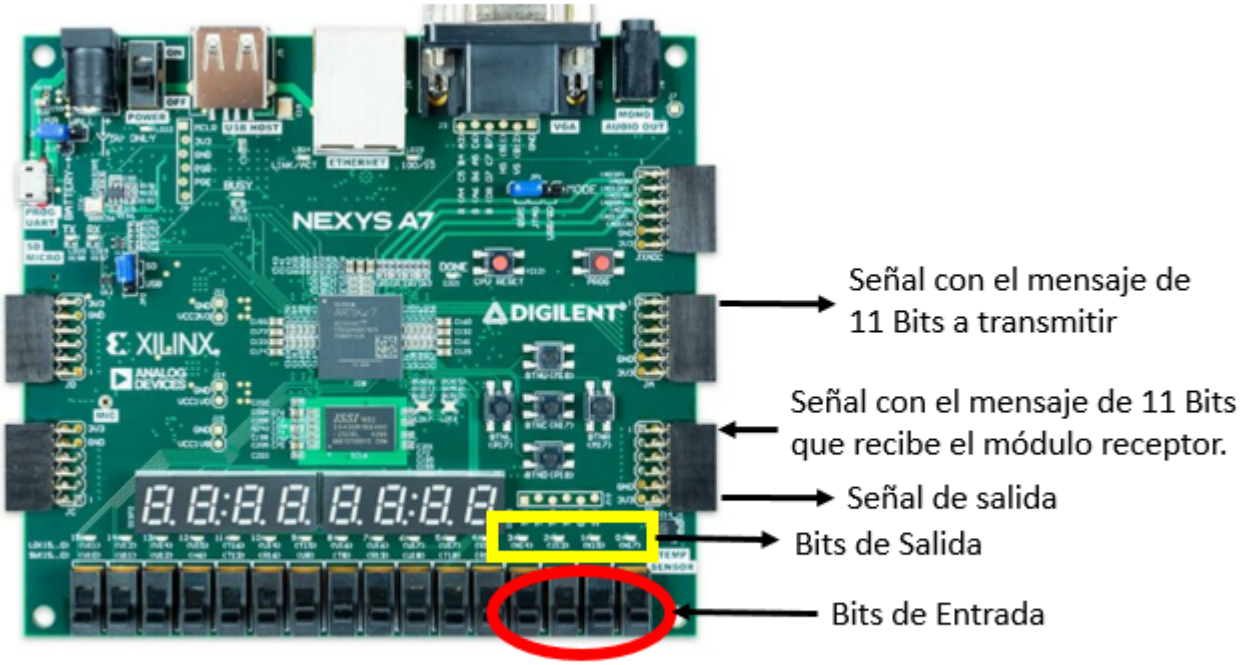

Figura 3.4: Esquemático Entradas / Salidas.

De los 16 interruptores disponibles se emplean cuatro de ellos para enviar el mensaje que queremos transmitir. Internamente se ha programado un módulo transmisor en donde se codifica el mensaje de cuatro bits en ocho bits coincidentes con una codificación Manchester. Seguidamente se añade el bit de inicio '0' y dos bits de stop '1', teniendo finalmente un mensaje de 11 bits cumpliendo con el protocolo RS-232.

Los 11 bits se modulan en OOK y se genera la señal que fisicamente sale del puerto indicado en la Figura 3.4, en donde se conecta la lámpara led encargada de transmitir los datos. La señal emitida por la lámpara es recogida por un circuito de recepción preparado para tal fin, que se emplea de entrada al módulo receptor.

Una vez se desmodule la señal recibida, se dispondrán de dos salidas físicas. Una visual a través de los leds que se sitúan en la parte superior de los interruptores. Y una señal física modulada en OOK apta para ser visualizada en un osciloscopio.

3.2. Bloque transmisor

La Figura 3.5 muestra los distintos bloques que conforman el módulo transmisor, que se encarga de recibir los bits de entrada, codificarlos en Manchester y empaquetarlos cumpliendo los requisitos del protocolo RS-232. El siguien paso es generar una señal modulada en OOK de 11 bits la cual es recibida por la lámpara led.

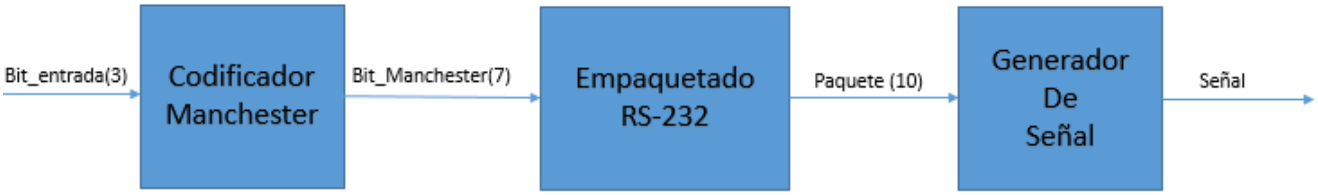

Figura 3.5: Bloques del módulo transmisor.

A continuación se van a detallar los elementos que conforman el bloque transmisor: Codificador Manchester, empaquetado RS-232, Generador de señal. También cabe destacar que la frecuencia del reloj interno de la placa es de 50 MHz. Es por ello que se implementa un bloque que genera las frecuencias necesarias. Para la transmisión de los 11 Bits emplearemos una tasa de bit de 100 kHz.

3.2.1. Bloque codificador Manchester

Recibe el array de cuatro bits introducidos como entrada en los correspondientes interruptores y los codifica en Manchester, siendo la salida los ocho bits resultantes de la codificación. En la tabla 3.1 se muestran las diferentes combinaciones y sus respectivas salidas mientras que en la Figura 3.6 se aprecia el diagrama correspondiente al codificador Manchester.

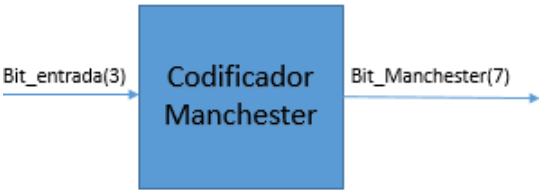

Figura 3.6: Codificador Manchester.

Entrada	Salida
0000	01010101
0001	01010110
0010	01011001
0011	01011010
0100	01100101
0101	01100110
0110	01101001
0111	01101010
1000	10010101
1001	10010110
1010	10011001
1100	10100101
1101	10100110
1110	10101001
1111	10101010

Tabla 3.1: Relación entrada / salida para cuatro bits

3.2.2. Bloque empaquetado RS-232

Este bloque recibe el array de ochos bits procedente de la codificación Manchester y añade el Bit de inicio '0' y los dos bits de stop '1'. El bit de paridad no está implementado en esta aplicación. Obteniendo una salida de 10 bits como se esclarece en la Figura 3.7

Figura 3.7: Paquete según protocolo RS232.

3.2.3. Bloque Generador de Frecuencias

Fundamentalmente vamos a emplear tres frecuencias. Partiendo de la base que la lámpara va a transmitir el mensaje con una frecuencia de bit de 100 kHz obtenemos las siguientes configuraciones, como se muestra en la Figura 3.8.

Figura 3.8: Entradas / salidas bloque generador de frecuencias.

- 100 kHz para el mensaje de 8 bits. (11 Bits con el paquete formado.)
- 50 kHz para el mensaje de 4 bits.
- 3200 kHz aproximadamente para el reloj de recepción que capta el inicio de un mensaje.

Partiendo de la base de que la placa de desarrollo tiene un reloj interno con una frecuencia de 50MHz, se ha diseñado un generador de frecuencias o prescaler que genera las frecuencias indicadas anteriormente a partir del uso de contadores de acuerdo a la ecuacion (2).

$$N\ Cuentas = \frac{Frecuencia\ Nexys}{Frecuencia\ Deseada} \tag{2}$$

El Bloque generador de frecuencias recibe como entradas el reloj interno de la placa Clk_nexys de 50 MHz y una señal de reset que servirá para resetear los valores de las cuentas. Sus salidas son las frecuencias de 100 kHz, 50 kHz y 3200 kHz.

3.2.4. Generador de señal

En la figura 3.9 se representa el bloque que se encarga de la modulacion OOK. Recibe como entrada el mensaje codificado en manchester y empaquetado según el protocolo RS-232, una señal de reloj de 100 kHz y una señal del reset. La salida es el mensaje de 11 bits codificado en OOK con unos niveles de voltaje de 0 a 3,3 V de acuerdo a las especificaciones de la placa de desarrollo y una tasa de bit de 100 kHz.

Figura 3.9: Entradas / salidas Bloque generador de señal.

En las simulaciones, tal y como se muestra en la Figura 3.10 se enseña el correcto funcionamiento del bloque transmisor generando el mensaje deseado y con el tiempo de bit esperado.

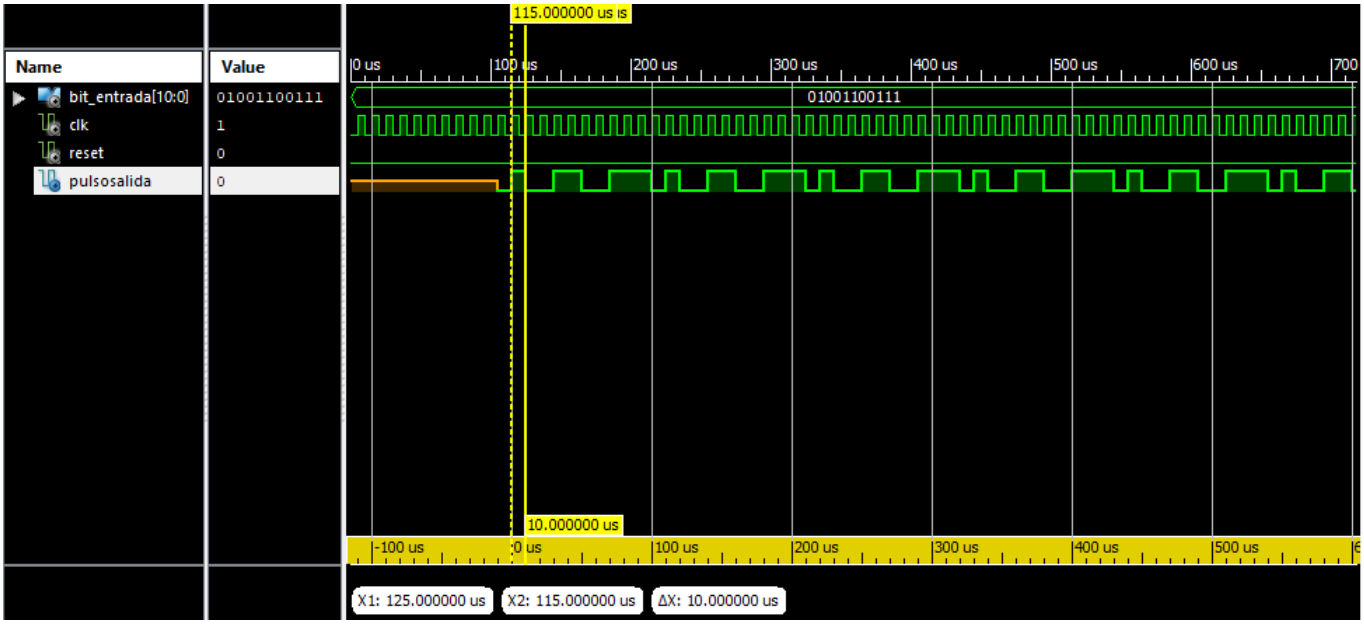

Figura 3.10: Simulación bloque transmisor

3.3. Emisor óptico

Las salidas físicas de la FPGA van de 0 V a 3,3 V mientras que la lámpara LED para su correcto funcionamiento debe recibir los datos con niveles entre 0 y 5 V. Es por ello que ha sido necesario implementar un circuito elevador de voltaje, cuya función es la de adaptar a dichos niveles de voltaje la señal procedente de la placa (0 y 3,3V). La Figura 3.11 muestra el diagrama de bloques para el proceso completo de la transmisión.

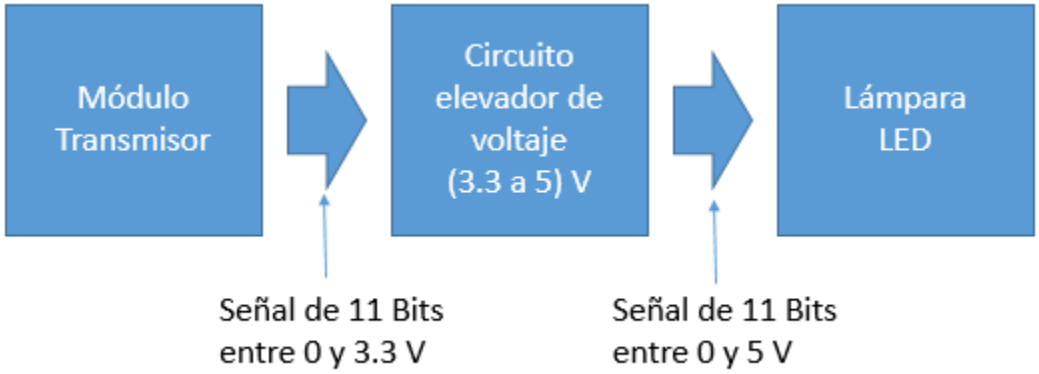

Figura 3.11: Diagrama de bloques de la electrónica de la transmisión.

3.3.1. Circuito elevador de voltaje

La implementación del circuito elevador de voltaje se basa en la utilización del circuito integrado SN74LS07. En la Figura 3.12 se muestra su imagen real.

Figura 3.12: Circuito integrado SN74LS07.

El SN74LS07 nos permite elevar el voltaje de 3,3 V a 5 V que es el requerido por la lámpara led para su correcto funcionamiento.El pin 1 se usa como entrada de datos y el pin 2 como salida. El pin 14 va destinado a la alimentación del búfer correspondiente a 5 V y el pin 7 es la tierra. Para el correcto funcionamiento es necesario añadir una resistencia *pull up* de 1 KΩ en el terminal de salida. En la Figura 3.13 se refleja el esquemático empleado.

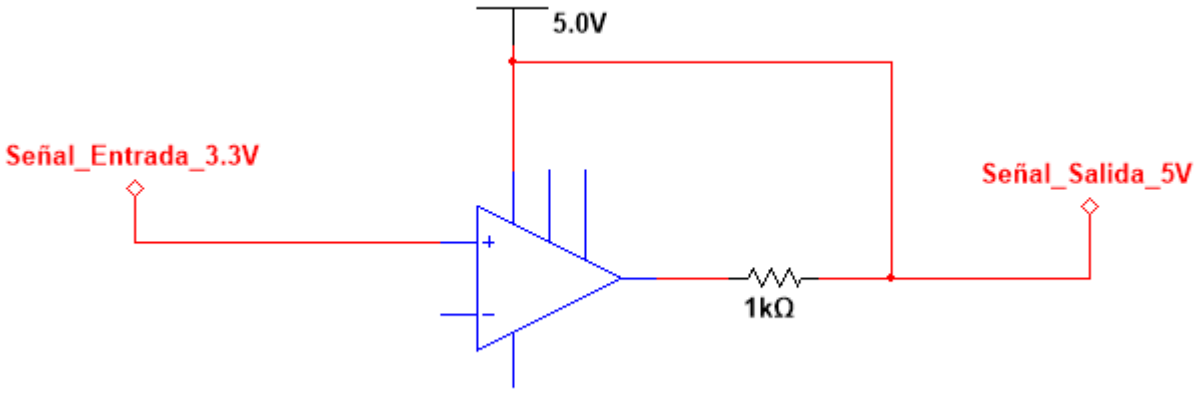

Figura 3.13: Circuito para elevar la tensión de 3.3V a 5V.

3.3.2. Lámpara LED

La Figura 3.13 muestra la forma física de la lámpara led que se emplea en este trabajo. La lámpara emplea lógica negativa y tiene dos conexiones. Una de ellas corresponde a la tensión de alimentación de 5 V y, la otra, es la entrada de los datos que se desean transmitir, que debe poseer niveles de 0 y 5 V.

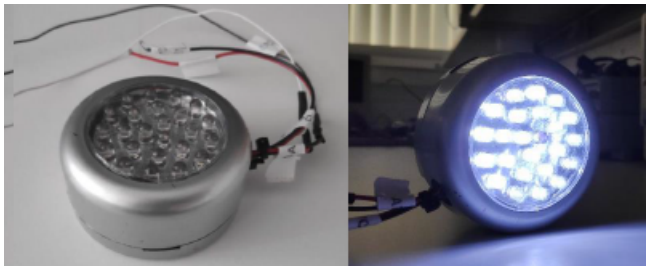

Figura 3.14: Lámpara led

3.4. Receptor óptico

La señal que se transmite a través de la lámpara led con el mensaje procedente del módulo transmisor es captada por un fotodiodo, por lo que la respuesta que nos aporta el sensor en relación a la intensidad lumínica que capta es necesario tratarla a través de un circuito de recepción que consta fundamentalmente de un amplificador operacional tal y como se ilustra en la Figura 3.15 del posterior apartado.

3.4.1. Circuito de recepción

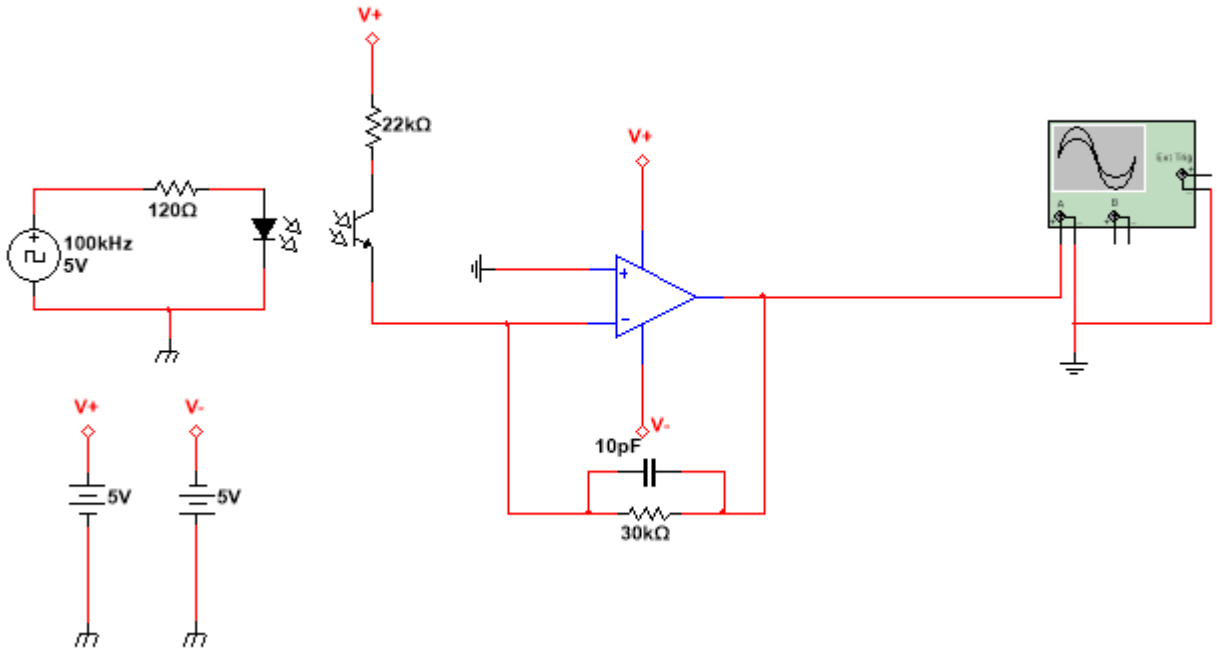

Figura 3.15: Circuito de recepción.

En la Figura 3.15 se muestra el circuito de recepción propuesto en este trabajo. En la parte izquierda de dicha figura se muestra el circuito que simula el comportamiento de la lámpara led, encargada de emitir la luz que porta la información.

En la parte derecha nos encontramos un fototransistor que va a simular el fotodiodo que se implementará fisicamente. El fotodiodo está alimentado a 5 V junto a una resistencia de 22 KΩ. Como fotodetector se emplea el fotodiodo S3071 de Hamamatsu y el operacional TL082 para implementar el amplificador de transimpedancia.

En la Figura 3.16 vemos los resultados obtenidos al simular el circuito.

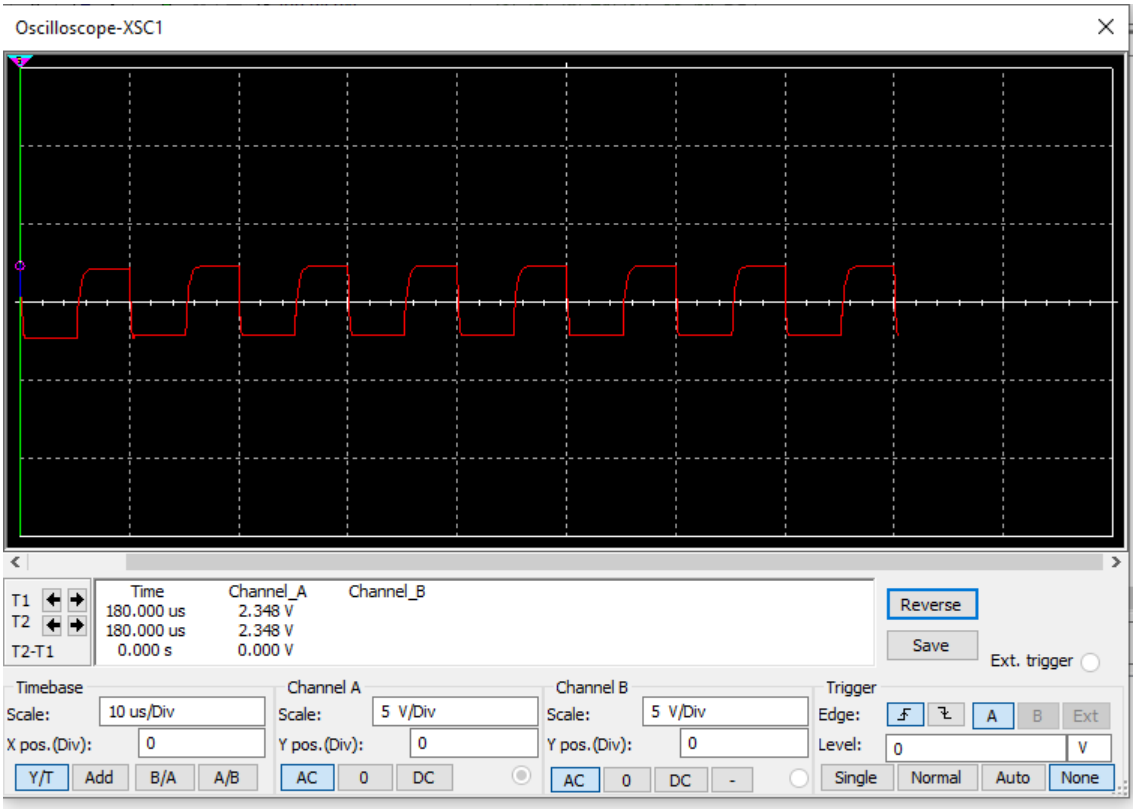

Figura 3.16: Resultado de la simulación del circuito de recepción.

3.5. Bloque Receptor

En La Figura 3.17 se muestran los elementos o bloques que conforman el bloque receptor.

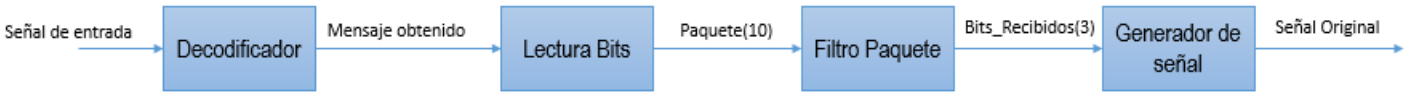

Figura 3.17: Diagrama de Bloques del módulo receptor.

La señal de entrada del bloque receptor es la señal procedente del receptor óptico, es decir, la señal proporcionada por el fotodiodo S3071 y su posterior etapa de amplificación. El bloque decodificador dispone de un reloj 16 veces más rápido que el reloj de transmisión de 200 kHz, esto es de 3200 kHz. La idea fundamental es que el receptor esté constantemente comprobando la señal de datos recibida, de tal manera que cuando se detecta un cambio de '1' a '0', el receptor activa una señal de enable que indica el comienzo de la recepción de un nuevo mensaje.

A partir de ese momento, el receptor baja su frecuencia de operación a 100 kHz para detectar y leer el mensaje recibido. Al paquete de 11 bits se le eliminan los bits de inicio y de parada, se realiza la decodificación Manchester, obteniendo los cuatro bits originales que se originaron en la transmisión. Finalmente, se emplea un generador de señal análogo al utilizado en la etapa de transmisión, pero con un reloj de 50 kHz para poder observar la señal recibida en un osciloscopio.

A continuación se van a describir los diferentes elementos que conforman el bloque receptor, es decir: el decodificador Manchester, lectura de bits, filtro paquete y el generador de señal.

3.5.1. Bloque Decodificador

El decodificador trabaja con un reloj 16 veces más rápido que el de transmisión, en este caso, de 3200 kHz. En la Figura 3.18 se muestra la relación entradas / salidas de dicho bloque.

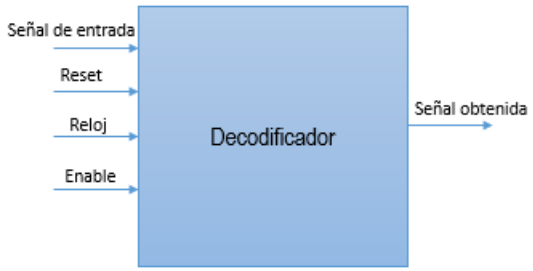

Figura 3.18: Bloque decodificador.

En la Figura 3.19 se muestra el diagrama de estados de la máquina tipo Moore que define el funcionamiento del bloque. En esta etapa con máquina de estado se detectan las transiciones mientras se espera a que la señal de enable se ponga a '1'. Esto ocurre cuando se detecta el flanco de bajada de '1' a '0'. En ese momento el contador del decodificador empieza sus cuentas. Cuando los 11 bits son transmitidos la señal de enable volverá a 0 hasta que vuelva a detectar otro flanco de bajada.

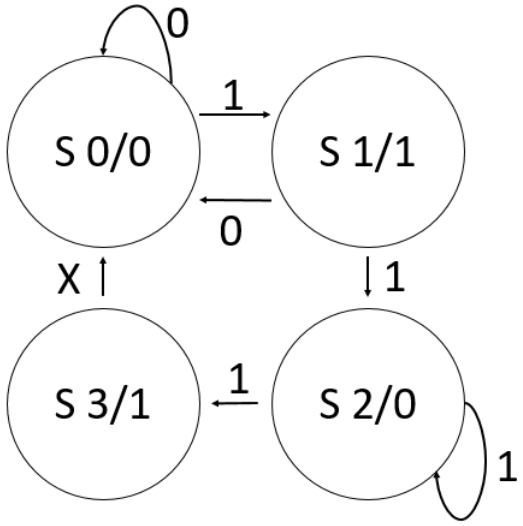

Figura 3.19: Etapa con máquina de estado.

3.5.2. Bloque Enable

Este bloque (Figura 3.20) se encarga de decidir cuando se empieza a leer el mensaje. Esto será cuando se detecte un cambio de 1 a 0, lo que significará que se empieza a transmitir el mensaje. Esta búsqueda se realiza con el reloj que va a una frecuencia de 3200 kHz. Una vez detectado el inicio de mensaje, se cambia a una etapa donde trabaja el reloj de 100 kHz que realizará una cuenta hasta que se transmitan los 11 Bits del mensaje. Momento en el que el enable volverá a '0'.

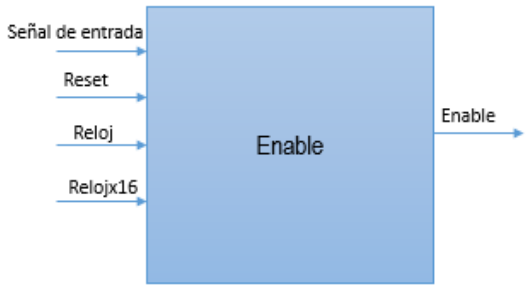

Figura 3.20: Bloque enable.

3.5.3. Bloque leer bit

La señal procedente del demodulador llega a este bloque (Figura 3.21) en el cual, con un reloj de 100 kHz se va leyendo el mensaje para obtener como salida el array de los 11 bits del mensaje transmitido.

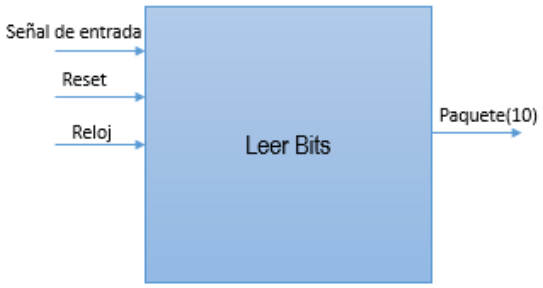

Figura 3.21: Bloque leer bit.

3.5.4. Bloque Filtro

En esta etapa(Figura 3.22) llega el paquete procedente de la lectura de bits y primero se le elimina el primer bit y los dos últimos que pertenecen al protocolo RS-232. Los ocho bits resultantes corresponden a la codificación Manchester, por lo que los descodificamos para obtener los cuatro bits resultantes del mensaje original transmitidos, realizando el proceso inverso al planteado en la Tabla 3.1 de esta memoria.

Figura 3.22: Bloque filtro.

3.5.5. Bloque generador de señal

Los 4 bits de entrada son los procedentes del filtro del bloque anterior. Se emplea un reloj de 50 kHz para generar la señal con el mensaje original. La Figura 3.23 muestra el bloque generador de señal con sus correspondientes entradas y salidas.

Figura 3.23: Bloque Generador de señal 4 bits.

CAPÍTULO 4

4. Resultados

En el presente capítulo se muestra el montaje físico empleado para la obtención de los resultados (Figura 4.1) acorde a los objetivos propuestos en la presente memoria. Primero para comprobar el buen funcionamientos de los bloques transmisor y receptor se realizó una primera prueba con un enlace cableado. Tras comprobar el buen funcionamiento se eliminó el cable y se incorporó el enlace óptico.

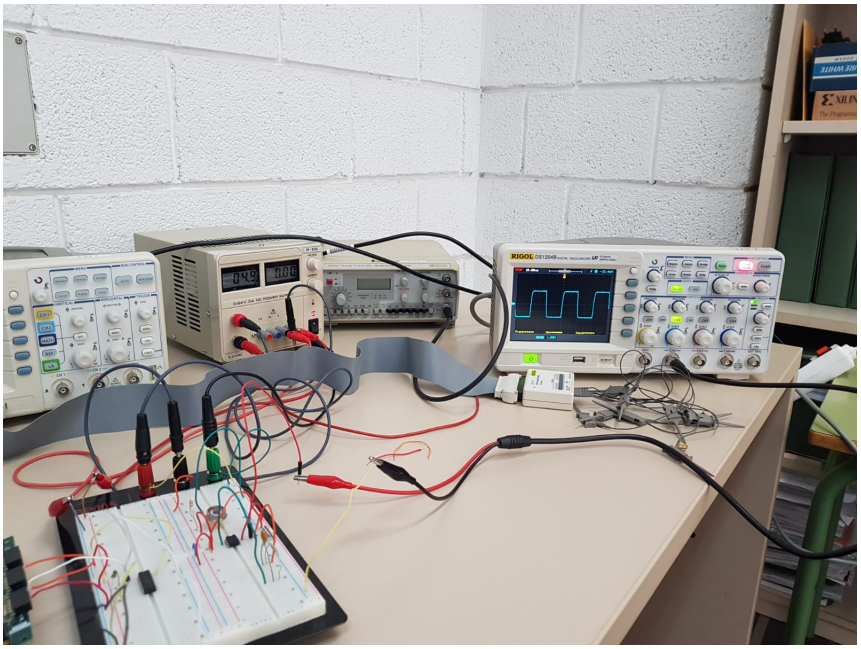

Figura 4.1: Montaje para la obteción de los resultados.

4.1. Enlace Cableado

Antes de comprobar el correcto funcionamiento del sistema de transmisión digital con modulación OOK y codificación Manchester utilizando como medio de transmisión la luz visible, es decir, empleando el enlace óptico formado por el emisor y receptor óptico, se ha implementado el sistema conectando, a través de un cable, la salida del bloque transmisor con la entrada del bloque receptor. De esta manera, se ha podido constatar el correcto funcionamiento de los elementos que constituyen el bloque transmisor (codificador Manchester y modulador OOK), el bloque receptor (demodulador OOK y decodificador Manchester), así como el proceso de comunicación asíncrona establecida con ayuda del protocolo RS-232; independientemente de los efectos debidos al establecimiento del enlace óptico.

En la Figura 4.2 se muestran los resultados obtenidos con el sistema haciendo uso de un enlace cableado. La secuencia de bits o de datos transmitidos fue 1010.

Figura 4.2: Resultado del enlace cableado.

La señal superior de la Figura 4.2 muestra la señal de salida del bloque transmisor, es decir, el conjunto de 11 bits que conforman la trama de datos enviadas según el estándar RS-232. El primer pulso es el bit de inicio (‘0’), los siguientes ocho pulsos (10011001) corresponden a los datos 1010 tras el proceso de codificación Manchester y, por último, los dos últimos pulsos son los bits de stop (00). En la señal inferior se muestra la señal en banda base detectada por el bloque receptor (1010), después de que la señal recibida haya sido sometida al proceso de sincronización, decodificación y demodulación. Como se puede observar, la transmisión y recepción de dicha secuencia se realiza correctamente, con lo que se pudo concluir que los módulos o elementos de los bloques de transmisión y recepción, así como el proceso de comunicación asíncrona funcionaba de manera satisfactoria.

4.2. Enlace Óptico

Tras comprobar el correcto funcionamiento del sistema de transmisión haciendo uso de un enlace cableado, en este aparatado se presenta la implementación del sistema con el enlace óptico. Es decir, respecto al montaje del apartado anterior, se ha sustituido el cable por el emisor óptico (circuito elevador de voltaje y la lámpara LED), y por el receptor óptico (fotodiodo y amplificador de transimpedancia). En la Figura 4.3 se muestra el montaje realizado sobre una placa de desarrollo de prototipos.

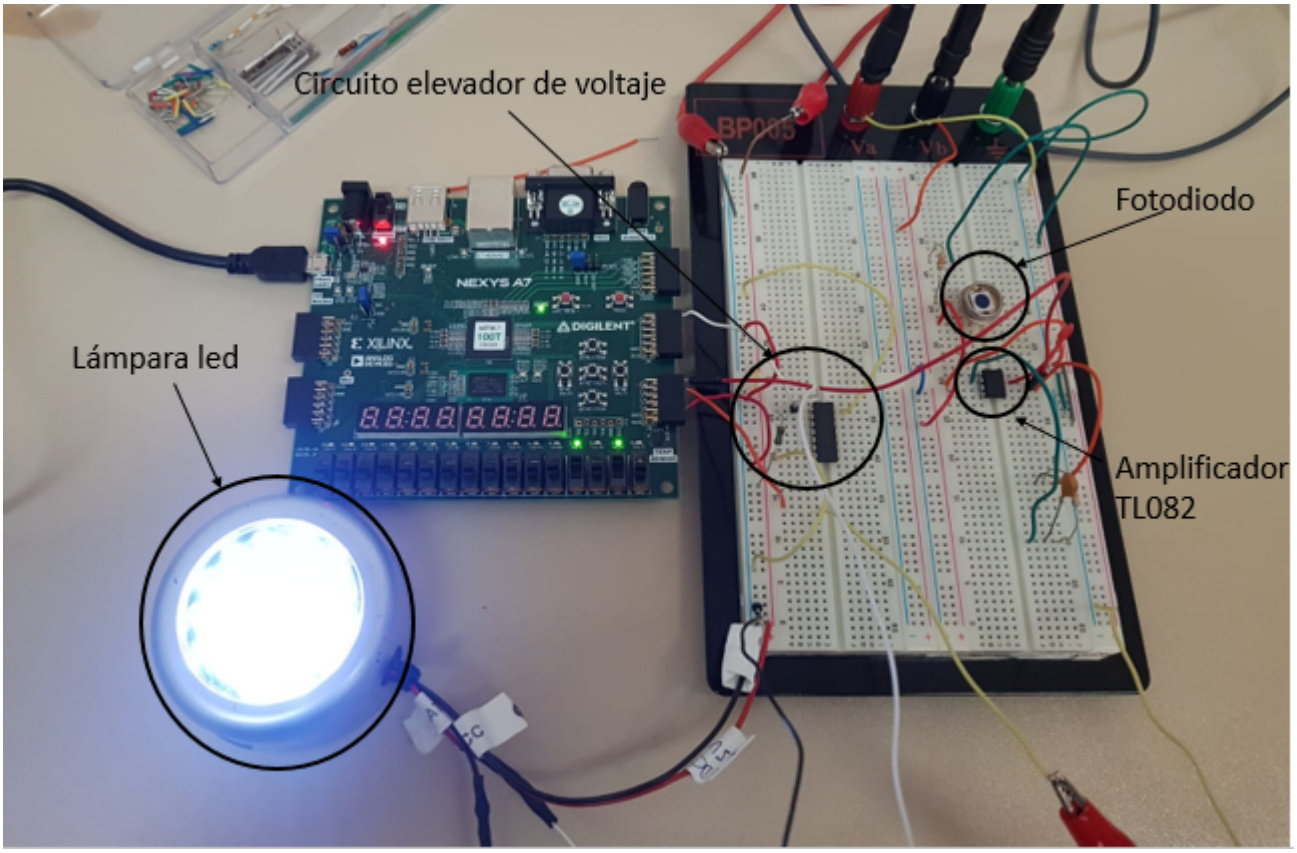

Figura 4.3: Montaje enlace óptico.

Para comprobar su correcto funcionamiento se ha transmitido la misma secuencia de bits o de datos, 1010, que se empleó para el enlace cableado. En la Figura 4.5 se muestra la señal recibida tras los procesos de decodificación y demodulación realizados por el bloque receptor. Como se puede observar, el mensaje obtenido coincide con el que se empleó en la transmisión, con lo que se concluye que el sistema de transmisión digital VLC con modulación OOK funciona correctamente.

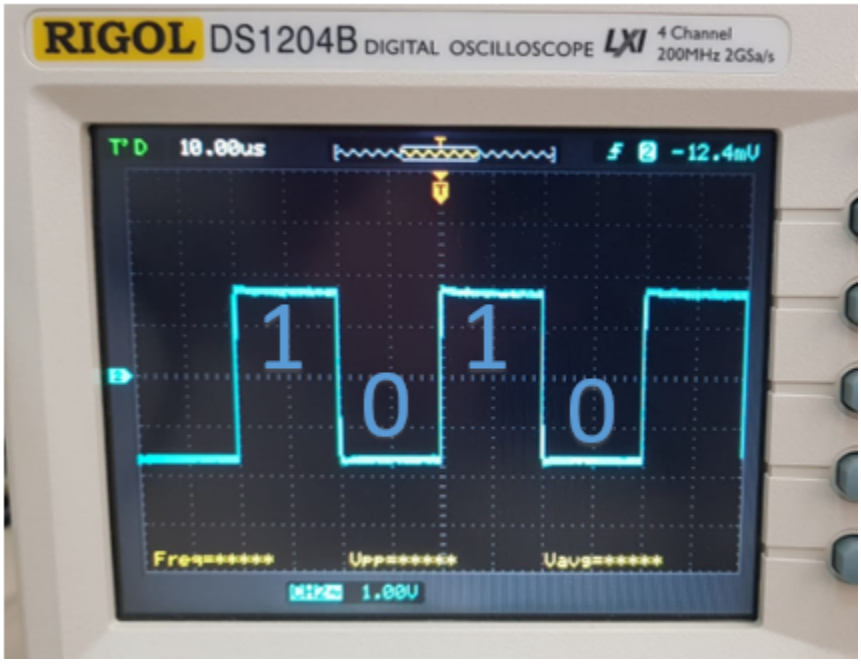

Figura 4.4: Resultado obtenido en el enlace óptico.

CAPÍTULO 5

5. Presupuesto

En este capítulo se presenta el coste de realización de este trabajo. Como se puede observar, dicho coste se divide en el coste de los materiales y el coste de mano de obra. Además, se incluyen los gastos generales, el beneficio industrial y el IGIC.

Concepto	Coste unitario (€)	Cantidad (u)	Coste Total (€)
Tarjeta de desarrollo Nexys A7	244,57 €	1,00 €	244,57 €
Lámpara LED	8,50 €	1,00 €	8,50 €
Fotodiodo S3071 de Hamamatsu	12,63 €	1,00 €	12,63 €
Circuito integrado TL082	0,55 €	1,00 €	0,55 €
Circuito integrado 74LS07	1,31 €	1,00 €	1,31 €
Resistencias(Diferentes valores)	0,08 €	3,00 €	0,24 €
Condensador 10pF	0,17 €	1,00 €	0,17 €
	Total Costes Materiales (MT)		267,97 €

Concepto	Coste unitario (€)	Cantidad (h)	Coste Total (€)
Tiempo de análisis	60,00 €	100,00 €	6.000,00 €
Tiempo de codificación	30,00 €	400,00 €	12.000,00 €
Tiempo de implementación	20,00 €	20,00 €	400,00 €
Tiempo de documentación	25,00 €	80,00 €	2.000,00 €
	Total Costes mano de obra (MO)		20.400,00 €

Total costes materiales (MT)	267,97 €
Total costes mano de obra (MO)	20.400,00 €
Gastos generales: 6% (MT+MO)	1.240,08 €
Beneficio Industrial: 13% (MT+MO)	2.686,84 €
IGIC 7%	1.721,64 €
Coste Total del Proyecto(€)	26.316,53 €

CAPÍTULO 6

6. Conclusiones

Durante la realización de este Trabajo de Fin de Grado se han alcanzado los objetivos inicialmente propuestos y orientados al diseño e implementación de un sistema transmisor y receptor que emplea modulación OOK y que transmite señales digitales utilizando como medio de transmisión la luz visible. Es decir, un sistema de transmisión enmarcado en el campo de las Comunicaciones por Luz Visible (VLC), en el cual se transmite información mediante radiación electromagnética con una longitud de onda comprendida en el espectro visible por el ojo humano (375 – 780nm).

En este sentido, se han diseñado y desarrollado los diferentes elementos de los que consta el transmisor: el codificador Manchester, el modulador OOK en banda base y el emisor óptico, compuesto por el circuito elevador de voltaje (circuito excitador) y la lámpara LED (fuente óptica). Del mismo modo, se han diseñado e implementado los bloques de los que consta el receptor: el receptor óptico, compuesto por el fotodiodo S3010 y el amplificador de transimpedancia; el demodulador OOK y decodificador Manchester. Asimismo, se ha establecido una estrategia de sincronización de tipo asíncrona entre el transmisor y el receptor basada en el protocolo de comunicación RS-232.

La programación de los bloques de codificación, decodificación, modulación, demodulación y sincronización de trama se ha hecho con el lenguaje de descripción hardware VHDL, con el software ISE Design Suite 14.7, y su implementación se ha realizado en la placa de desarrollo Nexys A7 Artix de Digitent.

Una vez diseñado e implementado el sistema de transmisión VLC, se han llevado a cabo simulaciones y pruebas de laboratorio que han puesto de manifiesto el correcto funcionamiento de cada uno de los elementos que conforman el sistema desarrollado. El sistema implementado es capaz de transmitir un mensaje a través del enlace óptico, demodularlo y decodificarlo para recuperar el mensaje original.

Por último, indicar que la tecnología VLC es una tecnología emergente, la cual va a tener un papel fundamental en el futuro de las comunicaciones, sobretodo en interiores. Este tipo de sistemas es una perfecta sustituta y, a la vez complementaria, de las ya conocidas comunicaciones por radiofrecuencia, pues permite proporcionar soluciones en aplicaciones donde la tecnología de radiofrecuencia no puede ser utilizada o donde el uso de su rango de aplicación espectral ya está saturado.

CAPÍTULO 7

7. Bibliografía

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CAPÍTULO 8

8. Anexos

Hojas de características

8.1. Nexys A7™ FPGA Board Reference Manua

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www.digilentinc.com

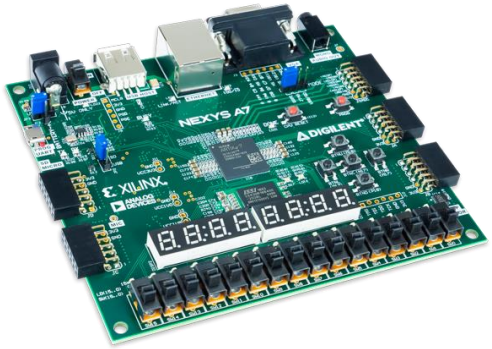
Nexys A7™ FPGA Board Reference Manual

Revised July 10, 2019

Table of Contents

Features

The Nexys A7 board is a complete, ready-to-use digital circuit development platform based on the latest Artix-7™ Field Programmable Gate Array (FPGA) from Xilinx®. With its large, high-capacity FPGA, generous external memories, and collection of USB, Ethernet, and other ports, the Nexys A7 can host designs ranging from introductory combinational circuits to powerful embedded processors. Several built-in peripherals, including an accelerometer, temperature sensor, MEMs digital microphone, a speaker amplifier, and several I/O devices allow the Nexys A7 to be used for a wide range of designs without needing any other components.



The Nexys A7 FPGA.

- **Artux-7 FPGA**
  - 15,850 Programmable logic slices, each with four 6-input LUTs and 8 flip-flops (*8,150 slices)
  - 1,188 Kbits of fast block RAM (*600 Kbits)
  - Six clock management tiles, each with phase-locked loop (PLL)
  - 240 DSP slices (*120 DSPs)
  - Internal clock speeds exceeding 450 MHz
  - Dual-channel, 1 MSPS internal analog-digital converter (XADC)
- **Memory**
  - 128MiB DDR2
  - Serial Flash
  - microSD card slot
- **Power**
  - Powered from USB or any 4.5V-5.5V external power source
- **USB and Ethernet**
  - 10/100 Ethernet PHY
  - USB-JTAG programming circuitry
  - USB-UART bridge
  - USB HID Host for mice, keyboards and memory sticks
- **Simple User Input/**Output
  - 16 Switches
  - 16 LEDs
  - Two RGB LEDs
  - Two 4-digit 7-segment displays
- **Audio and Video**
  - 12-bit VGA output
  - PWM audio output
  - PDM microphone
- **Additional Sensors**
  - 3-axis accelerometer
  - Temperature sensor
- **Expansion Connectors**
  - Pmod connector for XADC signals
  - Four Pmod connectors providing 32 total FPGA I/O

The Nexys A7-100T is compatible with Xilinx's Vivado® Design Suite as well as the ISE® toolset, which includes ChipScope™ and EDK. Xilinx ISE has been discontinued in favor of Vivado® Design Suite.

The Nexys A7-50T variant is compatible only with Vivado® Design Suite.

Xilinx offers free WebPACK™ versions of these toolsets, so designs can be implemented at no additional cost.

The Nexys A7 is not supported by the Digilent Adept Utility.

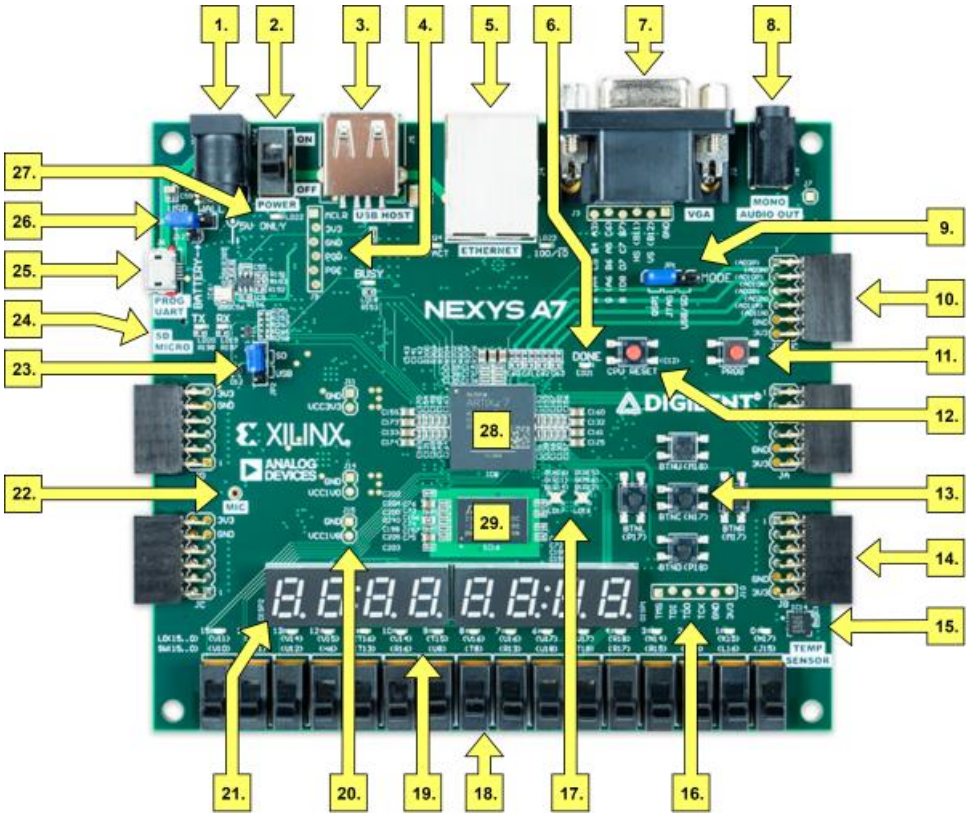


Figure 1. Nexys A7 Feature Callout.

Callout	Component Description	Callout	Component Description
1	Power jack	16	JTAG port for (optional) external cable
2	Power switch	17	Tri-color (RGB) LEDs
3	USB host connector	18	Slide switches (16)
4	PIC24 programming port (factory use)	19	LEDs (16)
5	Ethernet connector	20	Power supply test point(s)
6	FPGA programming done LED	21	Eight digit 7-seg display
7	VGA connector	22	Microphone
8	Audio connector	23	External configuration jumper (SD / USB)
9	Programming mode jumper	24	MicroSD card slot
10	Analog signal Pmod port (XADC)	25	Shared UART/ JTAG USB port

11	FPGA configuration reset button	**26**	Power select jumper and battery header
12	CPU reset button (for soft cores)	**27**	Power-good LED
13	Five pushbuttons	**28**	Xilinx Artix-7 FPGA
14	Pmod port(s)	**29**	DDR2 memory
15	Temperature sensor		

Purchasing Options

The Nexys A7 can be purchased with either a XC7A100T or XC7A50T FPGA loaded. These two Nexys A7 product variants are referred to as the Nexys A7-100T and Nexys A7-50T, respectively. When Digilent documentation describes functionality that is common to both of these variants, they are referred to collectively as the "Nexys A7". When describing something that is only common to a specific variant, the variant will be explicitly called out by its name.

The only difference between the Nexys A7-100T and Nexys A7-50T is the size of the Artix-7 part. The Artix-7 FPGAs both have the same capabilities, but the XC7100T has about a 2 times larger internal FPGA than the XC750T. The differences between the two variants are summarized below:

Product Variant	Nexys A7-100T	Nexys A7-50T
FPGA Part Number	XC7A100T-1CSG324C	XC7A50T-1CSG324I
Look-up Tables (LUTs)	63,400	32,600
Flip-Flops	126,800	65,200
Block RAM	1,188 Kb	600 Kb
DSP Slices	240	120
Clock Management Tiles	6	5

Board Revisions

The Nexys A7 is a rebrand of the Nexys 4 DDR board, which is an incremental update to the Nexys 4 board.

Migrating from Nexys 4 DDR

The only difference between the Nexys A7 and Nexys 4 DDR is the addition of the Nexys A7-50T variant of the Nexys A7, which has a smaller gate array. The Nexys A7-100T variant is functionally identical to the Nexys 4 DDR.

Users of the Nexys A7 may find resources produced for the Nexys 4 DDR helpful, which can be found at the Nexys 4 DDR's Resource Center.

Migrating from Nexys 4

The major improvement from the Nexys 4 to the Nexys 4 DDR is the replacement of the 16 MiB Cellular RAM with a 128 MiB DDR2 SDRAM memory. Furthermore, to accommodate the new memory, the pin-out of the FPGA banks changed as well.

The audio output (AUD_PWM) needs to be driven open-drain as opposed to push-pull on the Nexys 4.

1 Functional Description

1.1 Power Supplies

The Nexys A7 board can receive power from the Digilent USB-JTAG port (J6) or from an external power supply. Jumper JP3 (near the power jack) determines which source is used.

All Nexys A7 power supplies can be turned on and off by a single logic-level power switch (SW16). A power-good LED (LD22), driven by the "power good" output of the ADP2118 supply, indicates that the supplies are turned on and operating normally. An overview of the Nexys A7 power circuit is shown in Figure 1.1.

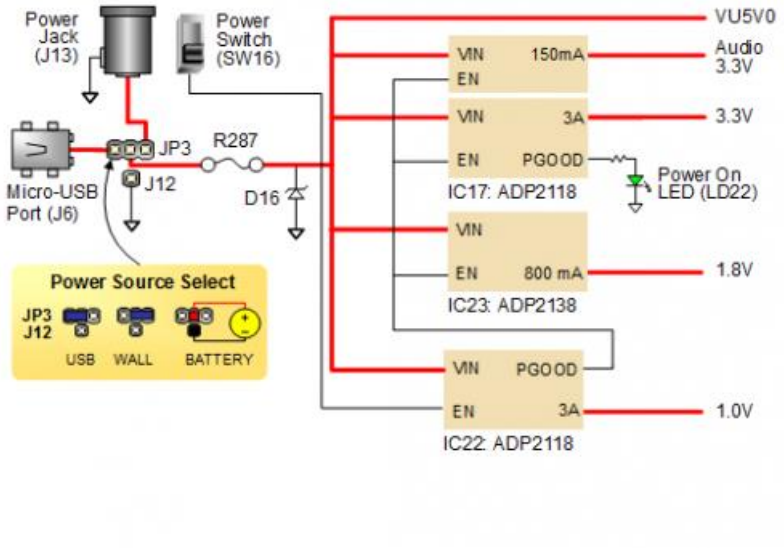


Figure 1.1 Nexys A7 Power Circuit

The USB port can deliver enough power for the vast majority of designs. In order to power the board from USB port set jumper JP3 to "USB". Our out-of-box demo draws ~400mA of current from the 5V input rail. A few demanding applications, including any that drive multiple peripheral boards, might require more power than the USB port can provide. Also, some applications may need to run without being connected to a PC's USB port. In these instances, an external power supply or battery pack can be used.

An external power supply can be used by plugging into to the power jack (J13) and setting jumper JP3 to "WALL". The supply must use a coax, center-positive 2.1mm internal-diameter plug, and deliver 4.5VDC to 5.5VDC and at least 1A of current (i.e., at least 5W of power). Many suitable supplies can be purchased from Digilent, through Digi-Key, or other catalog vendors.

An external battery pack can be used by connecting the battery's positive terminal to the center pin of JP3 and the negative terminal to the pin labeled J12, directly below JP3. Since the main regulator on the Nexys A7 cannot accommodate input voltages over 5.5VDC, an external battery pack must be limited to 5.5VDC. The minimum voltage of the battery pack depends on the application: if the USB Host function (J5) is used, at least 4.6V needs to be provided. In other cases, the minimum voltage is 3.6V.

Voltage regulator circuits from Analog Devices create the required 3.3V, 1.8V, and 1.0V supplies from the main power input. Table 1.1 provides additional information. Typical currents depend strongly on FPGA configuration and the values provided are typical of medium size/speed designs.

Supply	Circuits	Device	Current (Max/Typical)
3.3V	FPGA I/O, USB ports, Clocks, RAM I/O, Ethernet, SD slot, Sensors, Flash	IC17: ADP2118	3A/0.1 to 1.5A
1.0V	FPGA Core	IC22: ADP2118	3A/ 0.2 to 1.3A
1.8V	DDR2, FPGA Auxiliary and RAM	IC23: ADP2118	0.8A/ 0.5A

Table 1.1 Nexys A7 power supplies.

1.2 Protection

The Nexys A7 features overcurrent and overvoltage protection on the input power rail. A 3.5A fuse (R287) and a 5V Zener diode (D16) provide a non-resettable protection for other on-board integrated circuits, as displayed in Figure 2. Applying power outside of the specs outlined in this document is not covered by warranty. If this happens, either or both might get permanently damaged. The damaged parts are not user replaceable.

2 FPGA Configuration

After power-on, the Artix-7 FPGA must be configured (or programmed) before it can perform any functions. You can configure the FPGA in one of four ways:

1. A PC can use the Digilent USB-JTAG circuitry (portJ6, labeled "PROG") to program the FPGA any time the power is on.
2. A file stored in the nonvolatile serial (SPI) flash device can be transferred to the FPGA using the SPI port.
3. A programming file can be transferred to the FPGA from a micro SD card.
4. A programming file can be transferred from a USB memory stick attached to the USB HID port.

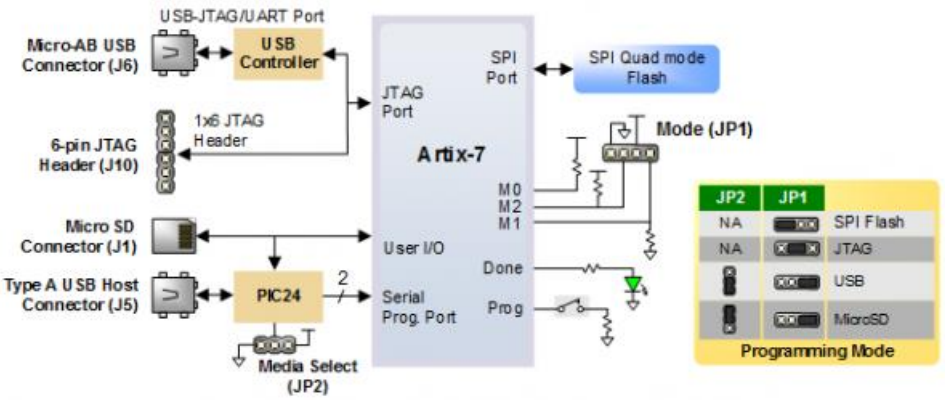


Figure 2.1 Nexys A7 DDR Configuration Options.

Figure 2.1 shows the different options available for configuring the FPGA. An on-board "mode" jumper (JP1) and a media selection jumper (JP2) select between the programming modes.

The FPGA configuration data is stored in files called bitstreams that have the .bit file extension. The ISE or Vivado software from Xilinx can create bitstreams from VHDL, Verilog®, or schematic-based source files (in the ISE toolset, EDK is used for MicroBlaze™ embedded processor-based designs).

Bitstreams are stored in SRAM-based memory cells within the FPGA. This data defines the FPGA's logic functions and circuit connections, and it remains valid until it is erased by removing board power, by pressing the reset button attached to the PROG input, or by writing a new configuration file using the JTAG port.

An Artix-7 100T bitstream is typically 30,606,304 bits and can take a long time to transfer. The time it takes to program the Nexys A7 can be decreased by compressing the bitstream before programming, and then allowing the FPGA to decompress the bitstream itself during configuration. Depending on design complexity, compression ratios of 10x can be achieved. Bitstream compression can be enabled within the Xilinx tools (ISE or Vivado) to occur during generation. For instructions on how to do this, consult the Xilinx documentation for the toolset being used. After being successfully programmed, the FPGA will cause the "DONE" LED to illuminate. Pressing the "PROG" button at any time will reset the configuration memory in the FPGA. After being reset, the FPGA will immediately attempt to reprogram itself from whatever method has been selected by the programming mode jumpers.

The following sections provide greater detail about programming the Nexys A7 using the different methods available.

2.1 JTAG Configuraiton

The Xilinx tools typically communicate with FPGAs using the Test Access Port and Boundary-Scan Architecture, commonly referred to as JTAG. During JTAG programming, a .bit file is transferred from the PC to the FPGA using the onboard Digilent USB-JTAG circuitry (port J6) or an external JTAG programmer, such as the Digilent JTAG-HS2, attached to port J10. You can perform JTAG programming any time after the Nexys A7 has been powered on, regardless of what the mode jumper (JP1) is set to. If the FPGA is already configured, then the existing configuration is overwritten with the bitstream being transmitted over JTAG. Setting the mode jumper to the JTAG setting (seen in Figure 3) is useful to prevent the FPGA from being configured from any other bitstream source until a JTAG programming occurs.

Programming the Nexys A7 with an uncompressed bitstream using the on-board USB-JTAG circuitry usually takes around five seconds. JTAG programming can be done using the hardware server in Vivado or the iMPACT tool included with ISE and the Lab Tools version of Vivado. The demonstration project available at http://www.digilentinc.com/ gives an in-depth tutorial on how to program your board.

2.2 Quad-SPI Configuration

Since the FPGA on the Nexys A7 is volatile, it relies on the Quad-SPI flash memory to store the configuration between power cycles. This configuration mode is called Master SPI. The blank FPGA takes the role of master and reads the configuration file out of the flash device upon power-up. To that effect, a configuration file needs to be downloaded first to the flash. When programming a nonvolatile flash device, a bitstream file is transferred to the flash in a two-step process. First, the FPGA is programmed with a circuit that can program flash devices, and then data is transferred to the flash device via the FPGA circuit (this complexity is hidden from the user by the Xilinx tools). This is called indirect programming. After the flash device has been programmed, it can automatically configure the FPGA at a subsequent power-on or reset event as determined by the mode jumper setting (see Figure 3). Programming files stored in the flash device will remain until they are overwritten, regardless of power-cycle events.

Programming the flash can take as long as four to five minutes, which is mostly due to the lengthy erase process inherent to the memory technology. Once written however, FPGA configuration can be very fast—less than a second. Bitstream compression, SPI bus width, and configuration rate are factors controlled by the Xilinx tools that can affect configuration speed. The Nexys A7 supports x1, x2, and x4 bus widths and data rates of up to 50 MHz for Quad-SPI programming.

Quad-SPI programming can be done using the iMPACT tool included with ISE or the Lab Tools version of Vivado.

2.3 USB Host and Micro SD Programming

You can program the FPGA from a pen drive attached to the USB Host port (J5) or a microSD card inserted into J1 by doing the following:

1. Format the storage device (Pen drive or microSD card) with a FAT32 file system.
2. Place a single .bit configuration file in the root directory of the storage device.
3. Attach the storage device to the Nexys A7.
4. Set the JP1 Programming Mode jumper on the Nexys A7 to “USB/SD”.
5. Select the desired storage device using JP2.
6. Push the PROG button or power-cycle the Nexys A7.

The FPGA will automatically configure with the .bit file on the selected storage device. Any .bit files that are not built for the proper Artix-7 device will be rejected by the FPGA.

The Auxiliary Function Status, or “BUSY” LED, gives visual feedback on the state of the configuration process when the FPGA is not yet programmed:

- When steadily lit, the auxiliary microcontroller is either booting up or currently reading the configuration medium (microSD or pen drive) and downloading a bitstream to the FPGA.
- A slow pulse means the microcontroller is waiting for a configuration medium to be plugged in.
- In case of an error during configuration, the LED will blink rapidly.

When the FPGA has been successfully configured, the behavior of the LED is application-specific. For example, if a USB keyboard is plugged in, a rapid blink will signal the receipt of an HID input report from the keyboard.

3 Memory

The Nexys A7 board contains two external memories: a 1Gib (128MiB) DDR2 SDRAM and a 128Mib (16MiB) non-volatile serial Flash device. The DDR2 modules are integrated on-board and connect to the FPGA using the industry standard interface. The serial Flash is on a dedicated quad-mode (x4) SPI bus. The connections and pin assignments between the FPGA and external memories are shown below.

3.1 DDR2

The Nexys A7 includes one Micron MT47H64M16HR-25:H DDR2 memory component, creating a single rank, 16-bit wide interface. It is routed to a 1.8V-powered HR (High Range) FPGA bank with 50 ohm controlled single-ended trace impedance. 50-ohm internal terminations in the FPGA are used to match the trace characteristics. Similarly, on the memory side, on-die terminations (ODT) are used for impedance matching.

For proper operation of the memory, a memory controller and physical layer (PHY) interface needs to be included in the FPGA design. There are two recommended ways to do that, which are outlined below and differ in complexity and design flexibility.

The straightforward way is to use the Digilent-provided DDR-to-SRAM adapter module which instantiates the memory controller and uses an asynchronous SRAM bus for interfacing with user logic. This module provides backward compatibility with projects written for older Nexys-line boards featuring a CellularRAM instead of DDR2. It trades memory bandwidth for simplicity.

More advanced users or those who wish to learn more about DDR SDRAM technology may want to use the Xilinx 7-series memory interface solutions core generated by the MIG (Memory Interface Generator) Wizard. Depending on the tool used (ISE, EDK or Vivado), the MIG Wizard can generate a native FIFO-style or an AXI4 interface to connect to user logic. This workflow allows the customization of several DDR parameters optimized for the particular application. Table 3.1 below lists the MIG Wizard settings optimized for the Nexys A7.

Setting	Value
Memory type	DDR2 SDRAM
Max. clock period	3000ps (667Mbps data rate)
Recommended clock period (for easy clock generation)	3077ps (650Mbps data rate)
Memory part	MT47H64M16HR-25E
Data width	16
Data mask	Enabled
Chip Select pin	Enabled
Rtt (nominal) – On-die termination	50ohms
Internal Vref	Enabled

Table 3.1.1 DDR2 settings for the Nexys A7.

Although the FPGA, memory IC, and the board itself are capable of the maximum data rate of 667Mbps, the limitations in the clock generation primitives restrict the clock frequencies that can be generated from the 100 MHz system clock. Thus, for simplicity, the next highest data rate of 650Mbps is recommended.

The MIG Wizard will require the fixed pin-out of the memory signals to be entered and validated before generating the IP core. For your convenience, an importable UCF file is provided on the Digilent website to speed up the process.

For more details on the Xilinx memory interface solutions, refer to the 7 Series FPGAs Memory Interface Solutions User Guide (ug586)[i].

3.2 Quad-SPI Flash

FPGA configuration files can be written to the Quad-SPI Flash (Spansion part number S25FL128S), and mode settings are available to cause the FPGA to automatically read a configuration from this device at power on. An Artix-7 100T configuration file requires just less than four MiB (mebibyte) of memory, leaving about 77% of the flash device available for user data. Or, if the FPGA is getting configured from another source, the whole memory can be used for custom data.

The contents of the memory can be manipulated by issuing certain commands on the SPI bus. The implementation of this protocol is outside the scope of this document. All signals in the SPI bus except SCK are general-purpose user I/O pins after FPGA configuration. SCK is an exception because it remains a dedicated pin even after configuration. Access to this pin is provided through a special FPGA primitive called STARTUPE2.

NOTE: Refer to the manufacturer's data sheets[ii] and Xilinx user guides[iii] for more information.

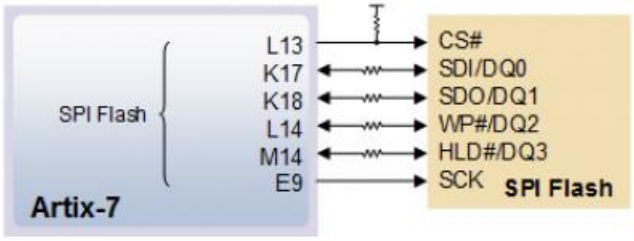


Figure 3.2.1 Nexys A7 DDR SPI Flash Pin-out

4 Ethernet PHY

The Nexys A7 board includes an SMSC 10/100 Ethernet PHY (SMSC part number LAN8720A) paired with an RJ-45 Ethernet jack with integrated magnetics. The SMSC PHY uses the RMII interface and supports 10/100 Mb/s. Figure 4.1 illustrates the pin connections between the Artix-7 and the Ethernet PHY. At power-on reset, the PHY is set to the following defaults:

- RMII mode interface
- Auto-negotiation enabled, advertising all 10/100 mode capable
- PHY address=00001

Two on-board LEDs (LD23 = LED2, LD24 = LED1) connected to the PHY provide link status and data activity feedback. See the PHY datasheet for details.

EDK-based designs can access the PHY using either the axi_ethernetlite (AXI EthernetLite) IP core or the axi_ethernet (Tri Mode Ethernet MAC) IP core. A mii_to_rmii core (Ethernet PHY MII to Reduced MII) needs to be inserted to convert the MAC interface from MII to RMII. Also, a 50 MHz clock needs to be generated for the

mii_to_rmii core and the CLKIN pin of the external PHY. To account for skew introduced by the mii_to_rmii core, generate each clock individually, with the external PHY clock having a 45 degree phase shift relative to the mii_to_rmii Ref_Clk. An EDK demonstration project that properly uses the Ethernet PHY can be found on the Nexys A7 product page at http://www.digilentinc.com/.

ISE designs can use the IP Core Generator wizard to create an Ethernet MAC controller IP core.

NOTE: Refer to the LAN8720A data sheet for further information[iv].

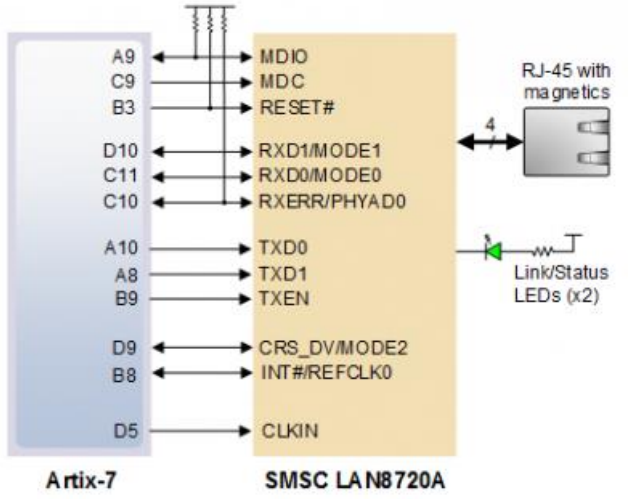


Figure 4.1 Pin Connections between the Artix-7 and the Ethernet PHY

5 Oscillators/Clocks

The Nexys A7 board includes a single 100 MHz crystal oscillator connected to pin E3 (E3 is a MRCC input on bank 35). The input clock can drive MMCMs or PLLs to generate clocks of various frequencies and with known phase relationships that may be needed throughout a design. Some rules restrict which MMCMs and PLLs may be driven by the 100 MHz input clock. For a full description of these rules and of the capabilities of the Artix-7 clocking resources, refer to the "7 Series FPGAs Clocking Resources User Guide" available from Xilinx.

Xilinx offers the Clocking Wizard IP core to help users generate the different clocks required for a specific design. This wizard will properly instantiate the needed MMCMs and PLLs based on the desired frequencies and phase relationships specified by the user. The wizard will then output an easy-to-use wrapper component around these clocking resources that can be inserted into the user's design. The clocking wizard can be accessed from within the Project Navigator or Core Generator tools.

6 USB-UART Bridge (Serial Port)

The Nexys A7 includes an FTDI FT2232HQ USB-UART bridge (attached to connector J6) that allows you use PC applications to communicate with the board using standard Windows COM port commands. Free USB-COM port drivers, available from http://www.ftdichip.com/ under the "Virtual Com Port" or VCP heading, convert USB packets to UART/serial port data. Serial port data is exchanged with the FPGA using a two-wire serial port (TXD/RXD) and optional hardware flow control (RTS/CTS). After the drivers are installed, I/O commands can be used from the PC directed to the COM port to produce serial data traffic on the C4 and D4 FPGA pins.

Two on-board status LEDs provide visual feedback on traffic flowing through the port: the transmit LED (LD20) and the receive LED (LD19). Signal names that imply direction are from the point-of-view of the DTE (Data Terminal Equipment), in this case the PC.

The FT2232HQ is also used as the controller for the Digilent USB-JTAG circuitry, but the USB-UART and USB-JTAG functions behave entirely independent of one another. Programmers interested in using the UART functionality of the FT2232 within their design do not need to worry about the JTAG circuitry interfering with the UART data transfers, and vice-versa. The combination of these two features into a single device allows the Nexys A7 to be programmed, communicated with via UART, and powered from a computer attached with a single Micro USB cable.

The connections between the FT2232HQ and the Artix-7 are shown in Figure 6.1.

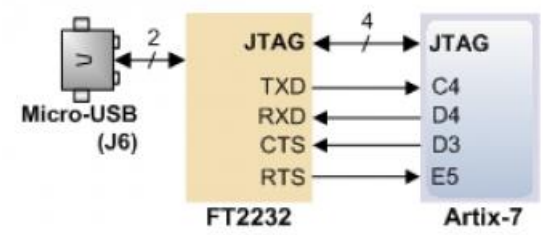


Figure 6.1 Nexys A7 FT2322HQ Connections

7 USB HID Host

The Auxiliary Function microcontroller (Microchip PIC24FJ128) provides the Nexys A7 with USB Embedded HID host capability. After power-up, the microcontroller is in configuration mode, either downloading a bitstream to the FPGA, or waiting to be programmed from other sources. Once the FPGA is programmed, the microcontroller switches to application mode, which is USB HID Host in this case. Firmware in the microcontroller can drive a mouse or a keyboard attached to the type A USB connector at J5 labeled "USB Host". Hub support is not currently available, so only a single mouse or a single keyboard can be used. Only keyboards and mice supporting the Boot HID interface are supported. The PIC24 drives several signals into the FPGA – two are used to implement a standard PS/2 interface for communication with a mouse or keyboard, and the others are connected to the FPGA's two-wire serial programming port, so the FPGA can be programmed from a file stored on a USB pen drive or microSD card.

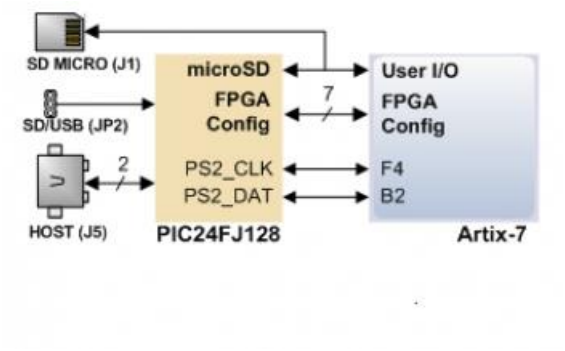
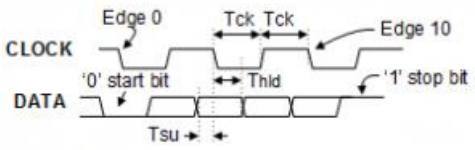


Figure 7.1 Nexys A7 PIC24 Connections

7.1 HID Controller

The Auxiliary Function microcontroller hides the USB HID protocol from the FPGA and emulates an old-style PS/2 bus. The microcontroller behaves just like a PS/2 keyboard or mouse would. This means new designs can re-use existing PS/2 IP cores. Mice and keyboards that use the PS/2 protocol use a two-wire serial bus (clock and data) to communicate with a host. On the Nexys A7, the microcontroller emulates a PS/2 device while the FPGA plays the role of the host. Both the mouse and the keyboard use 11-bit words that include a start bit, data byte (LSB first), odd parity, and stop bit, but the data packets are organized differently, and the keyboard interface allows bi-directional data transfers (so the host device can illuminate state LEDs on the keyboard). Bus timings are shown in Figure 7.1.1.



Symbol	Parameter	Min	Max
T_{CK}	Clock time	30us	50us
T_{SU}	Data-to-clock setup time	5us	25us
T_{HLD}	Clock-to-data hold time	5us	25us

Figure 7.1.1 PS/2 Device-to-Host Timing Diagram

The clock and data signals are only driven when data transfers occur; otherwise, they are held in the idle state at high-impedance (open-drain drivers). This requires that when the PS/2 signals are used in a design, internal pull-ups must be enabled in the FPGA on the data and clock pins. The clock signal is normally driven by the device, but may be held low by the host in special cases. The timings define signal requirements for mouse-to-host communications and bi-directional keyboard communications. A PS/2 interface circuit can be implemented in the FPGA to create a keyboard or mouse interface.

When a keyboard or mouse is connected to the Nexys A7, a “self-test passed” command (0xAA) is sent to the host. After this, commands may be issued to the device. Since both the keyboard and the mouse use the same PS/2 port, one can tell the type of device connected using the device ID. This ID can be read by issuing a Read ID

command (0xF2). Also, a mouse sends its ID (0x00) right after the "self-test passed" command, which distinguishes it from a keyboard.

7.2 Keyboard

PS/2-style keyboards use scan codes to communicate key press data. Each key is assigned a code that is sent whenever the key is pressed. If the key is held down, the scan code will be sent repeatedly about once every 100ms. When a key is released, an F0 key-up code is sent, followed by the scan code of the released key. If a key can be shifted to produce a new character (like a capital letter), then a shift character is sent in addition to the scan code and the host must determine which ASCII character to use. Some keys, called extended keys, send an E0 ahead of the scan code (and they may send more than one scan code). When an extended key is released, an E0 F0 key-up code is sent, followed by the scan code. Scan codes for most keys are shown in Figure 7.2.1.

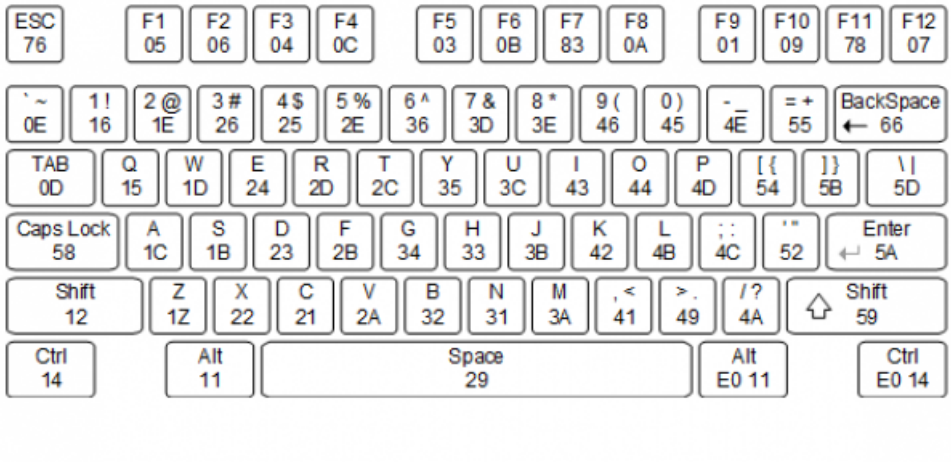


Figure 7.2.1 Keyboard Scan Codes

A host device can also send data to the keyboard. Table 7.2.1 shows a list of some common commands a host might send.

The keyboard can send data to the host only when both the data and clock lines are high (or idle). Because the host is the bus master, the keyboard must check to see whether the host is sending data before driving the bus. To facilitate this, the clock line is used as a "clear to send" signal. If the host drives the clock line low, the keyboard must not send any data until the clock is released. The keyboard sends data to the host in 11-bit words that contain a '0' start bit, followed by 8-bits of scan code (LSB first), followed by an odd parity bit, and terminated with a '1' stop bit. The keyboard generates 11 clock transitions (at 20 to 30 KHz) when the data is sent, and data is valid on the falling edge of the clock.

Command	Action
ED	Set Num Lock, Caps Lock, and Scroll Lock LEDs. Keyboard returns FA after receiving ED, then host sends a byte to set LED status: bit 0 sets Scroll Lock, bit 1 sets Num Lock, and bit 2 sets Caps lock. Bits 3 to 7 are ignored.
EE	Echo (test). Keyboard returns EE after receiving EE
F3	Set scan code repeat rate. Keyboard returns F3 on receiving FA, then host sends second byte to set the repeat rate.
FE	Resend. FE directs keyboard to re-send most recent scan code.

Table 7.2.1. Keyboard commands.

7.3 Mouse

Once entered in stream mode and data reporting is enabled, the mouse outputs a clock and data signal when it is moved; otherwise, these signals remain at logic '1.' Each time the mouse is moved, three 11-bit words are sent from the mouse to the host device, as shown in Figure 7.3.1. Each of the 11-bit words contains a '0' start bit, followed by 8 bits of data (LSB first), followed by an odd parity bit, and terminated with a '1' stop bit. Thus, each data transmission contains 33 bits, where bits 0, 11, and 22 are '0' start bits, and bits 11, 21, and 33 are '1' stop bits. The three 8-bit data fields contain movement data, as shown in Figure 7.3.1. Data is valid at the falling edge of the clock, and the clock period is 20 to 30 KHz.

The mouse assumes a relative coordinate system wherein moving the mouse to the right generates a positive number in the X field and moving to the left generates a negative number. Likewise, moving the mouse up generates a positive number in the Y field, and moving down represents a negative number (the XS and YS bits in the status byte are the sign bits – a '1' indicates a negative number). The magnitude of the X and Y numbers represent the rate of mouse movement; the larger the number, the faster the mouse is moving (the XV and YV bits in the status byte are movement overflow indicators. A '1' means overflow has occurred). If the mouse moves continuously, the 33-bit transmissions are repeated every 50ms or so. The L and R fields in the status byte indicate Left and Right button presses (a '1' indicates the button is being pressed).

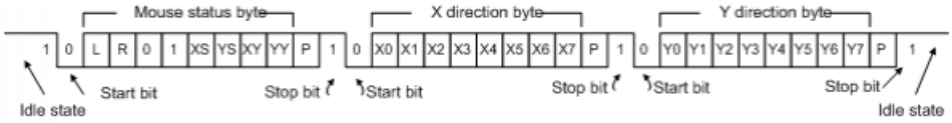


Figure 7.3.1 Mouse Data Format

The microcontroller also supports Microsoft® IntelliMouse®-type extensions for reporting back a third axis representing the mouse wheel, as shown in Table 7.3.1.

Command	Action
EA	Set stream mode. The mouse responds with "acknowledge" (0xFA) then resets its movement counters and enters stream mode.
F4	Enable data reporting. The mouse responds with "acknowledge" (0xFA) then enables data reporting and resets its movement counters. This command only affects behavior in stream mode. Once issued, mouse movement will automatically generate a data packet.
F5	Disable data reporting. The mouse responds with "acknowledge" (0xFA) then disables data reporting and resets its movement counters.
F3	Set mouse sample rate. The mouse responds with "acknowledge" (0xFA) then reads one more byte from the host. This byte is then saved as the new sample rate, and a new "acknowledge" packet is issued.
FE	Resend. FE directs mouse to re-send last packet.

Table 7.3.2. Microsoft IntelliMouse-Type extensions, commands, and actions.

8 VGA Port

The Nexys A7 board uses 14 FPGA signals to create a VGA port with 4 bits-per-color and the two standard sync signals (HS – Horizontal Sync, and VS – Vertical Sync). The color signals use resistor-divider circuits that work in conjunction with the 75-ohm termination resistance of the VGA display to create 16 signal levels each on the red, green, and blue VGA signals. This circuit, shown in Figure 8.1, produces video color signals that proceed in equal increments between 0V (fully off) and 0.7V (fully on). Using this circuit, 4096 different colors can be displayed, one for each unique 12-bit pattern. A video controller circuit must be created in the FPGA to drive the sync and color signals with the correct timing in order to produce a working display system.

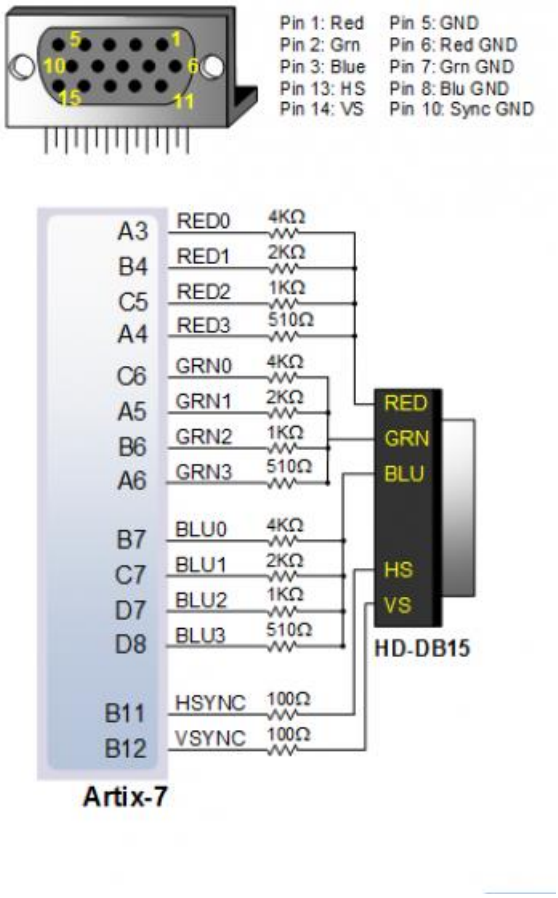


Figure 8.1 Nexys A7 VGA Interface

8.1 VGA System Timing

VGA signal timings are specified, published, copyrighted, and sold by the VESA® organization (http://www.vesa.org/). The following VGA system timing information is provided as an example of how a VGA monitor might be driven in 640 by 480 mode.

NOTE: For more precise information, or for information on other VGA frequencies, refer to documentation available at the VESA website.

CRT-based VGA displays use amplitude-modulated moving electron beams (or cathode rays) to display information on a phosphor-coated screen. LCD displays use an array of switches that can impose a voltage across a small amount of liquid crystal, thereby changing light permittivity through the crystal on a pixel-by-pixel basis. Although the following description is limited to CRT displays, LCD displays have evolved to use the same signal timings as CRT displays (so the "signals" discussion below pertains to both CRTs and LCDs). Color CRT displays use three electron beams (one for red, one for blue, and one for green) to energize the phosphor that coats the inner side of the display end of a cathode ray tube (see Figure 8.1.1).

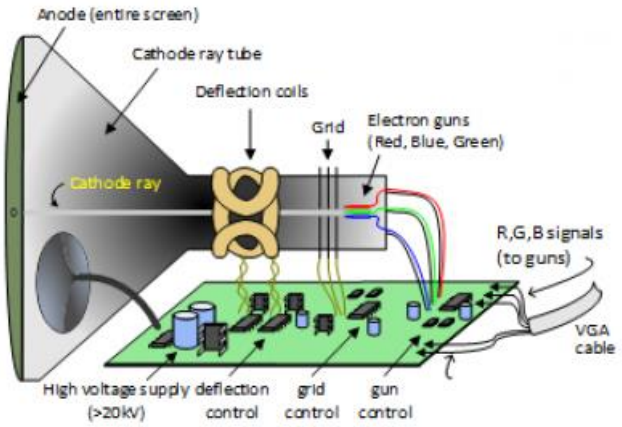


Figure 8.1.1 Color CRT Display

Electron beams emanate from "electron guns," which are finely-pointed heated cathodes placed in close proximity to a positively charged annular plate called a "grid." The electrostatic force imposed by the grid pulls rays of energized electrons from the cathodes, and those rays are fed by the current that flows into the cathodes. These particle rays are initially accelerated towards the grid, but they soon fall under the influence of the much larger electrostatic force that results from the entire phosphor-coated display surface of the CRT being charged to 20kV (or more). The rays are focused to a fine beam as they pass through the center of the grids, and then they accelerate to impact on the phosphor-coated display surface. The phosphor surface glows brightly at the impact point, and it continues to glow for several hundred microseconds after the beam is removed. The larger the current fed into the cathode, the brighter the phosphor will glow.

Between the grid and the display surface, the beam passes through the neck of the CRT where two coils of wire produce orthogonal electromagnetic fields. Because cathode rays are composed of charged particles (electrons), they can be deflected by these magnetic fields. Current waveforms are passed through the coils to produce magnetic fields that interact with the cathode rays and cause them to transverse the display surface in a "raster" pattern, horizontally from left to right and vertically from top to bottom, as shown in Figure 8.1.2. As the cathode ray moves over the surface of the display, the current sent to the electron guns can be increased or decreased to change the brightness of the display at the cathode ray impact point.

Information is only displayed when the beam is moving in the "forward" direction (left to right and top to bottom), and not during the time the beam is reset back to the left or top edge of the display. Much of the potential display time is therefore lost in "blanking" periods when the beam is reset and stabilized to begin a new horizontal or vertical display pass. The size of the beams, the frequency at which the beam can be traced across the display, and the frequency at which the electron beam can be modulated determine the display resolution.

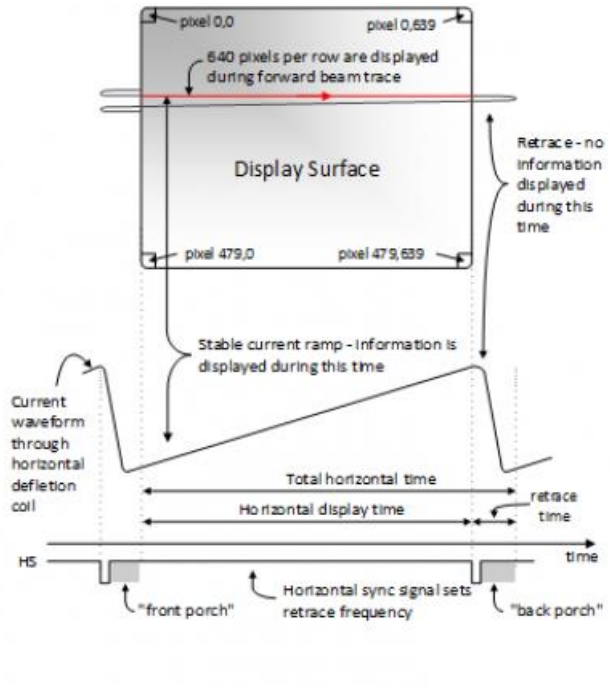


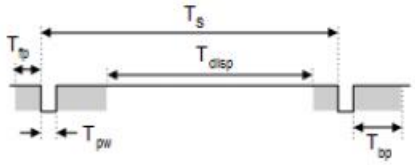
Figure 8.1.2 VGA Horizontal Synchronization

Modern VGA displays can accommodate different resolutions, and a VGA controller circuit dictates the resolution by producing timing signals to control the raster patterns. The controller must produce synchronizing pulses at 3.3V (or 5V) to set the frequency at which current flows through the deflection coils, and it must ensure that video data is applied to the electron guns at the correct time. Raster video displays define a number of "rows" that corresponds to the number of horizontal passes the cathode makes over the display area, and a number of "columns" that corresponds to an area on each row that is assigned to one "picture element," or pixel. Typical displays use from 240 to 1200 rows and from 320 to 1600 columns. The overall size of a display and the number of rows and columns determines the size of each pixel.

Video data typically comes from a video refresh memory; with one or more bytes assigned to each pixel location (the Nexys A7 uses 12 bits per pixel). The controller must index into video memory as the beams move across the display and retrieve and apply video data to the display at precisely the time the electron beam is moving across a given pixel.

A VGA controller circuit must generate the HS and VS timings signals and coordinate the delivery of video data based on the pixel clock. The pixel clock defines the time available to display one pixel of information. The VS signal defines the "refresh" frequency of the display, or the frequency at which all information on the display is redrawn. The minimum refresh frequency is a function of the display's phosphor and electron beam intensity, with practical

refresh frequencies falling in the 50Hz to 120Hz range. The number of lines to be displayed at a given refresh frequency defines the horizontal "retrace" frequency. For a 640-pixel by 480-row display using a 25 MHz pixel clock and 60 +/-1Hz refresh, the signal timings shown in Figure 8.1.3 can be derived. Timings for sync pulse width and front and back porch intervals (porch intervals are the pre- and post-sync pulse times during which information cannot be displayed) are based on observations taken from actual VGA displays.



Symbol	Parameter	Vertical Sync			Horiz. Sync	
		Time	Clocks	Lines	Time	Clks
T_S	Sync pulse	16.7ms	416,800	521	32 us	800
T_{disp}	Display time	15.36ms	384,000	480	25.6 us	640
T_{pw}	Pulse width	64 us	1,600	2	3.84 us	96
T_{fp}	Front porch	320 us	8,000	10	640 ns	16
T_{bp}	Back porch	928 us	23,200	29	1.92 us	48

Figure 8.1.3 Signal Timings for a 640-Pixel by 480-Row Display Using a 25 MHz Pixel Clock and 60 Hz Vertical Refresh

A VGA controller circuit, such as the one diagrammed in Figure 8.1.4, decodes the output of a horizontal-sync counter driven by the pixel clock to generate HS signal timings. You can use this counter to locate any pixel location on a given row. Likewise, the output of a vertical-sync counter that increments with each HS pulse can be used to generate VS signal timings, and you can use this counter to locate any given row. These two continually running counters can be used to form an address into video RAM. No time relationship between the onset of the HS pulse and the onset of the VS pulse is specified, so you can arrange the counters to easily form video RAM addresses, or to minimize decoding logic for sync pulse generation.

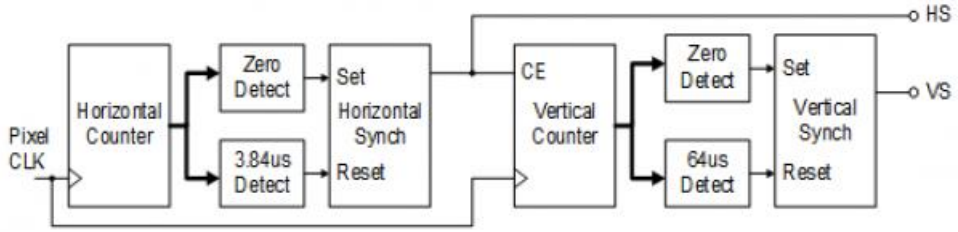


Figure 8.1.4 VGA Display Controller Block Diagram

9 Basic I/O

The Nexys A7 board includes two tri-color LEDs, sixteen slide switches, six push buttons, sixteen individual LEDs, and an eight-digit seven-segment display, as shown in Figure 9.1. The pushbuttons and slide switches are connected to the FPGA via series resistors to prevent damage from inadvertent short circuits (a short circuit could occur if an FPGA pin assigned to a pushbutton or slide switch was inadvertently defined as an output). The five pushbuttons arranged in a plus-sign configuration are “momentary” switches that normally generate a low output when they are at rest, and a high output only when they are pressed. The red pushbutton labeled “CPU RESET,” on the other hand, generates a high output when at rest and a low output when pressed. The CPU RESET button is intended to be used in EDK designs to reset the processor, but you can also use it as a general-purpose pushbutton. Slide switches generate constant high or low inputs depending on their position.

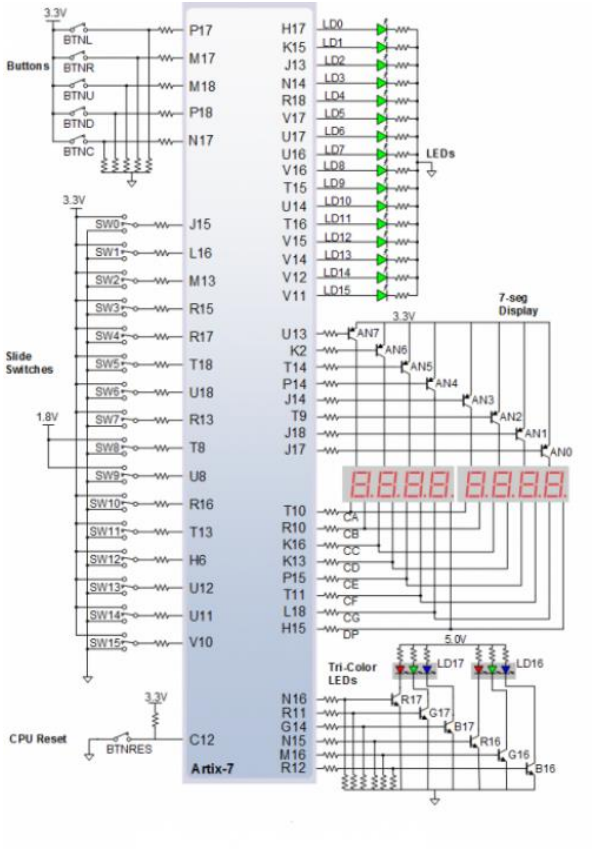


Figure 9.1 General Purpose I/O Devices on the Nexys A7

The sixteen-individual high-efficiency LEDs are anode-connected to the FPGA via 330-ohm resistors, so they will turn on when a logic high voltage is applied to their respective I/O pin. Additional LEDs that are not user-accessible indicate power-on, FPGA programming status, and USB and Ethernet port status.

9.1 Seven-Segment Display

The Nexys A7 board contains two four-digit common anode seven-segment LED displays, configured to behave like a single eight-digit display. Each of the eight digits is composed of seven segments arranged in a “figure 8” pattern, with an LED embedded in each segment. Segment LEDs can be individually illuminated, so any one of 128 patterns can be displayed on a digit by illuminating certain LED segments and leaving the others dark, as shown in Figure 9.1.1. Of these 128 possible patterns, the ten corresponding to the decimal digits are the most useful.

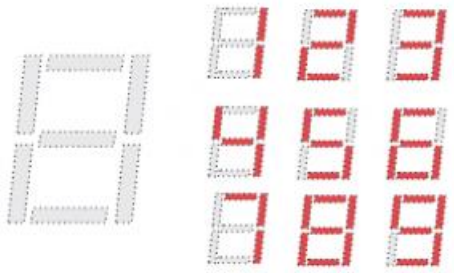


Figure 9.1.1 An Un-illuminated Seven-Segment Display and Nine Illumination Patterns Corresponding to Decimal Digits

The anodes of the seven LEDs forming each digit are tied together into one “common anode” circuit node, but the LED cathodes remain separate, as shown in Fig 18. The common anode signals are available as eight “digit enable” input signals to the 8-digit display. The cathodes of similar segments on all four displays are connected into seven circuit nodes labeled CA through CG. For example, the eight “D” cathodes from the eight digits are grouped together into a single circuit node called “CD.” These seven cathode signals are available as inputs to the 8-digit display. This signal connection scheme creates a multiplexed display, where the cathode signals are common to all digits but they can only illuminate the segments of the digit whose corresponding anode signal is asserted.

To illuminate a segment, the anode should be driven high while the cathode is driven low. However, since the Nexys A7 uses transistors to drive enough current into the common anode point, the anode enables are inverted. Therefore, both the AN0..7 and the CA..G/DP signals are driven low when active.

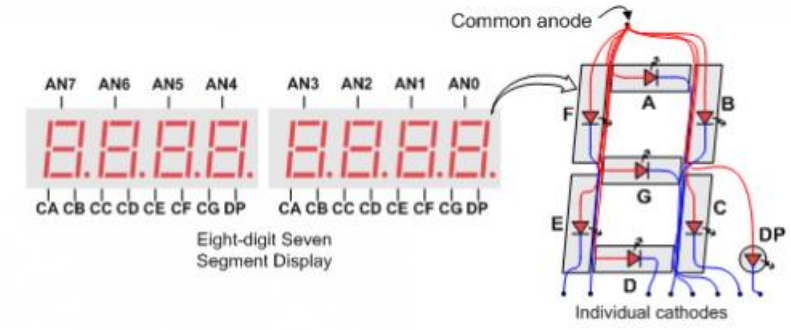


Figure 9.1.2 Common Anode Circuit Node

A scanning display controller circuit can be used to show an eight-digit number on this display. This circuit drives the anode signals and corresponding cathode patterns of each digit in a repeating, continuous succession at an update rate that is faster than the human eye can detect. Each digit is illuminated just one-eighth of the time, but because the eye cannot perceive the darkening of a digit before it is illuminated again, the digit appears continuously illuminated. If the update, or "refresh", rate is slowed to around 45Hz, a flicker can be noticed in the display.

For each of the four digits to appear bright and continuously illuminated, all eight digits should be driven once every 1 to 16ms, for a refresh frequency of about 1 KHz to 60Hz. For example, in a 62.5Hz refresh scheme, the entire display would be refreshed once every 16ms, and each digit would be illuminated for 1/8 of the refresh cycle, or 2ms. The controller must drive low the cathodes with the correct pattern when the corresponding anode signal is driven high. To illustrate the process, if AN0 is asserted while CB and CC are asserted, then a "1" will be displayed in digit position 1. Then, if AN1 is asserted while CA, CB, and CC are asserted, a "7" will be displayed in digit position 2. If AN0, CB, and CC are driven for 4ms, and then AN1, CA, CB, and CC are driven for 4ms in an endless succession, the display will show "71" in the first two digits. An example timing diagram for a four-digit controller is shown in Figure 9.1.3.

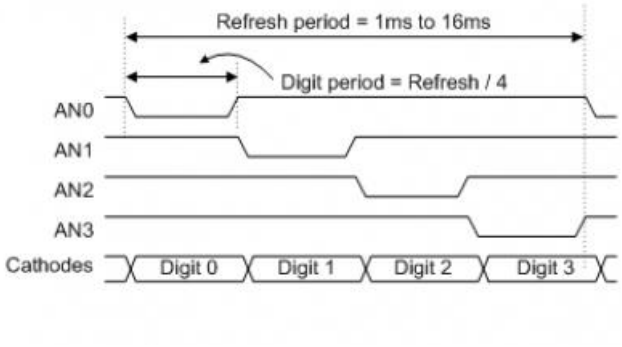


Figure 9.1.3 Four Digit Scanning Display Controller Timing Diagram

9.2 Tri-Color LED

The Nexys A7 board contains two tri-color LEDs. Each tri-color LED has three input signals that drive the cathodes of three smaller internal LEDs: one red, one blue, and one green. Driving the signal corresponding to one of these colors high will illuminate the internal LED. The input signals are driven by the FPGA through a transistor, which inverts the signals. Therefore, to light up the tri-color LED, the corresponding signals need to be driven high. The tri-color LED will emit a color dependent on the combination of internal LEDs that are currently being illuminated. For example, if the red and blue signals are driven high, and green is driven low, the tri-color LED will emit a purple color.

Note: Digilent strongly recommends the use of pulse-width modulation (PWM) when driving the tri-color LEDs (for information on PWM, see section 15.1 Pulse Density Modulation (PDM)). Driving any of the inputs to a steady logic '1' will result in the LED being illuminated at an uncomfortably bright level. You can avoid this by ensuring that none of the tri-color signals are driven with more than a 50% duty cycle. Using PWM also greatly expands the potential color palette of the tri-color led. Individually adjusting the duty cycle of each color between 50% and 0% causes the different colors to be illuminated at different intensities, allowing virtually any color to be displayed.

10 Pmod Ports

The Pmod ports are arranged in a 2×6 right-angle, and are 100-mil female connectors that mate with standard 2×6 pin headers. Each 12-pin Pmod port provides two 3.3V VCCsignals (pins 6 and 12), two Ground signals (pins 5 and 11), and eight logic signals, as shown in Figure 10.1. The VCC and Ground pins can deliver up to 1A of current. Pmod data signals are not matched pairs, and they are routed using best-available tracks without impedance control or delay matching. Pin assignments for the Pmod I/O connected to the FPGA are shown in Table 5.

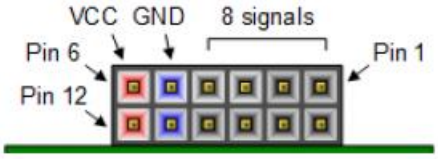


Figure 10.1 Pmod Connectors; Front View, as Loaded on PCB

Pmod JA	Pmod JB	Pmod JC	Pmod JD	Pmod XDAC
JA1: C17	JB1: D14	JC1: K1	JD1: H4	JXADC1: A13 (AD3P)
JA2: D18	JB2: F16	JC2: F6	JD2: H1	JXADC2: A15 (AD10P)
JA3: E18	JB3: G16	JC3: J2	JD3: G1	JXADC3: B16 (AD2P)
JA4: G17	JB4: H14	JC4: G6	JD4: G3	JXADC4: B18 (AD11P)
JA7: D17	JB7: E16	JC7: E7	JD7: H2	JXADC7: A14 (AD3N)
JA8: E17	JB8: F13	JC8: J3	JD8: G4	JXADC8: A16 (AD10N)
JA9: F18	JB9: G13	JC9: J4	JD9: G2	JXADC9: B17 (AD2N)

Table 10.1. Nexys A7 Pmod Pin Assignment

Digilent produces a large collection of Pmod accessory boards that can attach to the Pmod expansion connectors to add ready-made functions like A/D's, D/A's, motor drivers, sensors, as well as other functions.
See http://www.digilentinc.com/ for more information.

10.1 Dual Analog/Digital Pmod

The on-board Pmod expansion connector labeled "JXADC" is wired to the auxiliary analog input pins of the FPGA. Depending on the configuration, this connector can be used to input differential analog signals to the analog-to-digital converter inside of the Artix-7 (XADC). Any or all pairs in the connector can be configured either as analog input or digital input-output.

The Dual Analog/Digital Pmod on the Nexys A7 differs from the rest in the routing of its traces. The eight data signals are grouped into four pairs, with the pairs routed closely coupled for better analog noise immunity. Furthermore, each pair has a partially loaded anti-alias filter laid out on the PCB. The filter does not have capacitors C60-C63. In designs where such filters are desired, the capacitors can be manually loaded by the user.

NOTE: The coupled routing and the anti-alias filters might limit the data speeds when used for digital signals.

The XADC core within the Artix-7 is a dual channel 12-bit analog-to-digital converter capable of operating at 1 MSPS. Either channel can be driven by any of the auxiliary analog input pairs connected to the JXADC header. The XADC core is controlled and accessed from a user design via the Dynamic Reconfiguration Port (DRP). The DRP also provides access to voltage monitors that are present on each of the FPGA's power rails, and a temperature sensor

that is internal to the FPGA. For more information on using the XADC core, refer to the Xilinx document titled "7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter."

11 MicroSD Slot

The Nexys A7 provides a microSD slot for both FPGA configuration and user access. The on-board Auxiliary Function microcontroller shares the SD card bus with the FPGA. Before the FPGA is configured the microcontroller must have access to the SD card via SPI. Once a bit file is downloaded to the FPGA (from any source), the microcontroller power cycles the SD slot and relinquishes control of the bus. This enables any SD card in the slot to reset its internal state machines and boot up in SD native bus mode. All of the SD pins on the FPGA are wired to support full SD speeds in native interface mode, as shown in Figure 11.1. The SPI is also available, if needed. Once control over the SD bus is passed from the microcontroller to the FPGA, the SD_RESET signal needs to be actively driven low by the FPGA to power the microSD card slot. For information on implementing an SD card controller, refer to the SD card specification available at http://www.sdcard.org/

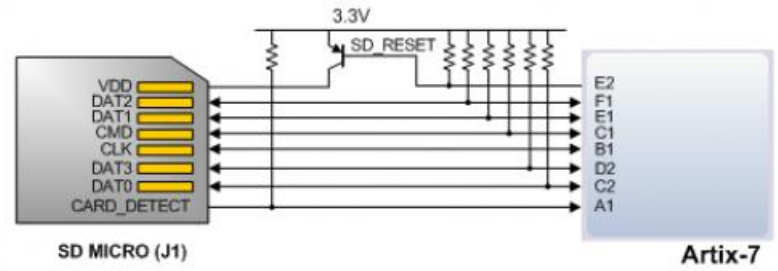


Figure 11.1 Artix-7 microSD Card Connector Interface (PIC24 Connections not Shown)

12 Temperature Sensor

The Nexys A7 includes an Analog Device ADT7420 temperature sensor. The sensor provides up to 16-bit resolution with a typical accuracy better than 0.25 degrees Celsius. The interface between the temperature sensor and FPGA is shown in Figure 12.1.

Figure 12.1 Temperature Sensor Interface

12.1 I²C Interface

The ADT7420 chip acts as a slave device using the industry standard I²C communication scheme. To communicate with ADT7420 chip, the I²C master must specify a slave address (0x4B) and a flag indicating whether the communication is a read (1) or a write (0). Once specifications are made for communication, a data transfer takes place. For ADT7420, the data transfer should consist of the address of the desired device register followed by the data to be written to the specified register. To read from a register, the master must write the desired register address to the ADT7420, then send an I²C restart condition, and send a new read request to the ADT7420. If the master does not generate a restart condition prior to attempting the read, the value written to the address register will be reset to 0x00. As some registers store 16-bit values as 8-bit register pairs, the ADT7420 will automatically increment the address register of the device when accessing certain registers, such as the temperature registers and the threshold registers. This allows for the master to use a single read or write request to access both the low and high bytes of these registers. A complete listing of registers and their behavior can be found in the ADT7420 datasheet available on the Analog Devices website.

12.2 Open Drain Outputs

The ADT7420 provides two open drain output signals to indicate when pre-set temperature thresholds are reached. If the temperature leaves a range defined by registers TLOW (0x06:0x07) and THIGH (0x04:0x05), the INT pin can be driven low or high based upon the configuration of the device. Similarly, the CT pin can be driven low or high if the temperature exceeds a critical threshold defined in TCRIT (0x08:0x09). Both of these pins need internal FPGA pull-ups when used.

For details on the electrical specifications and configuration of the INT and CT pins, refer to the ADT7420 datasheet.

12.3 Quick Start Operation

When the ADT7420 is powered up, it is in a mode that can be used as a simple temperature sensor without any initial configuration. By default, the device address register points to the temperature MSB register, so a two byte read without specifying a register will read the value of the temperature register from the device. The first byte read back will be the most significant byte (MSB) of the temperature data, and the second will be the least significant byte (LSB) of the data. These two bytes form a two's complement 16-bit integer. If the result is shifted to the right three bits and multiplied by 0.0625, the resulting signed floating point value will be a temperature reading in degrees Celsius.

For information on reading and writing to the other registers of the device, as well as notes on the accuracy of the temperature measurements, refer to the ADT7420 datasheet.

13 Accelerometer

The Nexys A7 includes an Analog Device ADXL362 accelerometer. The ADXL362 is a 3-axis MEMS accelerometer that consumes less than 2µA at a 100Hz output data rate and 270nA when in motion triggered wake-up mode. Unlike accelerometers that use power duty cycling to achieve low power consumption, the ADXL362 does not alias input signals by under-sampling; it samples the full bandwidth of the sensor at all data rates. The ADXL362 always provides 12-bit output resolution; 8-bit formatted data is also provided for more efficient single-byte transfers when a lower resolution is sufficient. Measurement ranges of ±2 g, ±4 g, and ±8 g are available with a resolution of 1 mg/LSB on the ±2 g range. The FPGA can talk with the ADXL362 via SPI interface. While the ADXL362 is in

Measurement Mode, it continuously measures and stores acceleration data in the X-data, Y-data, and Z-data registers. The interface between the FPGA and accelerometer can be seen in Figure 13.1.

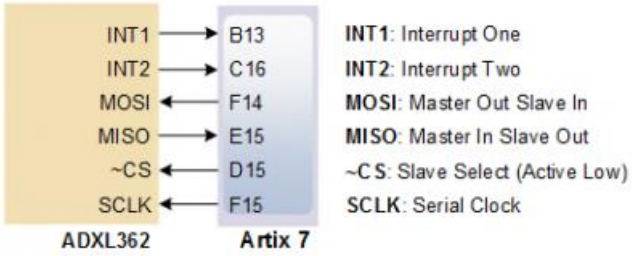


Figure 13.1 Accelerometer Interface

13.1 SPI Interface

The ADXL362 acts as a slave device using an SPI communication scheme. The recommended SPI clock frequency ranges from 1 MHz to 5 MHz. The SPI operates in SPI mode 0 with CPOL = 0 and CPHA = 0. All communications with the device must specify a register address and a flag that indicate whether the communication is a read or a write. Actual data transfer always follows the register address and communication flag. Device configuration can be performed by writing to the control registers within the accelerometer. Access accelerometer data by reading the device registers.

For a full list of registers, their functionality, and communication specifications, refer to the ADXL362 datasheet[v].

13.2 Interrupts

Several of the built-in functions of the ADXL362 can trigger interrupts that alert the host processor of certain status conditions. Interrupts can be mapped to either (or both) of two interrupt pins (INT1, INT2). Both of these pins require internal FPGA pull-ups when used. For more details about the interrupts, see the ADXL362 datasheet.

14 Microphone

The Nexys A7 board includes an omnidirectional MEMS microphone. The microphone uses an Analog Device ADMP421 chip which has a high signal to noise ratio (SNR) of 61dBA and high sensitivity of -26 dBFS. It also has a flat frequency response ranging from 100Hz to 15 kHz. The digitized audio is output in the pulse density modulated (PDM) format. The component architecture is shown in Figure 14.1.

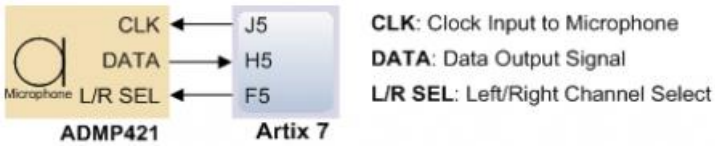


Figure 14.1 Microphone Block Diagram

14.1 Pulse Density Modulation (PDM)

PDM data connections are becoming more and more popular in portable audio applications, such as cellphones and tablets. With PDM, two channels can be transmitted with only two wires. The frequency of a PDM signal usually falls in the range of 1 MHz to 3 MHz. In a PDM bitstream, a 1 corresponds to a positive pulse and a 0 corresponds to a negative pulse. A run consisting of all '1's would correspond to the maximum positive value and a run of '0's would correspond to the minimum amplitude value. Figure 14.1.1 shows how a sine wave is represented in PDM signal.

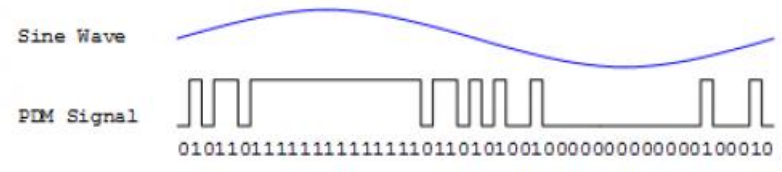


Figure 14.1.1 PDM Representation of a Sine Wave

A PDM signal is generated from an analog signal through a process called delta-sigma modulation. A simple idealized circuit of delta-sigma modulator is shown in Figure 14.1.2.

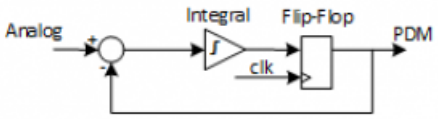


Figure 14.1.2 Simple Delta-Sigma Modulator Circuit

Sum	Integrator Out	Flip-flop Output
0.4-0=0.4	0+0.4=0.4	0
0.4-0=0.4	0.4+0.4=0.8	1
0.4-1=-0.6	0.8-0.6=0.2	0
0.4-0=0.4	0.2+0.4=0.6	1
0.4-1=-0.6	0.6-0.6=0	0
0.4-0=0.4	0+0.4=0.4	0
0.4-0=0.4	0.4+0.4=0.8	1

Table 14.1.2. Sigma delta modulator with a 0.4Vdd input.

To keep things simple, assume that the analog input and digital output have the same voltage range 0~Vdd. The input of the flip-flop acts like a comparator (any signal above Vdd/2 is considered as '1' and any input bellow Vdd/2 is considered '0'). The input of the integral circuit is the difference of the input analog signal and the PDM signal of the previous clock cycle. The integral circuit then integrates both of these inputs, and the output of the integral circuit is sampled by a D-Flip-flop. Table 6 shows the function of the delta-sigma modulator with an input of 0.4Vdd.

Note that the average of the flip-flop output equals the value of the input analog signal. So in order to get the value of analog input, all that is needed is a counter that counts the '1's for a certain period of time.

14.2 Microphone Digital Interface Timing

The clock input of the microphone can range from 1 MHz to 3.3 MHz based on the sampling rate and data precision requirement of the applications. The L/R Select signal must be set to a valid level, depending on which edge of the clock the data bit will be read. A low level on L/RSEL makes data available on the rising edge of the clock, while a high level corresponds to the falling edge of the clock, as shown in Figure 14.2.1.

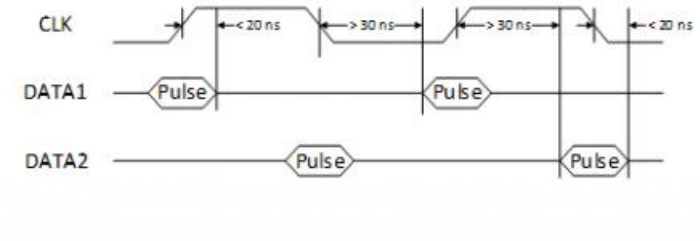


Figure 14.2.1 PDM Timing Diagram

The typical value of the clock frequency is 2.4 MHz. Assuming that the application requires 7-bit precision and 24 KHz, there can be two counters that count 128 samples at 12 KHz, as shown in Figure 14.2.2.

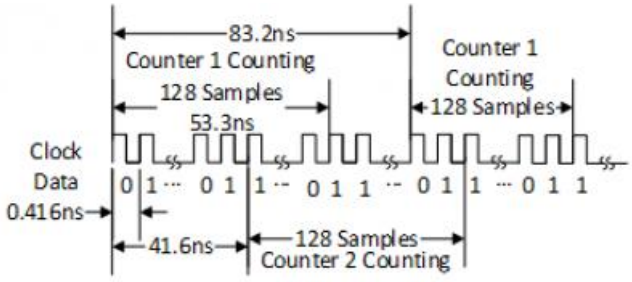


Figure 14.2.2 Sampling PDM with Two Counters

15 Mono Audio Output

The on-board audio jack (J8) is driven by a Sallen-Key Butterworth Low-pass 4th Order Filter that provides mono audio output. The circuit of the low-pass filter is shown in Figure 15.1. The input of the filter (AUD_PWM) is connected to the FPGA pin A11. A digital input will typically be a pulse-width modulated (PWM) or pulse density modulated (PDM) open-drain signal produced by the FPGA. The signal needs to be driven low for logic '0' and left in high-impedance for logic '1'. An on-board pull-up resistor to a clean analog 3.3V rail will establish the proper voltage for logic '1'. The low-pass filter on the input will act as a reconstruction filter to convert the pulse-width modulated digital signal into an analog voltage on the audio jack output.

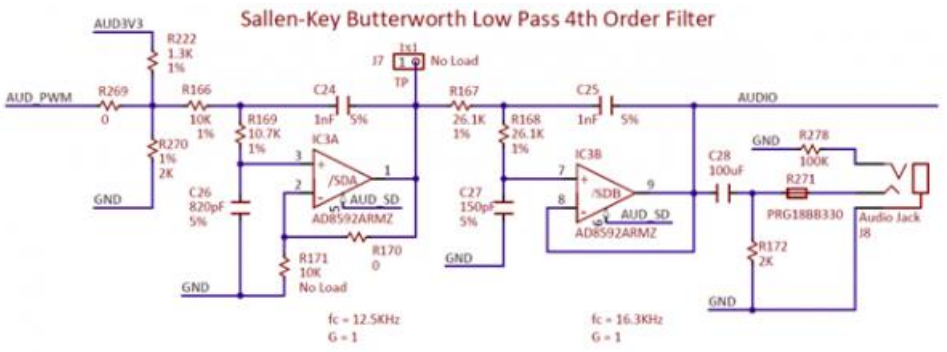


Figure 15.1 Sallen-Key Butterworth Low-Pass 4th Order Filter

The frequency response of SK Butterworth Low-Pass Filter is shown in Figure 15.2. The AC analysis of the circuit is done using NI Multisim 12.0.

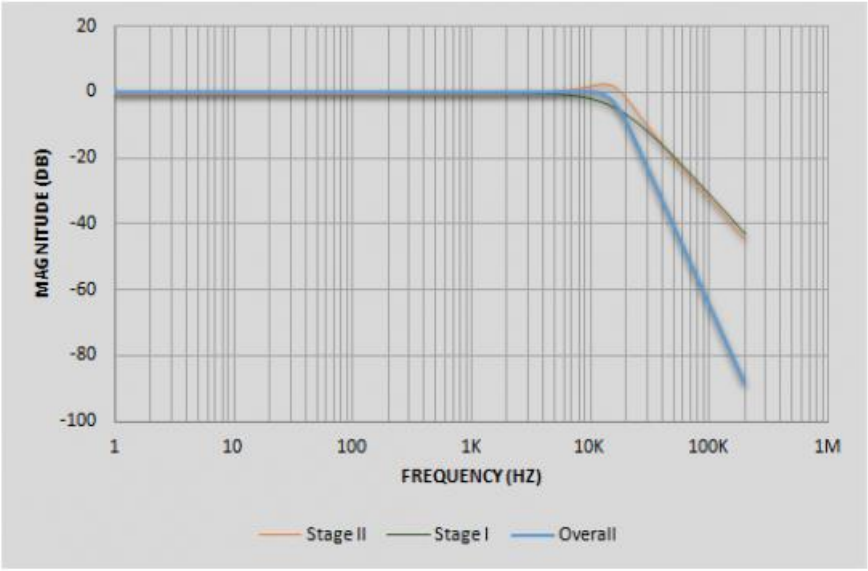


Figure 15.2 SK Butterworth Low-Pass Filter Frequency Response

15.2 Pulse-Width Modulation

A pulse-width modulated (PWM) signal is a chain of pulses at some fixed frequency, with each pulse potentially having a different width. This digital signal can be passed through a simple low-pass filter that integrates the digital waveform to produce an analog voltage proportional to the average pulse-width over some interval (the interval is

determined by the 3dB cut-off frequency of the low-pass filter and the pulse frequency). For example, if the pulses are high for an average of 10% of the available pulse period, then an integrator will produce an analog value that is 10% of the Vdd voltage. Figure 15.1.1 shows a waveform represented as a PWM signal.

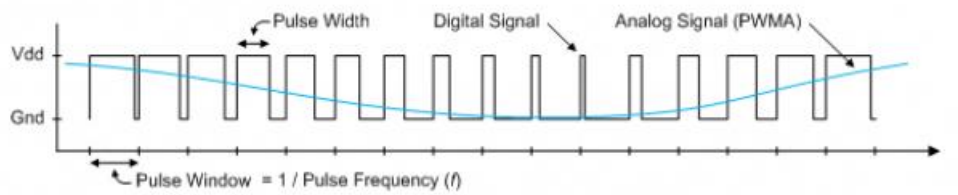


Figure 15.1.1 Simple Waveform Represented as PWM

The PWM signal must be integrated to define an analog voltage. The low-pass filter 3dB frequency should be an order of magnitude lower than the PWM frequency, so that signal energy at the PWM frequency is filtered from the signal. For example, if an audio signal must contain up to 5 KHz of frequency information, then the PWM frequency should be at least 50 KHz (and preferably even higher). In general, in terms of analog signal fidelity, the higher the PWM frequency, the better. Figure 15.1.2 shows a representation of a PWM integrator producing an output voltage by integrating the pulse train. Note the steady-state filter output signal amplitude ratio to Vdd is the same as the pulse-width duty cycle (duty cycle is defined as pulse-high time divided by pulse-window time).

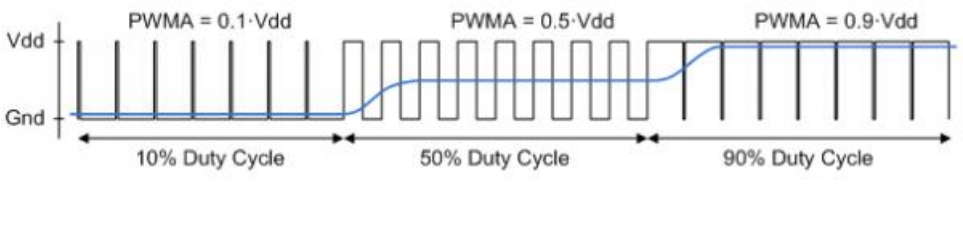


Figure 15.1.2 Representation of a PWM Integrator Producing an Output Voltage by Integrating the Pulse Train

Built-In Self-Test

A demonstration configuration is loaded into the Quad-SPI flash device on the Nexys A7 board during manufacturing. The source code and prebuilt bitstream for this design are available for download from the Digilent website. If the demo configuration is present in the flash and the Nexys A7 board is powered on in SPI mode, the demo project will allow basic hardware verification. Here is an overview of how this demo drives the different onboard components:

- The user LEDs are illuminated when the corresponding user switch is placed in the on position.
- The tri-color LEDs are controlled by some of the user buttons. Pressing BTNL, BTNC, or BTNR causes them to illuminate either red, green, or blue, respectively. Pressing BTND causes them to begin cycling through many colors. Repeatedly pressing BTND will turn the two LEDs on or off.
- Pressing BTNU will trigger a 5 second recording from the onboard PDM microphone. This recording is then immediately played back on the mono audio out port. The status of the recording and playback is displayed on the user LEDs. The recording is saved in the DDR2 memory.

- The VGA port displays feedback from the onboard microphone, temperature sensors, accelerometer, RGB LEDs, and USB Mouse.
- Connecting a mouse to the USB-HID Mouse port will allow the pointer on the VGA display to be controlled. Only mice compatible with the Boot Mouse HID interface are supported.
- The seven-segment display will display a moving snake pattern.

All Nexys A7 boards are 100% tested during the manufacturing process. If any device on the Nexys A7 board fails test or is not responding properly, it is likely that damage occurred during transport or during use. Typical damage includes stressed solder joints and contaminants in switches and buttons resulting in intermittent failures. Stressed solder joints can be repaired by reheating and reflowing solder and contaminants can be cleaned with off-the-shelf electronics cleaning products. If a board fails test within the warranty period, it will be replaced at no cost. Contact Digilent for more details.

[i] Zynq-7000 SoC and 7 Series Devices Memory Interface Solutions from Xilinx
[ii] Spansion S25FL032P_00 Datasheet
[iii] 7-Series FPGAs Configuration User Guide from Xilinx
[iv] SMSC LAN8720A Datasheet from Microchip
[v] ADXL362 Product Page from Analog Devices

8.2. SN74LS07

TEXAS INSTRUMENTS
SN74LS07
SDLS021D – MAY 1990 – REVISED APRIL 2016

SN74LS07 Hex Buffers and Drivers With Open-Collector High-Voltage Outputs

1 Features

- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Driver for Indicator Lamps and Relays

2 Applications

- AV Receivers
- Audio Docks: Portable
- Blu-ray Players and Home Theaters
- MP3 Players or Recorders
- Personal Digital Assistants (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid-State Drives (SSD): Client and Enterprise
- TVs: LCD, Digital, and High-Definition (HDTV)
- Tablets: Enterprise
- Video Analytics: Server
- Wireless Headsets, Keyboards, and Mice

3 Description

These hex buffers and drivers feature high-voltage open-collector outputs to interface with high-level circuits or for driving high-current loads. They are also characterized for use as buffers for driving TTL inputs. The SN74LS07 devices have a rated output voltage of 30 V. The maximum sink current is 40 mA.

These circuits are compatible with most TTL families. Inputs are diode-clamped to minimize transmission-line effects, which simplifies design. Typical power dissipation is 140 mW, and average propagation delay time is 12 ns.

Device Information(1)

PART NUMBER	PACKAGE (PINS)	BODY SIZE (NOM)
SN74LS07D	SOIC (14)	8.65 mm × 3.90 mm
SN74LS07DB	SSOP (14)	6.20 mm × 5.30 mm
SN74LS07N	PDIP (14)	19.30 mm × 6.35 mm
SN74LS07NS	SO (14)	10.30 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

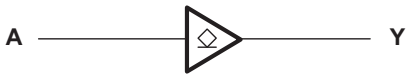


Table of Contents

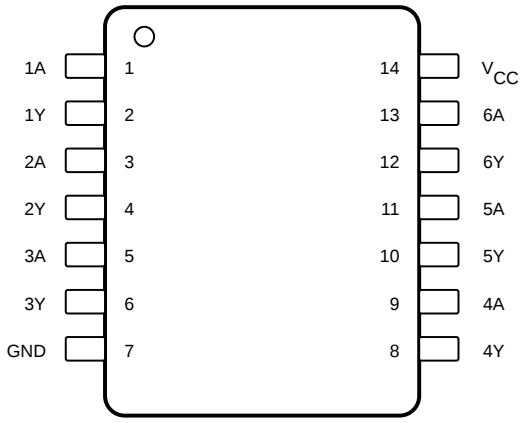
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2004) to Revision D	Page
• Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted SN54LS07 and SN74LS17 from the data sheet because they are obsolete and no longer supplied	1
• Deleted *Ordering Information* table.	1

5 Pin Configuration and Functions

D, DB, N, or NS Packages
14-Pin SOIC, SSOP, PDIP, SO
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1A	I	Input 1
2	1Y	O	Output 1
3	2A	I	Input 2
4	2Y	O	Output 2
5	3A	I	Input 3
6	3Y	O	Output 3
7	GND	—	Ground pin
8	4Y	O	Output 4
9	4A	I	Input 4
10	5Y	O	Output 5
11	5A	I	Input 5
12	6Y	O	Output 6
13	6A	I	Input 6
14	V_{CC}	—	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage		7	V
V_I	Input voltage(2)		7	V
V_O	Output voltage(2)(3)		30	V
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) This is the maximum voltage that should be applied to any output when it is in the off state.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage			30	V
I_{OL}	Low-level output current			40	mA
T_A	Operating free-air temperature	0		70	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LS07				UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.2	97.4	50.2	82.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	49.8	37.5	40.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.7	44.5	30	41.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.9	16.5	22.3	12.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.4	44	29.9	41.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = MIN, I_I = –12 mA				–1.5	V
I_{OH}	V_{CC} = MIN, V_{IH} = 2 V	V_{OH} = 30 V			0.25	mA
V_{OL}	V_{CC} = MIN, V_{IL} = 0.8 V	I_{OL} = 16 mA			0.4	V
		I_{OL} = MAX[2]			0.7	
I_I	V_{CC} = MAX, V_I = 7 V				1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V				20	µA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V				–0.2	mA
I_{CCH}	V_{CC} = MAX				14	mA
I_{CCL}	V_{CC} = MAX				45	mA

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) I_{OL} = 40 mA

6.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 110 Ω, C_L = 15 pF		6	10	ns
t_{PHL}					19	30	

6.7 Typical Characteristics

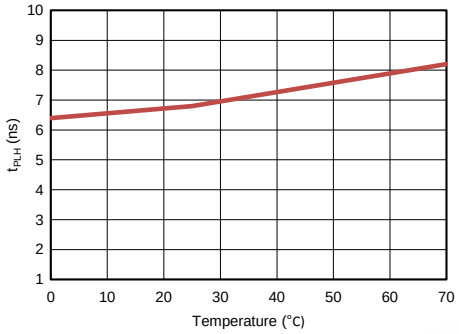
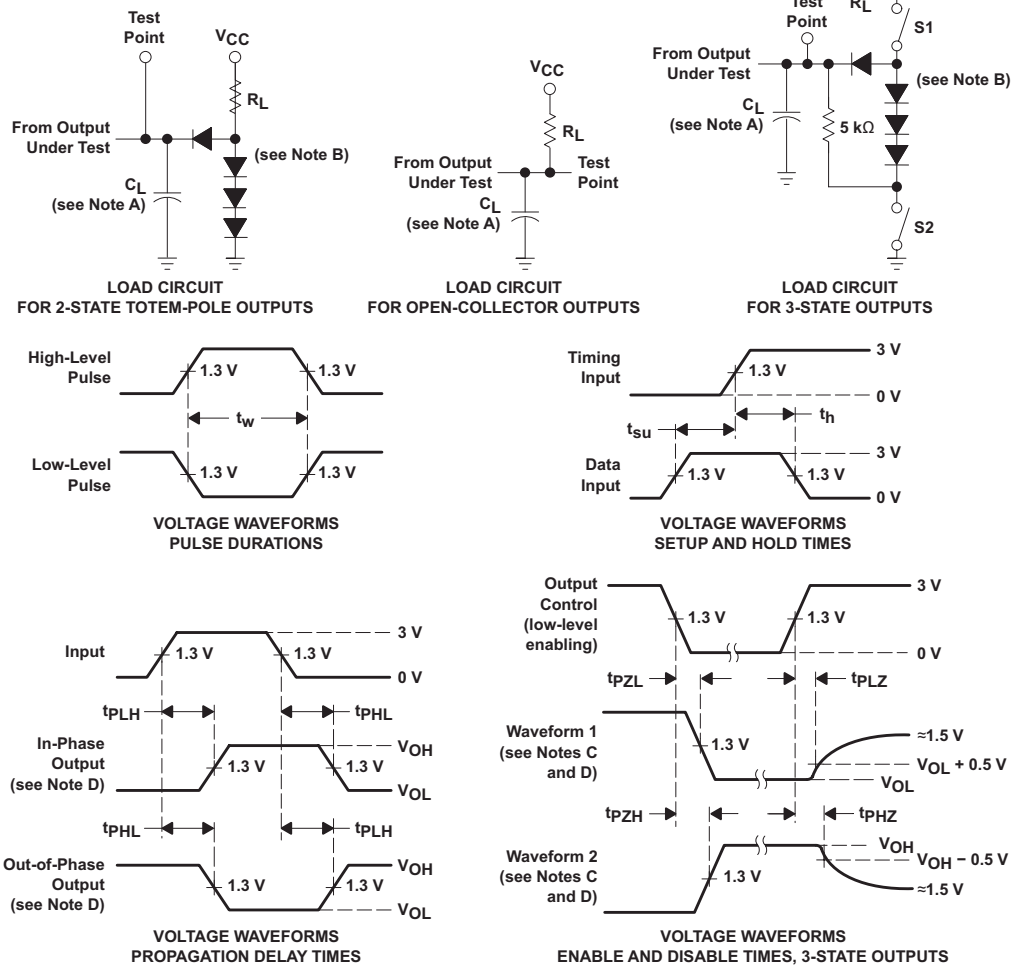


Figure 1. t_{PLH} vs. Temperature

7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. All diodes are 1N3064 or equivalent.

C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.

E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \le 1.5$ ns, $t_f \le 2.6$ ns.

G. The outputs are measured one at a time, with one input transition per measurement.

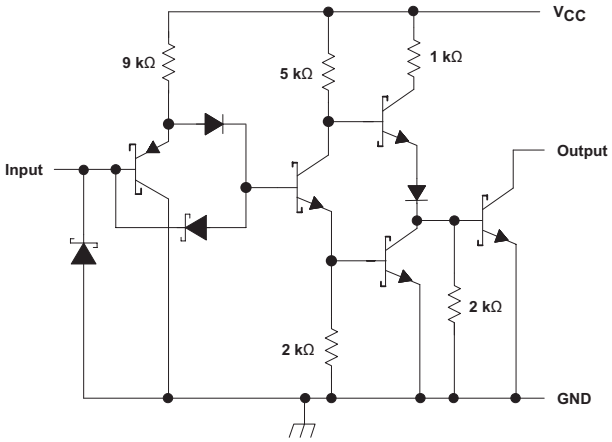
Figure 2. Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Overview

The outputs of the SN74LS07 device are open-collector and can be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current for the SN74LS07 is 40 mA.

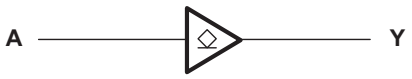
Inputs can be driven from 2.5-V, 3.3-V (LVTTL), or 5-V (CMOS) devices. This feature allows the use of this device as translators in a mixed-system environment.



Resistor values shown are nominal.

Figure 3. Schematic (Gate)

8.2 Functional Block Diagram



8.3 Feature Description

- Allows for up translation
  - Inputs accept voltages to 5.25 V
  - Outputs accept voltages to 30 V
- High Sink-Current Capability
  - Up to 40 mA

8.4 Device Functional Modes

Table 1 lists the functions of this device.

Table 1. Function Table

INPUT A	OUTPUT Y
H	Hi-Z
L	L

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LS07 device is a high-drive, open-drain CMOS device that can be used for a multitude of buffer-type functions. It can produce 40 mA of drive current at 5 V. Therefore, this device is ideal for driving multiple inputs. The inputs are 5.25-V tolerant and outputs are 30-V tolerant.

9.2 Typical Application

Multiple channels of the SN74LS07 device can be used to create a positive AND logic function, as shown in Figure 4. Additionally, the SN74LS07 device can be used to drive an LED by sinking up to 40 mA, which may be more than the previous stage can sink.

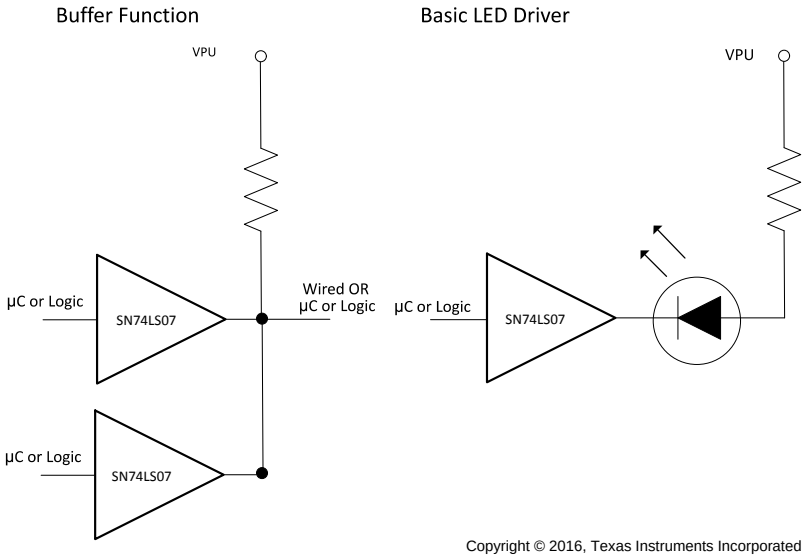


Figure 4. Typical Application Diagram

9.2.1 Design Requirements

Ensure that the inputs are in a known state as defined by V_{IH} and V_{IL} noted in *Recommended Operating Conditions*, or else the outputs may be in an unknown state.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For specified high and low level, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.25 V.
2. Recommend Output Conditions
   - Load currents must not exceed 40 mA per output.
   - Outputs must not be pulled above 30 V.

Typical Application (continued)

9.2.3 Application Curve

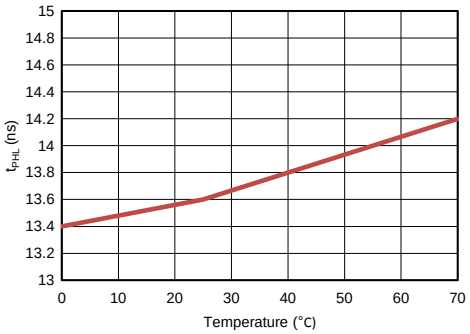


Figure 5. t_{PHL} vs Temperature

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating indicated in *Recommended Operating Conditions*.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor; if there are multiple V_{CC} pins, then TI recommends either a 0.01-µF or 0.022-µF capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-µF and a 1-µF capacitor are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 6 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

11.2 Layout Example

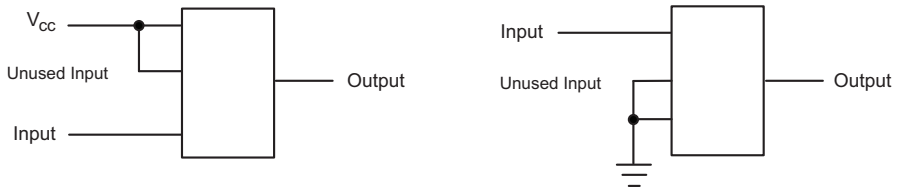


Figure 6. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the followign:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS07D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS07	Samples
SN74LS07DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS07	Samples
SN74LS07DBRG4	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS07	Samples
SN74LS07DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS07	Samples
SN74LS07DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS07	Samples
SN74LS07N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS07N	Samples
SN74LS07NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS07	Samples
SN74LS07NSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS07	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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10-Dec-2020

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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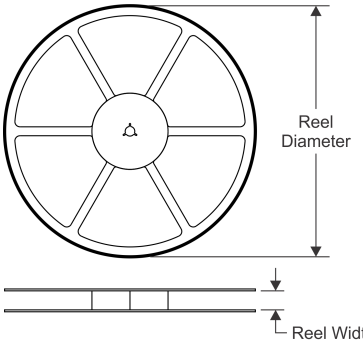
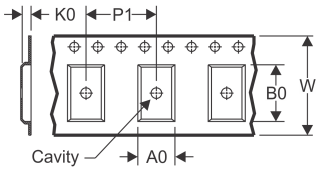
19-Jun-2021

TAPE AND REEL INFORMATION

REEL DIMENSIONS

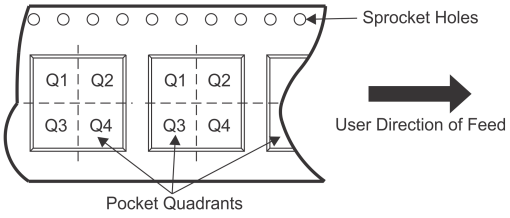


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS07DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LS07DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS07NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

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PACKAGE MATERIALS INFORMATION

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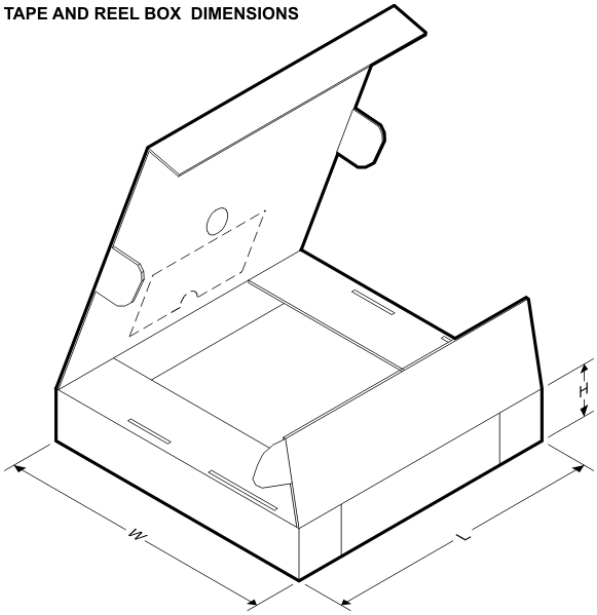
TAPE AND REEL BOX DIMENSIONS



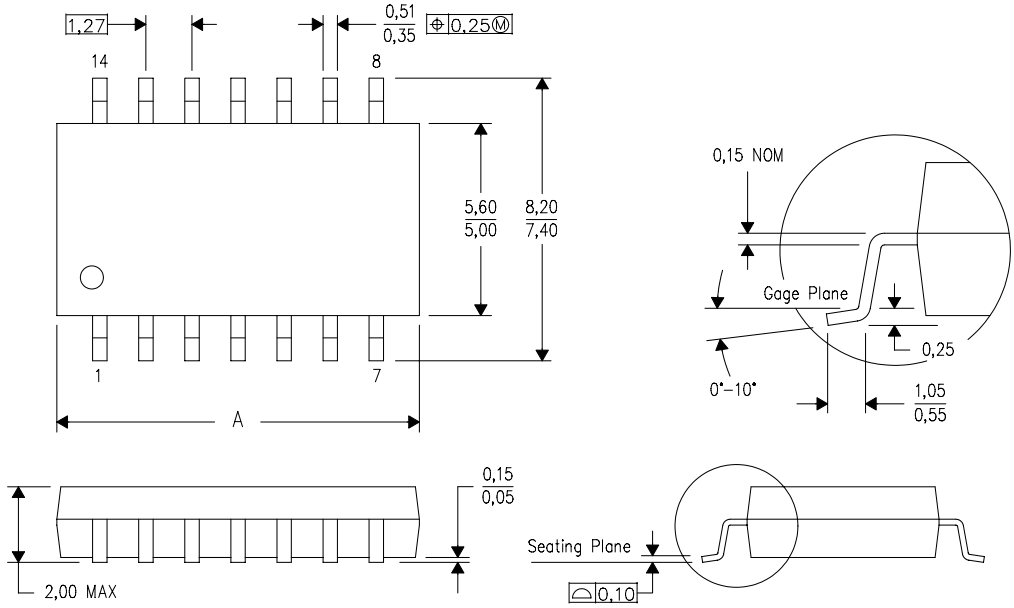
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS07DBR	SSOP	DB	14	2000	853.0	449.0	35.0
SN74LS07DR	SOIC	D	14	2500	853.0	449.0	35.0
SN74LS07NSR	SO	NS	14	2000	367.0	367.0	38.0

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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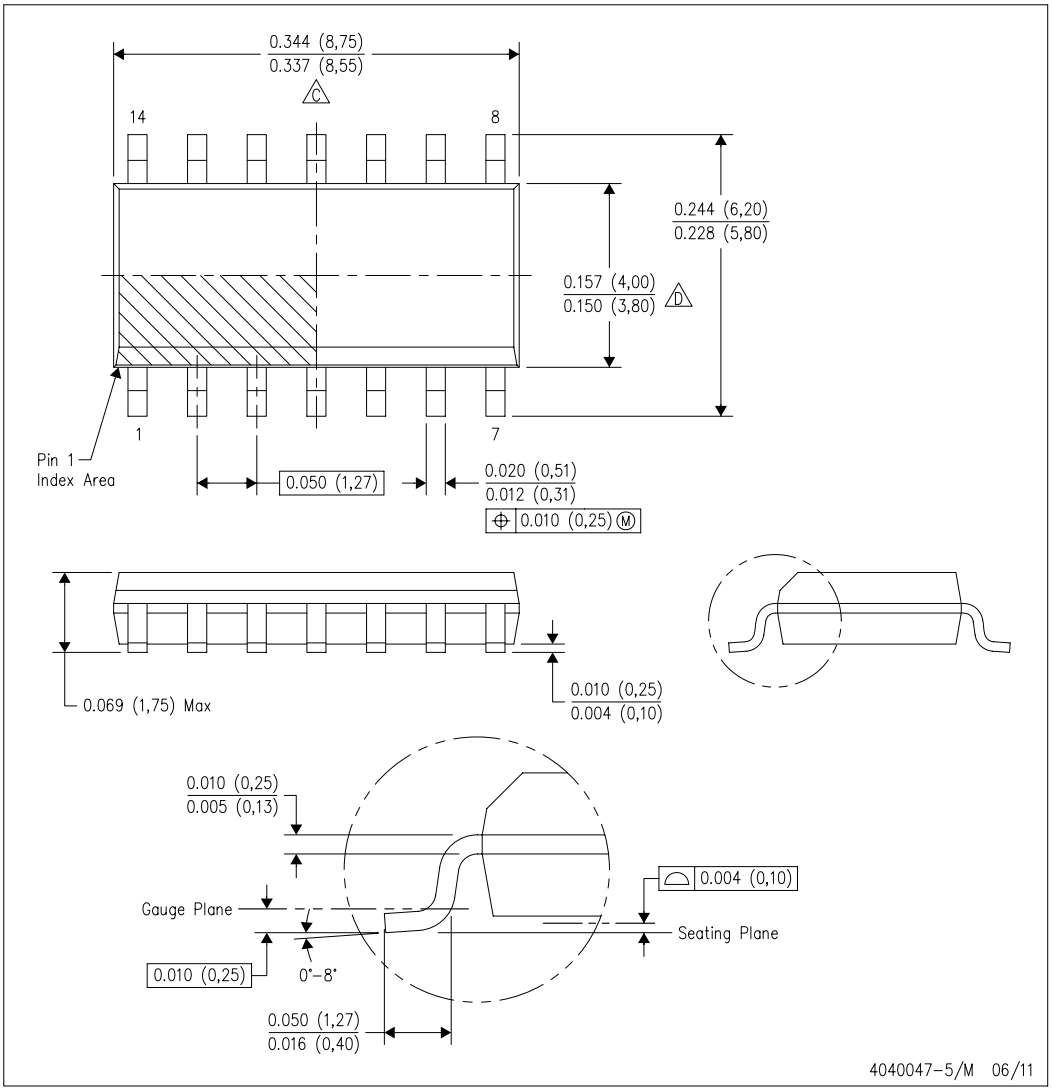
MECHANICAL DATA

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

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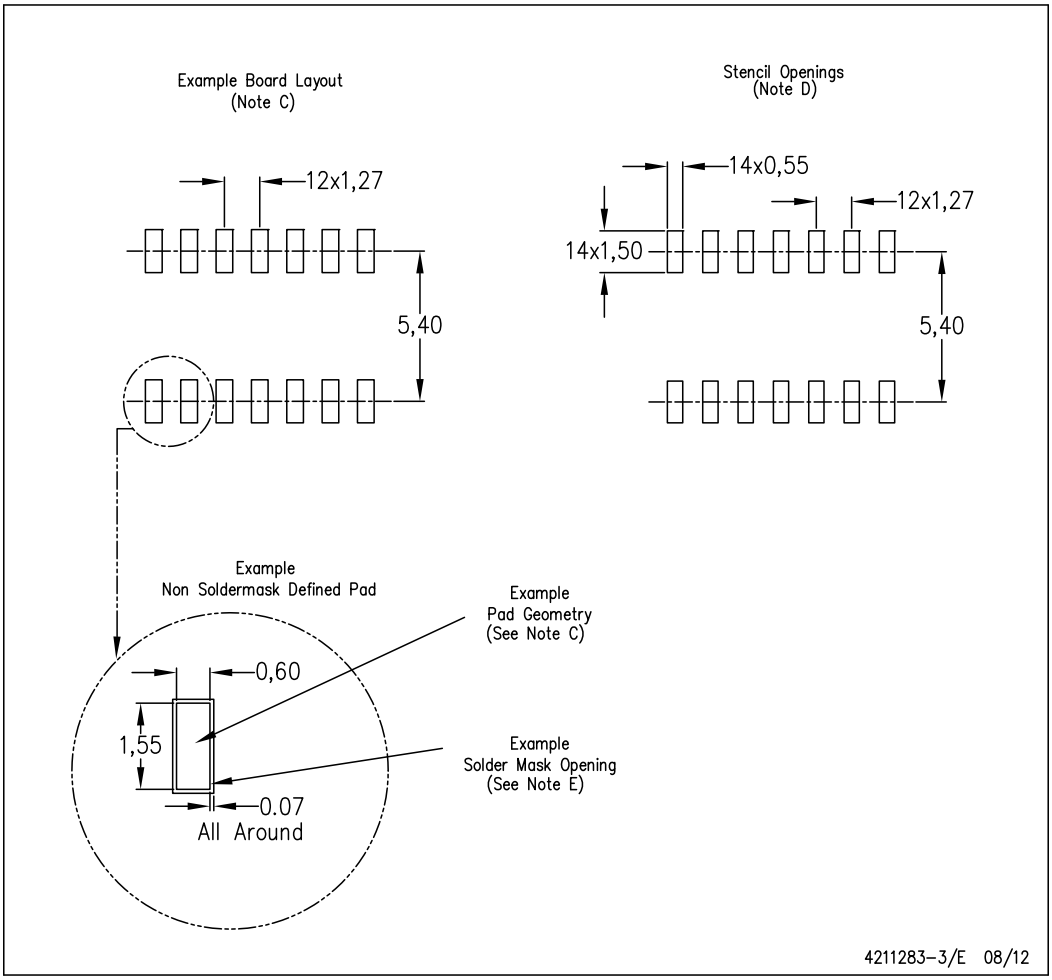
LAND PATTERN DATA

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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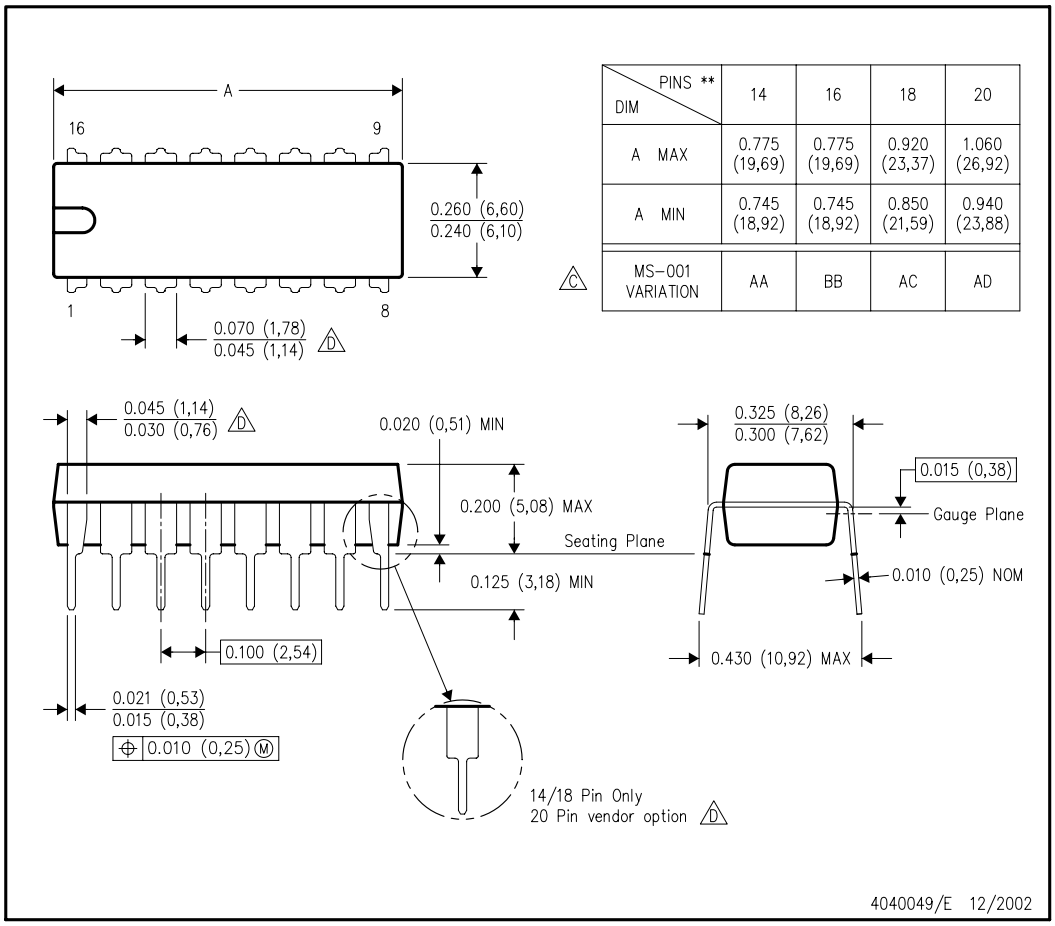
MECHANICAL DATA

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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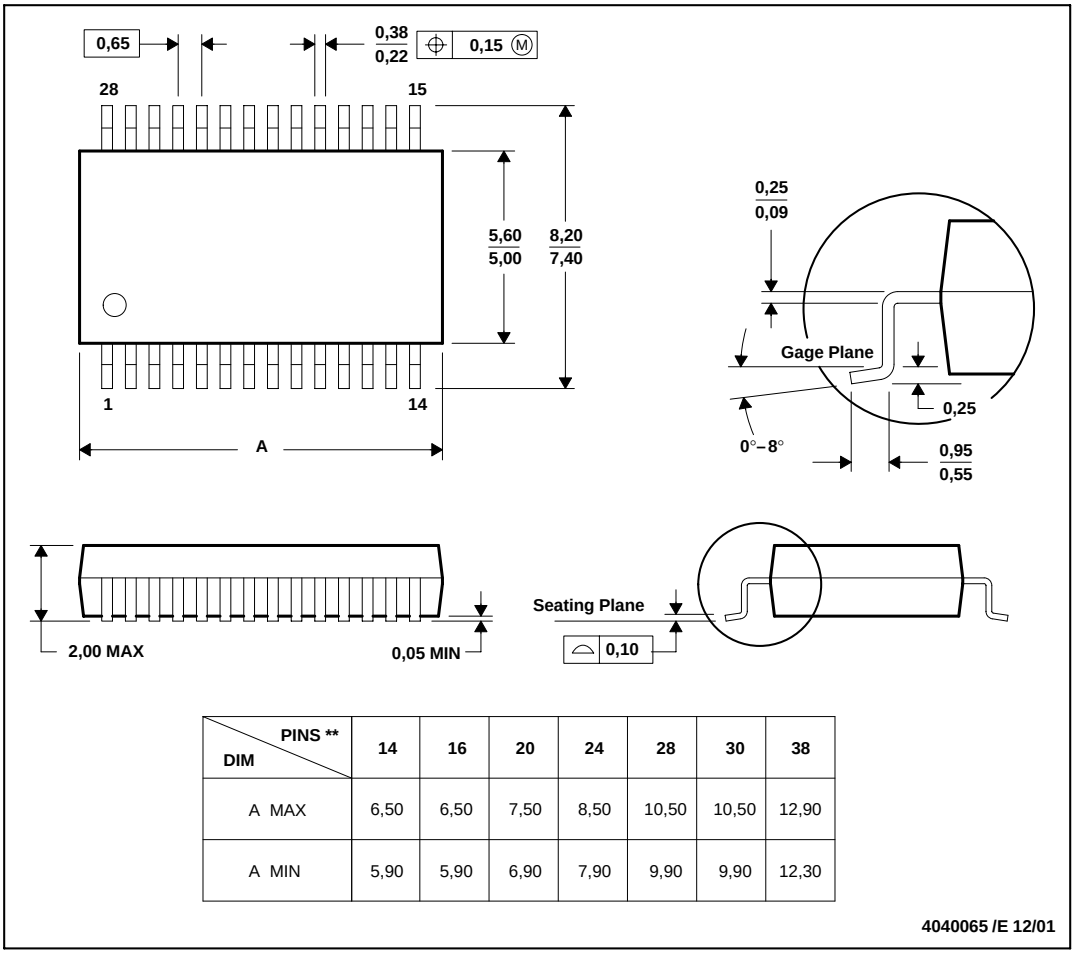
MECHANICAL DATA

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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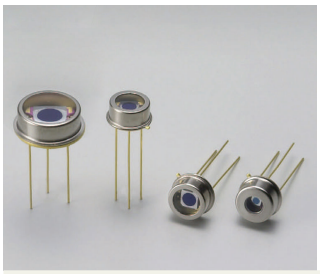
Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

8.3. S3071

HAMAMATSU
PHOTON IS OUR BUSINESS



Si PIN photodiodes

S3071 S3072 S3399 S3883

Large area, high-speed Si PIN photodiodes

The S3071, S3072, S3399 and S3883 are Si PIN photodiodes having a relatively large photosensitive area from ϕ1.5 to ϕ5.0 mm yet they offer excellent frequency response from 40 to 300 MHz. These photodiodes are suitable for FSO (free space optics) and high-speed pulsed light detection.

Features

- **Photosensitive area size**
  S3071: ϕ5.0 mm
  S3072: ϕ3.0 mm
  S3399: ϕ3.0 mm
  S3883: ϕ1.5 mm
- **Cutoff frequency**
  S3071: 40 MHz (VR=24 V)
  S3072: 45 MHz (VR=24 V)
  S3399: 100 MHz (VR=10 V)
  S3883: 300 MHz (VR=20 V)
- **High reliability: TO-5/8 metal package**

Applications

- **FSO**
- **High-speed pulsed light detection**

Structure / Absolute maximum ratings

Type no.	Dimensional outline/ Window material*1	Package	Photosensitive area size (mm)	Effective photosensitive area (mm²)	Absolute maximum ratings: Reverse voltage VR max. (V)	Power dissipation Pd (mW)	Operating temperature Topr (°C)	Storage temperature Tstg (°C)
S3071	(1)/K	TO-8	ϕ5.0	19.6	50	50	-40 to +100	-55 to +125
S3072	(2)/K	TO-5	ϕ3.0	7.0				
S3399	(3)/K		ϕ3.0	7.0	30			
S3883	(4)/K		ϕ1.5	1.7				

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.
*1: Window material K=borosilicate glass

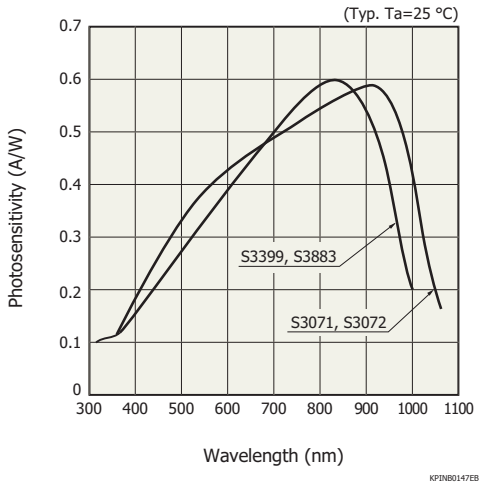
Electrical and optical characteristics (Typ. Ta=25 °C, unless otherwise noted)

Type no.	Spectral response range λ (nm)	Peak sensitivity wavelength λp (nm)	Photosensitivity S (A/W): λp	660 nm	780 nm	830 nm	Short circuit current Isc 100 lx (μA)	Dark current ID (nA): Typ.	Max.	Temp. coefficient of ID TCID (times/°C)	Cutoff frequency fc RL=50 Ω (MHz)	Terminal capacitance Ct f=1 MHz (pF)	Noize equivalent power NEP λ=λp (W/Hz^1/2)
S3071	320 to 1060	920	0.6	0.47	0.54	0.56	17	0.5*2	10*2	1.15	40*2	18*2	2.1×10^{-14} *2
S3072							6.5	0.3*2	10*2		45*2	7*2	1.6×10^{-14} *2
S3399	320 to 1000	840	0.6	0.45	0.58	0.6	5.6	0.1*3	1.0*3	1.12	100*3	20*3	9.4×10^{-15} *3
S3883							1.4	0.05*4	1.0*4		300*4	6*4	6.7×10^{-15} *4

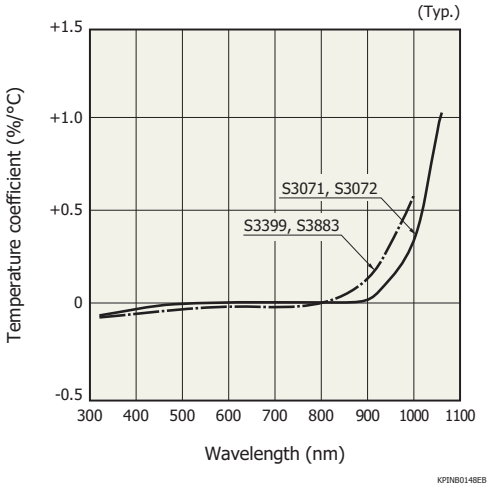
*2: VR=24 V
*3: VR=10 V
*4: VR=20 V

Si PIN photodiodes | **S3071, S3072, S3399, S3883**

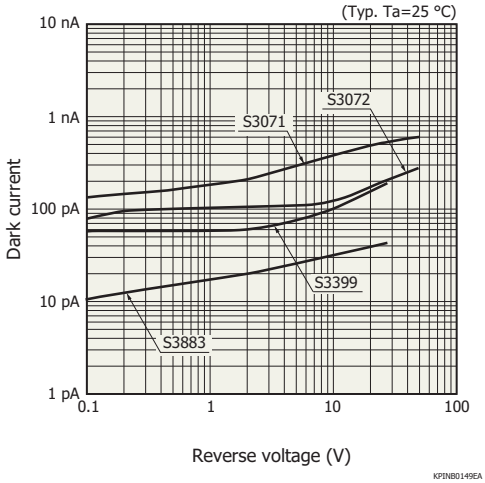
Spectral response



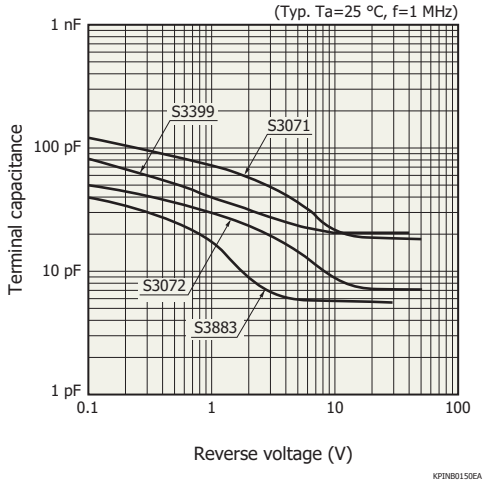
Photosensitivity temperature characteristics



Dark current vs. reverse voltage

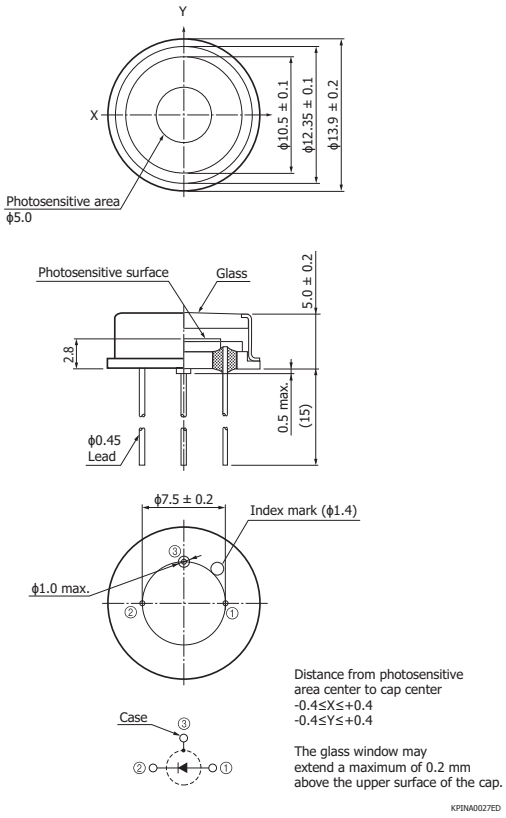


Terminal capacitance vs. reverse voltage



Dimensional outlines (unit: mm)

(1) S3071

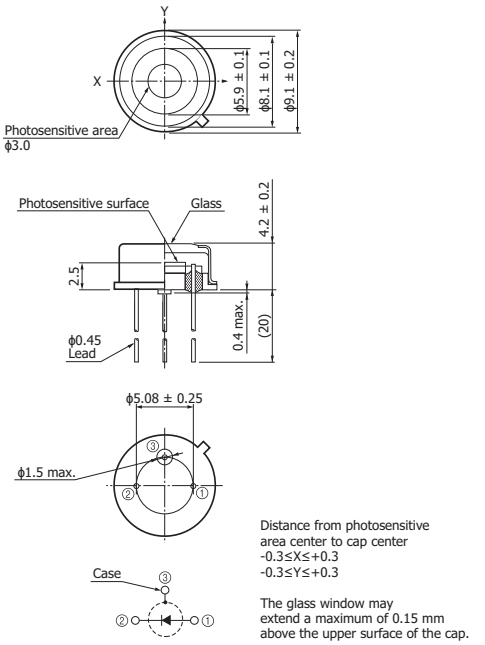


Distance from photosensitive area center to cap center
-0.4≤X≤+0.4
-0.4≤Y≤+0.4

The glass window may extend a maximum of 0.2 mm above the upper surface of the cap.

KPINA0027ED

(2) S3072

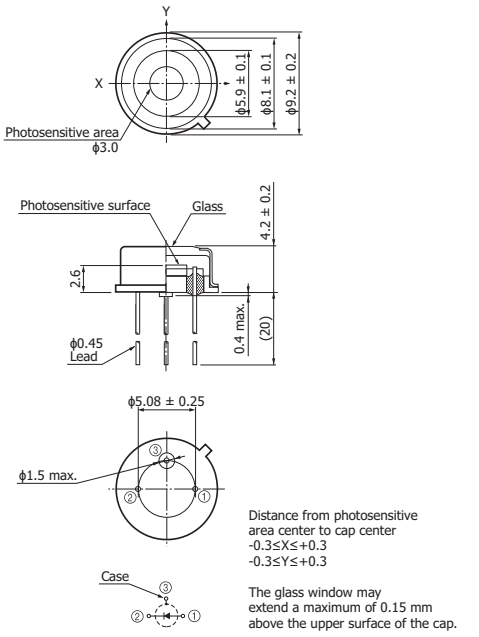


Distance from photosensitive area center to cap center
-0.3≤X≤+0.3
-0.3≤Y≤+0.3

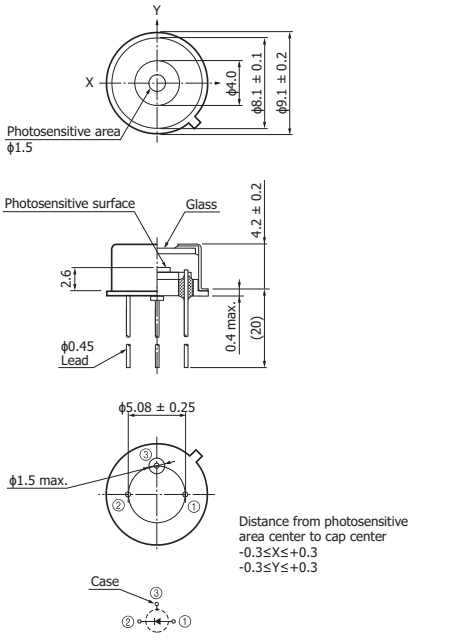
The glass window may extend a maximum of 0.15 mm above the upper surface of the cap.

KPINA0024EC

(3) S3399



(4) S3883



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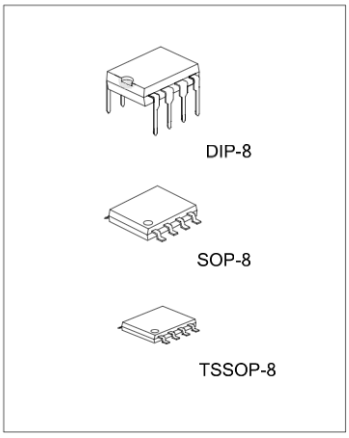
Cat. No. KPIN1044E06 Nov. 2014 DN

8.4. TL082

UTC UNISONIC TECHNOLOGIES CO., LTD

TL082 *LINEAR INTEGRATED CIRCUIT*

GENERAL PURPOSE DUAL J-FET OPERATIONAL AMPLIFIER



Lead-free: TL082L
Halogen-free:TL082G

■ DESCRIPTION

The UTC **TL082** is a high speed J-FET input dual operational amplifier. It incorporates well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The device features high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

■ FEATURES

* Low input bias and offset current
* Wide common-mode (up to V_{CC}^+) and differential voltage range
* Output short-circuit protection
* High input impedance J-FET input stage
* Internal frequency compensation
* Latch up free operation
* High slewrate:16V/μs(typ.)

■ ORDERING INFORMATION

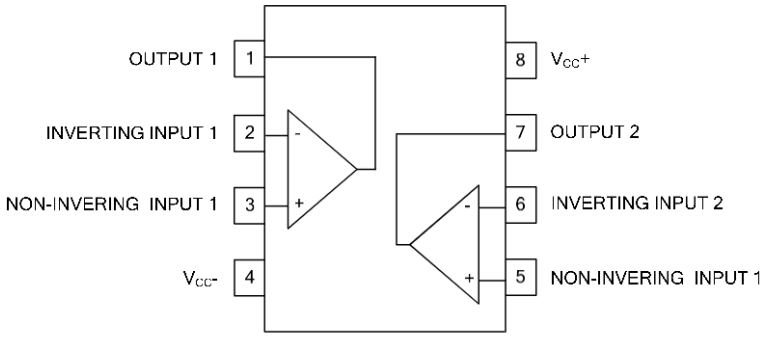
Ordering Number			Package	Packing
Normal	Lead Free Plating	Halogen Free		
TL082-D08-T	TL082L-D08-T	TL082G-D08-T	DIP-8	Tube
TL082-P08-R	TL082L-P08-R	TL082G-P08-R	TSSOP-8	Tape Reel
TL082-S08-R	TL082L-S08-R	TL082G-S08-R	SOP-8	Tape Reel

TL082L-D08-T
(1)Packing Type
(2)Package Type
(3)Lead Plating

(1) T: Tube, R: Tape Reel
(2) D08: DIP-8, P08: TSSOP-8, S08: SOP-8
(3) G: Halogen Free, L: Lead Free, Blank: Pb/Sn

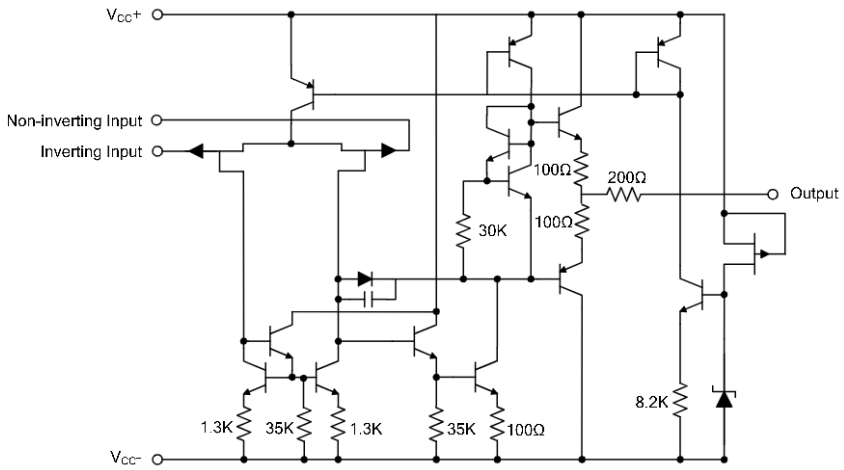
TL082 *LINEAR INTEGRATED CIRCUIT*

■ **PIN CONFIGURATION**



TL082 *LINEAR INTEGRATED CIRCUIT*

■ **BLOCK DIAGRAM**



TL082 *LINEAR INTEGRATED CIRCUIT*

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (Note 2)	V_{CC}	±18	V
Input Voltage (Note 3)	V_{IN}	±15	V
Differential Input Voltage (Note 4)	V_{ID}	±30	V
Power Dissipation	P_D	680	mW
Output Short-Circuit Duration (Note 5)		Infinite	
Operating Temperature	T_{OPR}	-20 ~ +85	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}- and V_{CC}+.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
5. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	θ_{JA}	125	°C/W
	DIP-8		85	°C/W
	TSSOP-8		120	°C/W
Junction to Case	SOP-8	θ_{JC}	40	°C/W
	DIP-8		41	°C/W
	TSSOP-8		37	°C/W

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=±15V, Ta=25°C, T_{MIN}=0°C, T_{MAX}=70°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage (R_S=50Ω)	V_{IO}	Ta=25°C		3	10	mV
		$T_{MIN} \le Ta \le T_{MAX}$			13	
Input Offset Voltage Drift	D_{VIO}			10		μV/°C
Input Offset Current (Note)	I_{IO}	T_a=25°C		5	100	pA
		$T_{MIN} \le Ta \le T_{MAX}$			10	nA
Input Bias Current (Note)	I_{IB}	T_a=25°C		20	400	pA
		$T_{MIN} \le Ta \le T_{MAX}$			20	nA
Input Common Mode Voltage Range	V_{ICM}		±11	-12~+15		V
Output Voltage Swing	$\pm V_{OPP}$	T_a=25°C, R_L=2kΩ,	10	12		V
		T_a=25°C, R_L=10kΩ	12	13.5		V
		$T_{MIN} \le Ta \le T_{MAX}$, R_L=2kΩ	10			V
		$T_{MIN} \le Ta \le T_{MAX}$, R_L=10kΩ	12			V
Large Signal Voltage Gain (R_L=2kΩ, V_{OUT}=±10V)	Avd	T_a=25°C	25	200		V/mV
		$T_{MIN} \le Ta \le T_{MAX}$	15			
Gain Bandwidth Product (Ta=25°C)	GBP	V_{IN}=10mV, R_L=2kΩ, C_L=100pF, f=100kHZ	2.5	4		MHz
Input Resistance	R_I			10^{12}		Ω
Common Mode Rejection Ratio (R_S=50Ω)	CMR	Ta=25°C	70	86		dB
		$T_{MIN} \le Ta \le T_{MAX}$	70			
Supply Voltage Rejection Ratio (R_S=50Ω)	SVR	Ta=25°C	70	86		dB
		$T_{MIN} \le Ta \le T_{MAX}$	70			

■ **ELECTRICAL CHARACTERISTICS (Cont.)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current, No Load	I_{CC}	Ta=25°C		3.6	5.6	mA
Channel Separation (Av=100, T_a=25°C)	V_{01}/V_{02}			120		dB
Output Short-Circuit Current	I_{OS}	Ta=25°C	10	40	60	mA
		$T_{MIN} \le Ta \le T_{MAX}$	10		60	mA
Slew Rate (T_a=25°C)	SR	V_{IN}=10V, R_L=2kΩ, C_L=100pF, unity gain	8	16		V/μs
Rise Time (T_a=25°C)	t_R	V_{IN} =20mV, R_L=2kΩ, C_L=100pF, unity gain		0.1		μs
Overshoot (T_a=25°C)	K_{OV}	V_{IN}=20mV, R_L=2kΩ, C_L=100pF, unity gain		10		%
Total Harmonic Distortion (T_a=25°C)	THD	A_V=20dB, f=1kHz, R_L=2kΩ, C_L=100pF, V_{OUT}=2Vpp)		0.01		%
Phase Margin	Φm			45		Degrees
Equivalent Input Noise Voltage (R_S=100Ω, f=1KHz)	eN			15		$\frac{nV}{\sqrt{Hz}}$

Note: The Input bias currents are junction leakage currents, which approximately double for every 10°C increase in the junction temperature.

■ PARAMETER MEASUREMENT INFORMATION

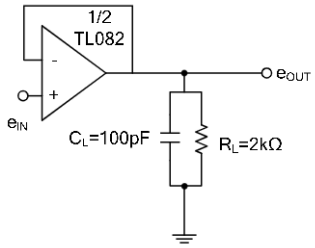


Figure 1. Voltage Follower

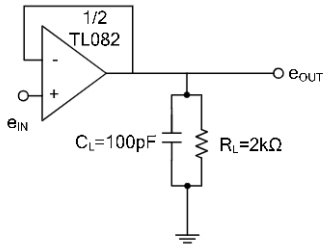
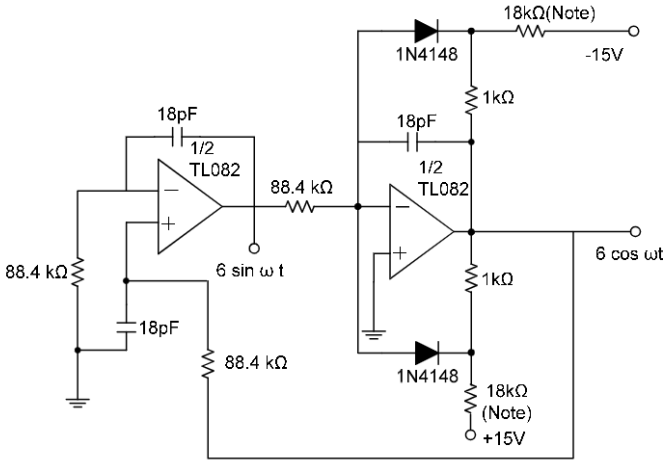


Figure 2. Gain-of-10 Inverting Amplifier

■ TYPICAL APPLICATION CIRCUIT

100 KHz Quadruple Oscillators



Note: These resistors values may be adjusted for a symmetrical output

■ TYPICAL CHARACTERISTICS