TRABAJO FIN DE GRADO

Diseño e implementación de la placa de circuito impreso LoMo del nanosatélite TEIDESAT-I

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Resumen

Este Trabajo de Fin de Grado tiene como objetivo aportar un avance en el desarrollo del nanosatélite TEIDESAT-I con la estructura CubeSat, diseñado por estudiantes universitarios de Canarias. El objetivo de esta misión es establecer comunicaciones ópticas entre La Tierra y su órbita baja (LEO).

Para promover el desarrollo de este nanosatélite, el TFG se centra en el diseño de la placa de circuito impreso LoMo (*Lord of Motherboards*), la cual cuenta con diferentes sistemas de direccionamiento y apuntado del satélite en el espacio, un ordenador de a bordo que controla todos los cambios que se efectúan dentro del satélite a alto nivel y un sistema de transmisión de potencia (EPS, *Electrical Power System*), el cual se encarga de suministrar energía a los diferentes dispositivos. Este primer prototipo de PCB (*Printed Circuit Board*) cumple con una serie de requisitos y normativa espacial necesaria para poder ser lanzado.

Esta placa de circuito impreso constituye uno de los núcleos más importantes del nanosatélite, puesto que la mayoría de señales necesitan pasar por dicha placa y por tanto, se debe asegurar la integridad de la señal.

Palabras clave: nanosatélite, cubesat, espacio, PCB.

Abstract

This Final Degree Project aims to provide an advance in the development of TEIDESAT-I nanosatellite with the CubeSat structure, designed by Canary Islands university students. The goal of this mission is to establish optical communications between Earth and its low orbit (LEO).

To promote the development of this nanosatellite, this Final Degree Project focuses on the printed circuit board LoMo (*Lord of Motherboards*), which has different direction and orientation systems of the satellite in space, an on board computer that controls each change it is made inside the satellite in a high level and a power transmission system (EPS) which provides energy to different devices. This first prototype of PCB follows a number of requisites and spatial rules needed to be launched.

This printed circuit board is part of one of the satellite major cores since almost every signal needs to go through it and, thus, signal integrity needs to be claimed.

Key words: nanosatellite, cubesat, space, PCB.

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1. Introducción

1.1. Objetivo principal

El objetivo de este Trabajo de Fin de Grado es implementar la placa de circuito impreso LoMo para el nanosatélite TEIDESAT-I. Este nanosatélite forma parte del tipo CubeSat, un estándar con unas dimensiones cúbicas de múltiplos de 10 cm de arista [1]. En este documento consta el proceso realizado para la recopilación de información y normativa necesaria para su diseño, la realización de esquemáticos y PCB y consideraciones a tener en cuenta para su fabricación y puesta en marcha.

1.2. Alcance del proyecto

Con este Trabajo de Fin de Grado se desea plantear un prototipo de diseño de placa circuito impreso que contenga el sistema de orientación y apuntado, memorias de almacenamiento de datos para experimentar su degradación debida a la radiación espacial y los circuitos de potencia que se encargan de transformar la energía de las baterías del satélite en distintos buses que alimentarán los sistemas de bajo consumo.

Se espera que el resultado de este proyecto sea un archivo editable de Altium Designer con el que poder trabajar en futuras iteraciones, teniendo la posibilidad de realizar cambios en cualquier momento. Con el diseño de esta PCB, también se espera obtener los ficheros Gerber para poder ser utilizados en las solicitudes de fabricación de la placa.

1.3. Estado del arte

A lo largo de los años, la tecnología espacial ha ido evolucionando paulatinamente a un ritmo inferior que la tecnología terrestre. Para promover la expansión del conocimiento en este ámbito, se ha dado un apoyo cada vez mayor a la tecnología CubeSat. Estos nanosatélites suelen tener una finalidad educativa y cada vez más universidades están desarrollando su propia versión para lanzar al espacio. Esto se debe a que fabricar uno de estos dispositivos tiene un costo y tiempo de desarrollo muchísimo menor que el de los satélites convencionales. A medida que pasa el tiempo, la tecnología que hay dentro de los CubeSats es cada vez más puntera, puesto que al tener un espacio limitado para realizar la misión, se ha intentado maximizar el ahorro de espacio, emplear componentes de menor tamaño (algunos de ellos de tecnología microscópica o nanoscópica) y principalmente de tecnología de montaje superficial (*Surface Mount Technology*, SMT).

En la Figura 1.1 se puede observar un aumento considerable de lanzamientos de nanosatélites desde 1998 hasta 2022 (las cantidades de años posteriores son previstas oficialmente). Cada uno de estos nanosatélites tiene un objetivo diferente: analizar diferentes parámetros de la atmósfera [2], investigar oscilaciones de brillo de estrellas luminosas masivas [3], realizar fotografías desde el espacio [4], etc.

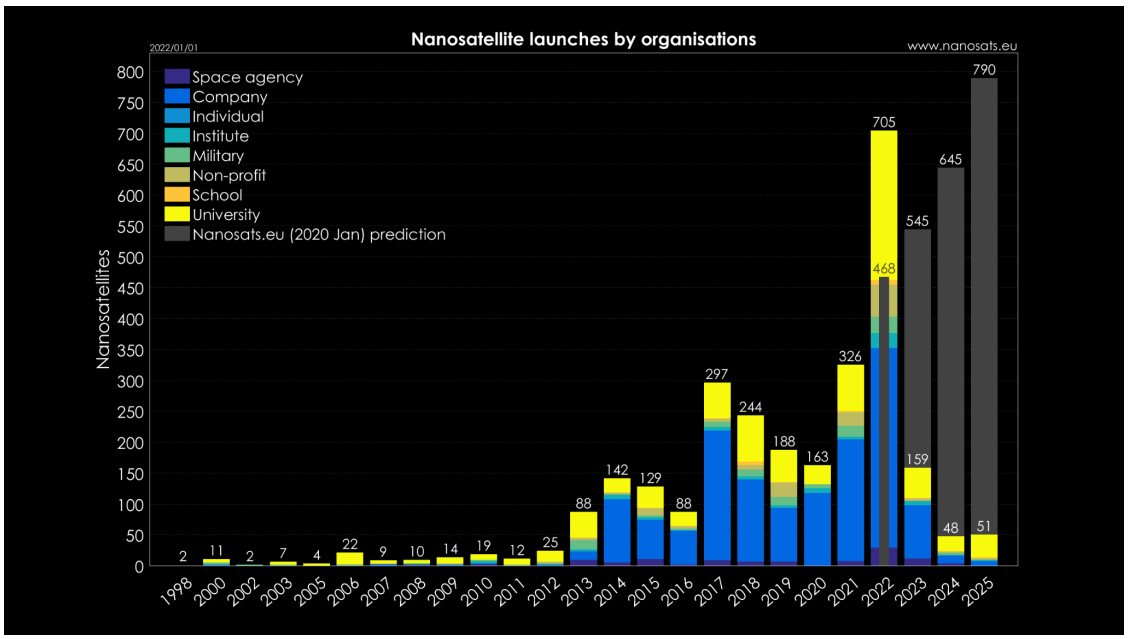


Figura 1.1: Lanzamiento de nanosatélites según su propósito. [5]

Para realizar las misiones espaciales con nanosatélites, estos se lanzan de manera que se sitúen en LEO (*Low Earth Orbit*, Órbita Baja de la Tierra). El rango de distancias consideradas parte de LEO es desde 160 km hasta los 1000 km con respecto al centro de la Tierra . En la Figura 1.2 se muestran las órbitas aproximadas dentro del rango de LEO en las que se sitúan los nanosatélites. Se puede observar que la gran mayoría llegaron a situarse en la misma órbita que la Estación Espacial Internacional (ISS), aunque la mayoría de ellas ya hayan decaído en dicha órbita.

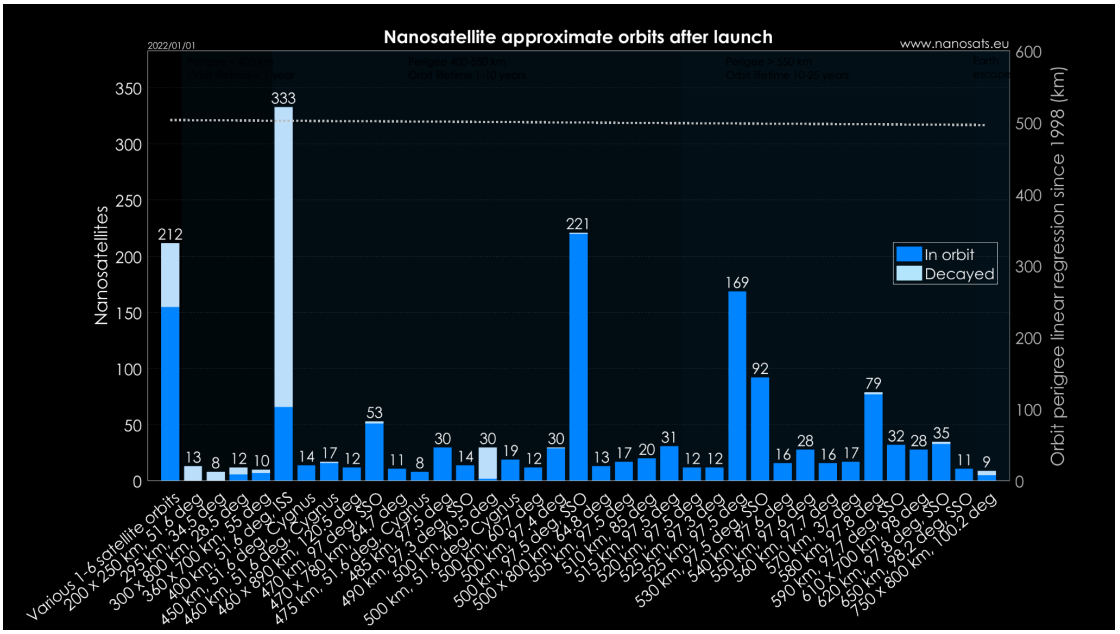


Figura 1.2: Órbita aproximada de los nanosatélites después del lanzamiento. [6]

La comunicación principal de los nanosatélites es vía radio. En la Figura 1.3 se puede observar las bandas de frecuencias que se suelen emplear en estas misiones. También se

puede apreciar una minoría de dispositivos que emplean tecnología láser u óptica. Esto se debe a que existen numerosos parámetros que afectan tanto a la emisión de luz como su recepción (ruido atmosférico, iluminación por parte de estrellas y otros satélites, reflexiones de la luz en otros satélites, contaminación lumínica terrestre, etc).

Con respecto a la comunicación por radio, el desfase tecnológico que existe entre el espacio y la Tierra conlleva que las comunicaciones también usen una tecnología más primitiva. Aunque un gran número de nanosatélites se sitúan entre los 8,2 GHz y los 10,5 GHz, más de la mitad de ellos aún emplean la escala de los megahertzios.

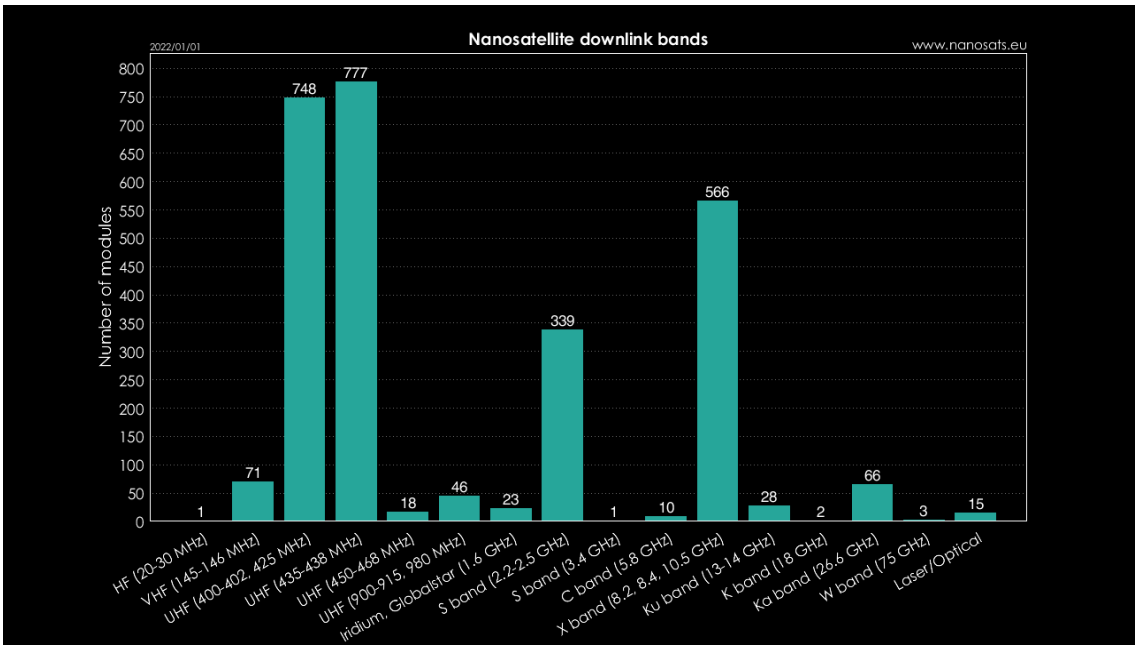


Figura 1.3: Frecuencia de radio de los nanosatélites. [7]

Uno de los recursos que se emplean para establecer comunicaciones más fluidas e intercambiar información con menos pérdida de datos es formar constelaciones de nanosatélites, donde estos estén conectados entre sí y puedan mandar todos los datos que se necesite para complementar su propia información obtenida.

1.4. El proyecto TEIDESAT

TEIDESAT es una misión para enviar un nanosatélite al espacio. Esta propuesta se creó en 2017 por parte de universitarios canarios [8]. El objetivo principal de TEIDESAT es diseñar y lanzar un nanosatélite del tipo CubeSat que logre establecer comunicaciones ópticas y analice el impacto de dichas comunicaciones y otras fuentes de luz procedentes de satélites en los Observatorios de Canarias. Este nanosatélite es el primero realizado por estudiantes canarios.

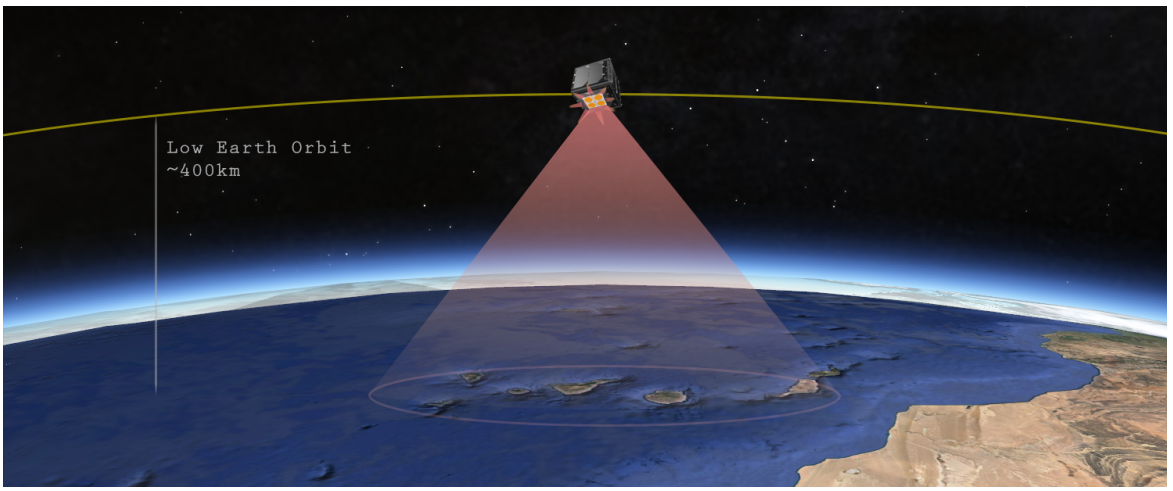


Figura 1.4: Concepto del nanosatélite TEIDESAT-I sobrevolando Canarias. [Elaboración propia]

TEIDESAT consta de cuatro bases principales:

- **Tecnológica:** Diseñar e integrar un nanosatélite perfectamente funcional que cumpla con los estándares de calidad de la Agencia Espacial Europea (ESA), y que sea capaz de establecer comunicación óptica de descarga entre el nanosatélite y La Tierra.

- **Científica:** Analizar el impacto de las comunicaciones ópticas y otras fuentes de luz procedentes de satélites en las observaciones astrofísicas de los Observatorios de Canarias.

- **Académica:** Aprender sobre áreas del conocimiento relacionadas con el espacio ajenas a la disciplina académica de cada miembro del equipo, con el objetivo de convertirse en un profesional mucho más completo y versátil. Como parte de este objetivo, se han realizado trabajos finales de título sobre subsistemas del satélite [9][10][11][12].

- **Divulgativa:** El equipo TEIDESAT cree en la importancia de la divulgación científico-técnica entre personas de todas la edades, haciendo especial hincapié en el público infantil y adolescente, y con especial atención a potenciar la presencia y la relevancia de las mujeres del equipo.

Para un mejor desarrollo del nanosatélite, este se divide en diferentes subsistemas, cada uno de ellos trabajado por un subgrupo de estudiantes coordinados. En la Figura 1.5 se puede observar la configuración inicial que tenía el planteamiento del CubeSat.

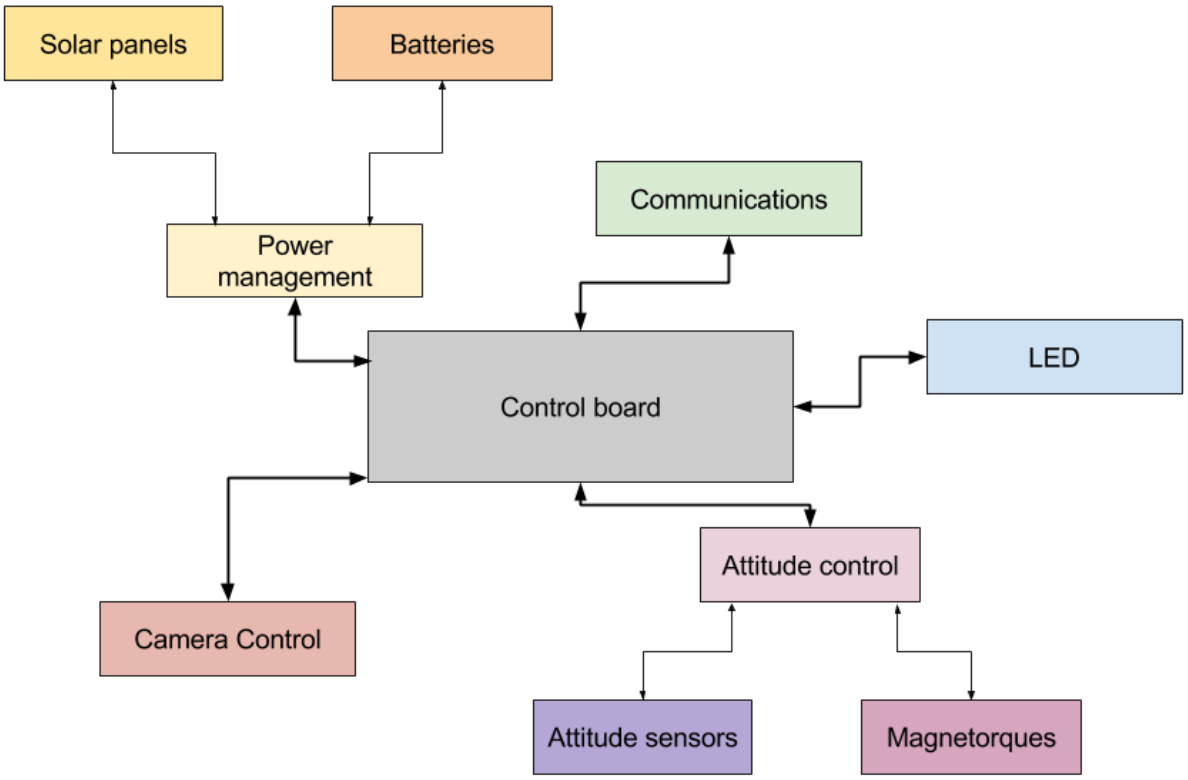


Figura 1.5: Esquema de subsistemas TEIDESAT-I. [Elaboración propia]

Actualmente, los subsistemas son los siguientes:

- **Mecánica/Térmica:** Se encarga de investigar todo lo relacionado con la estructura y propiedades térmicas de los materiales, circuitos impresos, etc.

- **Ordenador de a bordo (OBC, On Board Computer):** Núcleo principal de operaciones. Es el encargado de comunicar con todo el satélite, además de enviar y recibir información a través de los diferentes subsistemas.

- **ADCS (Attitude Determination and Control System):** Control de actitud y orientación. Se encarga de detectar la situación actual del nanosatélite y emplear diferentes actuadores pasivos o activos para apuntar el dispositivo hacia la Tierra.

- **Electrónica y telecomunicaciones:** Implementa todos los circuitos necesarios para que los demás subsistemas funcionen correctamente. Este Trabajo de Fin de Grado se encuentra dentro de este ámbito.

1.5. El origen de la PCB LoMo

A medida que el proyecto TEIDESAT avanza, los diferentes subsistemas empiezan a cerrar sus objetivos y propuestas de material a implementar. A raíz de ello, diversos subsistemas necesitan de un lugar donde colocar componentes que por otros motivos, bien sean térmicos, mecánicos o eléctricos, es necesario que se sitúen en un lugar diferente al especificado para dicho subsistema. El conjunto de todos estos elementos dan lugar a la necesidad de crear una placa de circuito impreso (PCB) dedicada a organizar estos elementos y agruparlos de la mejor manera posible para facilitar la trasmisión de información.

Esta placa se sometió democráticamente a votación para obtener una denominación. Por mayoría, se ha escogido el término *Lord of Motherboards* (Maestro de las placas madre) como referencia a ser la PCB que, conectada directamente con el ordenador de a bordo, maneja toda la información que entra y sale a los diferentes subsistemas. Para acortar el número de caracteres y mejorar el entendimiento, se utiliza el acrónimo LoMo.

La placa LoMo contiene tres elementos principales divididos en dos caras: nadir y cénit. La cara nadir es aquella que en condiciones normales apunta hacia a La Tierra, mientras que la cara cénit es la que apunta hacia el espacio.

En la cara nadir se encuentra el sistema eléctrico de potencia (EPS). En este caso, existen dos EPS para el TEIDESAT-I: de baja potencia (para el OBC, sensores, microcontroladores, etc.) y de alta potencia (para alimentar los LED de comunicaciones ópticas).

En la cara cénit se encuentran el OBC conectado, el sistema de ADCS (microcontrolador, IMU [*Inertial Measurement Unit*] y GPS [*Global Positioning System*]) y diversas memorias que se emplean para un segundo experimento: determinar el grado de deterioro de memorias en el espacio debido a la radiación cósmica.

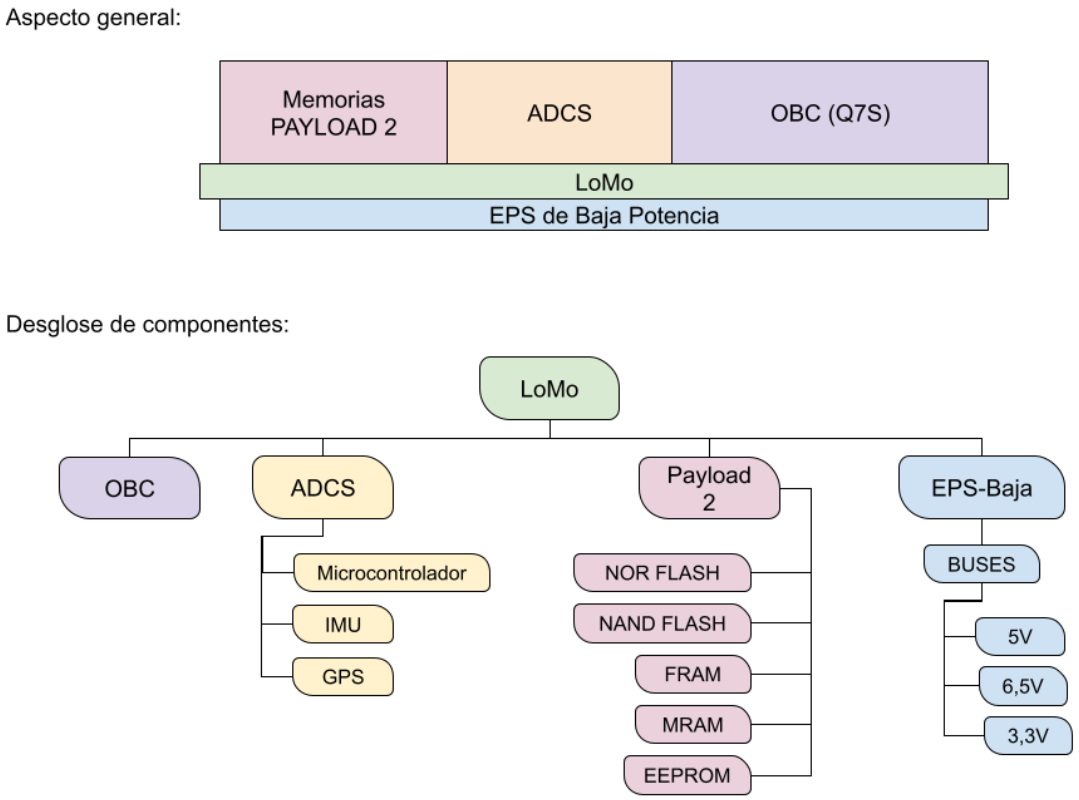


Figura 1.6: Idea de distribución de componentes y su desglose.

En la Figura 1.6 se puede observar la estructura que mantiene LoMo para la realización de la PCB. Todos los componentes, exceptuando el OBC que se unirá mediante un conector, estarán soldados sobre la placa. En definitiva, la placa LoMo maneja la mayoría de señales que se intercambian entre subsistemas y alimentará todo lo necesario que no conlleve los LED de alta potencia.

1.6. Normativa aplicable

Para poder diseñar correctamente la PCB y ser apta para la línea espacial, es necesario que el diseño cumpla una serie de requisitos físicos y eléctricos.

1.6.1. El estándar CubeSat

Un CubeSat es un tipo de nanosatélite que sigue unos estándares determinados [13] para realizar investigaciones en el espacio sobre diversos campos. Estos dispositivos cuentan con unas dimensiones de 10 x 10 x 10 cm (una unidad, o 1U) y pueden construirse contando con varias unidades. Para el caso más básico y el que se aplica a nuestro proyecto TEIDESAT, una unidad debe tener una masa máxima de 1,33 kg. Estos CubeSats pueden formar desde nanosatélites sencillos de pocas unidades hasta nanosatélites de mayor complejidad con 12U o 16U.

Este aumento de tamaño viene determinado por las especificaciones de la misión. En algunos casos, se utiliza ese espacio para recoger más información de los sensores lumínicos y atmosféricos, mientras que en otros se emplean para aumentar el número de paneles fotovoltaicos y obtener una mayor autonomía.

Un ejemplo de CubeSat de una unidad se puede ver en la Figura 1.7.

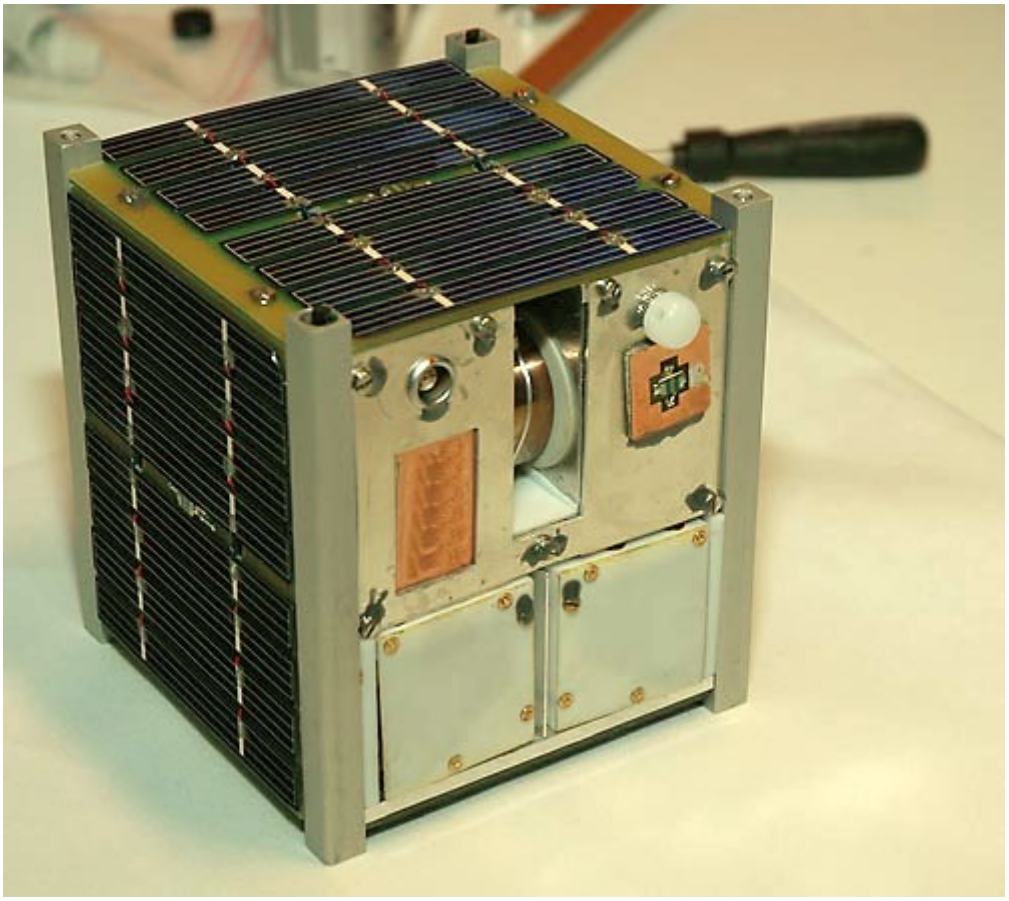


Figura 1.7: Cubesat de 1U. [14]

En la Figura 1.8 se puede observar los lanzamientos realizados en función del número de unidades de los nanosatélites. TEIDESAT-I se incluye dentro de los nanosatélites de 1U previstos a lanzar en unos años. Es posible que en el futuro se plantee la posibilidad de ampliar unidades para este nanosatélite, pero para esta iteración y tal y como está planteado actualmente el diseño, mantiene la unidad.

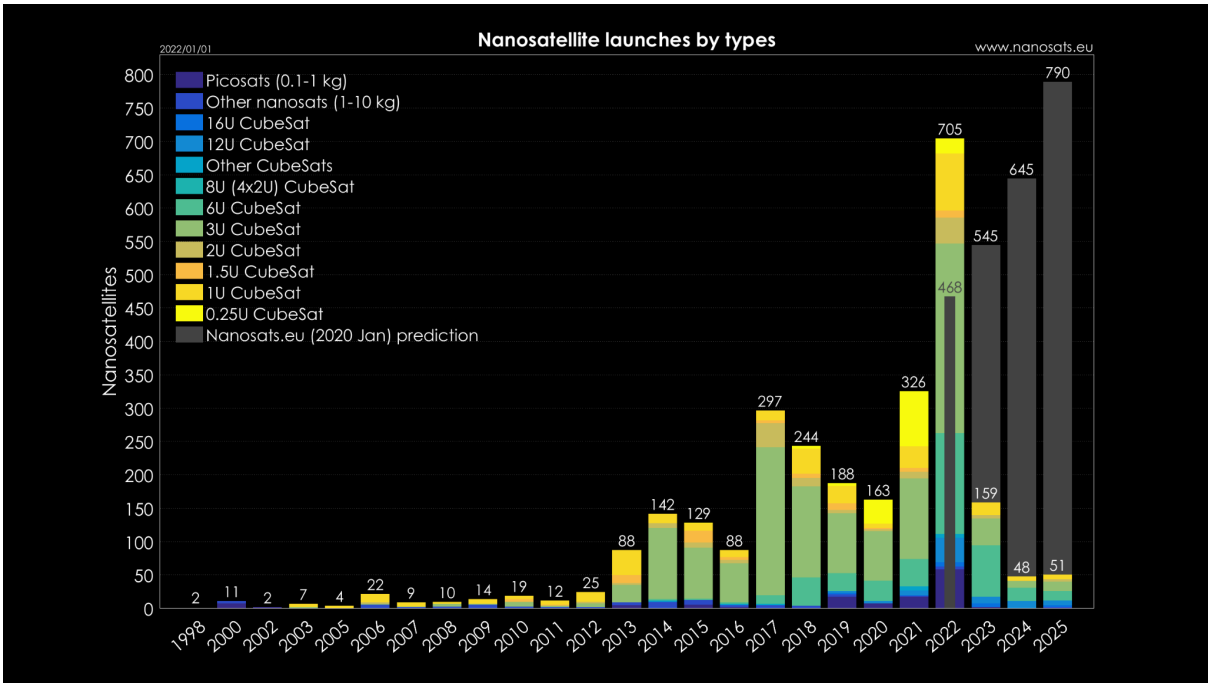


Figura 1.8: Lanzamientos por tipo de nanosatélite. [15]

1.6.2. Los estándares ECSS

Además de seguir el propio estándar CubeSat para su diseño y construcción, es necesario añadir unas reglas dadas por la Cooperación Europea para la Estandarización en el Espacio (ECSS, *European Cooperation for Space Standardization*), creada por la Agencia Espacial Europea (ESA, *European Space Agency*). Estas pautas pretenden normalizar el diseño de cualquier dispositivo que vaya a tener actividad en el espacio. De esta manera, existe una coherencia entre todas las misiones espaciales.

Los estándares ECSS incluyen más de 100 documentos con guías y recomendaciones diferentes y relacionadas entre sí para garantizar la seguridad y la calidad de nuestro nanosatélite. Dada la naturaleza de este Trabajo de Fin de Grado, se mencionan solamente aquellos estándares que estén relacionados directamente con el diseño de la LoMo.

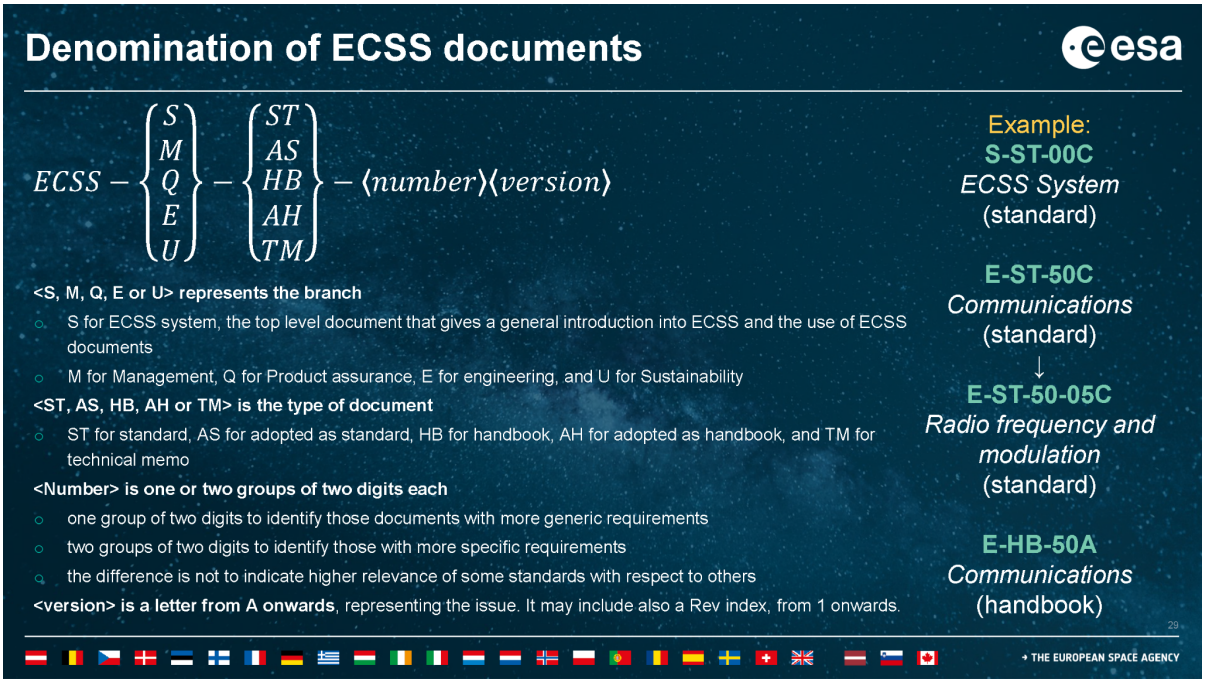


Figura 1.9: Codificación de los documentos estándares de la ECSS. [16]

Como se puede ver en la Figura 1.9, existen cinco ramas principales de los estándares que conforman la primera letra: Sistema (S), Administración (M), Calidad del producto (Q), Ingeniería (E) y Sustentabilidad (U).

Dentro de cada rama principal, podemos encontrar otra clasificación para el tipo de documento, el número de dicho documento y la versión actual. Los estándares ECSS que se seguirán en este TFG son del tipo ECSS-E-ST, es decir, estándares de ingeniería.

Concretamente, la normativa de la ESA a seguir para el diseño de la PCB es la siguiente:

- **ECSS-E-ST-20C-Rev.1, Electrical and electronic** [17]: Es el estándar principal de la parte electrónica del nanosatélite. Cubre la mayoría de campos para el diseño de la PCB (alimentación, compatibilidad electromagnética, radiofrecuencia, etc).

- **ECSS-E-ST-20-07C-Rev.2, Electromagnetic Compatibility** [18]: Este estándar se centra exclusivamente en la Compatibilidad Electromagnética (EMC). Detalla las situaciones e interferencias que pueden darse y las condiciones que se tienen que cumplir para reducirlas.

- **ECSS-E-ST-20-06C-Rev.1, Spacecraft Charging** [19]: Se encarga de especificar las soluciones a las descargas eléctricas en el espacio por altas diferencias de potencial.

- **ECSS-E-ST-20-01C, Multipactor Design and test** [20]: Prevé los posibles riesgos dados por el efecto multipactor, donde puede darse una descarga amplificada de electrones en los sistemas de radiofrecuencia (RF).

1.6.3. La convocatoria Fly Your Satellite!

Fly Your Satellite! (FYS) es un programa ofrecido por la ESA donde cada año se reúnen una cantidad de CubeSats que, cumpliendo con la normativa mencionada anteriormente, junto con una serie de pautas dadas por esta convocatoria, pueden garantizar el lanzamiento del nanosatélite. Este evento está dirigido principalmente a estudiantes, de manera que puedan ampliar sus conocimientos y su experiencia en el campo espacial [21].

Tras presentar la propuesta de CubeSat, se realiza una selección de los proyectos más óptimos, los cuales tendrán acceso a una plataforma de lanzamiento de CubeSats.

1.6.4. Altium Designer

Para poder implementar la LoMo, es necesario elegir un software de diseño de esquemáticos y PCB. Existen multitud de opciones en el mercado, desde software libre como KiCAD, hasta soluciones de pago como las ofertadas por Cadence. Se ha escogido Altium como software a emplear por las siguientes razones:

- Reúne el diseño de esquemáticos y PCB en un único programa.
- Tiene una amplia variedad de componentes registrados del mercado, con acceso a sus hojas de datos, además de símbolos y huellas.
- Es uno de los programas más empleados en la industria.
- Tiene una licencia de estudiante fácil de aplicar y sin dificultades a la hora de instalar.

Aprovechando las características que tiene Altium, el diseño de esquemáticos de la placa LoMo seguirá una jerarquía, puesto que los diferentes circuitos están suficientemente estructurados para poderse dividir en diferentes niveles.

El flujo de trabajo que se sigue con Altium viene descrito en la Figura 1.10.

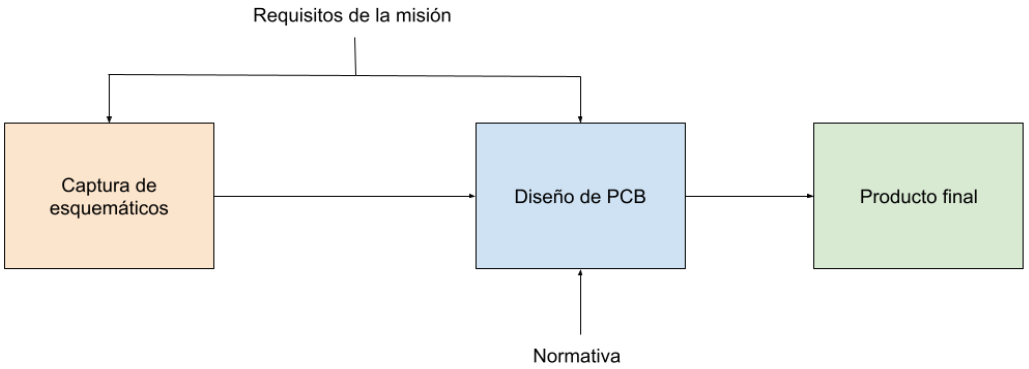


Figura 1.10: Diagrama de flujo de trabajo de Altium.

Las unidades que se van a emplear para este proyecto se muestran en la Tabla 1.1.

Grosor de vías y pistas	mils
Grosor de capas	mm
Peso del cobre	oz
Esquemáticos	mm

Tabla 1.1: Unidades empleadas en este proyecto.

La versión de Altium Designer utilizada en este proyecto es la 22.4.2.

1.6.5. Repositorio extra con Altium Library Loader

Algunos símbolos y *footprints* no se encuentran en el repositorio de Altium. Sin embargo, existen otros repositorios donde hay una mayor cantidad de componentes. Para poder acceder al repositorio de SamacSys desde Altium, es necesario instalar el plugin *Altium Library Loader* [22]. Algunos componentes pueden llevar asignado un símbolo, una huella o ambos. En este caso, nos interesa que los componentes tengan ambas características para poder situarlas correctamente en Altium. En caso de que falte alguna de ellas y no se encuentre en el repositorio de Altium ni en el de SamacSys, se creará manualmente. En la Figura 1.11 se muestra un ejemplo de búsqueda empleando esta herramienta.

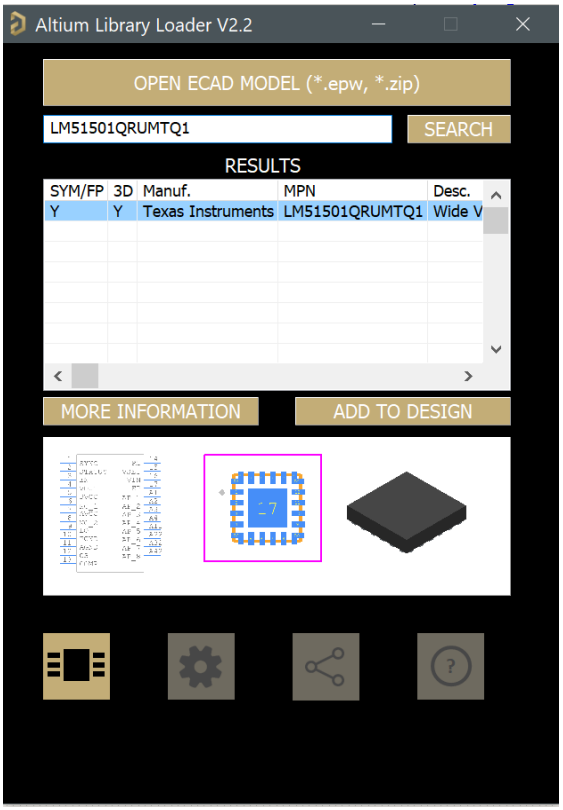


Figura 1.11: Búsqueda de un componente en *Altium Library Loader*.

2. Procedimiento

2.1. Diseño de los buses de potencia

2.1.1. Herramienta WEBENCH

Para optimizar el diseño de las diferentes alimentaciones que ofrece la placa LoMo se ha empleado la herramienta WEBENCH de Texas Instruments [23]. Esta herramienta proporciona una configuración de circuitos de potencia en función de los requisitos: tamaño, coste, eficacia o un equilibrio entre todos estos. Para esta misión no supervisada presencialmente una vez se haya lanzado el nanosatélite, cuanta menos energía se pierda, mayor autonomía tendrá este y disminuirán las probabilidades de fallo.

Al estar alimentado a través de unas baterías de ion de litio, su voltaje puede variar desde aproximadamente 4,20 V (carga máxima) hasta 2,5 V (descarga total) [24]. A pesar de que estos valores rara vez se produzcan y normalmente se mantienen en torno a los 3,7 V, es necesario prever la conversión de voltaje. Es decir, no se puede depender de un único valor de entrada para diseñar el convertidor, sino que es necesario establecer un rango de trabajo. Por ello, en la herramienta WEBENCH se ha empleado el rango de 2,5 V hasta los 4,35 V, superando un poco el máximo de las baterías para evitar fallos por situaciones de sobrevoltaje imprevistas.

2.1.2. Bus de potencia de 6,5 V

Seleccionando el rango de entradas anterior, un objetivo de eficiencia máxima y empleando componentes de tamaño reducido, se ha obtenido una configuración que emplea el circuito integrado LM51501-Q1RUM, un convertidor *boost* con un amplio rango de entrada (desde 1,5 V hasta 42 V). Para verificar que este componente se puede emplear en el espacio, observamos su rango de temperaturas de trabajo. Al soportar desde -40 ºC hasta 125 ºC, es apto para dicha situación. En la Figura 2.1 se puede observar la simulación de la alimentación al encender el sistema.

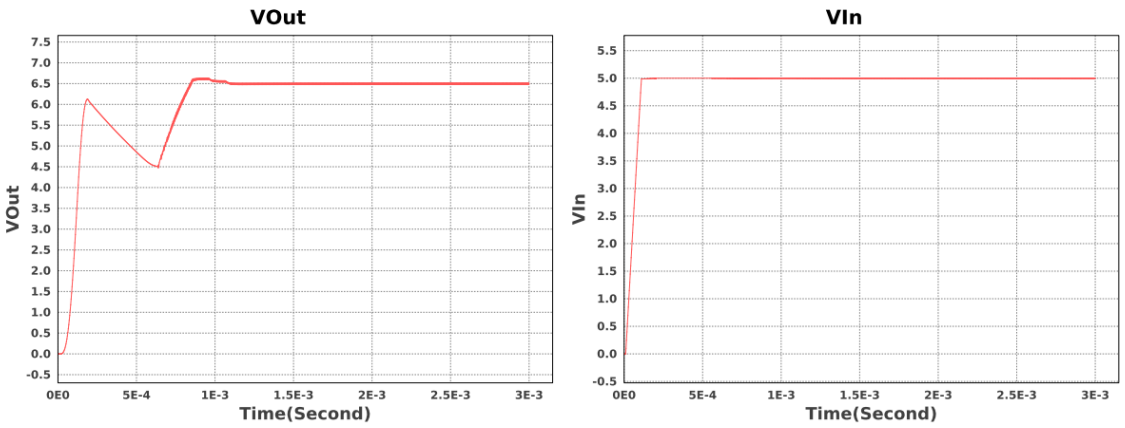


Figura 2.1: Simulación de arranque de 6,5 V. [Elaboración propia]

Se puede apreciar que el estado estacionario se alcanza aproximadamente en 1 ms, por lo que para una aplicación constante como es la de alimentar el OBC durante todo el ciclo, no existe ningún problema en cuanto al arranque.
Para comprobar el rizado que puede tener esta señal, se realiza otra simulación dentro del estado estacionario. El resultado de dicha simulación se puede observar en la Figura 2.2.

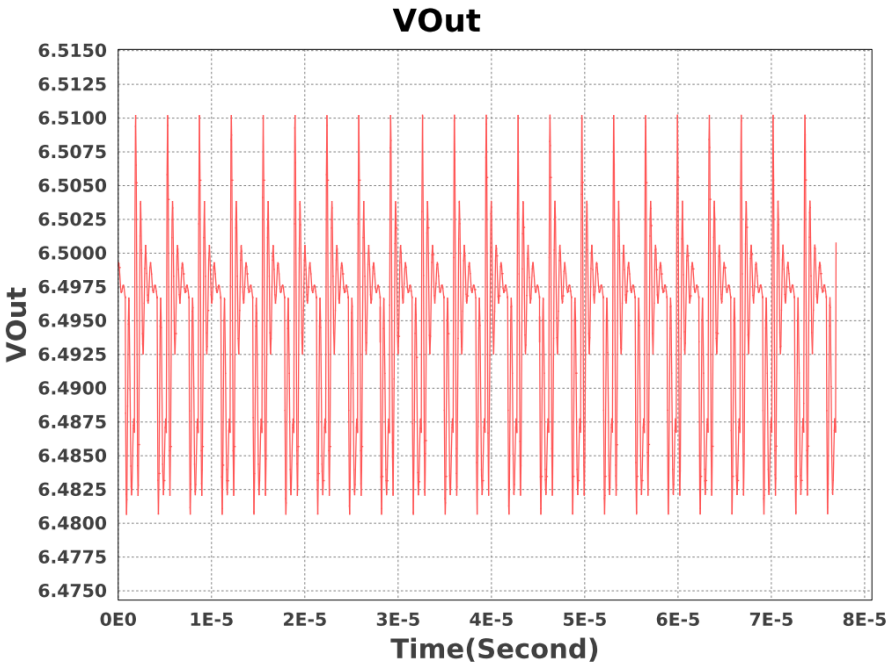


Figura 2.2: Simulación del estado estacionario de 6,5 V. [Elaboración propia]

En la Tabla 2.1 se muestra un resumen de las características principales del convertidor, extraídas del reporte generado por la propia herramienta WEBENCH que se encuentra en el Anexo IV.

Convertidor de 6,5 V	
Topología	Boost
Voltaje de entrada mínimo	2,5 V
Voltaje de entrada máximo	4,35 V
Voltaje de salida	6,5 V
Corriente de salida	0,8 A
Potencia de salida	5,2 W
Ciclo de trabajo	63,348%
Frecuencia	4,419 kHz
Rendimiento	92,166%
Rizado pico a pico	9,259 mV

Tabla 2.1: Características del convertidor de 6,5 V.

El circuito cuenta con dos etiquetas de tierra: una de ellas indica principalmente la tierra común de los convertidores, es decir, la tierra donde descargan las señales de potencia, mientras que la otra tierra (con forma triangular cerrada) se emplea para el resto de señales de información. Esto se debe a que combinar ambas tierras para diferentes tipos de señales puede provocar un solapamiento del ruido de ambas, empeorando la transmisión de información. En la Figura 2.3 se puede observar el esquemático final.

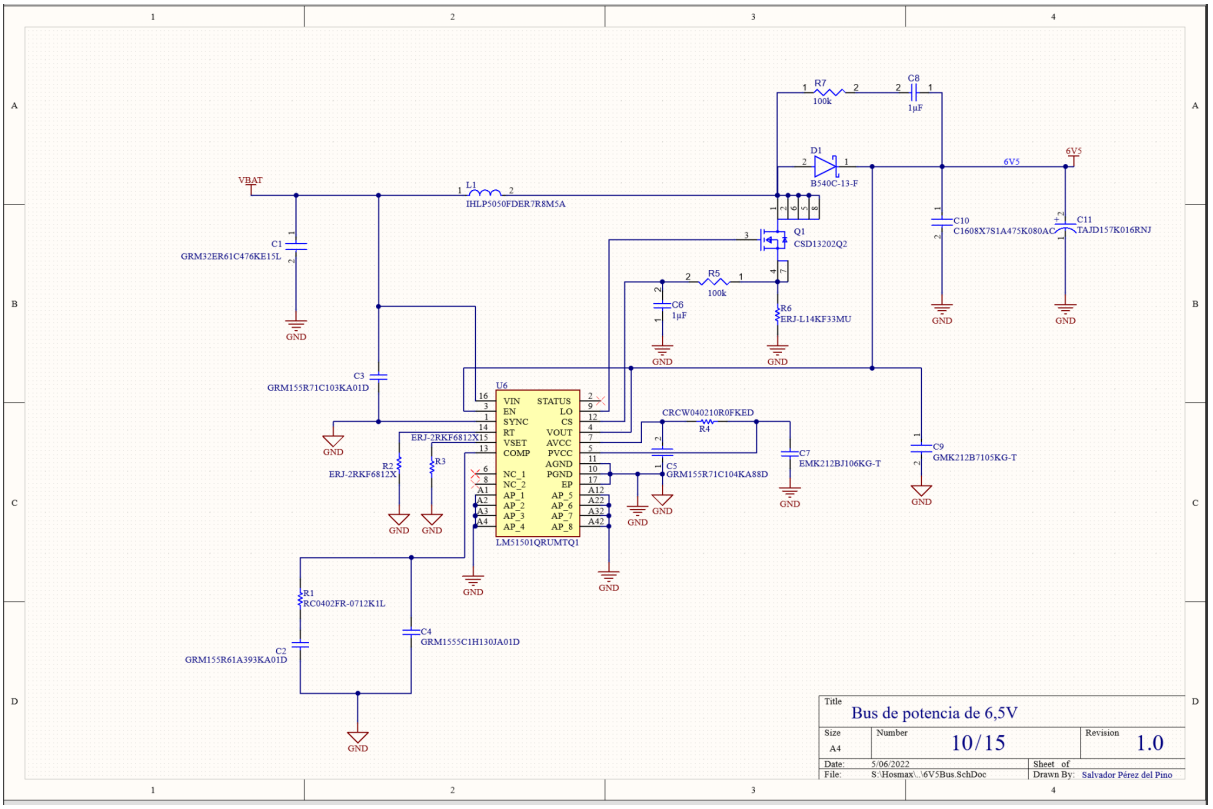


Figura 2.3: Esquemático del circuito de potencia de 6,5 V.

A la hora de exportar el esquemático a Altium, según el tipo de circuito integrado, existe la posibilidad de crear un archivo con los componentes ya previstos. En el caso de 6,5 V, esto no es posible, por lo que se ha replicado manualmente el esquemático que se obtuvo en el documento generado por la herramienta WEBENCH, adjunto en el Anexo IV.

Para adaptar el esquemático teórico al real, es necesario eliminar las fuentes de tensión de entrada y de corriente o resistencias de salida. Como la alimentación viene dada por las baterías, se coloca un conector específico para ello, del cual se hablará más adelante. Las entradas y salidas de tensión se sustituyen por puertos de potencia (*power ports* en Altium). Estos puertos se encargan de enlazar la alimentación de toda la placa en caso de no establecer dicha conexión por jerarquía. Para mayor sencillez, solamente se emplea la jerarquía de esquemáticos para señales que no conlleven alimentación.
Los puertos cuyos voltajes llevan un decimal se denominarán mediante una V en el lugar de la coma. Para el caso de 6,5 V, el puerto de salida se anota como “6V5”.

En el Anexo II se puede observar la lista de componentes definitivos.

2.1.3. Buses de potencia de 5 V

Para el diseño del circuito de potencia de 5 V se ha optado por dividir este en dos: un circuito principal, mayoritariamente activo y un circuito secundario en caso de fallo.

Siguiendo el mismo procedimiento que en el apartado anterior, a través de la herramienta WEBENCH se ha obtenido un circuito de potencia que emplea el circuito integrado TPS61236PRWLR, un convertidor *boost* con un rango de voltajes que cumple el requerido (de 2,3 V a 4,9 V), además de un gran porcentaje de eficiencia (97%).

La respuesta transitoria de la Figura 2.4 también es rápida: alcanza el estacionario aproximadamente 2,5 ms después de recibir la entrada necesaria.

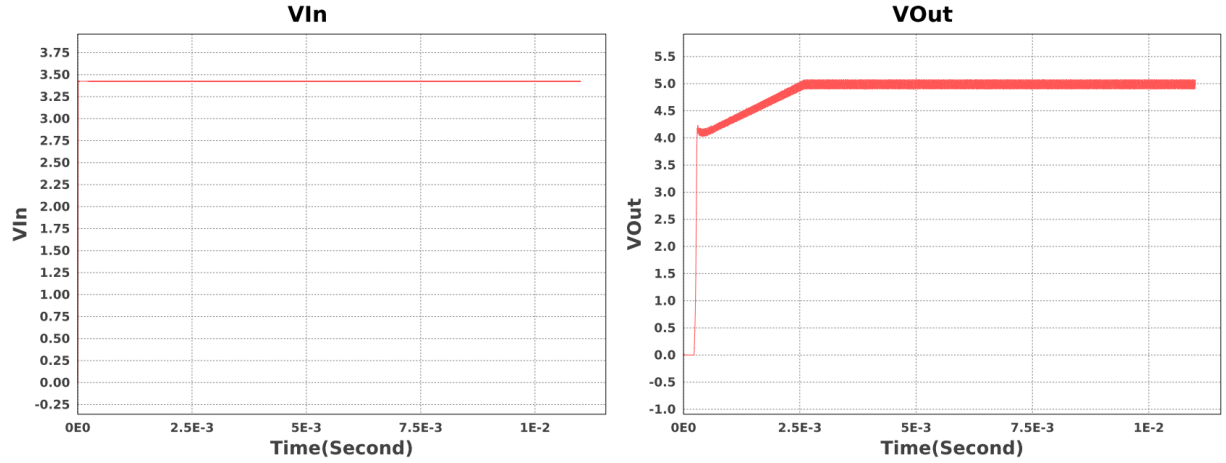


Figura 2.4: Respuesta transitoria de 5 V. [Elaboración propia]

Las características de este convertidor se pueden ver en la Tabla 2.2.

Convertidor de 5 V	
Topología	Boost
Voltaje de entrada mínimo	2,5 V
Voltaje de entrada máximo	4,35 V
Voltaje de salida	5 V
Corriente de salida	0,3 A
Potencia de salida	1,5 W
Ciclo de trabajo	50,226%
Frecuencia	1 MHz
Rendimiento	96,651%
Rizado pico a pico	23,592 mV

Tabla 2.2: Características principales del convertidor de 5 V.

En este caso, la herramienta WEBENCH dispone de la exportación directa a Altium, por lo que se ha importado el archivo con la extensión ".SchDoc", a la cual se ha modificado también las entradas y salidas. En la Figura 2.5 se muestra el resultado final de este circuito.

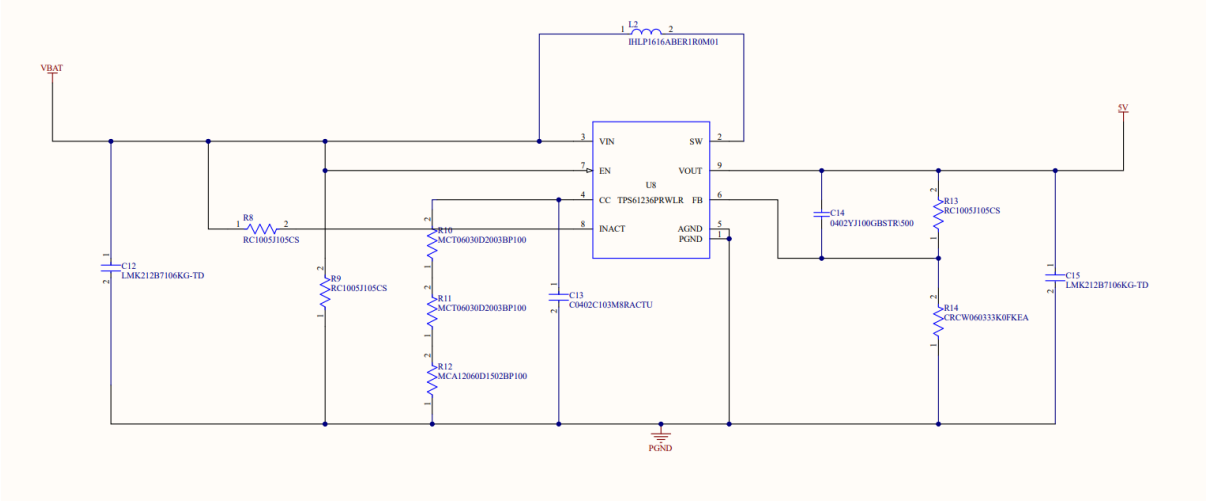


Figura 2.5: Esquemático del circuito de potencia de 5 V principal.

Para el circuito de 5 V secundario, se ha duplicado el circuito principal. Para evitar errores en el puerto de potencia, se denomina este "5VNE" (5 V No Esencial). En la Figura 2.6 se encuentra el circuito con esta etiqueta modificada.

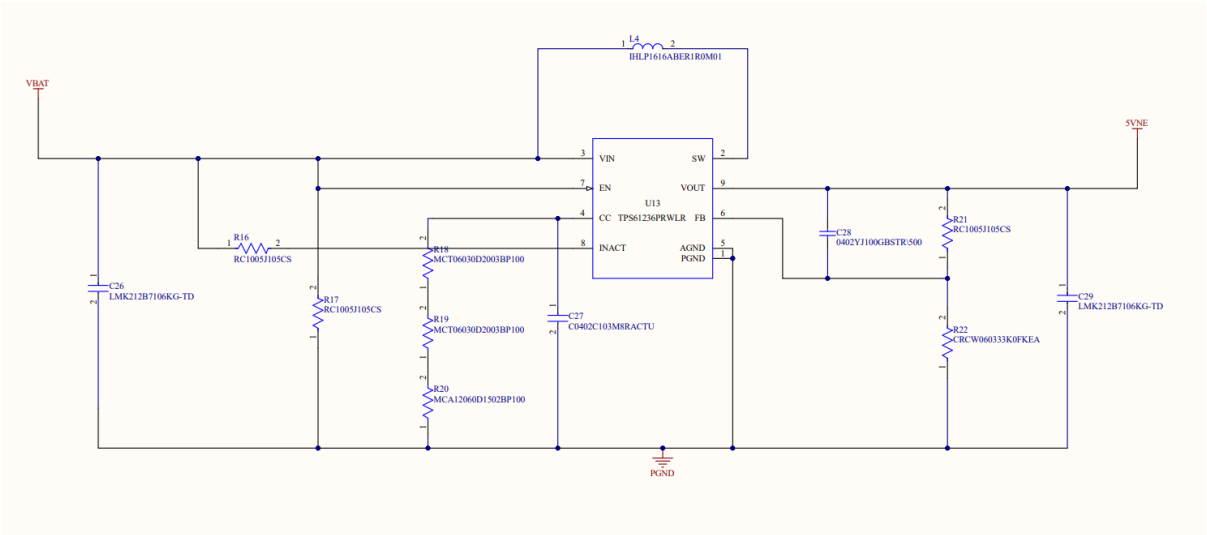


Figura 2.6: Esquemático del circuito de potencia de 5 V secundario.

2.1.4. Bus de potencia de 3,3 V

Similar al apartado anterior, el circuito de 3,3 V se ha obtenido a través de la herramienta WEBENCH. El resultado muestra un convertidor *Buck-Boost* del 95% de eficiencia. Esta

alimentación también es fundamental para los sensores que se emplean en el nanosatélite, además de los alimentados en el ADCS.

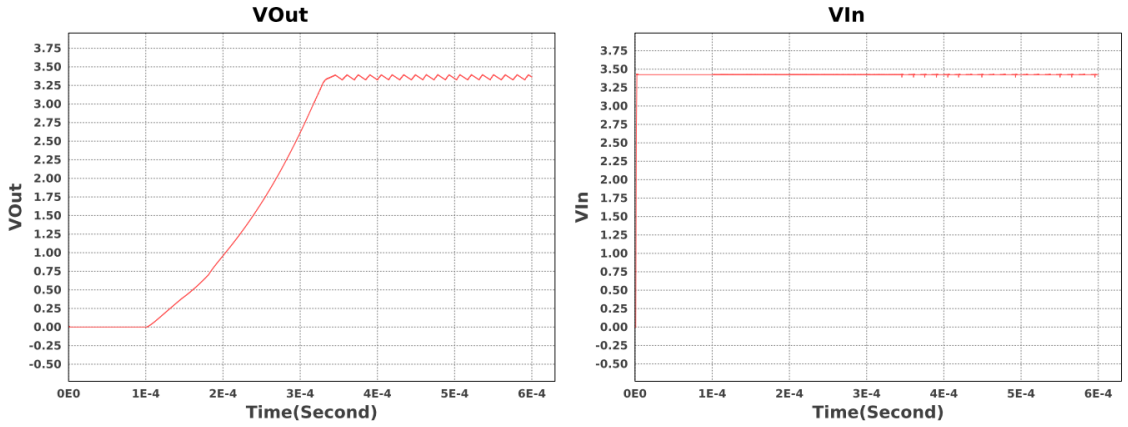


Figura 2.7: Arranque del convertidor de 3,3V. [Elaboración propia]

En la Figura 2.7 se puede observar que el estado estacionario se obtiene aproximadamente a los 0,35 ms, por lo que no implica ningún inconveniente.

En la Tabla 2.3 se muestran las características principales de este convertidor.

Convertidor de 3,3 V	
Topología	Buck-Boost
Voltaje de entrada mínimo	2,5 V
Voltaje de entrada máximo	4,35 V
Voltaje de salida	3,3 V
Corriente de salida	0,2 A
Potencia de salida	0,66 W
Ciclo de trabajo	25,381%
Frecuencia	2,5 MHz
Rendimiento	94,184%
Rizado pico a pico	735,538 µV

Tabla 2.3: Características principales del convertidor de 3,3 V.

El circuito final con los puertos colocados correctamente (“3V3” para esta alimentación) se puede apreciar en la Figura 2.8.

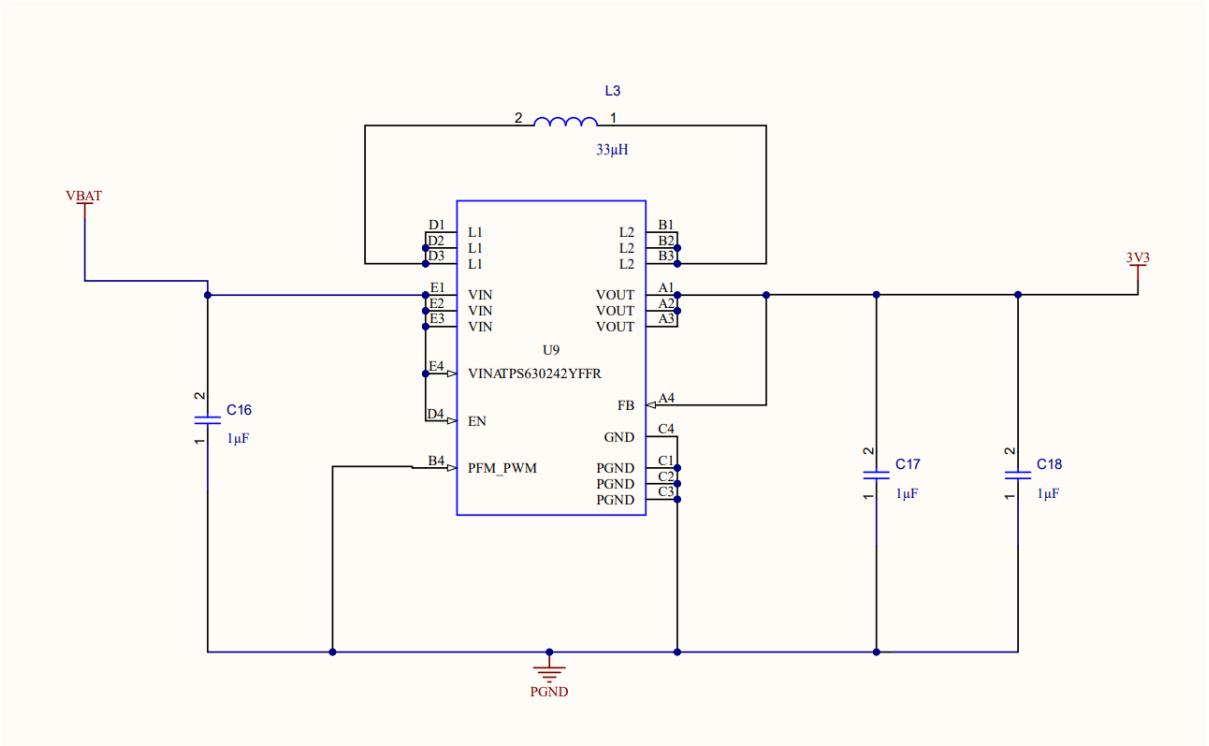


Figura 2.8: Esquemático del circuito de potencia de 3,3 V.

2.1.5. Memorias del segundo experimento

Para el segundo experimento que se desea realizar en este nanosatélite, se emplean cinco memorias: MRAM, FRAM, NOR FLASH, NAND FLASH y EEPROM. En estas memorias se situarán combinaciones de 0 y 1 conocidas, además de algún archivo de imagen. Se espera poder analizar el deterioro de las mismas y observar cómo el espacio puede modificar a esa combinación de números binarios.

En la Figura 2.9 se puede observar la distribución de los pines de las mismas en el esquemático.

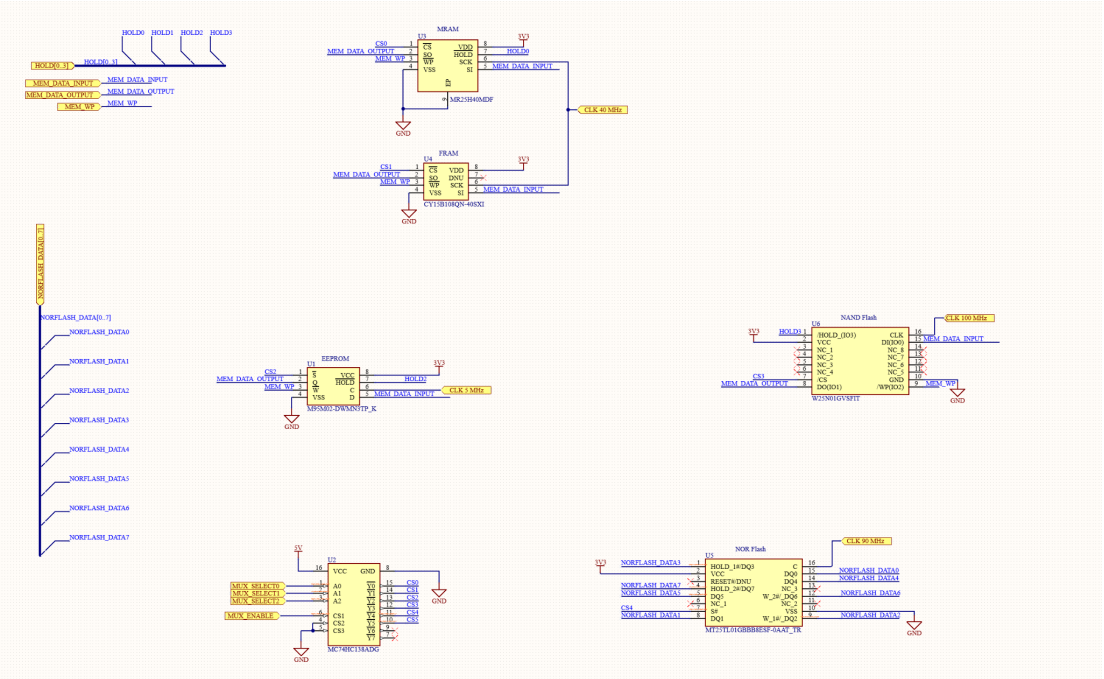


Figura 2.9: Esquemático del conexionado de las memorias.

Como la comunicación entre el OBC y las memorias se realiza mediante el protocolo SPI, solamente puede quedar una memoria activa a la vez. Para optimizar el número de pines, se ha optado por utilizar un demultiplexor de 3 bits, donde utilizando tres líneas del OBC, se puede seleccionar hasta 8 memorias diferentes. En este caso, se emplean las primeras cinco salidas para seleccionar cada memoria mediante su entrada *Chip Select* (CS, selección de circuito integrado). También, al utilizar una única memoria a la vez, se puede emplear una única señal de datos de salida y de entrada, puesto que no va a ser sobreescrita por varias memorias en un mismo tiempo. El mismo principio se aplica al pin de *Write Protect* (WP, protección de escritura). Para el caso de la memoria NOR FLASH, como internamente funciona de manera que se activen dos memorias en paralelo, se ha optado por emplear señales únicas para este caso exclusivamente.
Para retener los datos, se utiliza un bus de señales HOLD para las cuatro primeras memorias.

Resumidamente, se emplean los siguientes pines que provienen del OBC:

- 4 pines para el demultiplexor (tres selectores, uno de activación).
- 4 pines del bus HOLD, para retener los valores actuales.
- 1 pin de datos de entrada.
- 1 pin de datos de salida.
- 1 pin de protección de escritura.
- 8 pines para la configuración de la memoria NOR FLASH.

2.1.6. Microcontrolador del ADCS

Para el sistema que controla la orientación del satélite, es necesario implementar un algoritmo que transforme las señales de los sensores en controles hacia los magnetorques que controlan

el giro. Eléctricamente, se provee de un microcontrolador el cual manejará dicha información. Para tener mayor información a la hora de realizar los esquemáticos, se emplea el ATMEGA328P, un microcontrolador muy común por su uso en dispositivos como Arduino [25]. En los primeros prototipos se empleará este microcontrolador, mientras que en la versión final se utilizará una versión idéntica diseñada para espacio. En la Figura 2.10 se muestra el conexionado de este dispositivo.

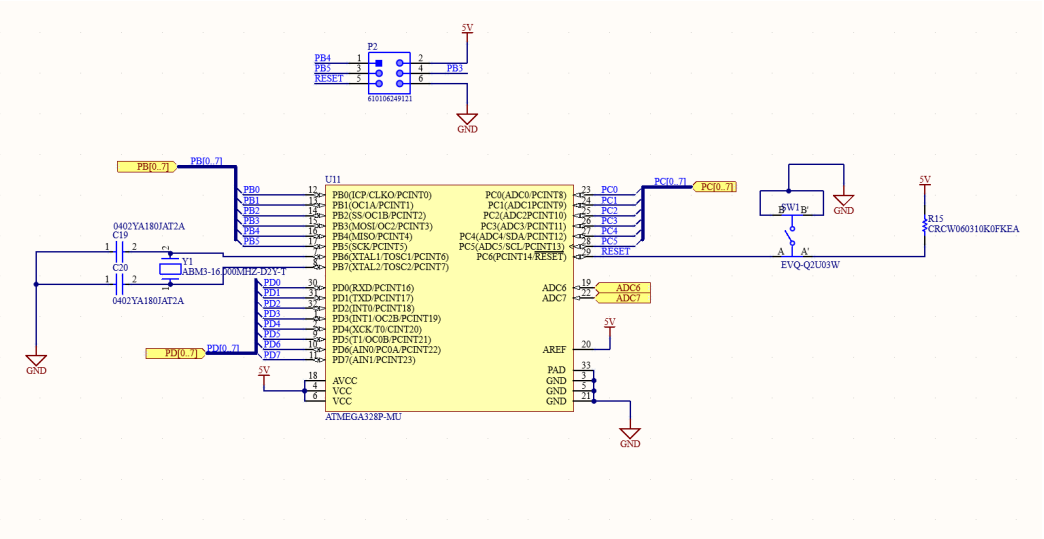


Figura 2.10: Esquemático del conexionado del microcontrolador.

El microcontrolador cuenta con tres puertos principales: B, C, D, además de pines específicos como el de reset, para reiniciar por completo el sistema sin borrar el programa escrito y los pines ADC, cuya función es la de convertir información analógica en digital.
Los últimos dos bits del puerto B se emplean para dar la señal de reloj del ATMEGA328P, por lo que se ha colocado un circuito oscilador a su lado para poder proveer un reloj de 16 MHz.
A la señal de reset se le ha incorporado un interruptor con una resistencia de *pull-up*, de manera que al pulsar dicho interruptor, la referencia de tierra atraviesa el interruptor hasta llegar al pin de reset (este pin se activa a baja). Este interruptor es útil a la hora de realizar pruebas en tierra, para evitar fallos o detenciones del sistema.

2.1.7. IMU del ADCS

Para determinar el estado actual del nanosatélite en el espacio (orientación con respecto a la Tierra, aceleración y posición actual) se emplea una IMU. Como la conexión que tiene con el OBC se realiza a través del protocolo I2C, podemos observar en la Figura 2.11 los pines correspondientes a dicha comunicación. Para las interrupciones y datos de salida, los pines se separan en función de si la información está relacionada con el acelerómetro o giroscopio (pines con la denominación A/G) o con el magnetómetro. Todos los pines de la IMU se conectan directamente al ordenador de a bordo.

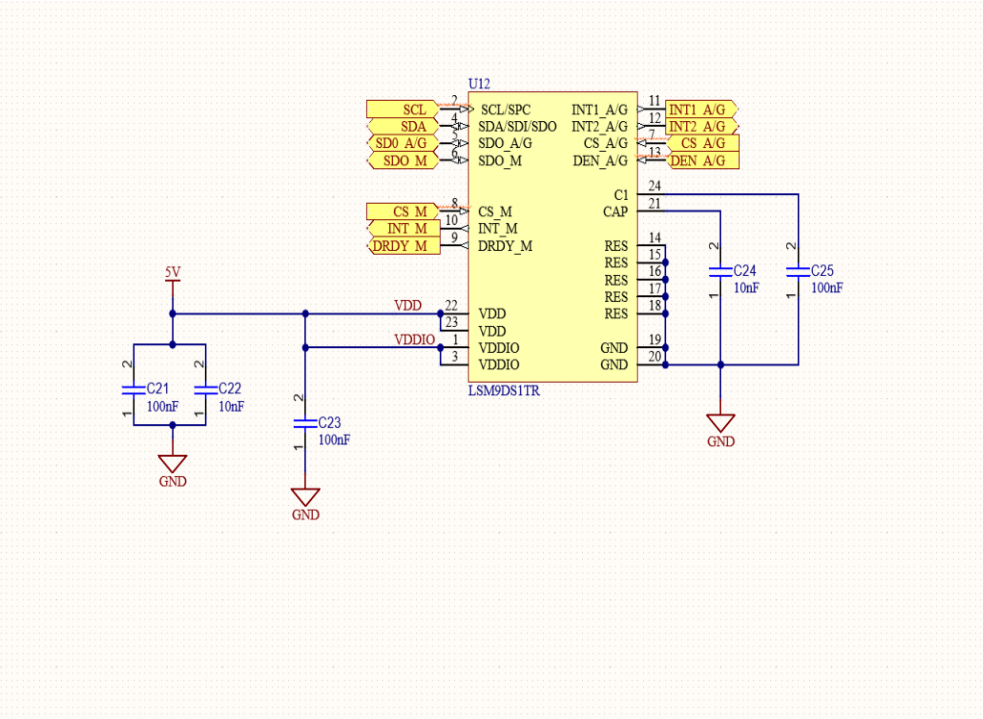


Figura 2.11: Esquemático del conexionado de la IMU.

2.1.8. GPS del ADCS

Para rastrear el lugar donde se encuentra el nanosatélite en el espacio, se emplea un GPS. Este dispositivo mantiene su eficacia puesto que el CubeSat se encuentra en LEO, por lo que se mantiene relativamente cerca del planeta. Al no encontrar un símbolo específico para el GPS, se ha optado por crearlo. Para ello, se crea un nuevo componente en el repositorio de Altium y se selecciona la opción de “Crear nuevo símbolo”.

Se ha optado por agrupar las alimentaciones por un lado, las tierras por debajo, los pines no conectados por encima y todas las señales ordenadas del 0 al 31 en los laterales. En la Figura 2.12 se puede ver la distribución de estos pines.

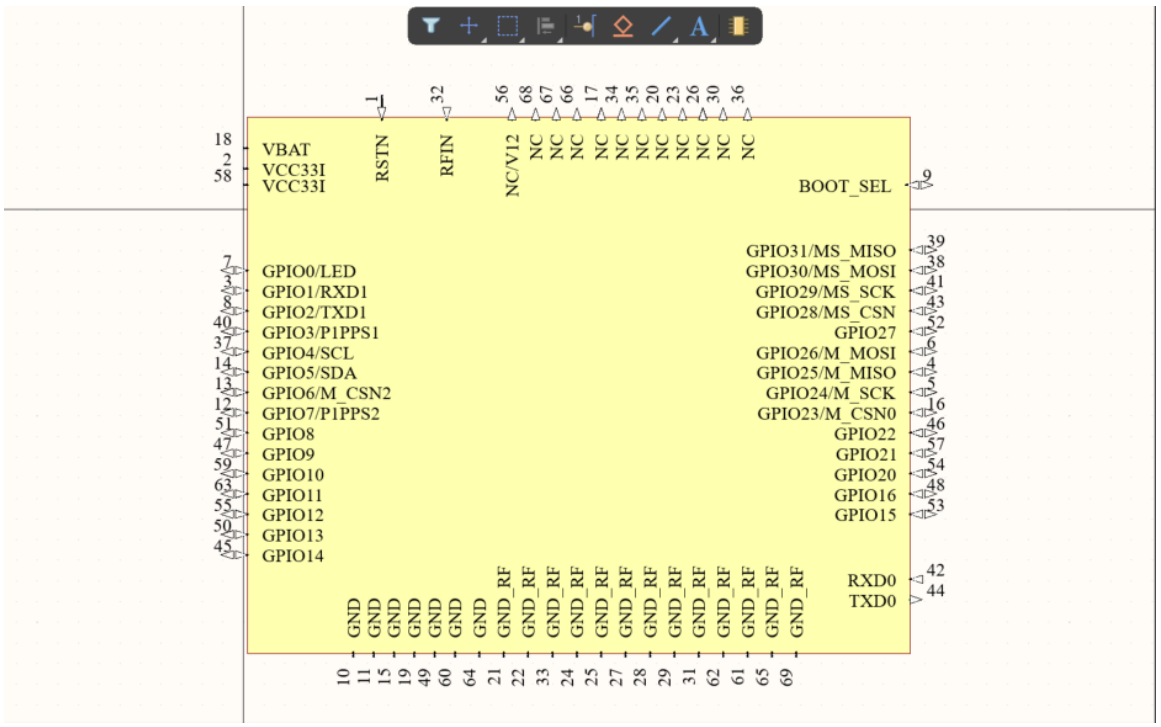


Figura 2.12: Vista del editor de componentes.

En la Figura 2.13 se puede observar el conexionado que tiene este GPS con el resto de componentes.

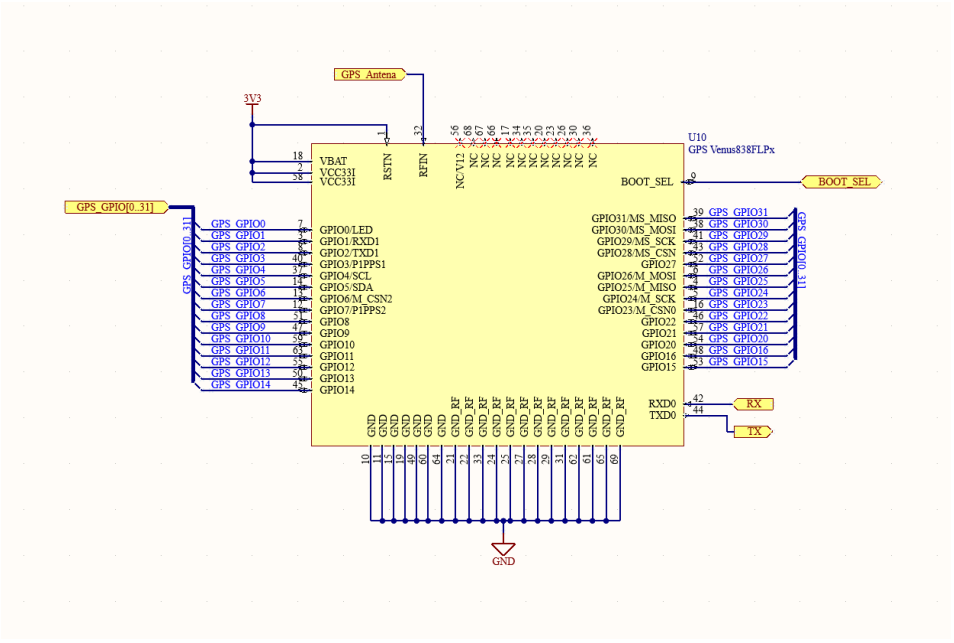


Figura 2.13: Esquemático del conexionado del GPS.

El GPS cuenta con 32 pines que se pueden configurar como entradas y salidas. Estos pines se conectan directamente al OBC. Además, hay un pin para recibir información directa de una antena externa.

2.1.9. Conexionado con el bus PCI/104

Además de realizar las diferentes conexiones con el OBC, es posible que algunos de los datos sean requeridos por otros subsistemas, por lo que para facilitar el acceso, se conectan al bus PCI/104. En la Figura 2.14 se muestra toda la información compartida al resto de subsistemas.

Algunos de los pines sirven de alimentación para otros elementos conectados, mientras que otros leerán las señales desde diferentes dispositivos.

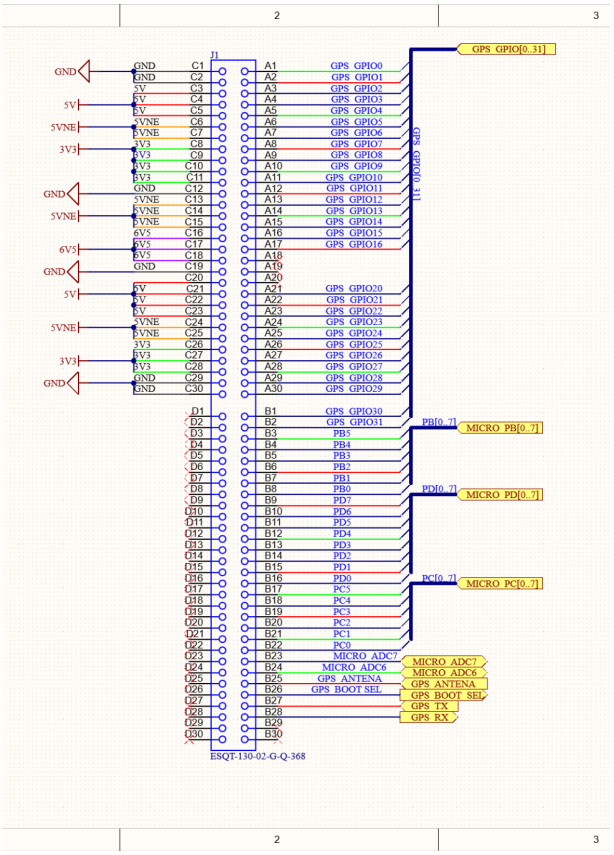


Figura 2.14: Esquemático del conector PCI/104.

Los pines de la fila D del conector PCI/104 se han reservado para el transceptor del nanosatélite. Este transceptor aún no ha sido definido totalmente, por lo que, para asegurar que existen suficientes pines disponibles, se han bloqueado estos. Se espera que, en futuras iteraciones, sea posible modificar el lugar de los pines teniendo en cuenta el transceptor, de manera que la modificación necesaria en la PCB sea la menor posible.

2.1.10. Conexionado con el conector del OBC

Además de conectarse mediante el PCI/104, las señales también llegarán al OBC, desde donde se procesarán para dar instrucciones al resto del satélite. En la Figura 2.15 se pueden observar sus pines.

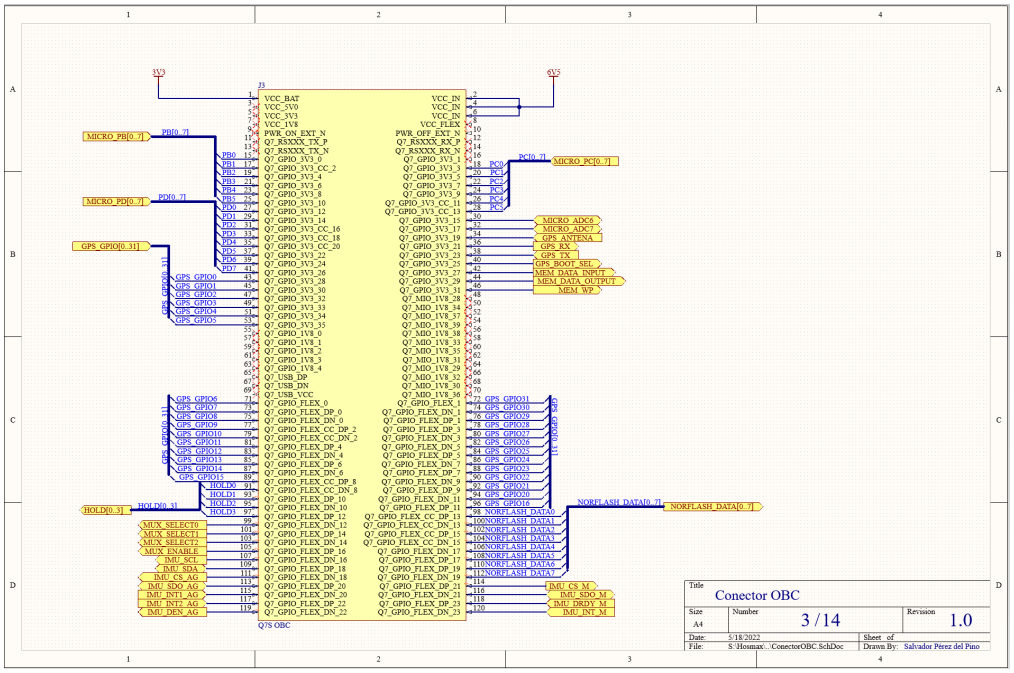


Figura 2.15: Esquemático del conector del OBC.

Todos los esquemáticos anteriores se pueden observar a gran tamaño y mejor resolución en el Anexo I. Además, el listado completo de materiales o *Bill of Materials* (BOM) se puede ver en el Anexo II.

2.2. Aspectos previos al diseño de la PCB

Una vez se han definido el tipo de conexiones que van a tener los componentes entre sí, es posible diseñar la PCB. Antes de avanzar hasta este punto, es necesario establecer una serie de pautas para el diseño de la misma:

- **Número de capas:** Determinar el número de capas exacto para la PCB previamente a su diseño es una tarea compleja, puesto que la implementación de una idea establecida de cómo colocar las pistas puede verse afectada a la hora de plasmar dicha idea en el diseño. Como aproximación, se considera que para establecer los buses de alimentación se emplean tres capas y para el resto de componentes, entre siete y diez capas. Se comienza con un total de diez capas y se añaden más en caso de que sea necesario.

- **Tamaño de capa:** La altura que tendrá cada capa dependerá de las capacidades que tenga el fabricante a la hora de preparar la placa. Por ello, se suelen emplear unas tablas prediseñadas que sirven de guía a la hora de definir esta dimensión. En este caso, se emplea la tabla de la empresa española Cipsa Circuits [26]. Existen múltiples tablas en función del número de capas a fabricar, por lo que, aunque sea un parámetro a tener en cuenta antes del diseño, los valores precisos se determinan una vez se tenga el número de capas final.

CIPSA

CONSTRUCCIONES ESTANDAR 12 CAPAS

ESPESOR NOMINAL	1.6 mm		2 mm		2.4 mm	
Cobre de base externo	18 µm	0,02	18 µm	0,02	18 µm	0,02
Prepreg	2 x 1080	0,13	2 x 1080	0,13	2 x 1080	0,13
Cobre de base interno	35 µm	0,04	35 µm	0,04	35 µm	0,04
Capa interna 2-3	0.10 (4 mils)	0,10	0.20 (8 mils)	0,20	0.25 (10 mils)	0,26
Cobre de base interno	35 µm	0,04	35 µm	0,04	35 µm	0,04
Prepreg	2 x 1080	0,13	2 x 1080	0,13	2 x 1080	0,13
Cobre de base interno	35 µm	0,04	35 µm	0,04	35 µm	0,04
Capa interna 4-5	0.10 (4 mils)	0,10	0.20 (8 mils)	0,20	0.25 (10 mils)	0,26
Cobre de base interno	35 µm	0,04	35 µm	0,04	35 µm	0,04
Prepreg	2 x 1080	0,13	2 x 1080	0,13	2 x 1080	0,13
Cobre de base interno	35 µm	0,04	35 µm	0,04	35 µm	0,04
Capa interna 6-7	0.10 (4 mils)	0,10	0.20 (8 mils)	0,20	0.25 (10 mils)	0,26
Cobre de base interno	35 µm	0,04	35 µm	0,04	35 µm	0,04
Prepreg	2 x 1080	0,13	2 x 1080	0,13	2 x 1080	0,13
Cobre de base interno	35 µm	0,04	35 µm	0,04	35 µm	0,04
Capa interna 8-9	0.10 (4 mils)	0,10	0.20 (8 mils)	0,20	0.25 (10 mils)	0,26
Cobre de base interno	35 µm	0,04	35 µm	0,04	35 µm	0,04
Prepreg	2 x 1080	0,13	2 x 1080	0,13	2 x 1080	0,13
Cobre de base interno	35 µm	0,04	35 µm	0,04	35 µm	0,04
Capa interna 10-11	0.10 (4 mils)	0,10	0.20 (8 mils)	0,20	0.25 (10 mils)	0,26
Cobre de base interno	35 µm	0,04	35 µm	0,04	35 µm	0,04
Prepreg	2 x 1080	0,13	2 x 1080	0,13	2 x 1080	0,13
Cobre de base externo	18 µm	0,02	18 µm	0,02	18 µm	0,02
		1,67		2,17		2,47

Figura 2.16: Especificaciones del fabricante para una configuración de 12 capas[1]. [27]

- **Anchura de pista:** Para determinar el ancho de pista que deben tener las señales, es necesario tener en cuenta el tamaño de capa y otros parámetros como la corriente que va a circular a través de la pista. La fórmula con la que se halla el área mínima es la siguiente:

$$A\,[mils^2] = k_3 \cdot \sqrt{\frac{I[A]}{k_1 \cdot \Delta T^{k_2}}} \qquad (1)$$

Según IPC-2221 [28], estos valores de k dependen de si las pistas son externas o internas. En la Tabla 2.4 se muestran sus valores. I es la intensidad que pasa por la pista, y ΔT es el incremento de temperatura máximo que queremos restringir.

	Pistas externas	Pistas internas
k_1	0,048	0,024
k_2	0,44	0,44
k_3	0,725	0,725

Tabla 2.4: Valores de las constantes k_i.

[1] Un mil es la milésima parte de una pulgada, lo que equivale a 25,4 micrómetros.

Una vez tenemos el área calculada con la fórmula (1), el ancho de pista mínimo se obtiene de:

$$w[mils] = \frac{A[mils^2]}{h[\frac{oz}{ft^2}] \cdot 1{,}378[\frac{mils}{oz}]} \quad (2)$$

Donde *h* es el grosor de la capa.

En este punto, es necesario conocer la intensidad máxima que puede circular por cada una de las pistas. El peor caso es el de la alimentación por parte de las baterías. Sumando las intensidades de los diferentes convertidores, la intensidad máxima se aproxima a los 10 amperios. Como la corriente en este punto es elevada, el valor del ancho de pista calculado con la fórmula (2) se aproxima a los 200 mils (5,08 mm). En la PCB, es una cantidad demasiado grande para trabajar correctamente, por lo que se ha optado por realizar planos de potencia que se mostrarán más adelante. En puntos más pequeños, donde se trabaja con señales de voltaje y la corriente es despreciable o muy reducida, se emplean pistas de 10 mils (0,254 mm) o 5 mils (0,127 mm).

- **Vías:** Para las vías, se han diseñado dos plantillas específicas que se pueden observar en la Figura 2.17 y 2.18.

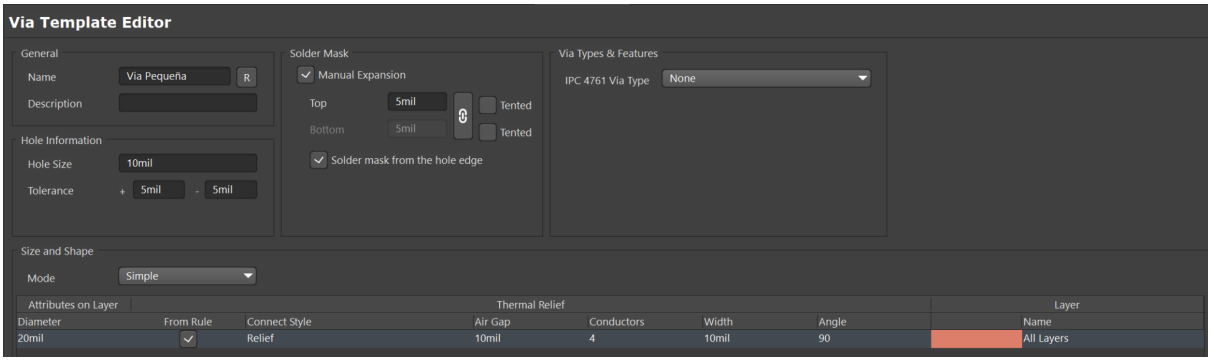


Figura 2.17: Parámetros de la vía pequeña.

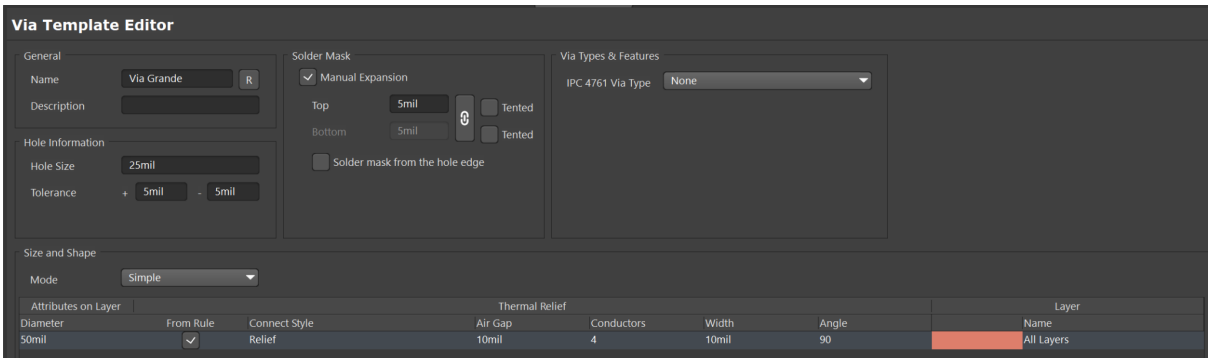


Figura 2.18: Parámetros de la vía grande.

Los términos grande y pequeño se emplean para una mayor facilidad a la hora de preparar las pistas. Las vías pequeñas se utilizan en pistas cuya anchura es menor que 20 mils (0,508 mm). Las vías grandes, para pistas mayores o iguales a 20 mils.

Existen tres clasificaciones de vías a usar: las que atraviesan toda la placa, las que comienzan en uno de los extremos hacia el interior de la placa o las vías intercapas que no rozan la superficie. Se emplea una combinación de estos tres tipos para optimizar el diseño.

- **Conector PCI/104:** Para poder realizar apilamientos de placas entre sí para futuras configuraciones del satélite, se ha optado por emplear el factor de forma que tiene el estándar PCI/104. En la Figura 2.19 se muestra el factor de forma provisto desde el repositorio de Altium.

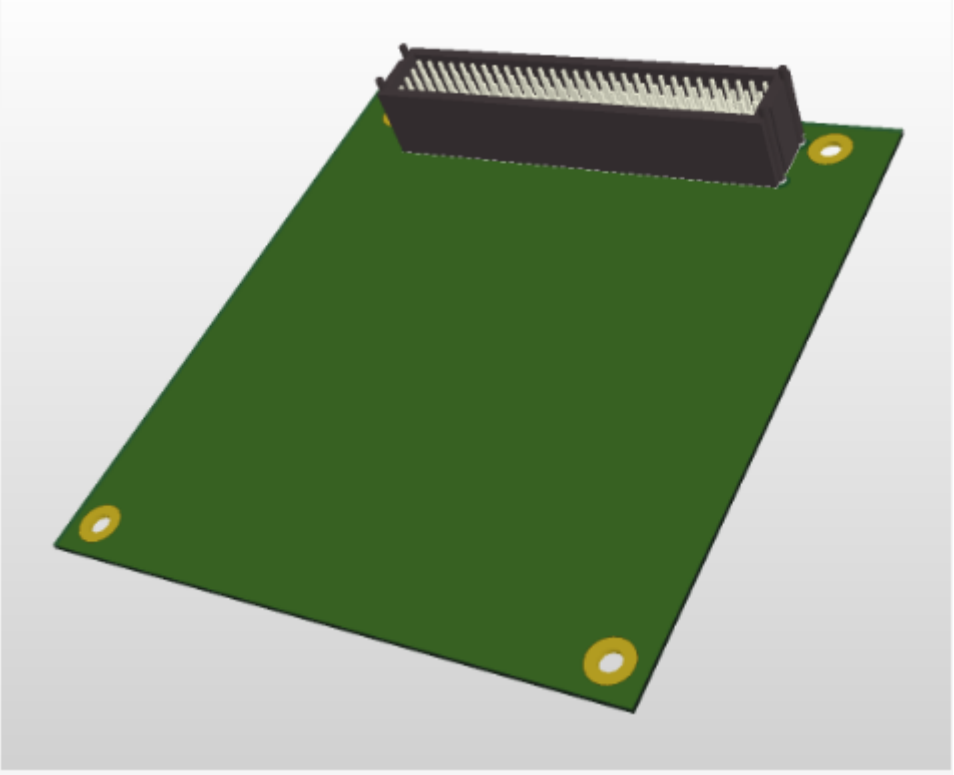


Figura 2.19: Factor de forma del estándar PCI/104 (cara inferior). [29]

El repositorio cuenta con el diseño de la placa según este formato y un esquemático de acuerdo al conector. Ambos archivos se emplean para simplificar el proceso y evitar errores a la hora de realizar el diseño externo de la PCB. El esquemático original difiere del mostrado en la Figura 2.14, debido a que el planteamiento inicial de este esquemático contaba con una pequeña jerarquía interna, además del uso de puertos que no proceden en nuestro caso. Tras eliminar dichos puertos y organizar los pines en función de nuestras necesidades, se obtiene el esquemático de la Figura 2.14.

- **Ordenador de a bordo:** El OBC se colocará encima de la placa LoMo a través de un conector *mezzanine*. En la galería de Altium, se encuentra disponible el modelo 3D y la huella de este conector, por lo que se ha empleado el esquemático diseñado de la Figura 26, combinado con la huella obtenida de la galería. El OBC debe colocarse en la cara superior, de manera que se encuentre lo más cerca posible del puerto de acceso. Este puerto de acceso se sitúa en uno de los laterales de la placa, puesto que va a ser el único lado donde, previo al lanzamiento, es posible su desmontaje para acceder al interior del satélite y realizar pequeñas modificaciones. Por tanto, el espacio de la cara superior de LoMo se verá limitado por esta ocupación.

2.3. Diseño de la PCB

2.3.1. Colocación de los componentes

Una vez se han establecido los requisitos para este prototipo y dibujado los esquemáticos correspondientes, se diseña la PCB.

Se ha escogido el EPS de baja potencia como primer elemento a colocar por su sencillez con respecto al resto de componentes (la única señal que se dirige al conector PCI/104 es la de alimentación, además de no conectarse directamente al OBC exceptuando el bus de 6,5 V). Como el EPS obtiene energía de una fuente externa, es necesario colocar un conector en uno de los laterales diferentes al puerto de acceso. En la Figura 2.20 se puede observar su colocación en la cara inferior de la placa.

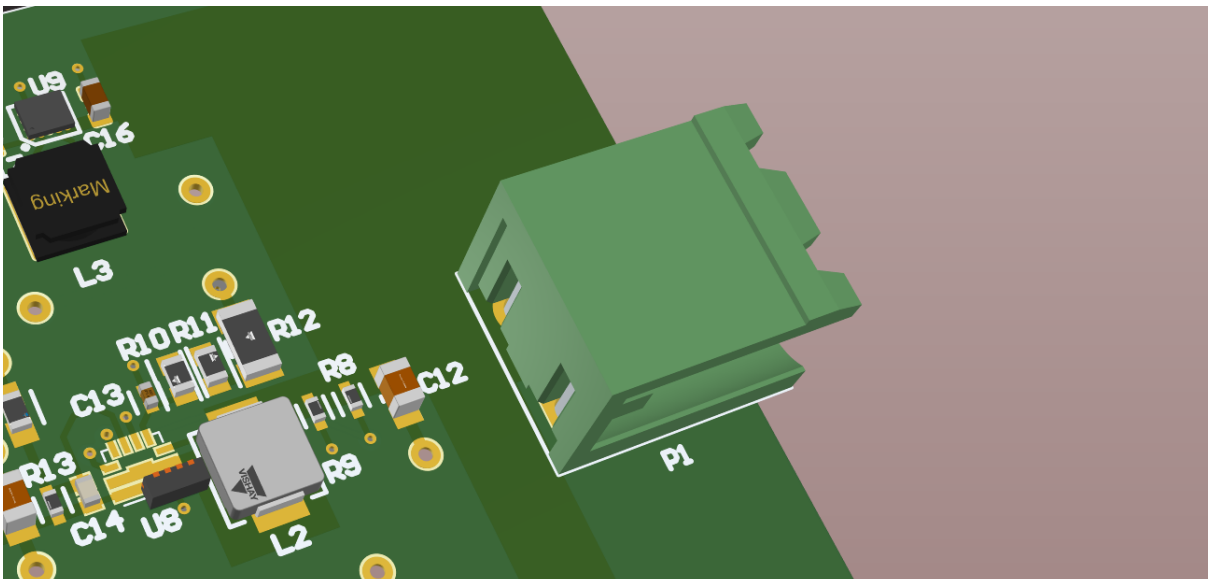


Figura 2.20: Conector de las baterías visto en 3D.

Una vez establecido el lugar de referencia del voltaje de las baterías, es necesario colocar los diferentes buses de potencia. Se realiza un diseño completo para cada bus antes de pasar al siguiente para obtener la información del espacio disponible cada vez que se diseña uno.

En la Figura 2.21 se destacan las áreas donde se sitúan los buses de potencia.

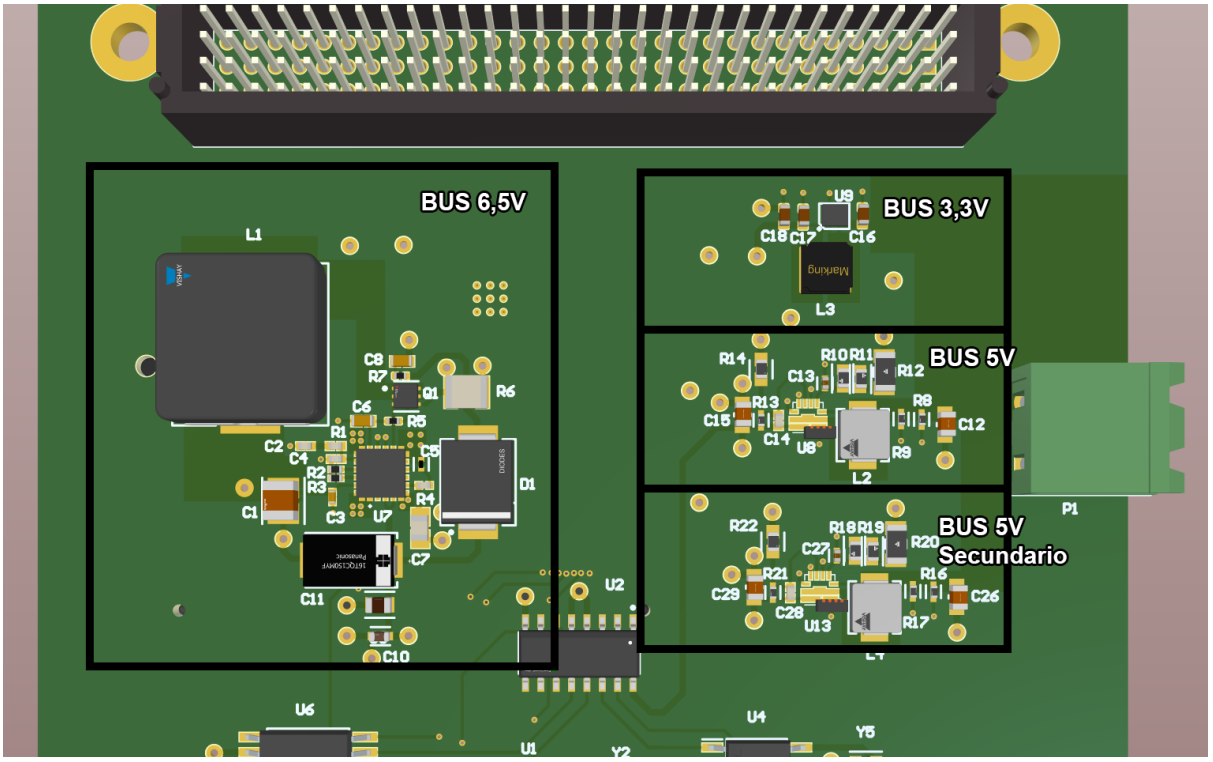


Figura 2.21: Distribución del EPS de baja potencia.

Se ha realizado esta configuración para separar la parte de mayor consumo (alimentación del ordenador de a bordo) del resto de buses. De esta manera, se distribuye mejor el calor generado al no concentrarse en un único punto.

Como se puede observar en la Figura 2.21, la distribución del EPS requiere un uso aproximado de la mitad del área disponible en la cara inferior.

En el planteamiento del problema inicial, se esperaba colocar las memorias del segundo experimento en la cara superior de la placa, pero el aumento del número de capas debido a la complejidad que ofrecen el GPS junto con el microcontrolador tienden a centrar la parte superior únicamente en estos dos circuitos, junto con la IMU. Por tanto, las memorias a experimentar junto con el demultiplexor se han colocado en la superficie inferior.

En la Figura 2.22 se puede observar cómo han sido colocadas las diferentes memorias.

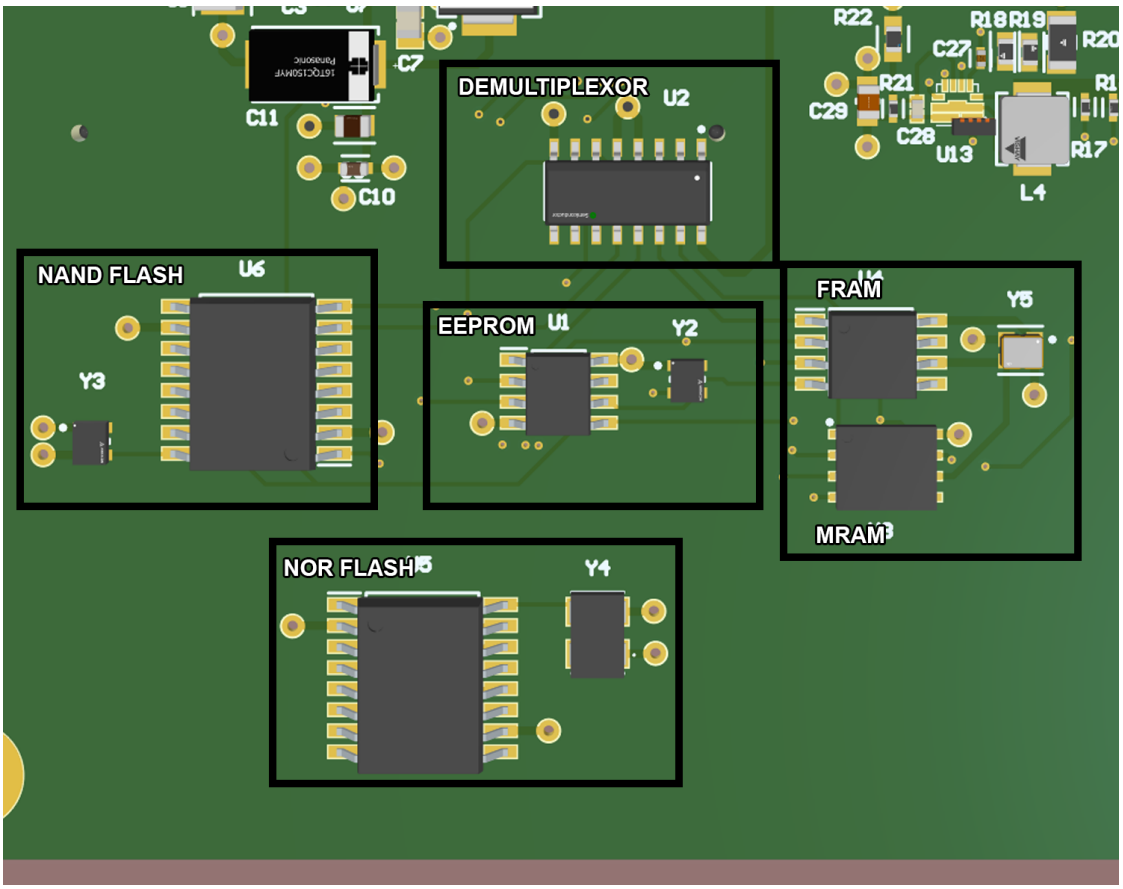


Figura 2.22: Distribución de las memorias en la cara inferior.

Tras determinar el espacio ocupado en la cara inferior, se distribuyen los elementos previstos para la superior. En la Figura 2.23 se puede observar la posición del GPS ligeramente alejada con respecto a la del microcontrolador e IMU. Esto se debe a que por las características de su huella, es necesario trabajar con varias capas en las proximidades. Esto se detalla en el siguiente apartado.

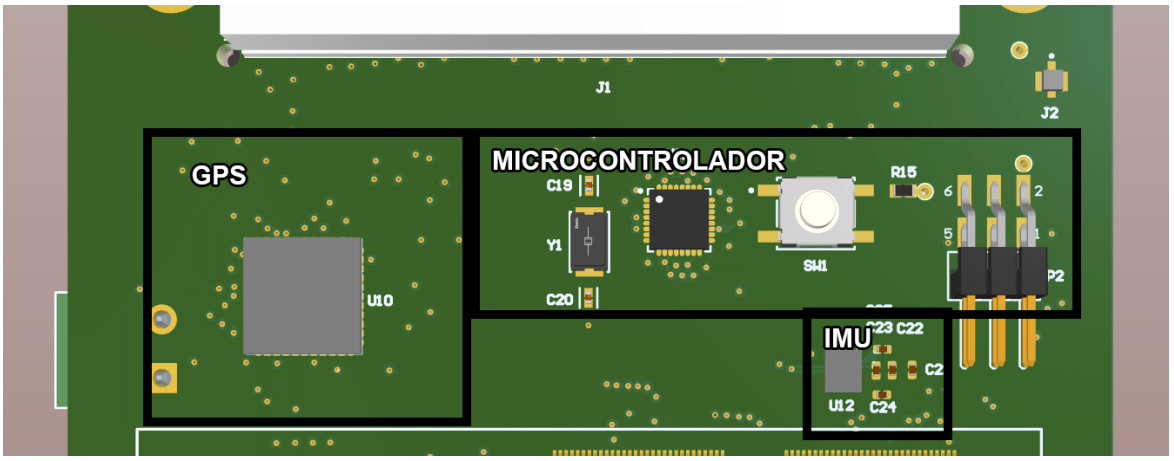


Figura 2.23: Distribución de circuitos en la cara superior.

El espacio reservado para el OBC tiene su conector en el lugar donde se va a situar encima de LoMo. Este área no puede ser invadida por otros componentes, puesto que ambas placas van a estar casi en contacto. Sin embargo, pueden atravesar pistas y vías por el área reservada.

A continuación se detallarán los componentes, conexiones y capas necesarias para el diseño.

2.3.2. Elaboración en detalle

Una vez se han definido dónde se colocarán los componentes, se procede al conexionado de todos sus pines. En las Figuras 2.24 y 2.25 se muestra la capa inferior de dicha configuración.

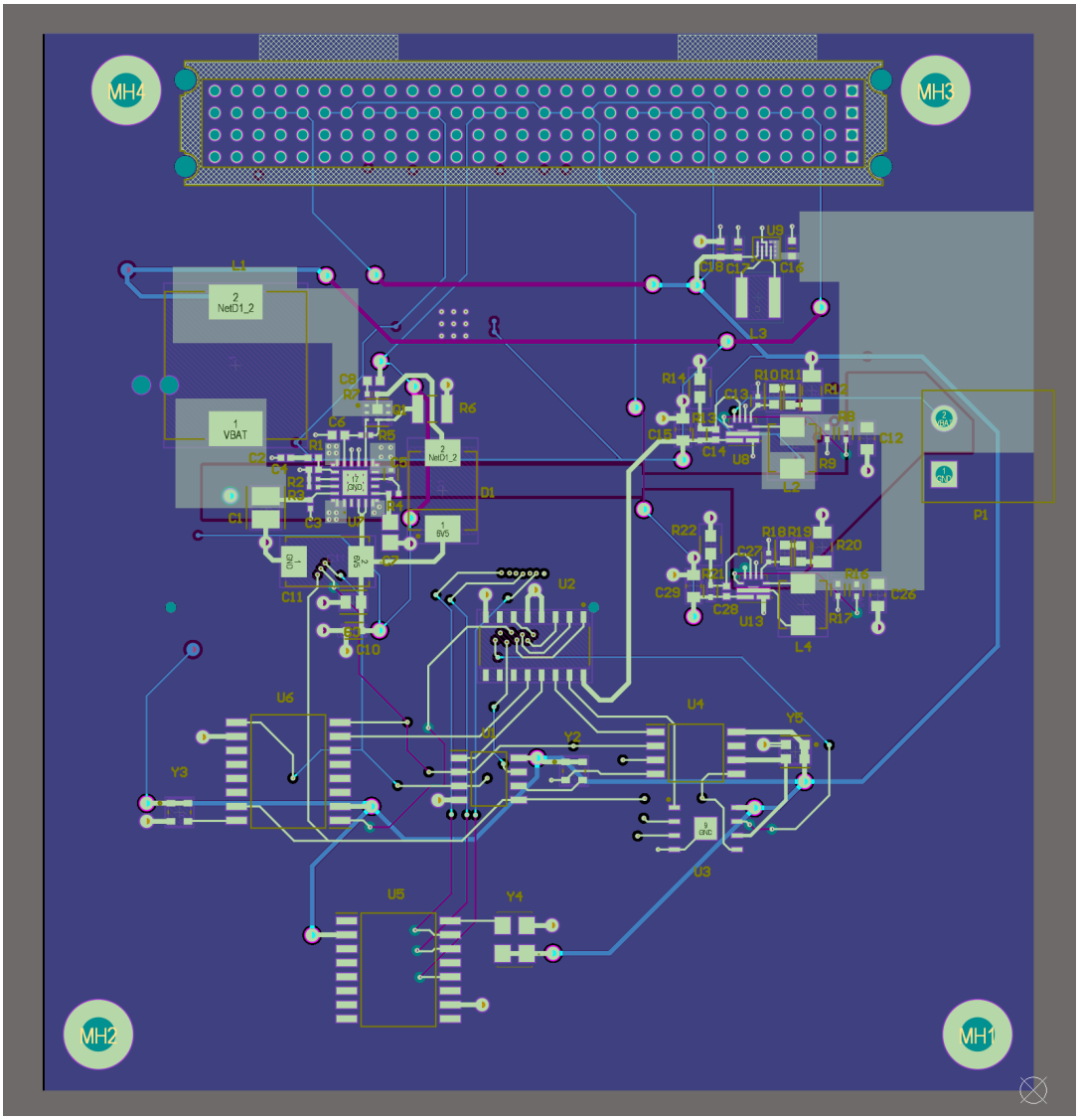


Figura 2.24: Vista inferior (modo multicapa).

Los detalles de cada capa individual se pueden apreciar en el Anexo III.

En el modo multicapa se pueden visualizar las diferentes pistas en función de su capa (diferentes colores). Ocultando las capas innecesarias, es una manera sencilla de observar cómo se dirige la señal a través de la placa.

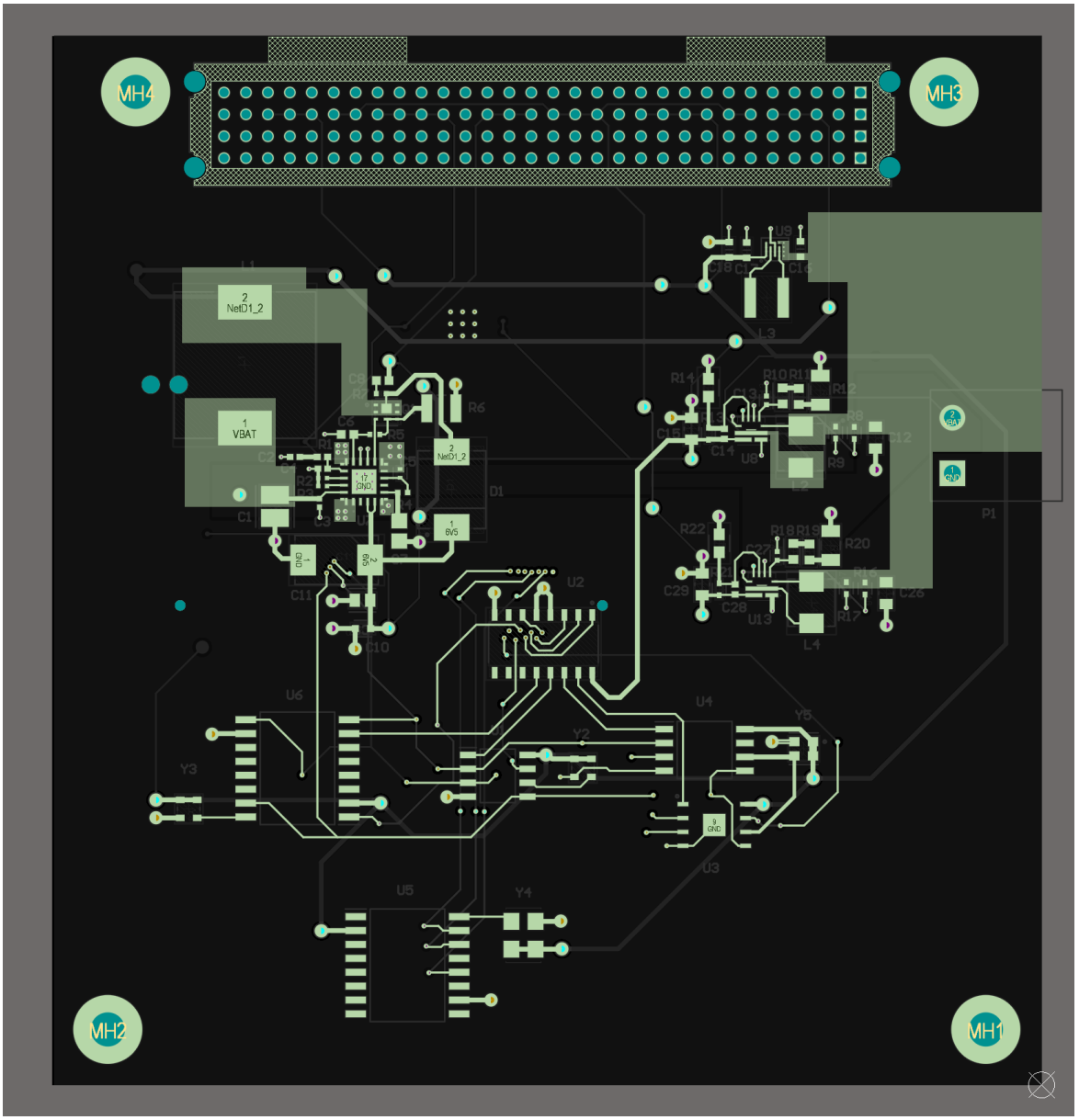


Figura 2.25: Vista inferior (modo monocapa).

Para alimentar los convertidores, es necesario recibir la energía de las baterías. Como este camino lo recorren diferentes convertidores a la vez, es necesario sobredimensionar para evitar que ninguna pista sea dañada. En la Figura 2.26 se muestra cómo se añade un plano de potencia.

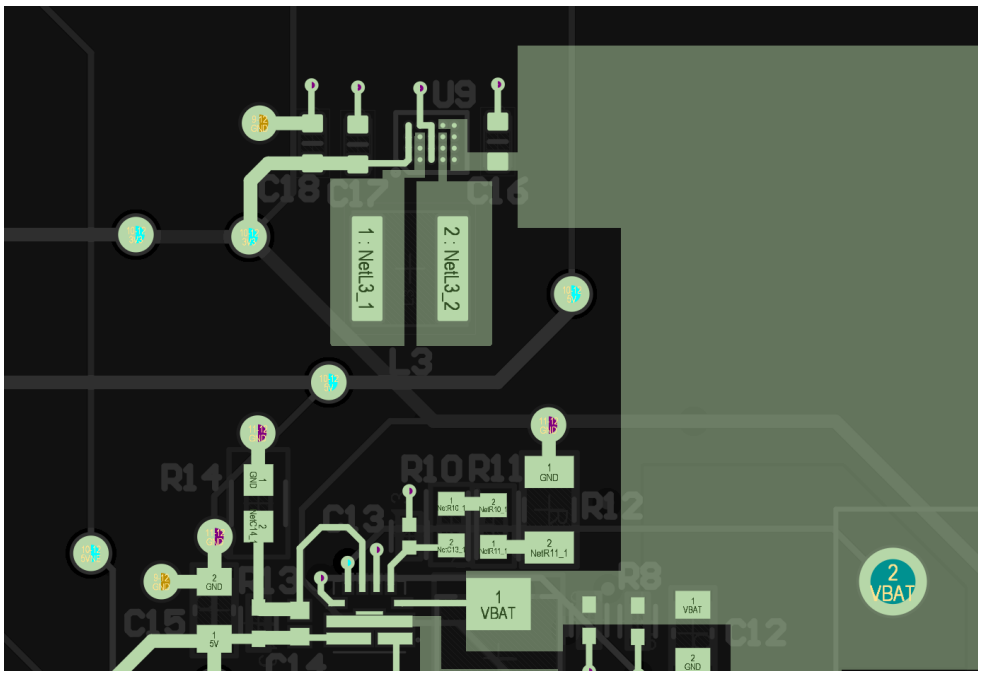


Figura 2.26: Plano de potencia de las baterías.

Este plano se crea mediante la elaboración de un polígono con la misma red asignada a las baterías. Se ha intentado optimizar el espacio de manera que exista una distancia de separación con respecto a otras pistas o *pads*, pero con una superficie lo más grande posible.

Tal y como se muestra en la Figura 2.27, los convertidores de 3,3 V y 5 V primario y secundario están enlazados directamente con esta alimentación.

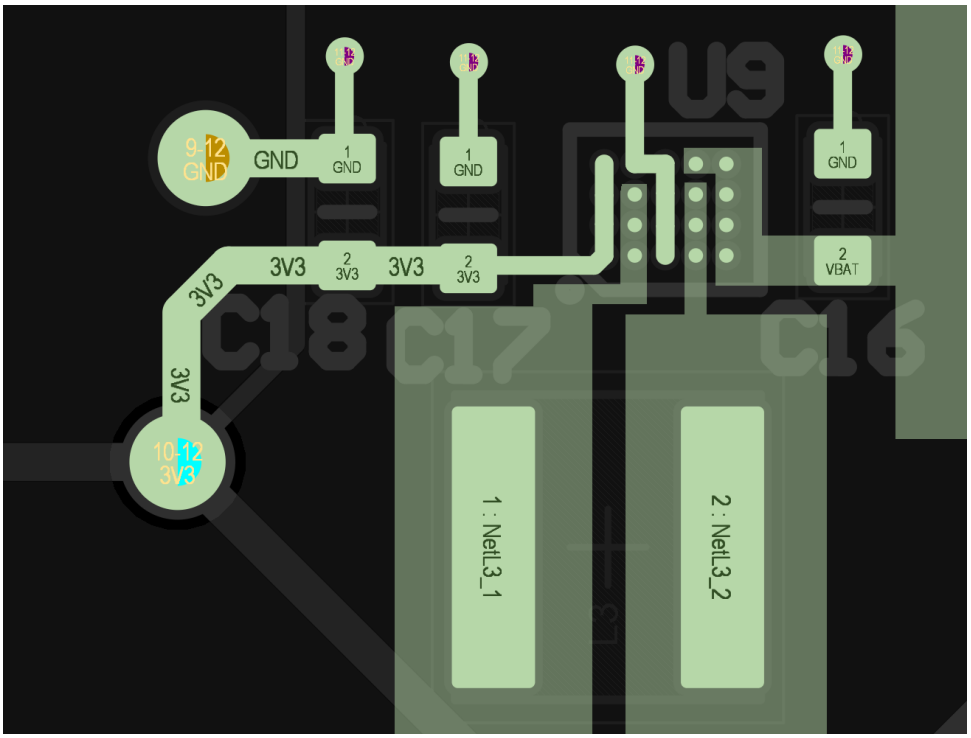


Figura 2.27: Circuito de conversión a 3,3 V.

El bus de alimentación de 3,3 V es el más sencillo de los utilizados. Consiste en el propio convertidor *Buck-Boost* (TPS630242YFFR), una bobina para producir la reducción y unos condensadores de acoplo y desacoplo. Al igual que se aplica con la alimentación de las baterías, la bobina también emplea un plano para sus extremos (Figura 2.27), puesto que al conmutar en este caso a una frecuencia de aproximadamente 2,5 MHz es necesario asegurar la integridad de la señal en este punto.

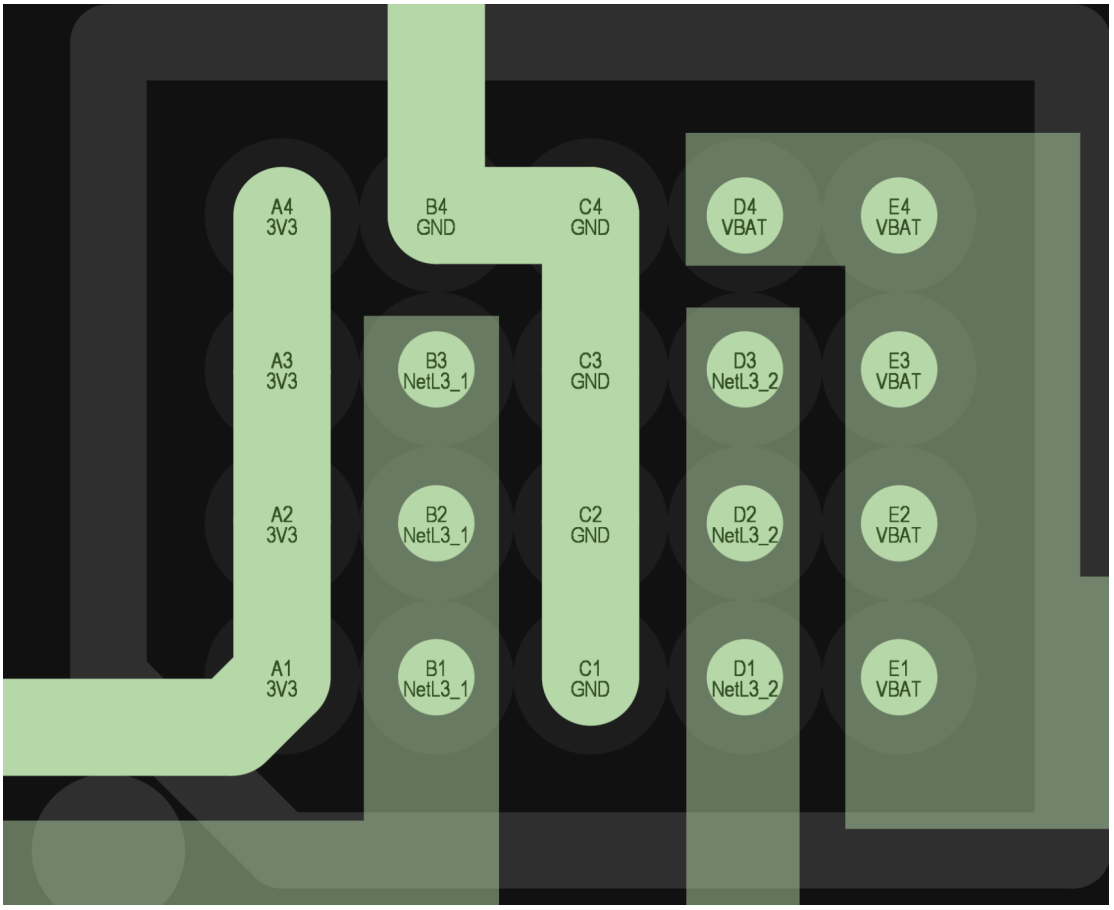


Figura 2.28: Pines del convertidor de 3,3 V.

Por las características que tiene la distribución de pines en el convertidor (Figura 2.28), es posible colocar esos planos con señales o alimentación sin problema. Para la tierra se emplea una pista que conecta con una vía directa al plano de la tierra de potencia. En el caso de la salida, tras pasar por los condensadores de desacoplo, viaja a la capa de potencia donde distribuirá las líneas necesarias para alimentar con 3,3 V. Como el convertidor tiene una corriente máxima de 0,2 A, se puede emplear vías de 10 mils (0,254 mm) sin problema.

El bus de 5 V principal y secundario tienen la misma forma en la PCB. Los condensadores de acoplo y desacoplo están colocados lo más cercano posible a los pines de entrada y salida de alimentación. Tras esto, se colocan las resistencias y condensadores necesarios para la conversión. Al igual que con el circuito de 6,5 V, se ha utilizado planos en los dos *pads* de la bobina conmutadora para mejorar la integridad de la señal. En la Figura 2.29 se puede observar la distribución de este bus en la capa inferior.

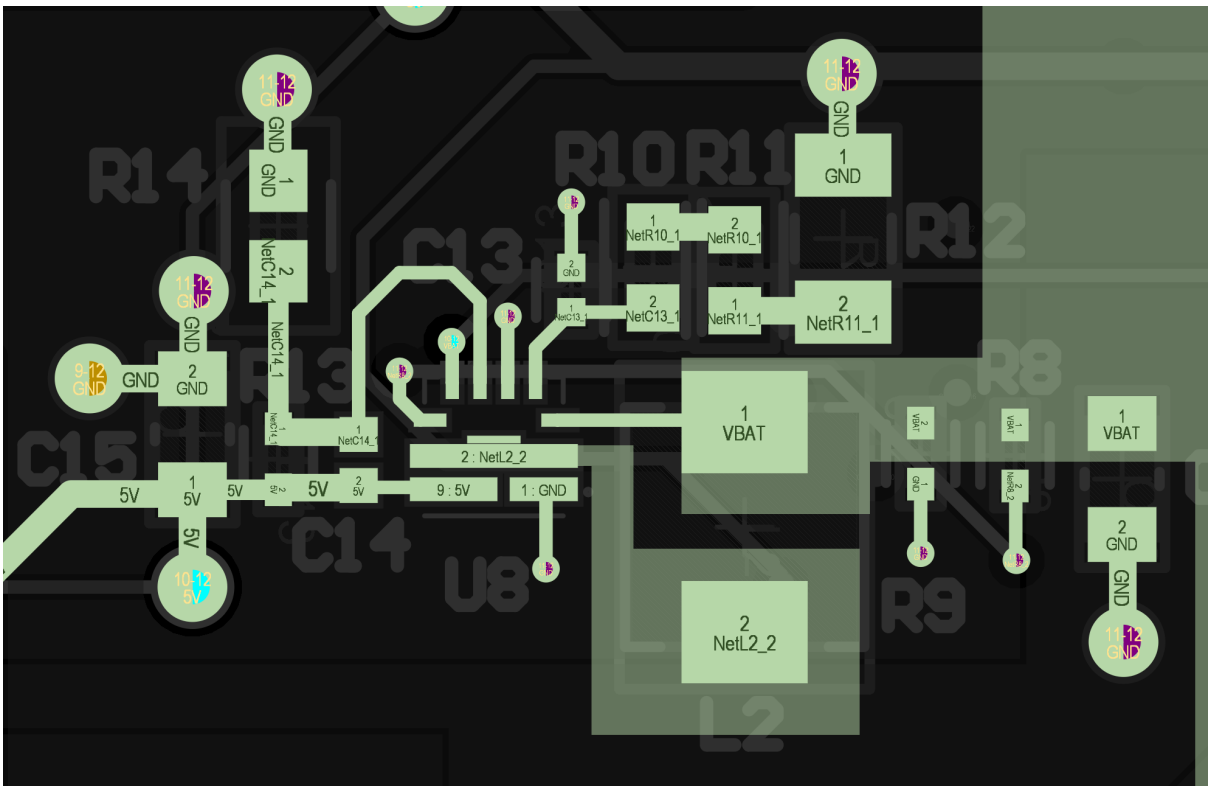


Figura 2.29: Circuito de conversión de 5 V.

Una vez preparadas las alimentaciones, se diseña el circuito de los demás componentes, de manera que se utilice primero el espacio necesario para conectar cada circuito integrado con sus componentes pasivos y más tarde, conectar la alimentación necesaria para dicho integrado. De esta manera, el espacio no se ve limitado previamente a la colocación de las pistas.

El siguiente circuito a conectar en la cara inferior es el demultiplexor. Este circuito tiene como entrada las señales del ordenador de a bordo que se colocarán más adelante. Las salidas corresponden al pin CS de cada memoria, por lo que se coloca una pista hacia cada una de ellas. En la Figura 2.30 se puede observar cómo quedan dichas conexiones.

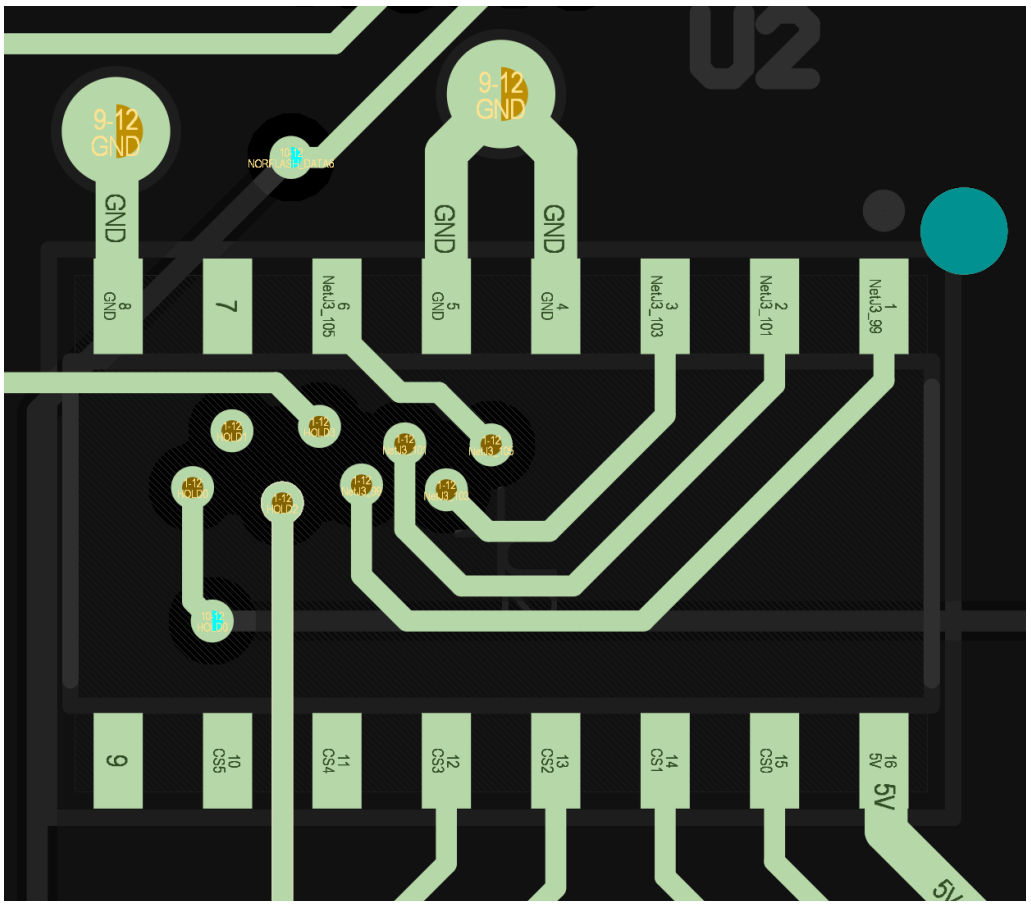


Figura 2.30: Pistas del demultiplexor.

Para las memorias, primero se realiza la conexión con su reloj para colocar la pista lo más cerca posible y tener una señal de reloj más fiable. En las Figuras 2.31, 2.32, 2.33 y 2.34 se pueden observar estas pistas.

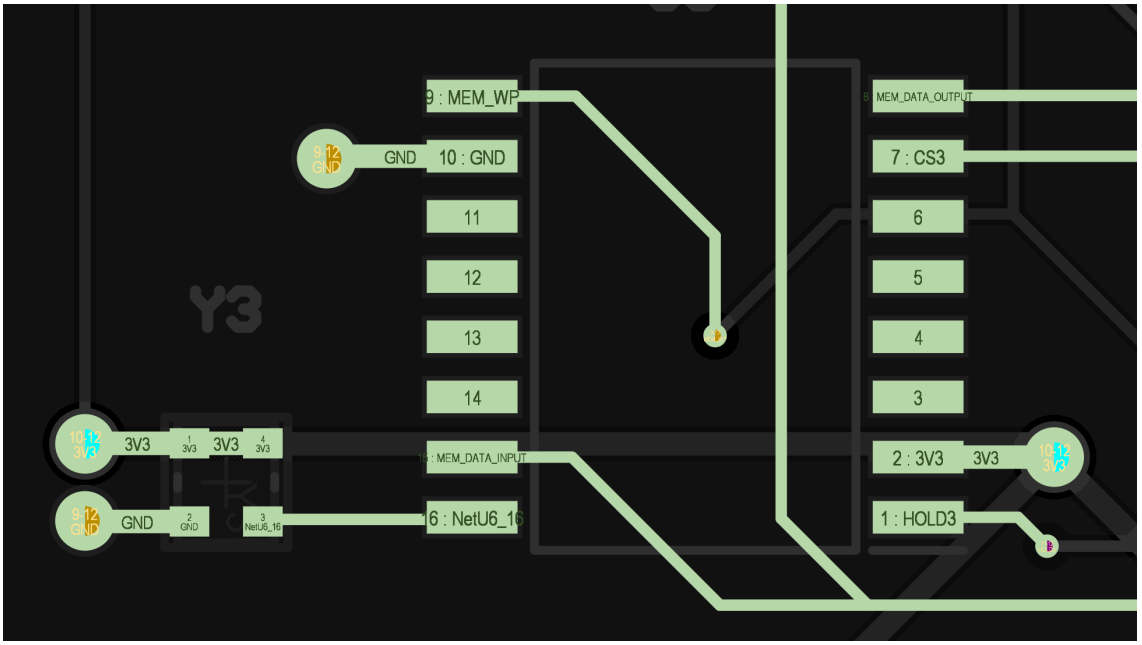


Figura 2.31: Memoria NAND FLASH junto con su reloj.

Para la memoria NAND FLASH, en la Figura 2.31 se observa el pin CS mencionado anteriormente, además de llevar su pin de protección de escritura (WP) a través de otra capa y los pines de entrada y salida de datos a través de una misma red de pistas. En algunos casos, estos pines atraviesan pads de otras memorias como la de la Figura 2.32, de manera que se establezca una única pista que lleve toda la información. Este método hace que la pista tarde un poco más en transmitir los datos, pero elimina la necesidad de colocar una o varias pistas de la memoria al conector.

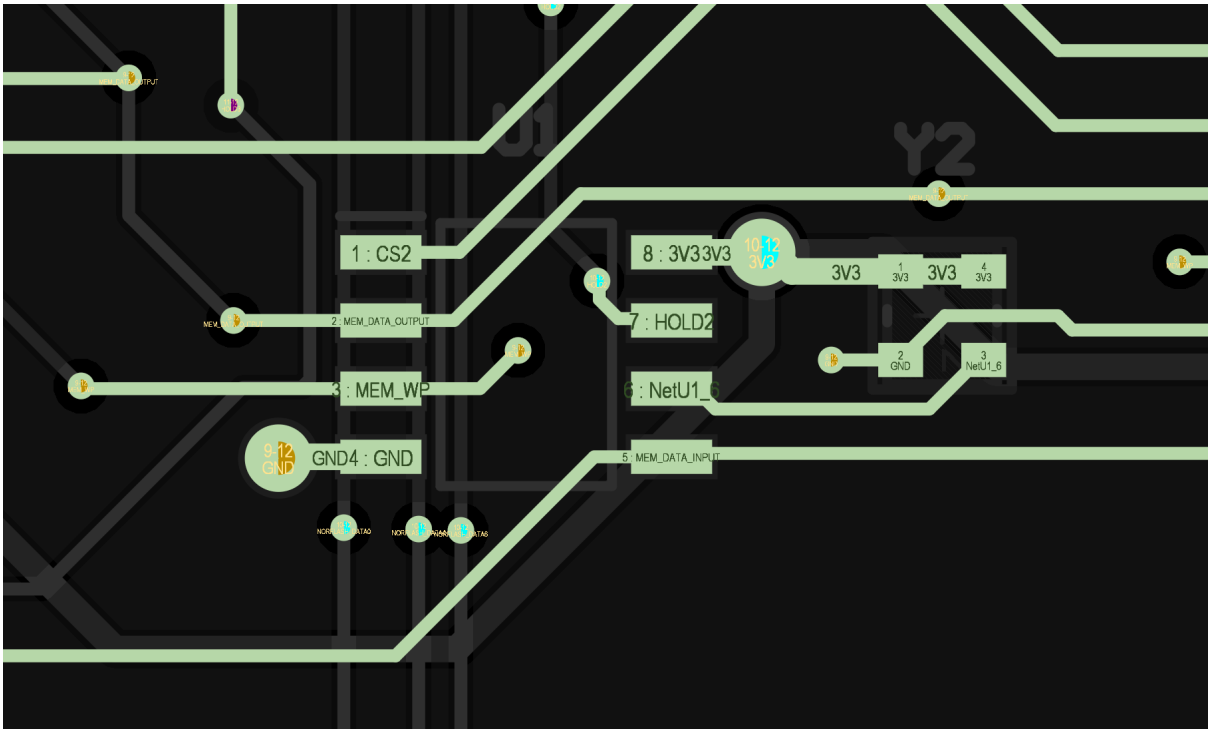


Figura 2.32: Memoria EEPROM junto con su reloj.

Para el caso de la memoria NOR FLASH, todos los pines de información se llevan directamente al conector del OBC, por lo que no existe la necesidad de enlazar ninguna pista con las demás memorias. Esta memoria también lleva su reloj asignado.
En la Figura 2.33 se muestra el resultado de colocar las pistas.

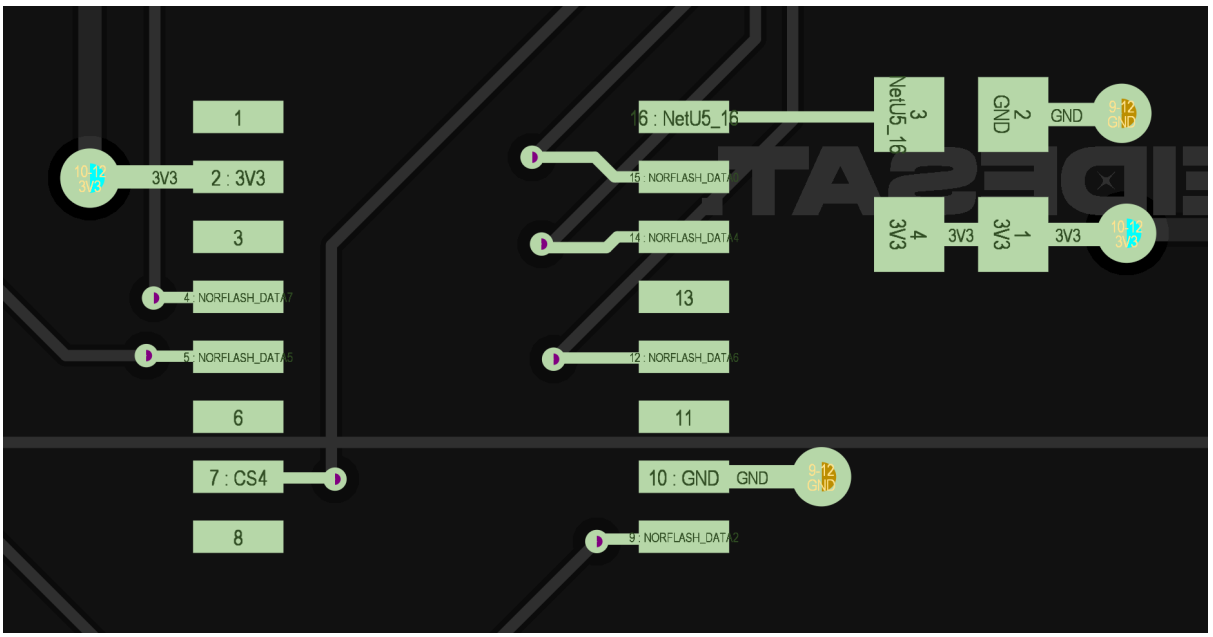


Figura 2.33: Memoria NOR FLASH junto con su reloj.

Para el caso de las memorias MRAM y FRAM, estas se han colocado juntas para compartir un único reloj y aumentar el espacio disponible en la placa. También comparten la entrada y salida de datos del protocolo SPI. En la Figura 2.34 se muestra el resultado de colocar sus pistas.

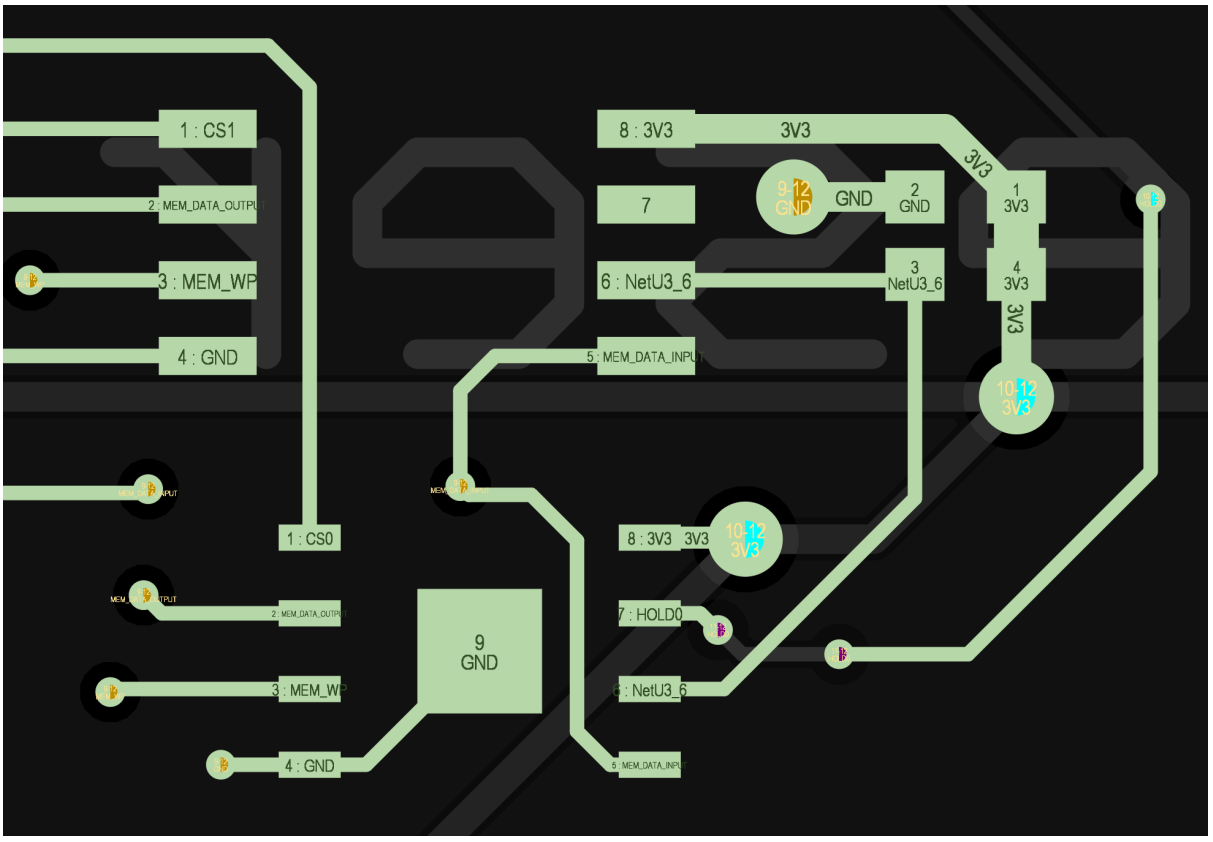


Figura 2.34: Memorias MRAM y FRAM junto con su reloj compartido.

Una vez se ha completado la colocación de pistas en la cara inferior, se plantea el diseño de la cara superior. Los elementos de mayor a menor complejidad son: el GPS, el microcontrolador y la IMU. Por tanto, se comienza a crear las pistas de los elementos con mayor complejidad, dejando el espacio que vaya restando a los siguientes.

Para el GPS, es necesario emplear diferentes capas debido a la composición de sus pines. Siguiendo las recomendaciones de Zach Peterson [30], la manera más óptima de distribuir los pines con el encapsulado BGA, es empleando una gran cantidad de vías hacia capas internas que redirigen las señales. En este caso, el encapsulado es una mezcla de pines internos tipo bola de BGA con pads externos tipo LCC. En la Figura 2.35 se puede observar la distribución de estas pistas y vías.

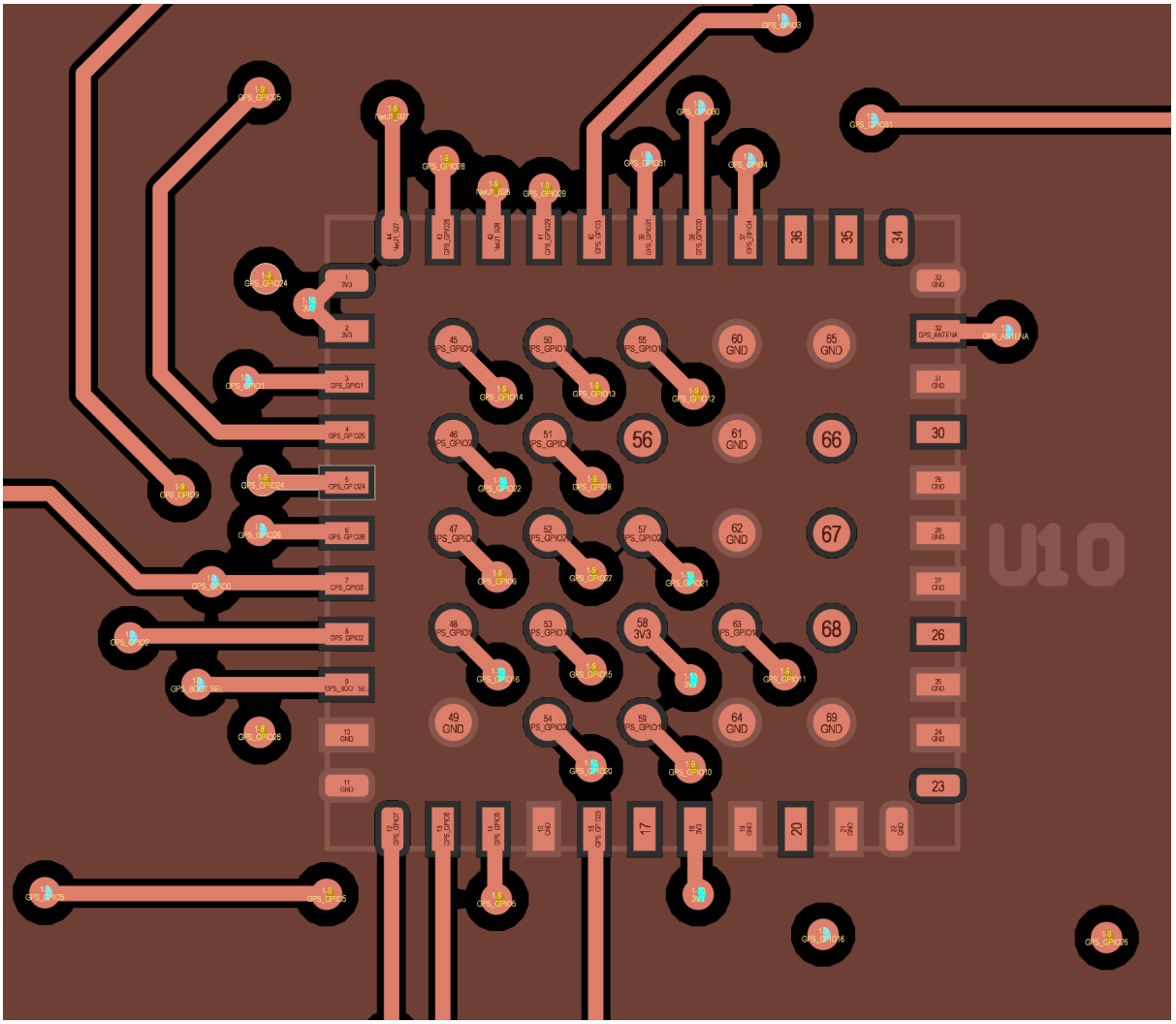
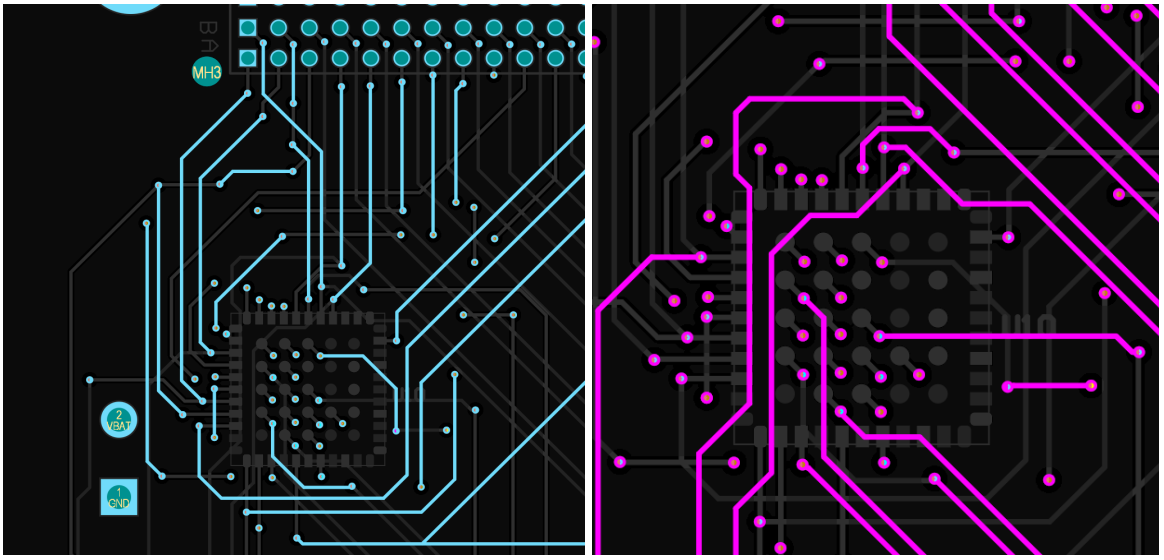


Figura 2.35: Pistas y vías conectadas al GPS.

La idea de esta huella era dividir las filas y columnas de pines con diferentes capas: las más externas, asociadas con la segunda capa; las siguientes más internas, con la tercera, etc. Sin embargo, la disposición de pines que tiene este componente no sigue un orden establecido, por lo que próximo al pin GPIO0 puede encontrarse cualquier otro número no consecutivo.

Por ello, las capas intermedias han sido mezcladas en función de la utilidad que se le puedan dar en cuanto a pistas más cortas o saltos de capas mediante la adición de más vías. En las Figuras 2.36 y 2.37 se puede observar cómo se utiliza este método.



Figuras 2.36 y 2.37: Combinaciones de pistas intermedias para lograr el conexionado del GPS.

Tras establecer el circuito del GPS, se continúa con el del microcontrolador. A diferencia del GPS, los pines establecidos en el microcontrolador no suponen un problema en cuanto a su orden. Por tanto, al situar vías alrededor de él, la mayoría de las pistas se dirigen directamente al pin correspondiente en el conector. A su lado, se coloca la señal de reloj lo más próxima posible para mejorar la estabilidad de la señal. Esto se puede observar en la Figura 2.38.

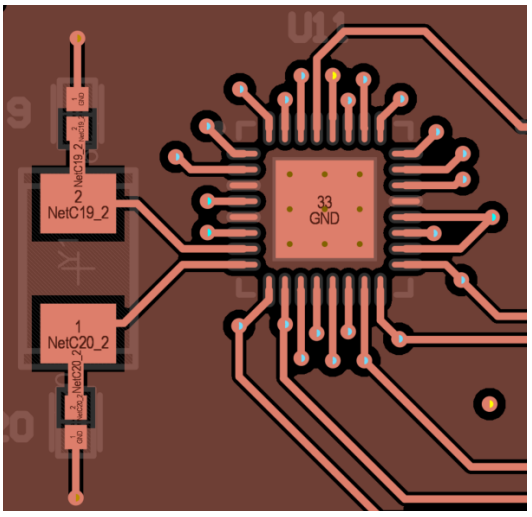


Figura 2.38: Pistas del microcontrolador.

Las pistas dirigidas directamente de la Figura 2.39 comparten capa con el GPS. Aun así, no existe un conflicto entre ellas dada la colocación de los componentes y el uso del GPS de diferentes capas distintas de esta.

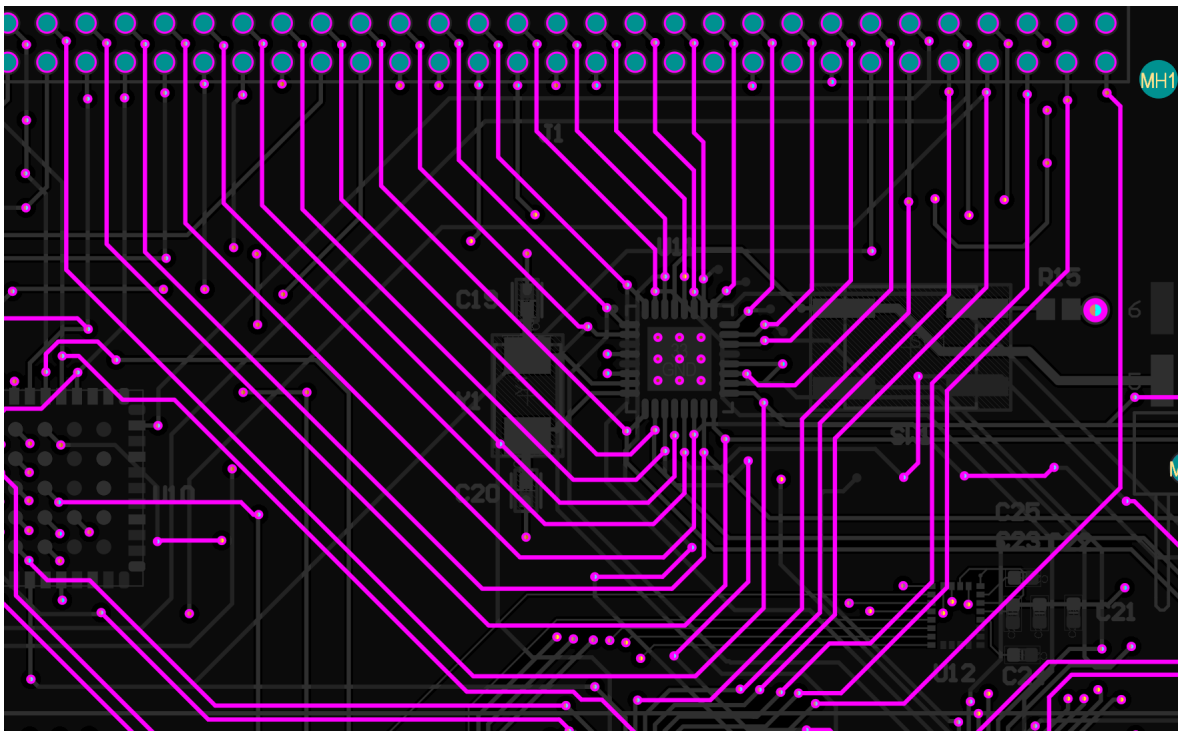


Figura 2.39: Pistas internas del microcontrolador.

Para evitar bloqueos en el programa del microcontrolador se emplea un botón, el cual activa la señal de reset. Este botón lleva una resistencia de pull-up que mantiene la entrada del pad con un valor constante en todo momento y evita un punto flotante. La señal de reset se envía directamente al microcontrolador tal y como se muestra en la Figura 2.40.

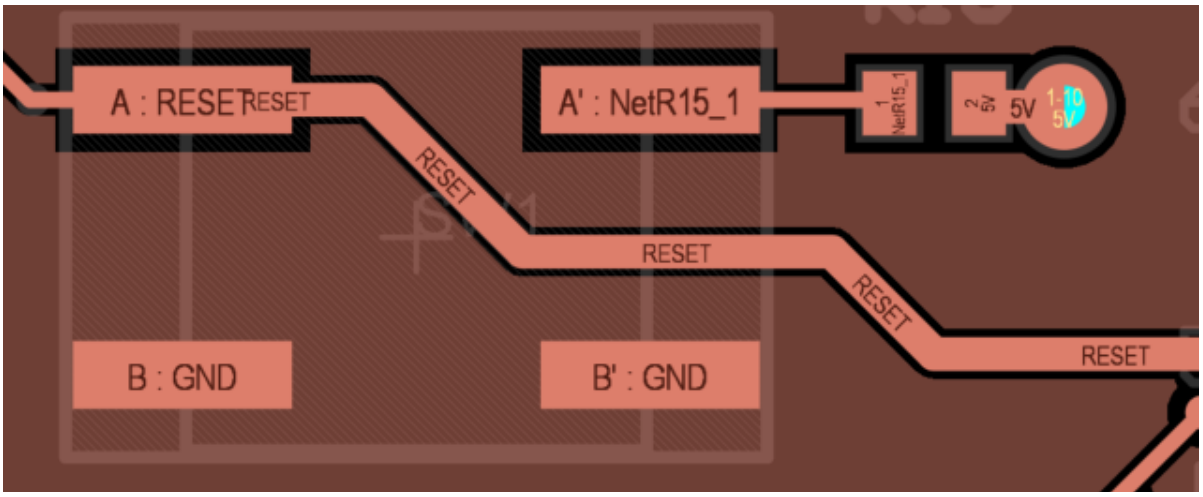


Figura 2.40: Interruptor de reset.

Además del reset, para esta iteración se va a colocar un conector de programación del microcontrolador. Este conector tiene los pines necesarios para poder enviar un programa escrito en C# o sus variantes compatibles con ATMEGA328P. Por tanto, se colocan las pistas directamente hacia el microcontrolador. En la Figura 2.41 se observa que el pin PB3 se sitúa

por encima, alargando la pista. Esto se debe a que es preferible evitar el propio conector debido a las posibles EMI que se produzcan.

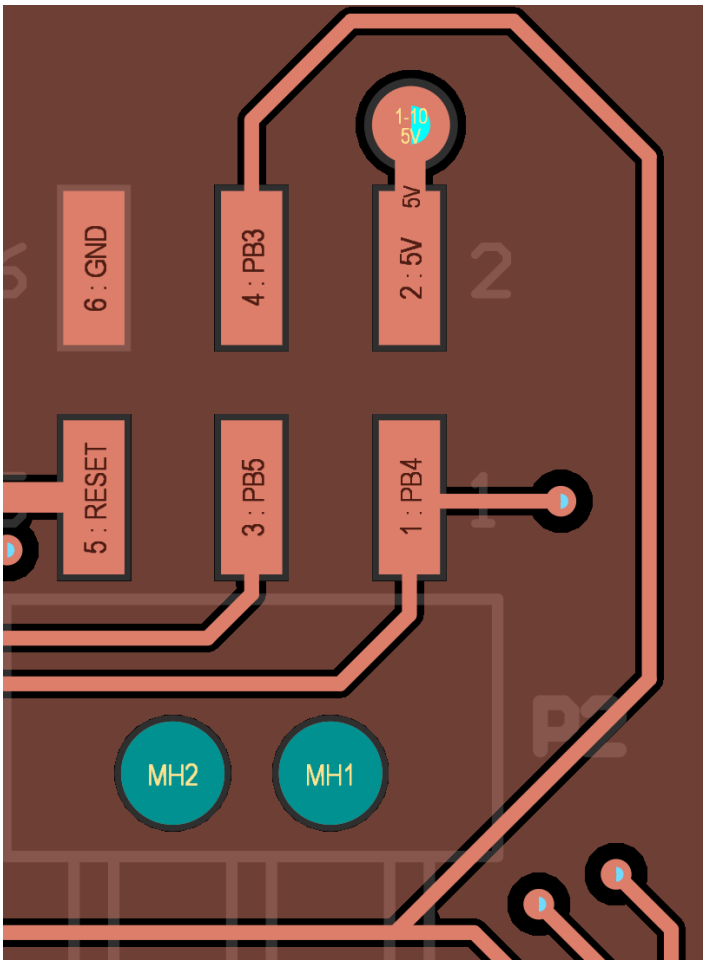


Figura 2.41: Puerto de programación del microcontrolador.

Tras colocar las pistas de todos los elementos del microcontrolador, se procede a realizar el mismo proceso para la IMU y de esta manera finalizar el *routing* del ADCS.

Esta IMU tiene una escala reducida en comparación con los demás componentes, por lo que todas sus pistas deben colocarse con 5 mils (0,127 mm) de ancho, ya que las señales establecidas por este sensor son muy débiles y no suponen un inconveniente en cuanto a riesgo térmico.

La alimentación de la IMU lleva unos condensadores de acoplo, como se puede ver en la Figura 2.42. También lleva un par de condensadores extra en los pines dedicados a ello.

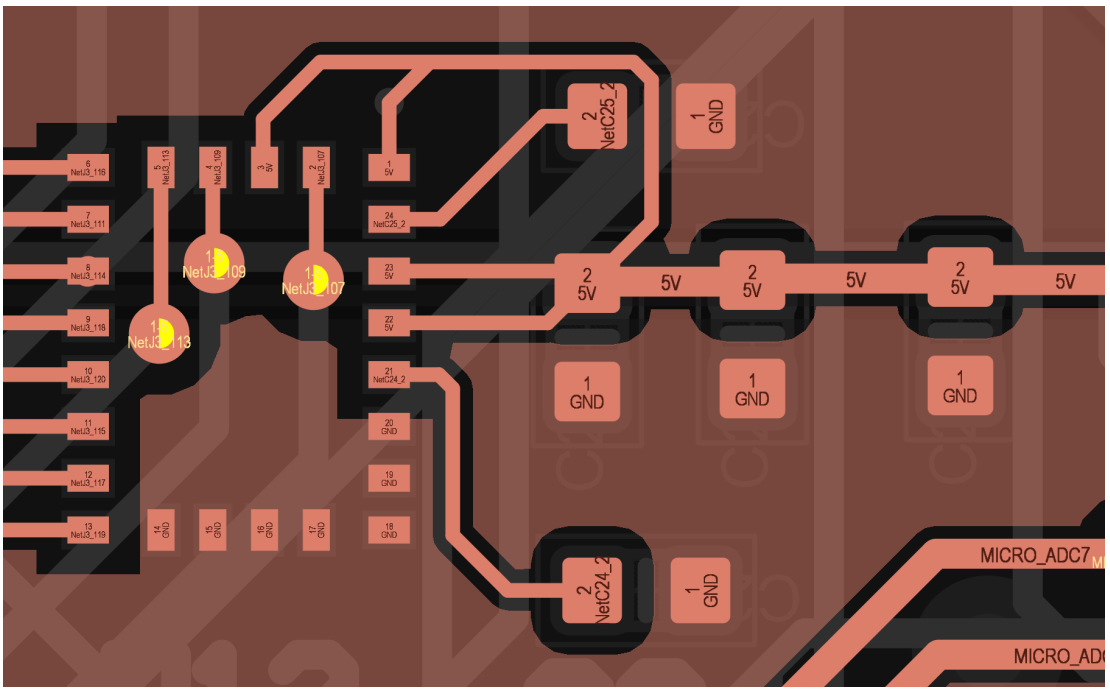


Figura 2.42: Circuito de la IMU.

Una vez realizadas las pistas de las señales de todos los componentes, se conectan a la alimentación mediante una vía que se dirige al plano de potencia.

Todas las señales que llevan información útil para los diferentes subsistemas se llevan al conector PCI/104. En la Figura 2.43 se muestra un ejemplo de cómo se ha realizado la conexión a estos pines: los que llevan una señal de potencia, se ha aprovechado el propio plano; los que llevan información, se ha empleado el mismo método que con el GPS para los pines internos y se ha redireccionado a otras capas, mientras que los pines externos se han conectado directamente o mediante vías.

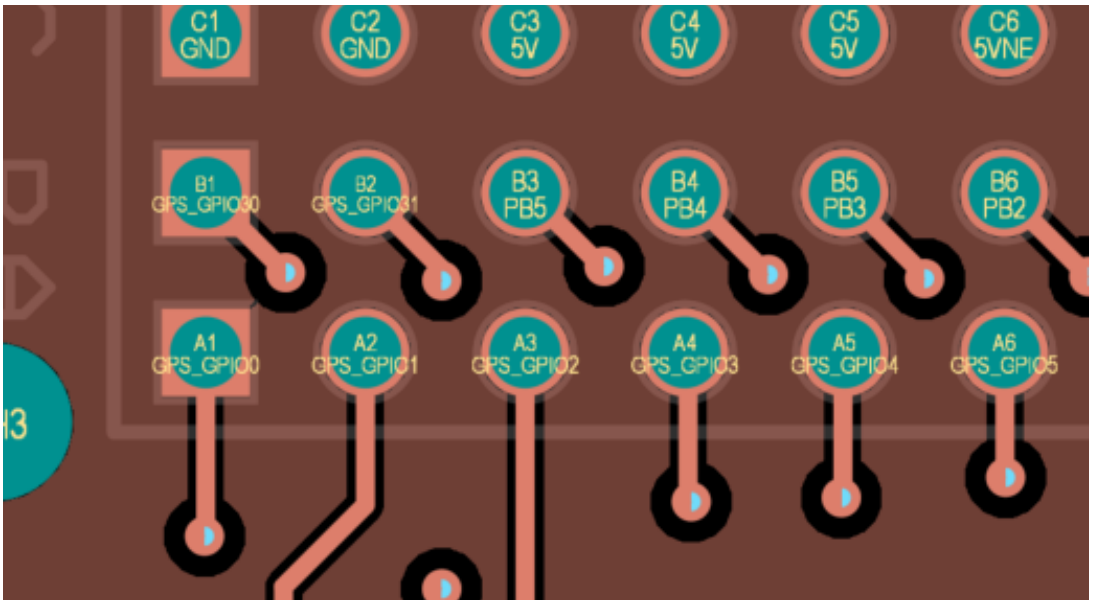


Figura 2.43: Conexión del bus PCI/104 en la capa superior.

Por otro lado, toda aquella información programable, como la de las memorias, o información proveniente de los sensores también se dirige al ordenador de a bordo mediante el conector *mezzanine*. Este conector cuenta con 120 pines de los cuales aproximadamente 100 son útiles, puesto que algunos de ellos solo trabajan a 1,8V. Existen cuatro áreas principales con 40 *pads* cercanos entre sí, por lo que es necesario emplear diferentes vías para distribuir correctamente las redes. En la Figura 2.44 se muestra el resultado final de esta conexión.

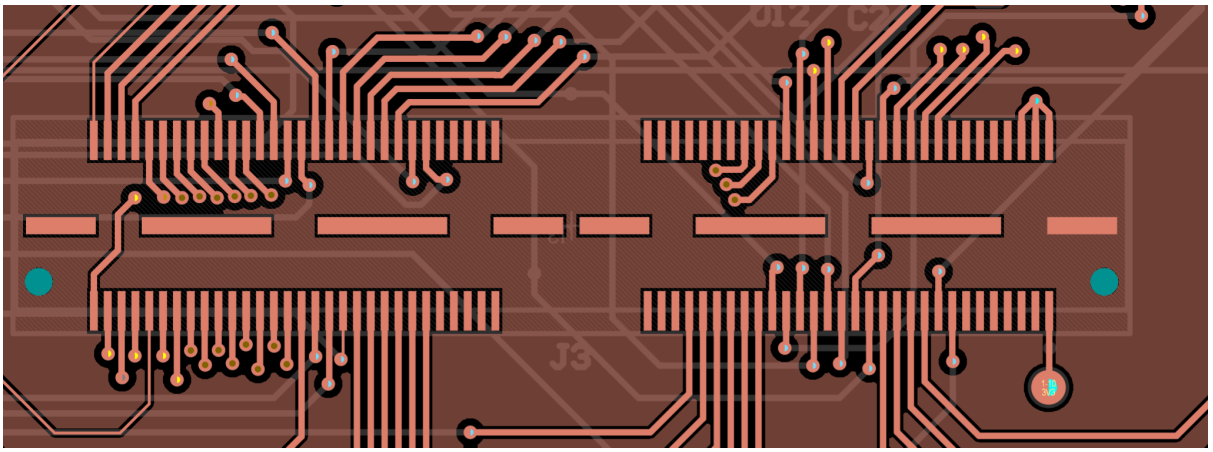


Figura 2.44: Conector mezzanine del OBC.

El conector lleva consigo unos *pads* intermedios, los cuales se pueden conectar a tierra o dejar como no conectados. Dada la cercanía de algunas pistas y vías, se ha optado por dejar sin conectar. El pad de la derecha tiene la red de tierra colocada por defecto.
El último componente independiente de la placa es el conector de la antena. En la Figura 2.45 se muestra cómo emplea una vía para situarse en otra capa y poder dirigirse tanto al OBC como al PCI/104.

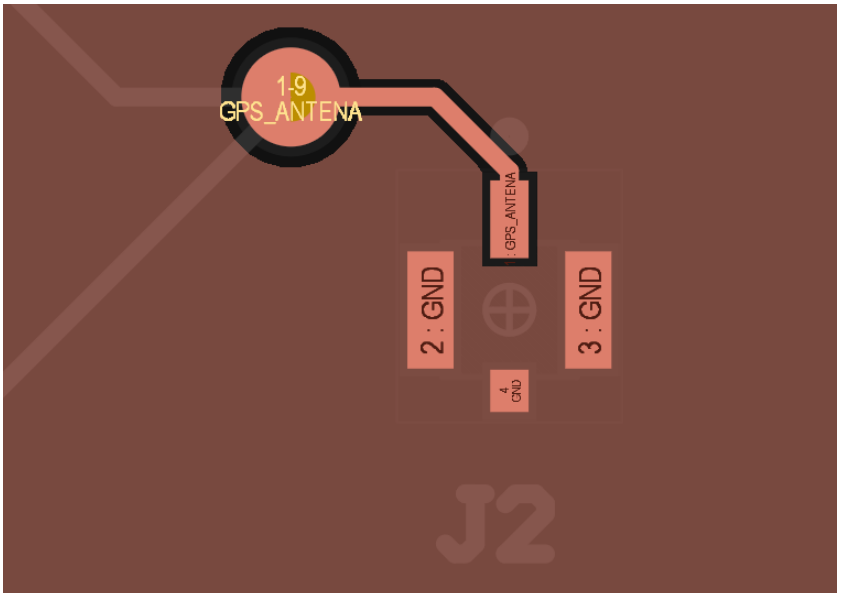


Figura 2.45: Conector de la antena.

Tras esto, se ha realizado toda la conexión existente en la placa LoMo.

2.3.3. *Design Rules Check*

El *Design Rules Check* o DRC es una herramienta provista por la mayoría de programas de diseño de PCB. Esta herramienta realiza una revisión de toda la placa para analizar en función de unas reglas impuestas previamente si se está cometiendo un error. Al terminar el diseño de la placa, el DRC mostraba algunos errores de cortocircuito debido a pequeñas conexiones de las vías intercapa con algunas pistas. También se ha mostrado errores de pistas no conectadas debido a elementos residuales a la hora de realizar modificaciones en esas redes. En el ejemplo de la Figura 2.46 se muestra un mensaje típico del *Design Rules Check* donde se informa el tipo de error cometido y el lugar donde se sitúa. Al pinchar en el texto destacado, el programa lleva al usuario directamente a las coordenadas del error.

Rule Violations	Count
Short-Circuit Constraint (Allowed=No) (All),(All)	3
Un-Routed Net Constraint ((All))	0
Width Constraint (Min=5mil) (Max=20mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4) (All)	0
Total	**3**

Short-Circuit Constraint (Allowed=No) (All),(All)
Short-Circuit Constraint: Between Track (1098mil,2677mil)(2299mil,2677mil) on PGND And Via (2033.693mil,2696.693mil) from Signal1 to Signal6 Location : [X = 5311.252mil][Y = 7450.706mil]
Short-Circuit Constraint: Between Track (1098mil,2677mil)(2299mil,2677mil) on PGND And Via (2077mil,2696.693mil) from Signal1 to Signal6 Location : [X = 5354.559mil][Y = 7450.706mil]
Short-Circuit Constraint: Between Track (1098mil,2677mil)(2299mil,2677mil) on PGND And Via (2120.307mil,2696.693mil) from Signal1 to Signal6 Location : [X = 5397.866mil][Y = 7450.706mil]

Figura 2.46: Ejemplo de *Design Rules Check* con errores.

Una vez corregido todos los errores, el DRC genera el documento que muestra la ausencia de fallos eléctricos.

2.3.4. Obtención de los ficheros Gerber

Una vez corregido todos los errores existentes en la placa, es posible generar un archivo con el formato Gerber. Este formato es muy usado en la manufactura de circuitos impresos puesto que tiene la información de todas las dimensiones, el número de capas y las distintas redes que componen cada capa de cobre. Para poder generar los ficheros Gerber en Altium, es necesario crear un nuevo documento con el formato CAM. Para ello, en los ajustes de exportación se selecciona “Ficheros Gerber”. Una vez aparezca este archivo, se escogen las capas a exportar y se escoge de entre las diferentes opciones (fichero de taladros, *netlist*, etc.) el fichero Gerber. De esta manera, se crea una carpeta con todas las capas activas. En la Figura 2.47 se pueden observar estas capas.

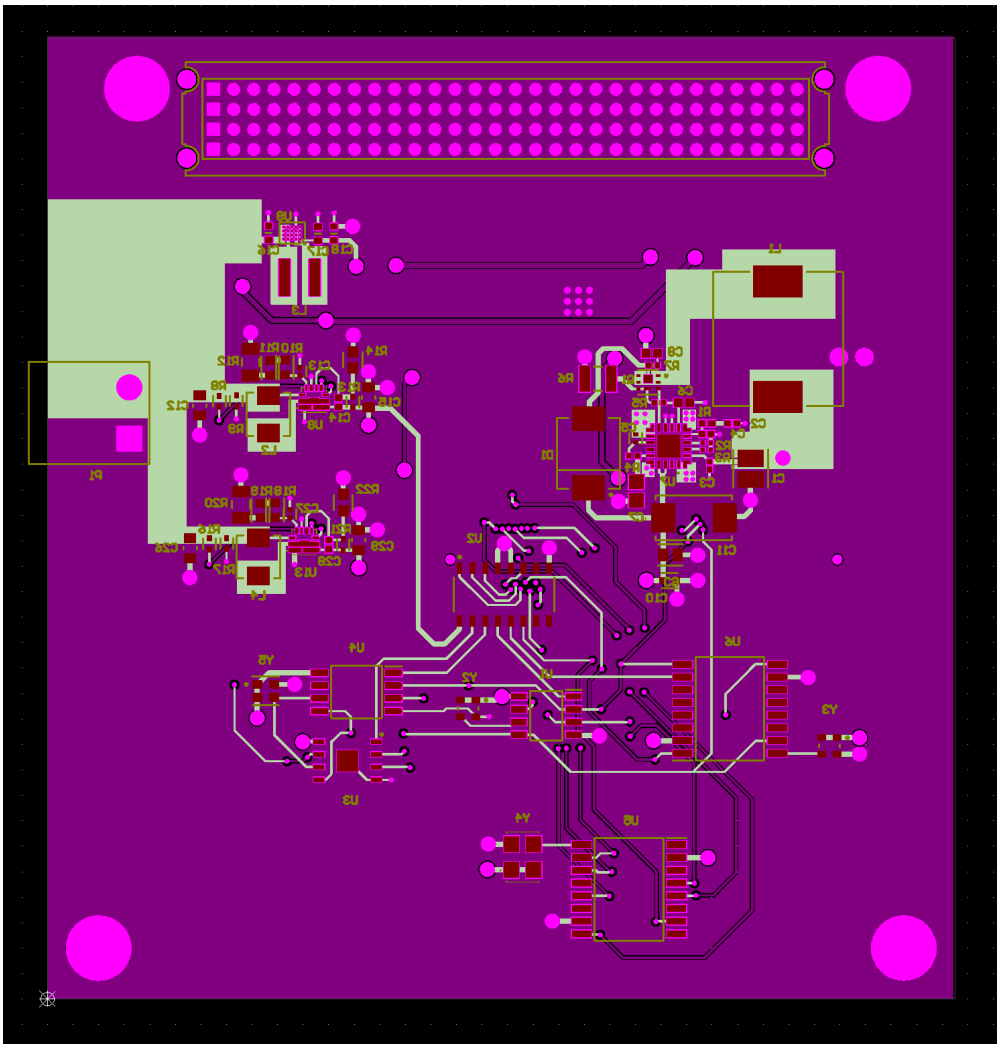


Figura 2.47: Fichero CAM con todas las capas activadas.

Con este fichero se pueden realizar los diferentes presupuestos y manufactura, puesto que conlleva toda la información necesaria para su fabricación.

3. Presupuesto

Al confirmarse todos los elementos que componen la LoMo en su totalidad y tener el diseño completo de la PCB, es posible determinar el coste total de dichos componentes y de la manufactura del circuito impreso. Para obtener el presupuesto, se ha recurrido a una empresa de Reino Unido, PCBWay [31], y una empresa de España, Cipsa Circuits [26].

En la Tabla 3.1 se puede observar que el precio por cada LoMo que se realice en PCBWay tiene un costo de 134,52€, para pedidos de cinco en cinco.

Presupuesto PCBWay	
Opciones:	
Tipo	Piezas sueltas
Cantidad	5
Dimensiones	90,2 x 95,9 mm
Capas	12 capas
Material	FR-4
FR4-TG	TG 150-160
Grosor	2,4 mm
Máscara de soldadura	Verde
Serigrafía	Blanco
Acabado	HASL con plomo
Acabado de cobre	1 oz
Precios:	
PCBs	672,62 €
Envío	18,69 €
Total	691,31 €
Precio por placa:	134,52 €

Tabla 3.1: Presupuesto de PCBWay para cinco placas.

Para el fabricante Cipsa Circuits, se ha contactado para obtener un presupuesto aproximado. El presupuesto respondido se muestra en la Tabla 3.2.

Presupuesto Cipsa Circuits	
Opciones:	
Acabado	EniG
Cantidad	10
Precios:	
PCBs	750,00 €
Envío	90,00 €
Total	840,00 €
Precio por placa:	75,00 €

Tabla 3.2: Presupuesto de Cipsa Circuits para diez placas.

Como se puede ver en la Tabla 3.2, el precio por placa de Cipsa Circuits es muy inferior al de PCBWay para un mayor número de placas, pero con un mayor coste total. Estas dos opciones son útiles en función de si se desea un coste menor y con características propias de un prototipo o un coste mayor con un acabado más complejo y cercano al resultado final.

El presupuesto total de los componentes para una única placa es de aproximadamente 430€. El desglose de los mismos se puede observar en el BOM del Anexo II.

4. Resultados y discusión

Tras realizar el diseño del primer prototipo de circuito impreso se ha observado la necesidad de realizar un cambio de configuración debido al espacio disponible. Esto se debe a que el espacio ocupado por las pistas del microcontrolador y el GPS es superior al previsto. Esto podría arreglarse si en futuras iteraciones se escogiera un GPS con una huella que sitúe sus pines en orden, o plantear otra configuración que implique un mayor salto de capas en el GPS. Aun así, este cambio realizado no supone un inconveniente, puesto que en la cara inferior existía un espacio libre al emplear un EPS de dimensiones reducidas. En la Figura 4.1 se muestra una distribución espacial de los componentes a alto nivel con respecto al planteamiento inicial.

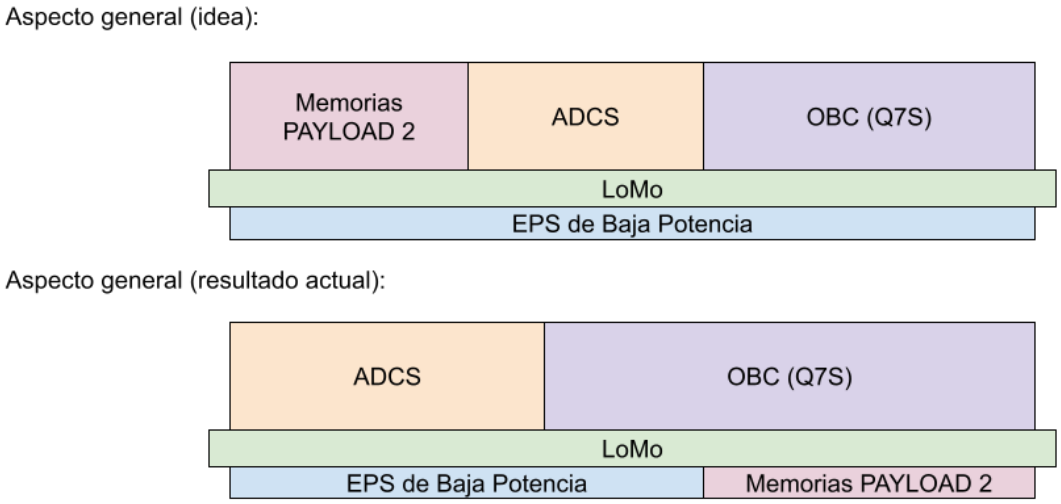


Figura 4.1: Comparativa de la distribución final con respecto a la idea.

Además de este cambio, se ha observado que algunas capas son más densas en cuanto a número de pistas que otras. Esta iteración forma una base sólida para poder aprender más en lo referente al diseño de PCB, puesto que se han aplicado técnicas de distribución de capas (asignando capas diferentes para la distribución de energía y el envío de señales) y un intento de optimizar de la mejor forma posible la longitud de las pistas, de manera que las señales más rápidas puedan tener una transmisión de información más fiable.

En las Figuras 4.2 y 4.3 se observan los modelos 3D de la PCB mediante el visor en tres dimensiones de Altium. Este tipo de visualización también ayuda a observar las zonas más densas o zonas con mayor posibilidad de calentamiento, de manera que a la hora de hacer un estudio térmico de la misma se puede intuir *grosso modo* los puntos calientes de la placa.

Durante el desarrollo de esta placa se ha observado que el conector de la antena tiene una utilidad bastante reducida al apilarse diferentes capas encima de LoMo. Para la misión espacial, utilizar un cable flexible que redirige la antena no es viable, por lo que para futuras iteraciones se puede plantear un diseño de antena integrado dentro de la PCB, a falta de ser estudiado frente a las EMI.

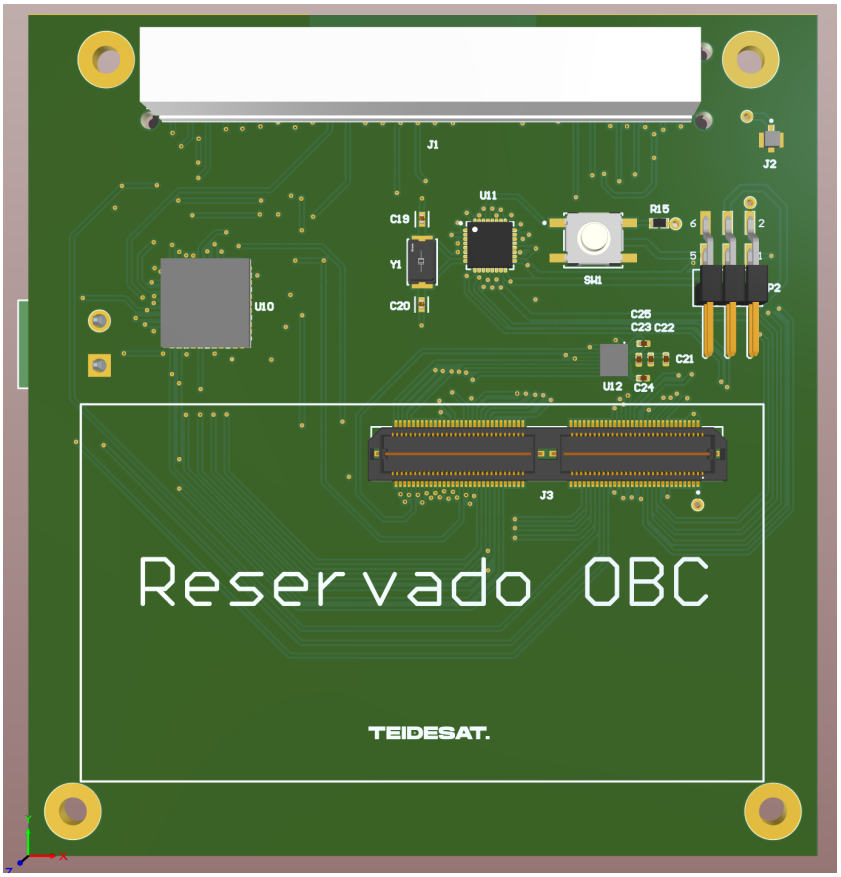


Figura 4.2: Modelo 3D de la PCB LoMo (cara superior).

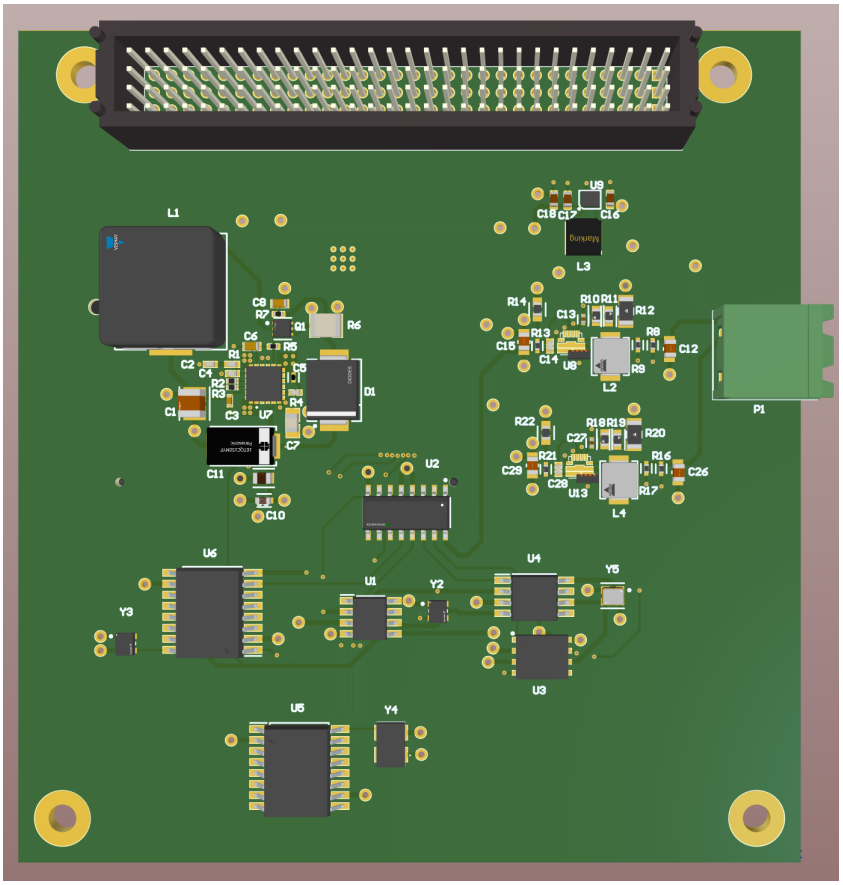


Figura 4.3: Modelo 3D de la PCB LoMo (cara inferior).

5. Conclusiones y líneas futuras

5.1. Conclusiones

En este TFG se ha realizado el proceso de diseño de la PCB LoMo para el nanosatélite TEIDESAT-I. Para este diseño, se ha recogido información acerca de la normativa espacial y se ha realizado un proyecto de Altium Designer siguiendo estos pasos:

1. Revisión de todos los componentes existentes y colocación de nuevos componentes necesarios para su funcionamiento.

2. Realización de los esquemáticos de cada función independientemente.

3. Realización de la jerarquía de funciones.

4. Colocación de los componentes en la PCB.

5. Diseño final de la PCB.

Una vez completado este proceso, se obtiene la primera iteración de esta placa principal del nanosatélite.

Como la mayoría de diseños que se lanzan al mercado, este prototipo tenderá a ser modificado poco a poco mediante ensayo y error, además de la aplicación de nuevos conocimientos que se vayan obteniendo. Como propuesta de mejora en adelante, es posible tener en cuenta los siguientes aspectos:

1. Es muy importante comprobar el funcionamiento de los diferentes bloques realizando diseños pequeños según la funcionalidad (por ejemplo, una PCB de prueba del EPS).

2. Se espera colocar circuitos de conmutación de las alimentaciones principales y auxiliares para asegurar la operación tras fallo.

3. Una de las capas que no se utiliza demasiado puede aprovecharse de una mejor manera teniendo en cuenta el diseño en conjunto.

4. Posiblemente alguna de las señales como la de la IMU sean muy débiles y sea necesario colocar un amplificador de señal próxima a ellas para asegurar que no haya pérdida de información.

5.2. Conclusions

In this end-of-degree project the process of designing the PCB LoMo for TEIDESAT-I nanosatellite was made. In this design, information about space rules was gathered and an Altium Designer project was created following these steps:

1. Checking of all the existing components and placement of new components, needed for the PCB functionality.

2. Development of schematics for each independent function.

3. Development of the function hierarchy.

4. Component placement on PCB.
5. Final PCB design.

Once this process is completed, the result of this first core board iteration for the nanosatellite is obtained.

As most of the market designs, this prototype will be likely to change over trial and error, as well as applying more acquired knowledge. As a suggestion for future improvements, it is possible to keep these aspects in mind:

1. It is very important to check each block functionality by designing a prototype for each function (i.e. making a PCB to check if EPS works correctly).

2. Switching circuits to change between main and secondary power supply are planned to be sure the nanosatellite works in case of failure.

3. The layer that has a lack of copper traces could be optimized by looking at the general distribution of layers.

4. It is possible that some signals like the IMU ones are not strong enough to carry the information through the whole trace. It could be better to add some amplifiers in order to carry the information without losses.

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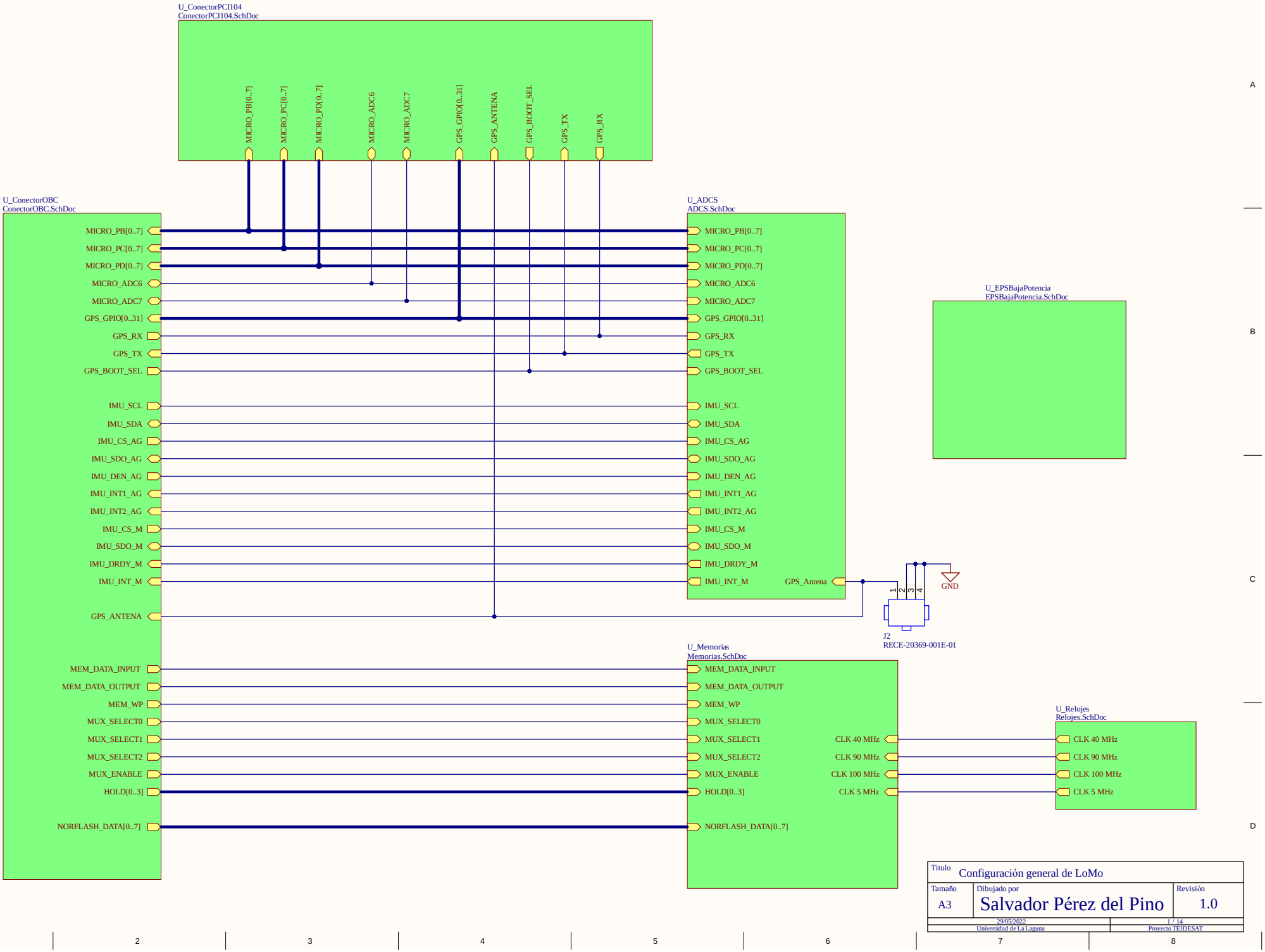
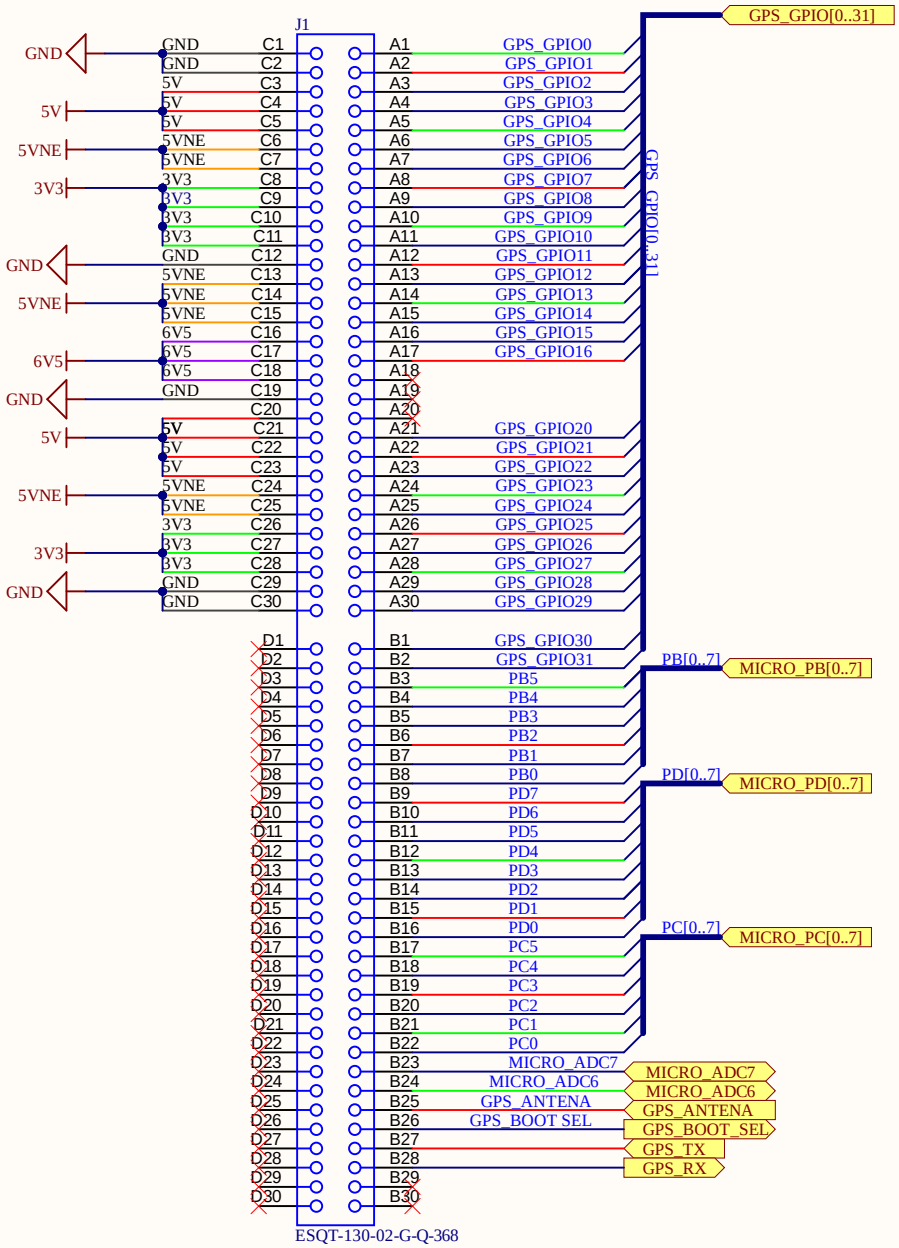
ANEXO I

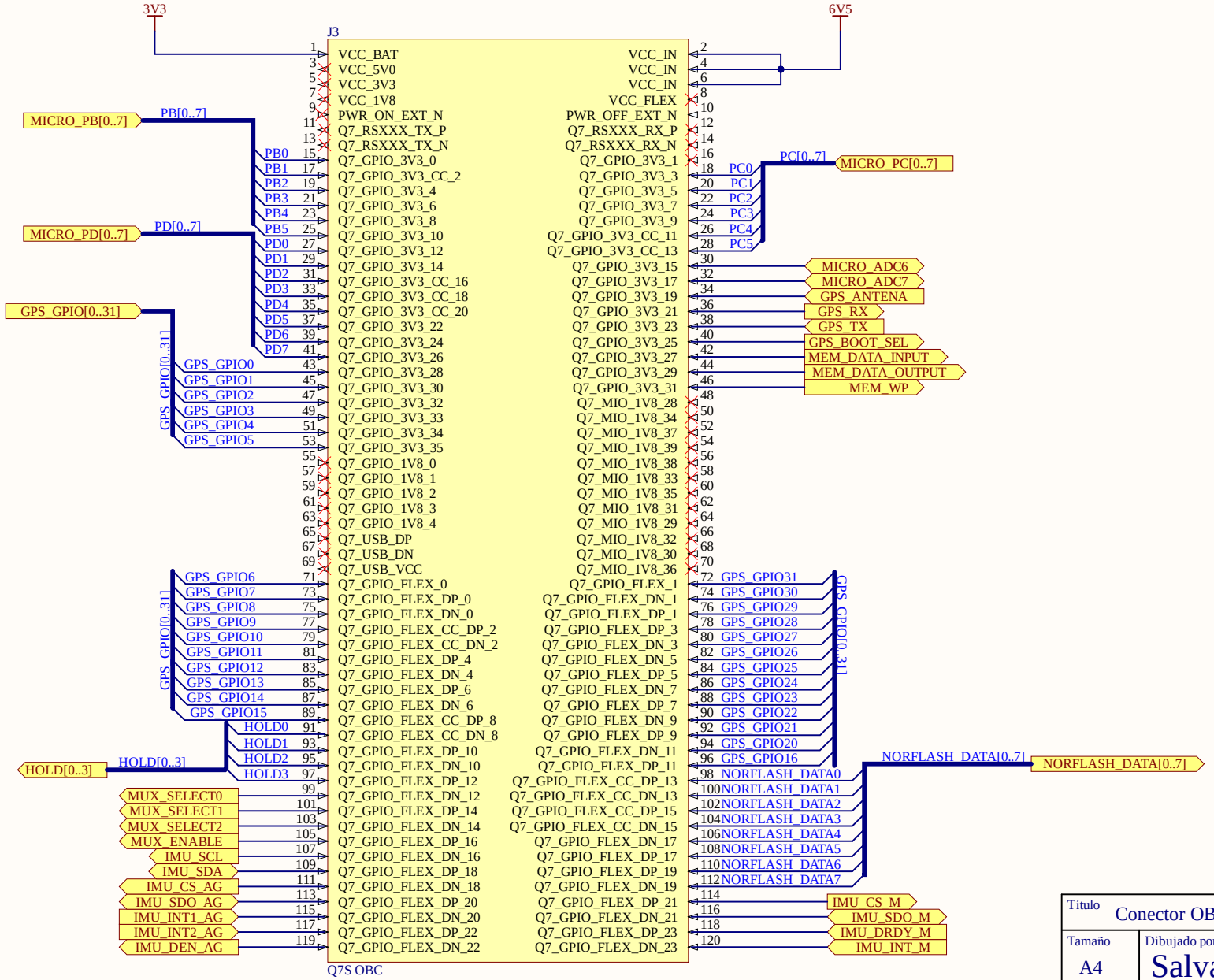
Esquemáticos



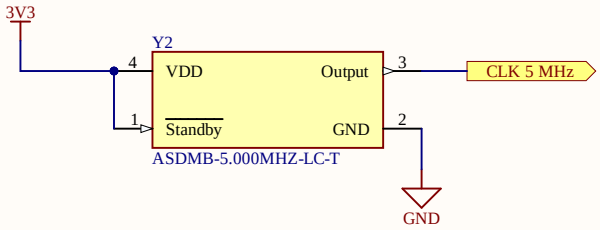
Título	Configuración general de LoMo	
Tamaño	Dibujado por	Revisión
A3	Salvador Pérez del Pino	1.0
29/05/2022		1 / 14
Universidad de La Laguna		Proyecto TEIDESAT

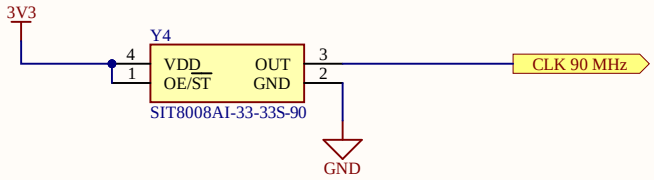


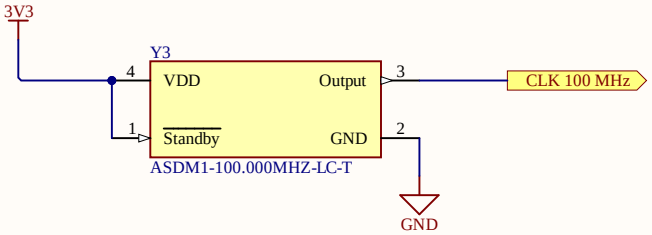
Título: Conector PCI 104		
Tamaño: A4	Dibujado por: Salvador Pérez del Pino	Revisión: 1.0
29/05/2022		2 / 14
Universidad de La Laguna		Proyecto TEIDESAT

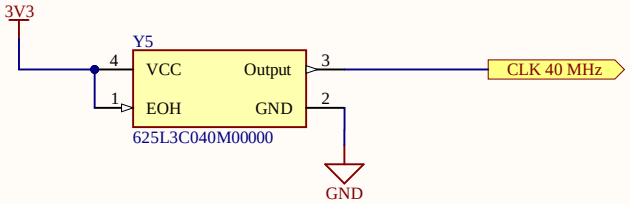


Título	Conector OBC	
Tamaño: A4	Dibujado por: Salvador Pérez del Pino	Revisión: 1.0
29/05/2022		3 / 14
Universidad de La Laguna		Proyecto TEIDESAT

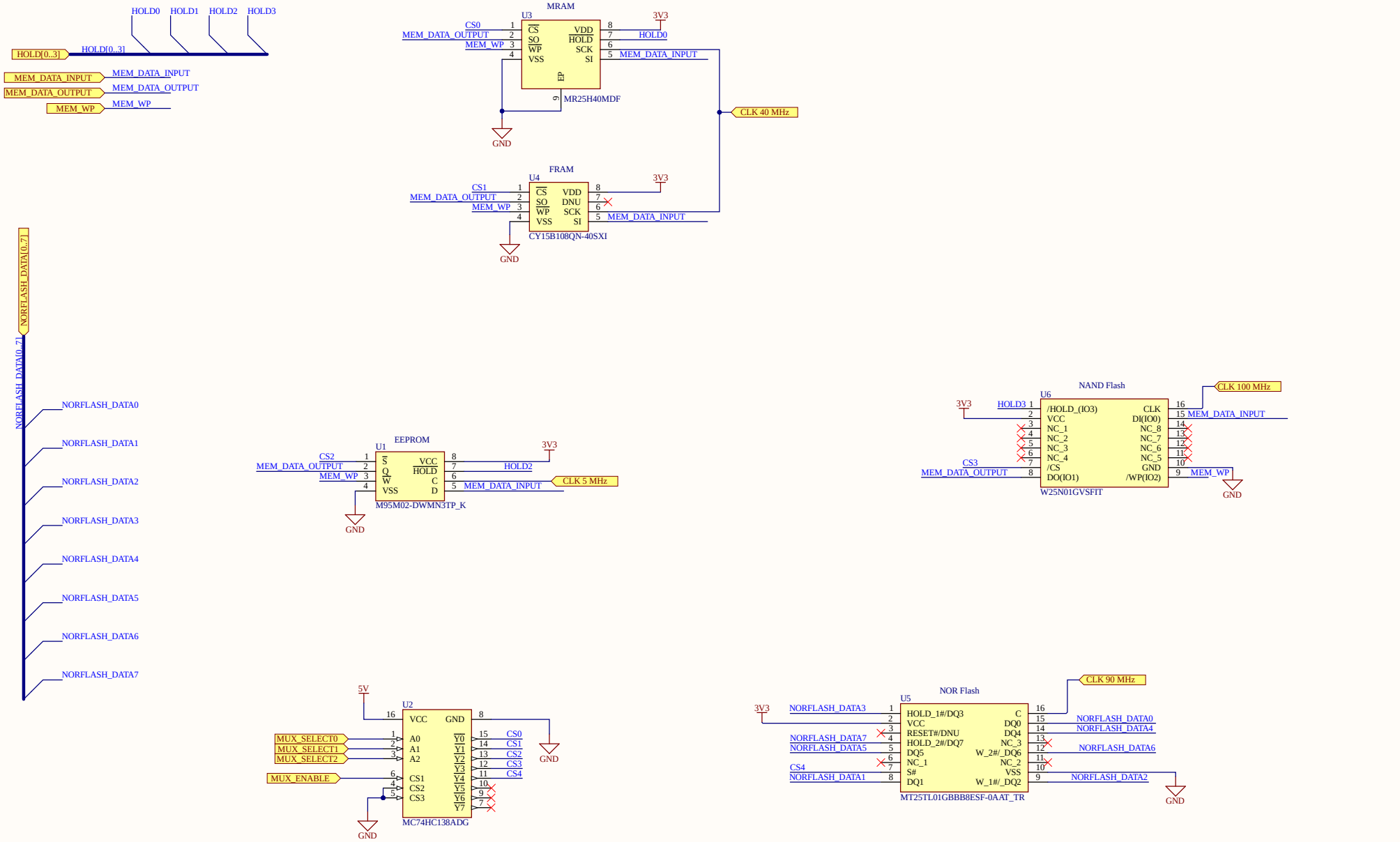




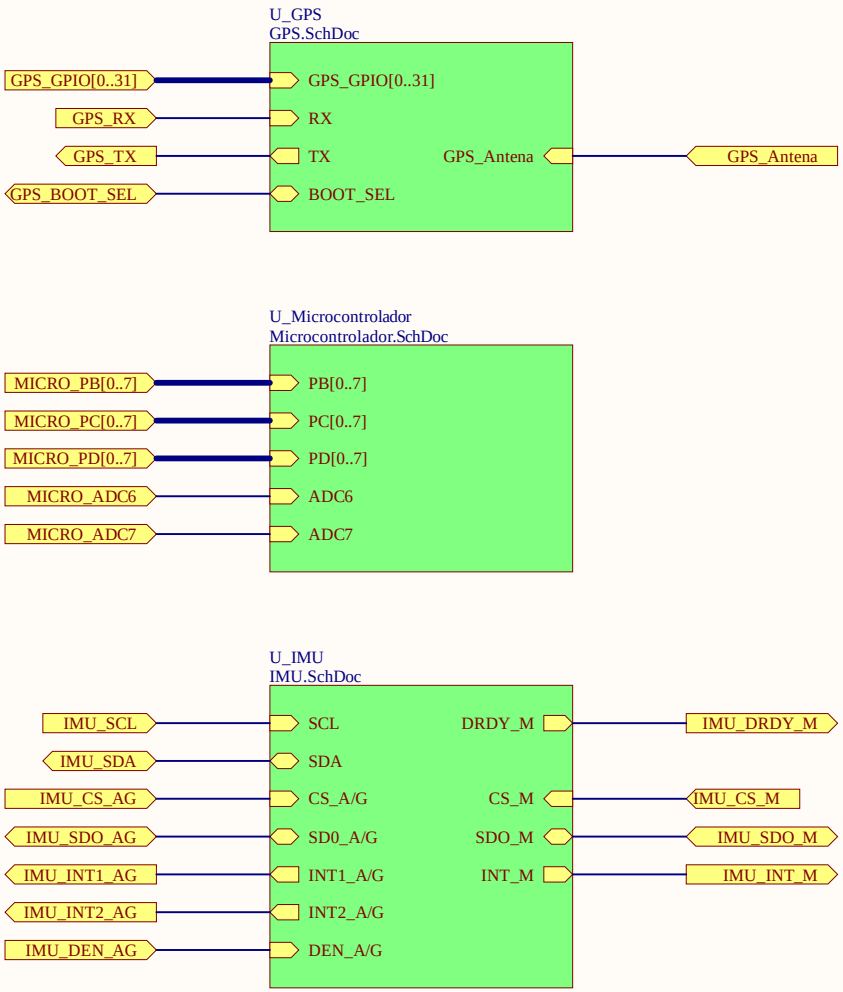




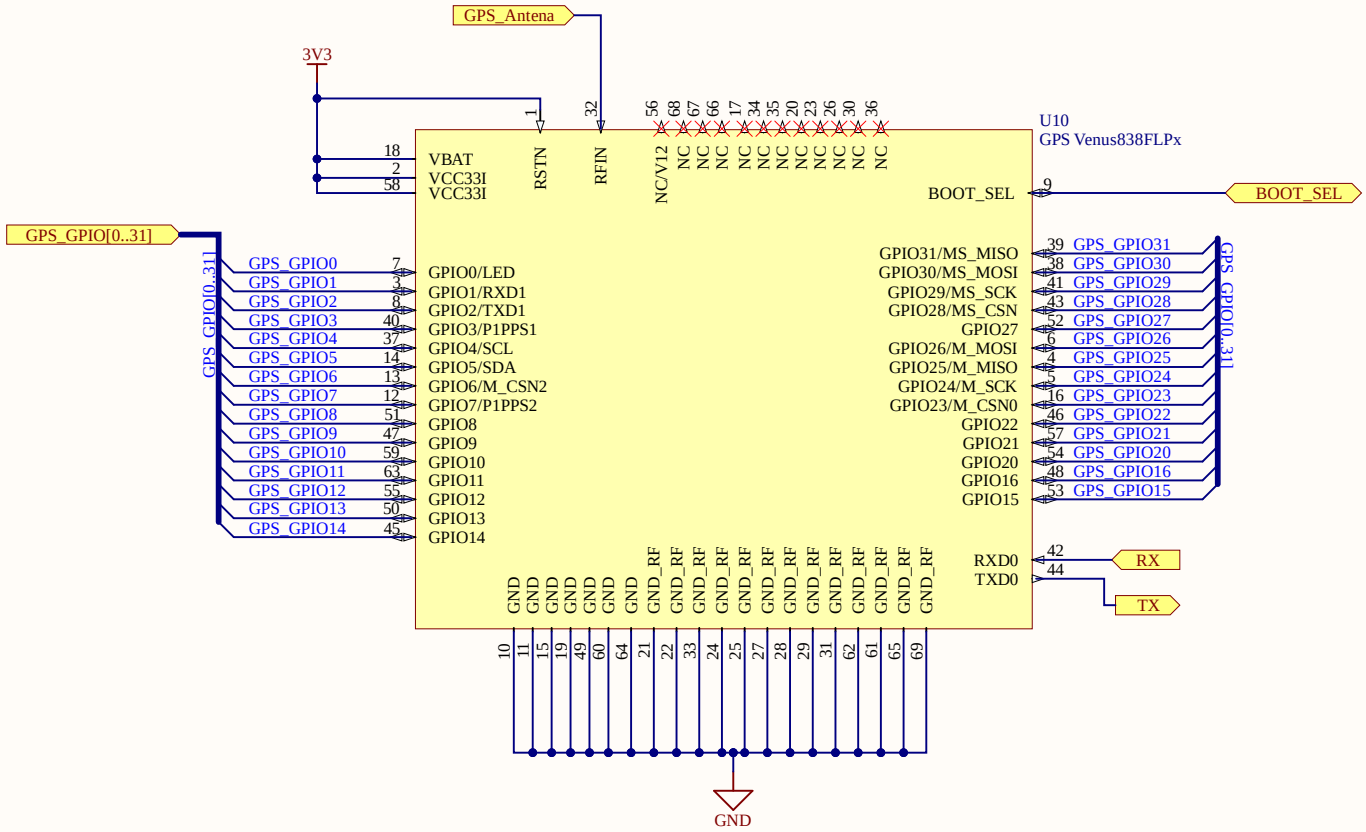
Título: Circuitos osciladores para las memorias		
Tamaño: A4	Dibujado por: Salvador Pérez del Pino	Revisión: 1.0
29/05/2022		4 / 14
Universidad de La Laguna		Proyecto TEIDESAT



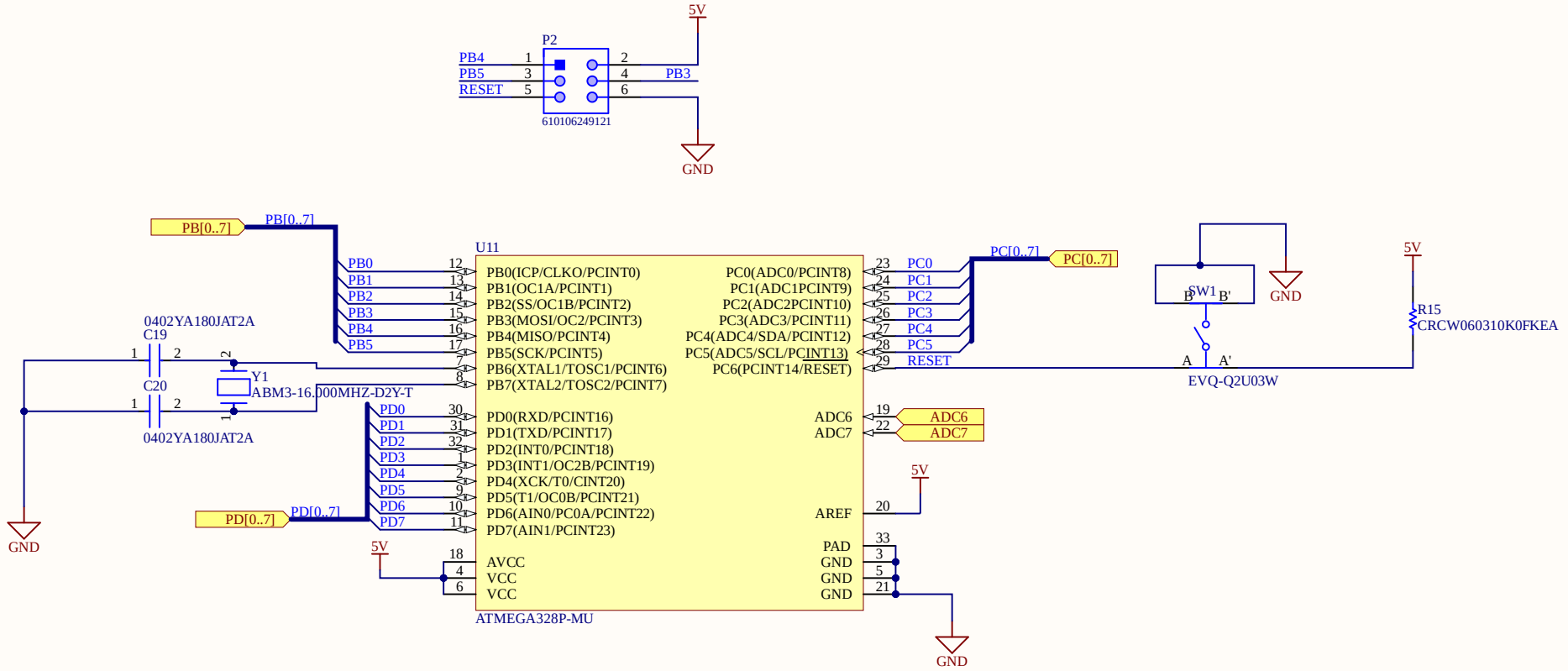
Título	Memorias del segundo experimento	
Tamaño: A3	Dibujado por: Salvador Pérez del Pino	Revisión: 1.0
29/05/2022		5 / 14
Universidad de La Laguna		Proyecto TEIDESAT



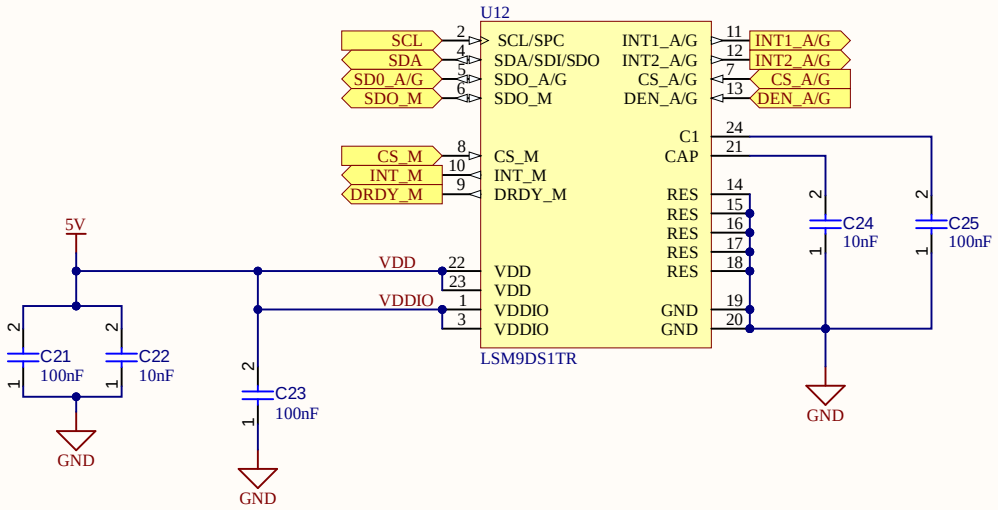
Título	Sistema de control de actitud (ADCS)	
Tamaño: A4	Dibujado por: Salvador Pérez del Pino	Revisión: 1.0
29/05/2022		6 / 14
Universidad de La Laguna		Proyecto TEIDESAT



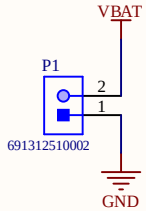
Título	Conexionado del GPS	
Tamaño: A4	Dibujado por: Salvador Pérez del Pino	Revisión: 1.0
29/05/2022		7 / 14
Universidad de La Laguna		Proyecto TEIDESAT



Título	Conexionado del microcontrolador	
Tamaño: A4	Dibujado por: Salvador Pérez del Pino	Revisión: 1.0
29/05/2022		8 / 14
Universidad de La Laguna		Proyecto TEIDESAT



Título	Conexionado de la IMU	
Tamaño: A4	Dibujado por: Salvador Pérez del Pino	Revisión: 1.0
29/05/2022		9 / 14
Universidad de La Laguna		Proyecto TEIDESAT



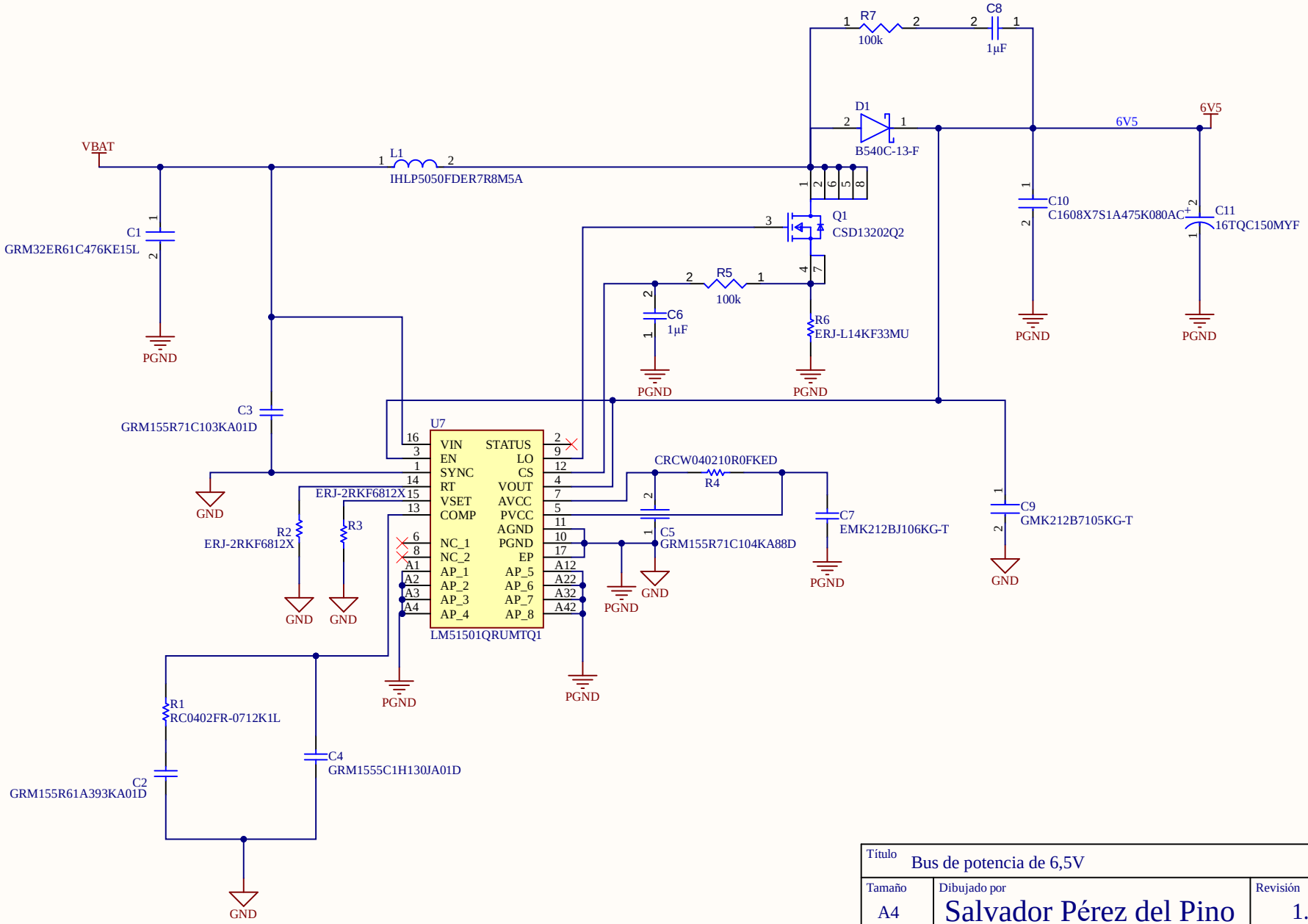
Bus de 3,3V
3V3Bus.SchDoc

Bus de 5V Principal
5VBUS.SchDoc

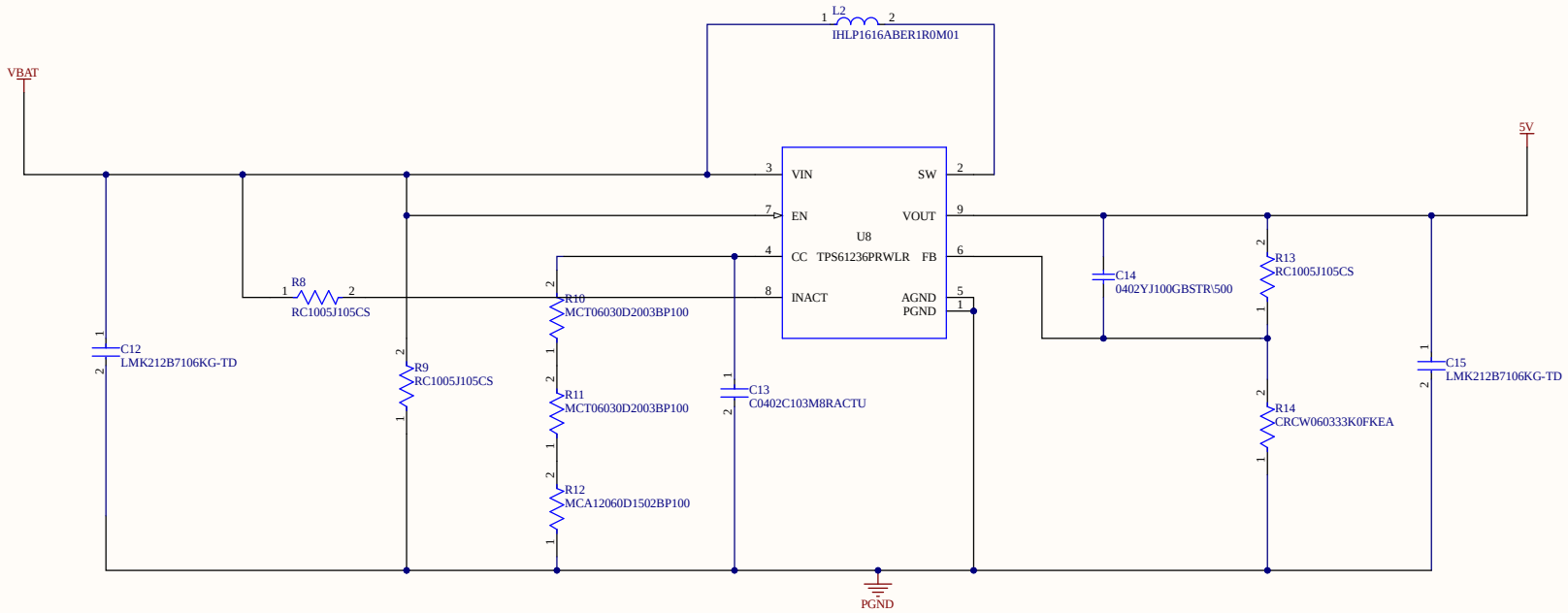
Bus de 6,5V
6V5Bus.SchDoc

Bus de 5V Secundario
5VNEBus.SchDoc

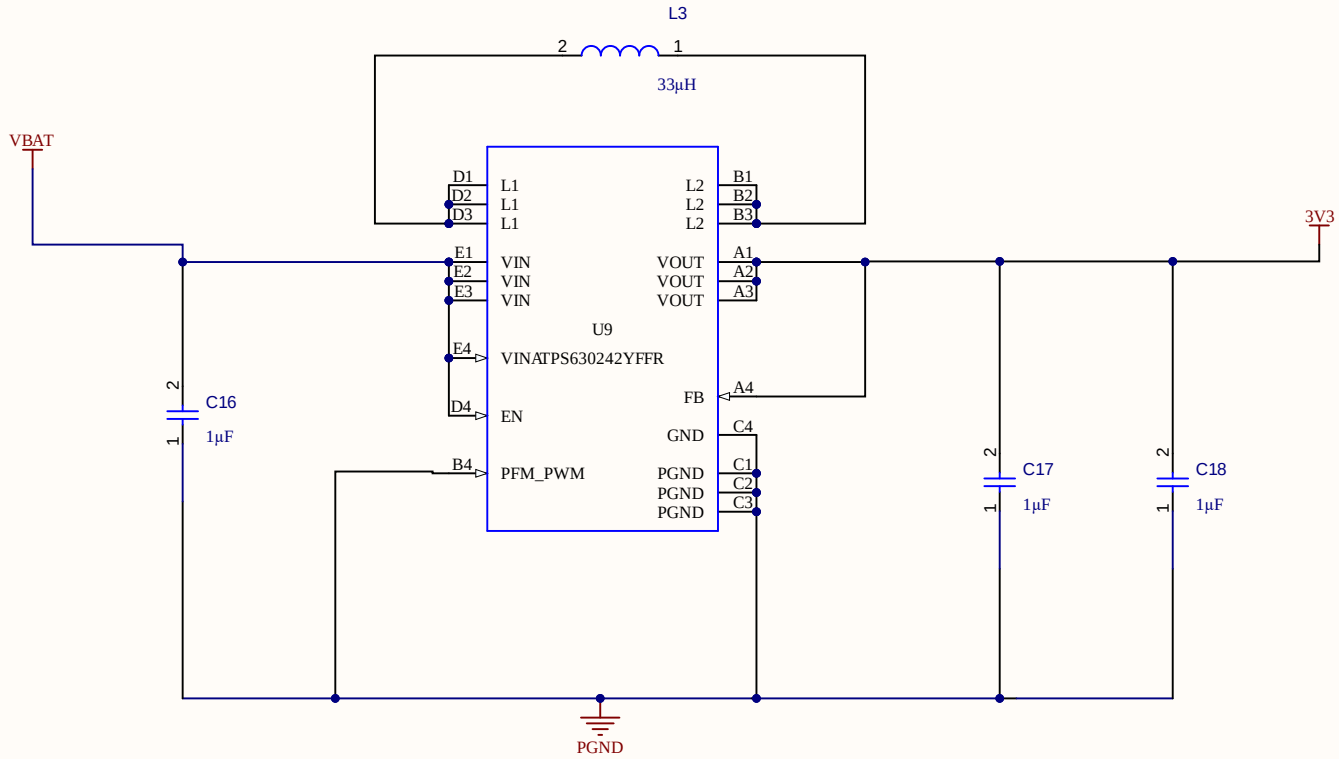
Título: EPS de baja potencia		
Tamaño: A4	Dibujado por: Salvador Pérez del Pino	Revisión: 1.0
29/05/2022		10 / 14
Universidad de La Laguna		Proyecto TEIDESAT



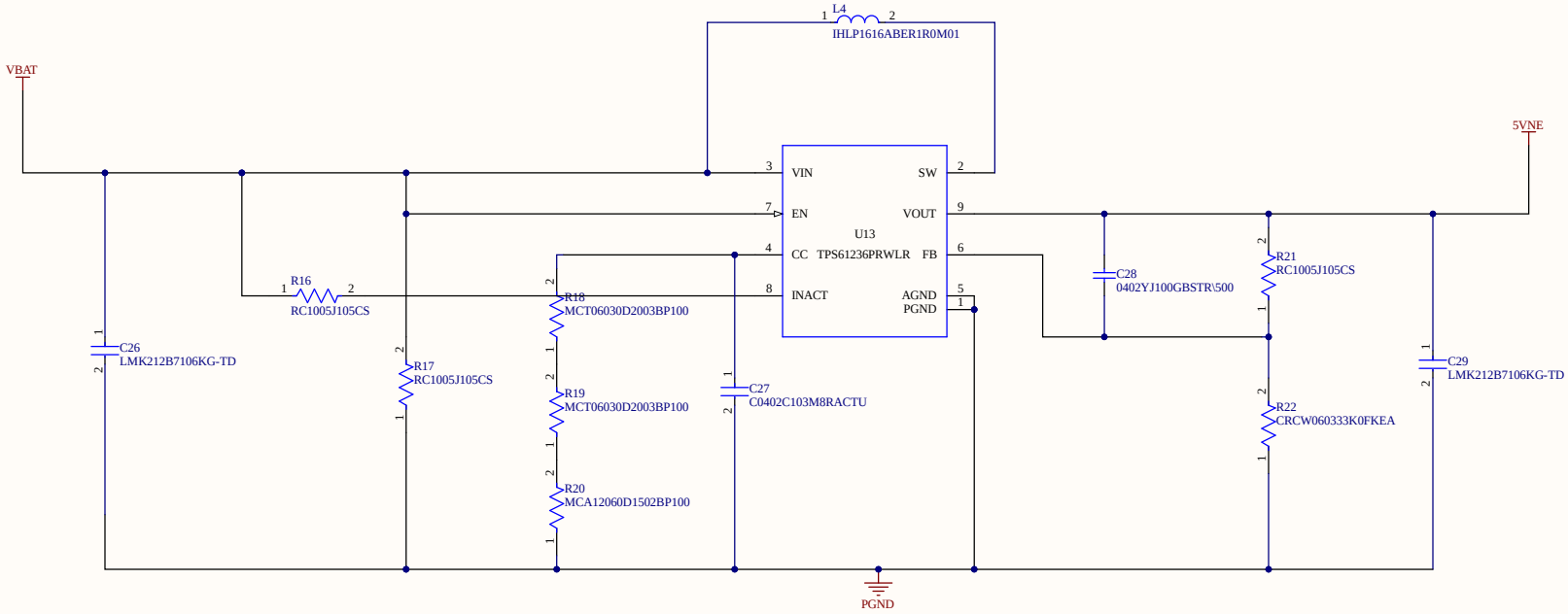
Título	Bus de potencia de 6,5V	
Tamaño: A4	Dibujado por: Salvador Pérez del Pino	Revisión: 1.0
29/05/2022		11 / 14
Universidad de La Laguna		Proyecto TEIDESAT



Título	Bus de Potencia de 5V	
Tamaño: A3	Dibujado por: Salvador Pérez del Pino	Revisión: 1.0
29/05/2022		12 / 14
Universidad de La Laguna		Proyecto TEIDESAT



Título	Bus de potencia de 3,3V	
Tamaño: A4	Dibujado por: Salvador Pérez del Pino	Revisión: 1.0
29/05/2022		13 / 14
Universidad de La Laguna		Proyecto TEIDESAT



Título	Bus de potencia de 5V secundario	
Tamaño: A3	Dibujado por: Salvador Pérez del Pino	Revisión: 1.0
29/05/2022		14 / 14
Universidad de La Laguna		Proyecto TEIDESAT

ANEXO II

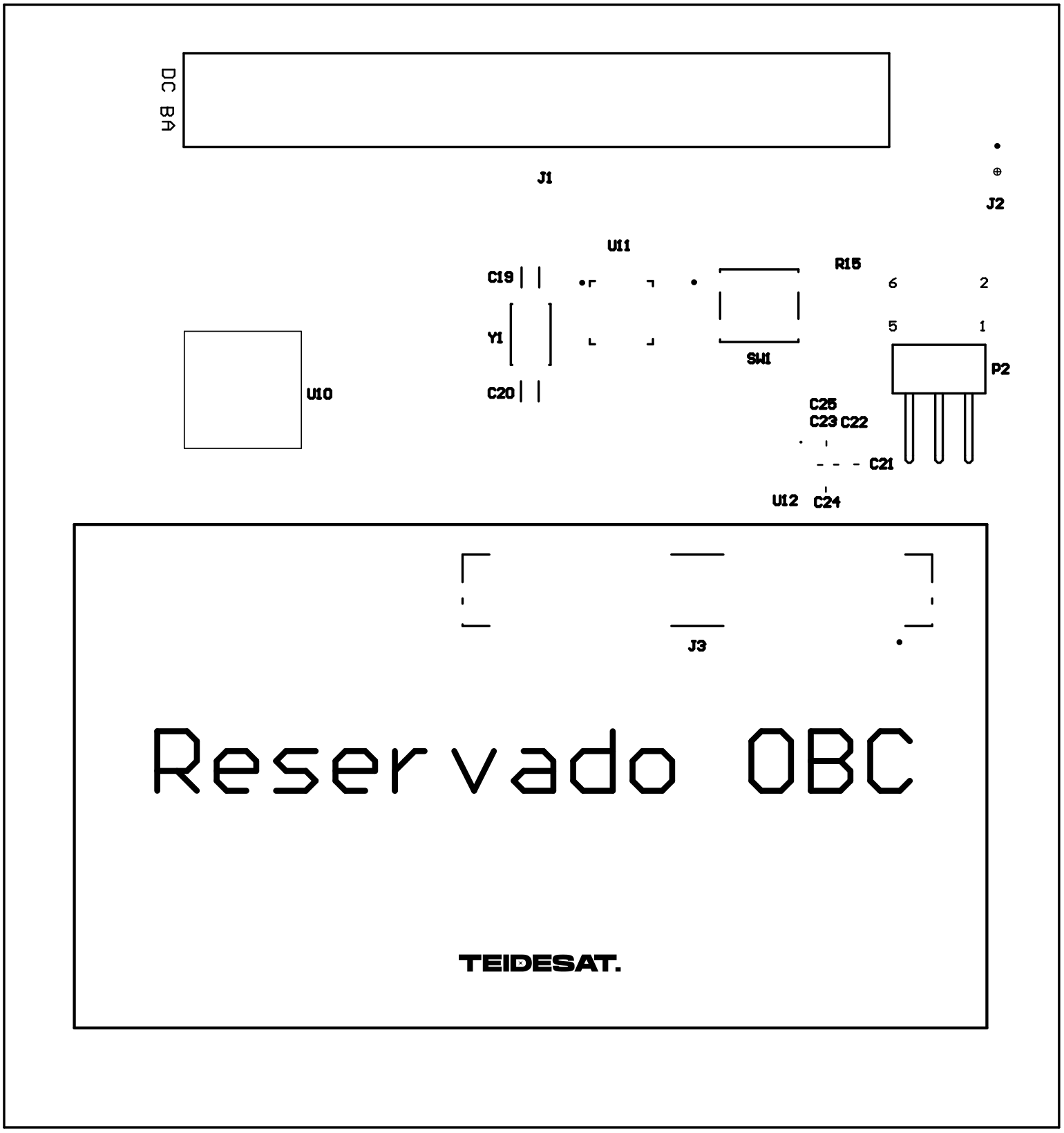
Bill of Materials

Description	Designator	Quantity	Name	Manufacturer 1	Supplier 1	Supplier Unit Price 1	Supplier Subtotal 1
CAP CER 47UF 16V X5R 1210	C1	1	GRM32ER61C476KE15L	Murata	Future Electronics	0,86643	0,86643
CAP	C2	1	GRM155R61A393KA01D	Murata	Arrow Electronics	0,07884	0,07884
Chip Capacitor, 10 nF, 16 V, 10%, -55 to 125 degC, 0402 (1005 Metric), RoHS, Tape and Reel	C3	1	GRM155R71C103KA01D	Murata	Digi-Key	0,09073	0,09073
CAP	C4	1	GRM1555C1H130JA01D	Murata	Arrow Electronics	0,07793	0,07793
CAP CER 0.1UF 16V X7R 0402	C5	1	GRM155R71C104KA88D	Murata	Digi-Key	0,09073	0,09073
Chip Capacitor, 1 uF, +/- 10%, 25 V, 0603 (1608 Metric)	C6, C8	2	Capacitor 1 uF +/- 10% 25 V 06	Yageo	Newark	0,04544	0,09088
Chip Capacitor, 10 uF, +/- 10%, 16 V, -25 to 85 degC, 0805 (2012 Metric), RoHS, Tape and Reel	C7	1	EMK212BJ106KG-T	Taiyo Yuden	Newark	0,03901	0,03901
Multilayer Ceramic Capacitor 1 uF 35V X7R 10% SMD 0805 T/R	C9	1	GMK212B7105KG-T	Taiyo Yuden	Digi-Key	0,2	0,2
CAP CER 4.7UF 10V X7S 0603	C10	1	C1608X7S1A475K080AC	TDK	Mouser	0,285	0,285
CAP TANT POLY 150UF 16V 2917	C11	1	16TQC150MYF	Panasonic	Digi-Key	4,9	4,9
CAP CER 10UF 10V X7R 0805	C12, C15, C26, C29	4	LMK212B7106KG-TD	Taiyo Yuden	Newark	0,08165	0,32661
CAP CER 10000PF 10V X7R 0402	C13, C27	2	C0402C103M8RACTU	KEMET	Mouser	0,30847	0,61693
CAP	C14, C28	2	0402YJ100GBSTR\500	Kyocera AVX	Mouser	0,808	1,616
Chip Capacitor, 1µF +/-0.1%, 25V, 0603, Thickness 1 mm	C16, C17, C18	3	Capacitor 1µF +/-0.1% 25V 06	Samsung	Newark	0,00742	0,02226
General Purpose Ceramic Capacitor, 0402, 18pF, 5%, C0G, 30ppm/°C, 16V	C19, C20	2	0402YA180JAT2A	Kyocera AVX	Mouser	0,30351	0,60702
Chip Capacitor, 100nF +/-20%, 50V, 0402, Thickness 0.6 mm	C21, C22, C23, C25	4	Capacitor 100nF +/-20% 50V 0	Yageo	Newark	0,00742	0,02967
Chip Capacitor, 10nF +/-20%, 50V, 0402, Thickness 0.6 mm	C24	1	Capacitor 10nF +/-20% 50V 04	KEMET	Newark	0,00185	0,00185
DIODE SCHOTTKY 40V 5A SMC	D1	1	B540C-13-F	Diodes	RSComponents	0,51028	12,76
Board-to-Board Connector, PCI104, Self-Nesting Socket, Stackthrough, Vertical, 4-Row, Pitch 2mm, 120-Position, Stack 15.24mm, Receptacle	J1	1	ESQT-130-02-G-Q-368	Harwin	Farnell	16,48	16,48
RF Connector, Onboard Receptacle, IPEX MHFIII	J2	1	RECE-20369-001E-01	Taoglas	Digi-Key	1,44	1,44
Automotive Inductors, High Temperature (155 °C) Series 7.8uH 13.5A 13.48mΩ 20%	L1	1	IHLP5050FDER7R8M5A	Vishay Dale	Mouser	2,6	2,6
Fixed Inductors Commercial High Saturation Series SMT 1uH 4A 52.5mΩ 20%	L2, L4	2	IHLP1616ABER1R0M01	Vishay Dale	Digi-Key	1,13	2,26
WE-LQS SMD Power Inductor, L=33 µH	L3	1	74404042330	Wurth Electronics	Newark	1	1
Serie 312 - 5.08mm Open Horizontal PCB Header WR-TBL, 2 pin	P1	1	691312510002	Wurth Electronics	Digi-Key	0,32248	0,32248
SMT Angled Pin Header WR-PHD, Pitch 2.54 mm, Dual Row, 6 pins	P2	1	610106249121	Wurth Electronics	RSComponents	1,47	1,47
MOSFET N-CH 12V 76A 6SON	Q1	1	CSD13202Q2	Texas Instruments	Mouser	0,589	0,589
RESISTOR	R1	1	RC0402FR-0712K1L	Yageo	Newark	0,00379	0,00379
Chip Resistor, 68.1 KOhm, +/- 1%, 100 mW, -55 to 155 degC, 0402 (1005 Metric), RoHS, Tape and Reel	R2, R3	2	ERJ-2RKF6812X	Panasonic	Newark	0,00379	0,00759
RESISTOR	R4	1	CRCW040210R0FKED	Vishay	Newark	0,11856	0,11856
100K 0.063W 1% 0402 (1005 Metric) SMD	R5, R7	2	100KR2F	Vishay	Mouser	0,722	1,444
RESISTOR	R6	1	ERJ-L14KF33MU	Panasonic	Arrow Electronics	0,095	0,29867
Res Thick Film 0402 1MΩ 5% 0.063W ±100ppm/°C Molded SMD T/R	R8, R9, R13, R16, R17, R2	6	RC1005J105CS	Samsung	Avnet	0,00322	32,25
RES SMD 100 OHM 1% 1/8W 0603	R10, R11, R18, R19	4	MCT06030D2003BP100	Vishay BCcomponent	RSComponents	0,72921	3,65
Res MC Precision Thin Film 1206 15kΩ 0.1% 0.25W ±25ppm/°C Molded Paper T/R	R12, R20	2	MCA12060D1502BP100	Vishay	Digi-Key	0,27079	0,54158
RES Thick Film, 33kΩ, 1%, 0.1W, 100ppm/°C, 0603	R14, R22	2	CRCW060333K0FKEA	Vishay	Newark	0,09485	0,18969
Chip Resistor, 10 KOhm, +/- 1%, 100 mW, -55 to 155 degC, 0603 (1608 Metric), RoHS, Tape and Reel	R15	1	CRCW060310K0FKEA	Vishay	Newark	0,1214	0,1214
SWITCH TACTILE SPST-NO 0.02A 15V	SW1	1	EVQ-Q2U03W	Panasonic	Avnet	0,10991	0,10991
EEPROM E-EPROM	U1	1	M95M02-DWMN3TP_K	STMicroelectronics	RSComponents	4,64	23,18
IC, 74HC CMOS, SMD, 74HC138, SOIC16	U2	1	MC74HC138ADG	ON Semiconductor	Future Electronics	0,32248	0,32248
NVRAM 4Mb 3.3V 512Kx8 SPI	U3	1	MR25H40MDF	Everspin	Mouser	30,88	30,88
CY15B108QN-40SXI	U4	1	CY15B108QN-40SXI	Cypress	Mouser	38,37	38,37
NOR Flash SPI FLASH NOR SLC 128MX8 SOIC DDP	U5	1	MT25TL01GBBB8ESF-0AAT_TR	Micron Technology	Mouser	19,71	19,71
NAND Flash 1G-bit Serial NAND flash	U6	1	W25N01GVSFIT	Winbond	Mouser	3,12	3,12
Integrated Circuit	U7	1	LM51501QRUMTQ1	Texas Instruments	Mouser	2,73	2,73
TPS61236PRWLR	U8, U13	2	TPS61236PRWLR	Texas Instruments	Mouser	2,23	4,46
TPS630242YFFR	U9	1	TPS630242YFFR	Texas Instruments	Mouser	1,23	1,23
GPS Venus	U10	1	GPS Venus838FLPx	KNCTREK	-	185,42	185,42
MCU, 8-Bit, ATMEGA, 20 MHz, 1.8 to 5.5 V, -40 to 85 degC, 32-Pin QFN (32M1-A), RoHS	U11	1	ATMEGA328P-MU	Microchip / Atmel	Mouser	2,64	2,64
iNEMO Inertial Module: 3D Accelerometer, 3D Gyroscope, 3D Magnetometer, 1.9 to 3.6 V, -40 to 85 degC, 24-Pin LGA, RoHS, Tape and Reel	U12	1	LSM9DS1TR	STMicroelectronics	Mouser	24,23	24,23
Crystal 16MHz ±20ppm 18pF SMD-2 5mm x 3.2mm	Y1	1	ABM3-16.000MHZ-D2Y-T	ABRACON	Mouser	0,608	0,608
MEMS Oscillator 5MHz ±50ppm LVCMOS 1.8V~3.3V SMD 2.5x2mm	Y2	1	ASDMB-5.000MHZ-LC-T	ABRACON	Mouser	1,84	1,84
MEMS Oscillator 100MHz ±50ppm LVCMOS 3.3V SMD 2.5x2mm	Y3	1	ASDM1-100.000MHZ-LC-T	ABRACON	Mouser	1,87	1,87
Crystal or Oscillator	Y4	1	SIT8008AI-33-33S-90	SiTime	Mouser	0,231	0,231
XTAL OSC XO 40.0000MHZ CMOS SMD	Y5	1	625L3C040M00000	CTS	Digi-Key	1,75	1,75
						TOTAL	430,19 €

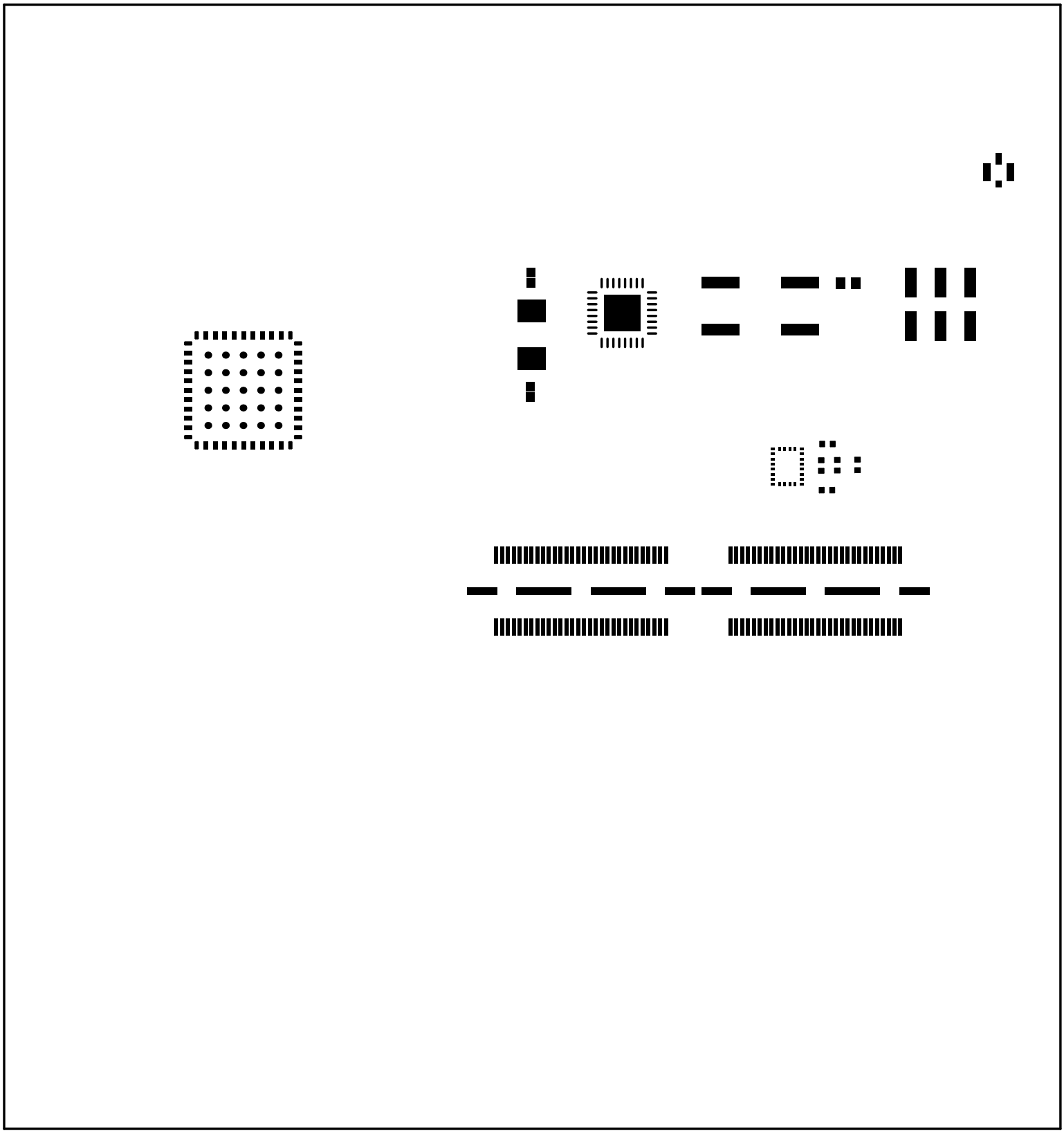
ANEXO III

Capas de la PCB

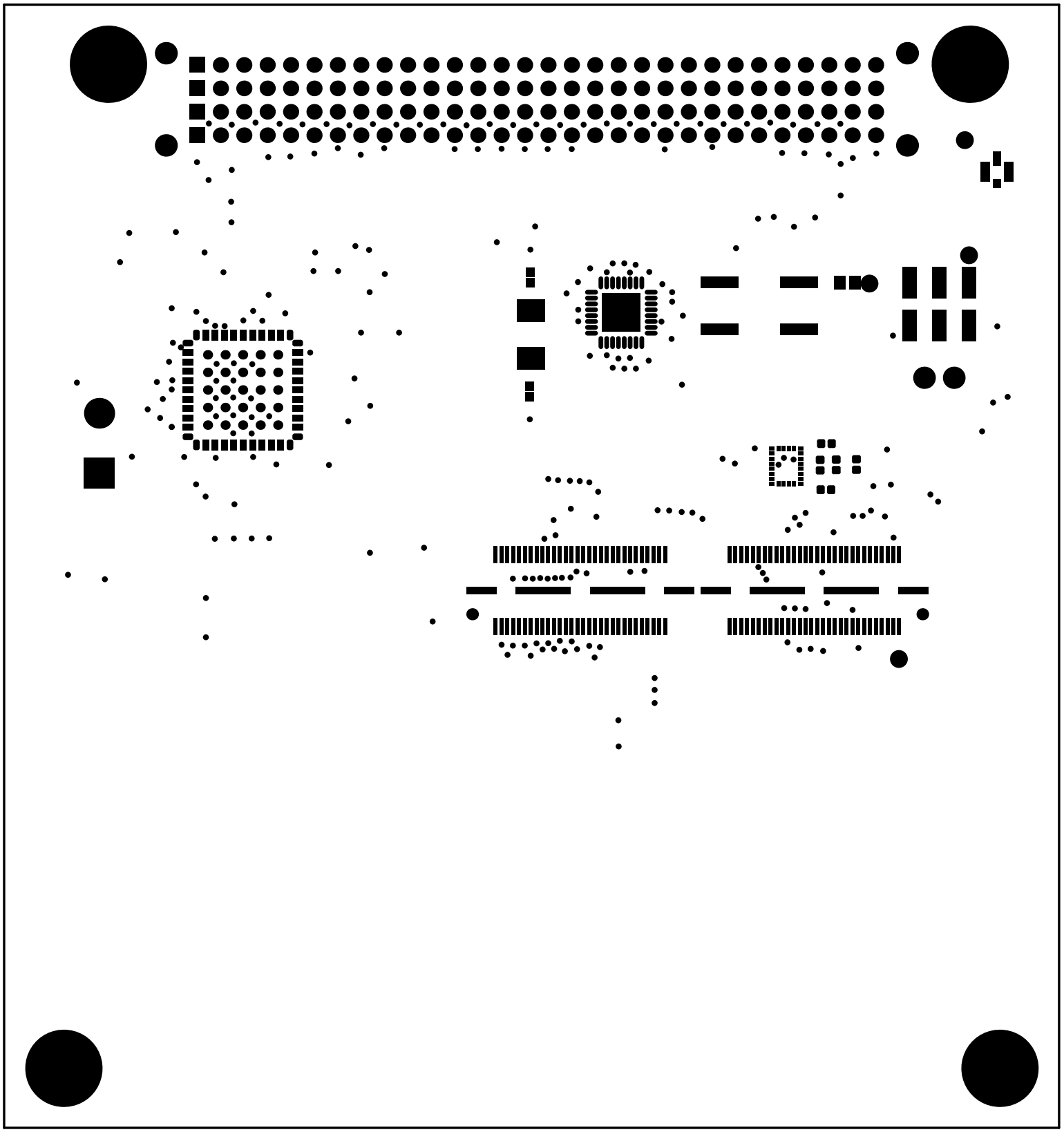
Serigrafía superior



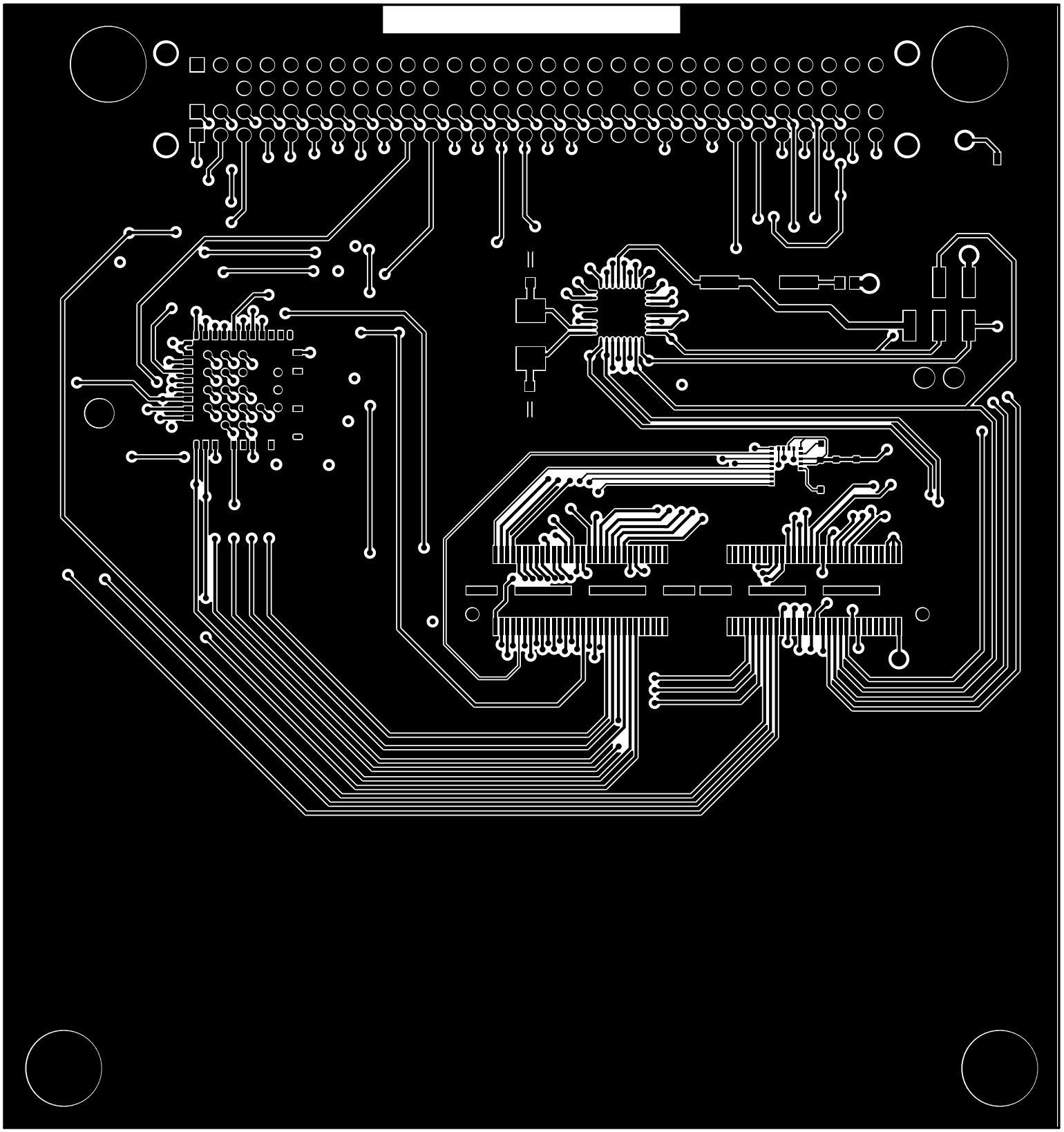
Pasta de soldadura superior



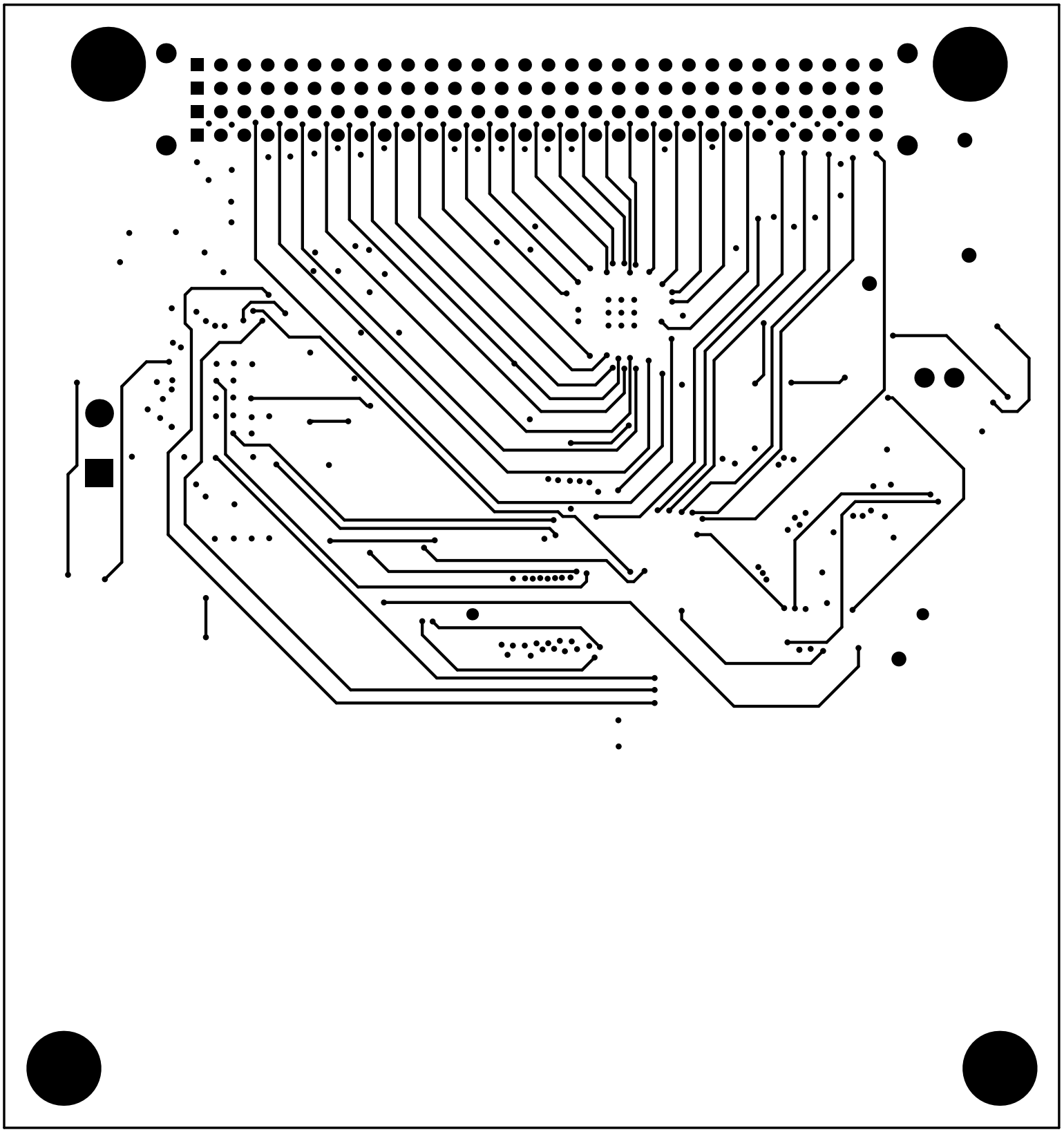
Máscara de soldadura superior



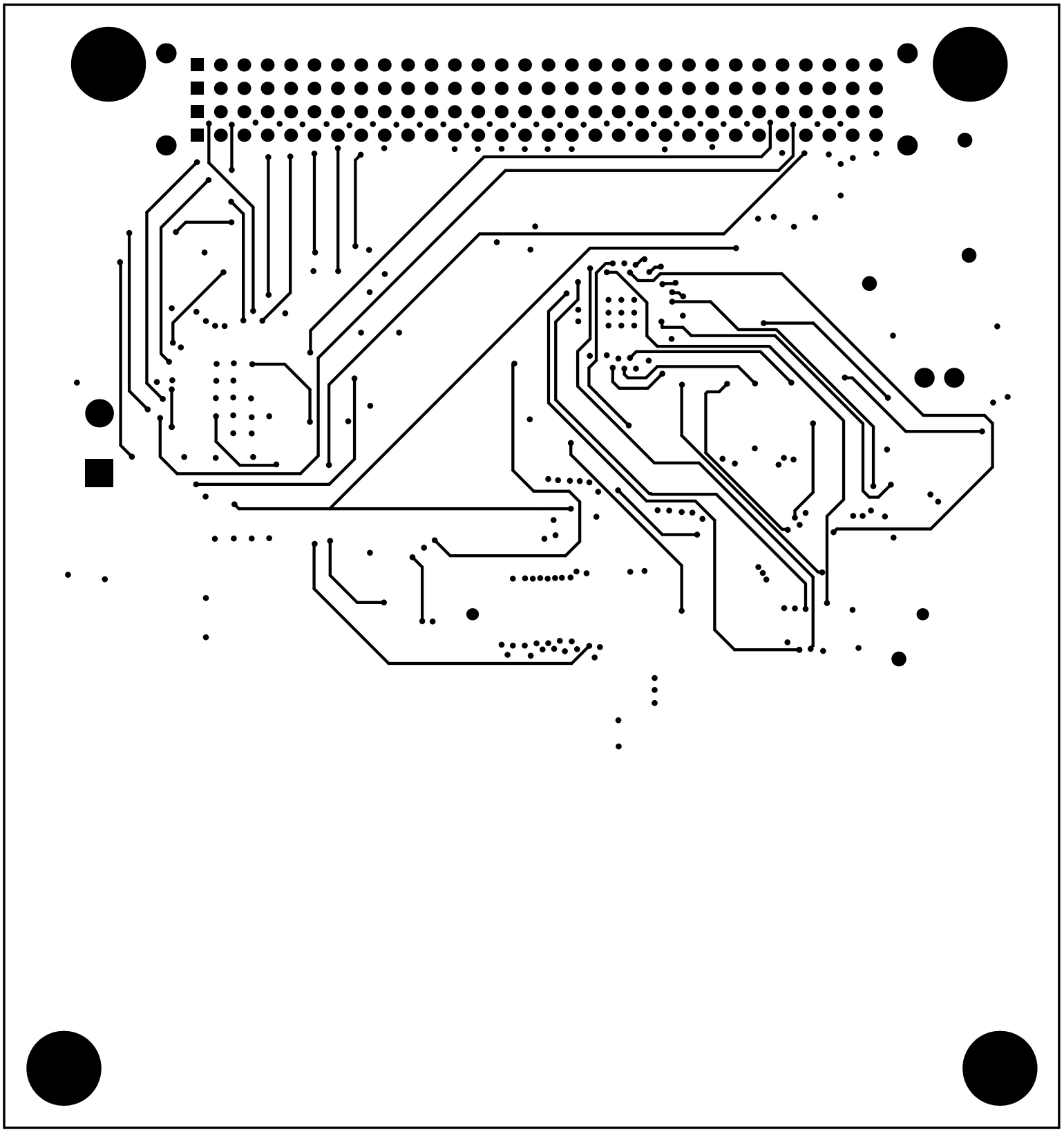
Capa 1



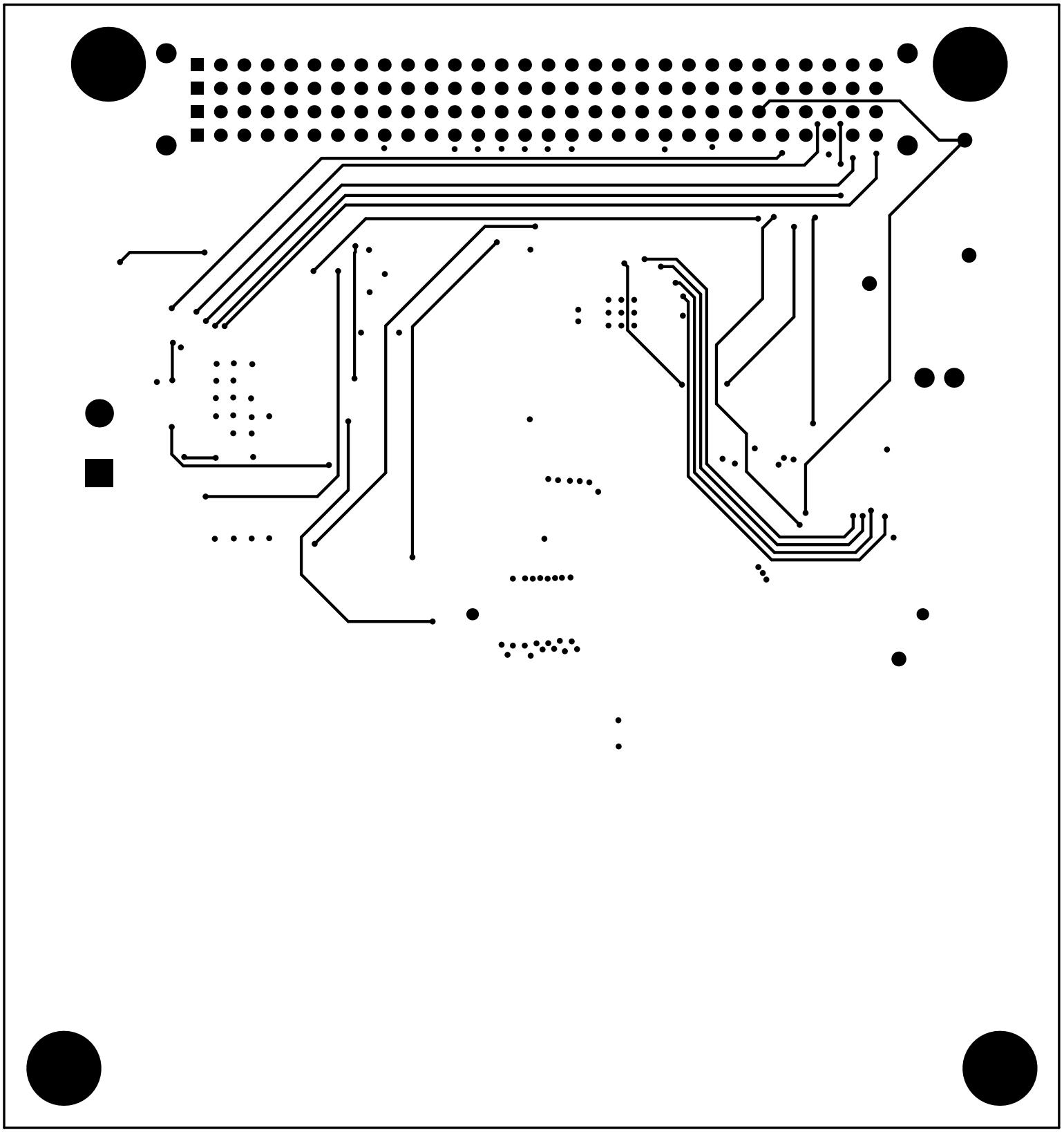
Capa 2



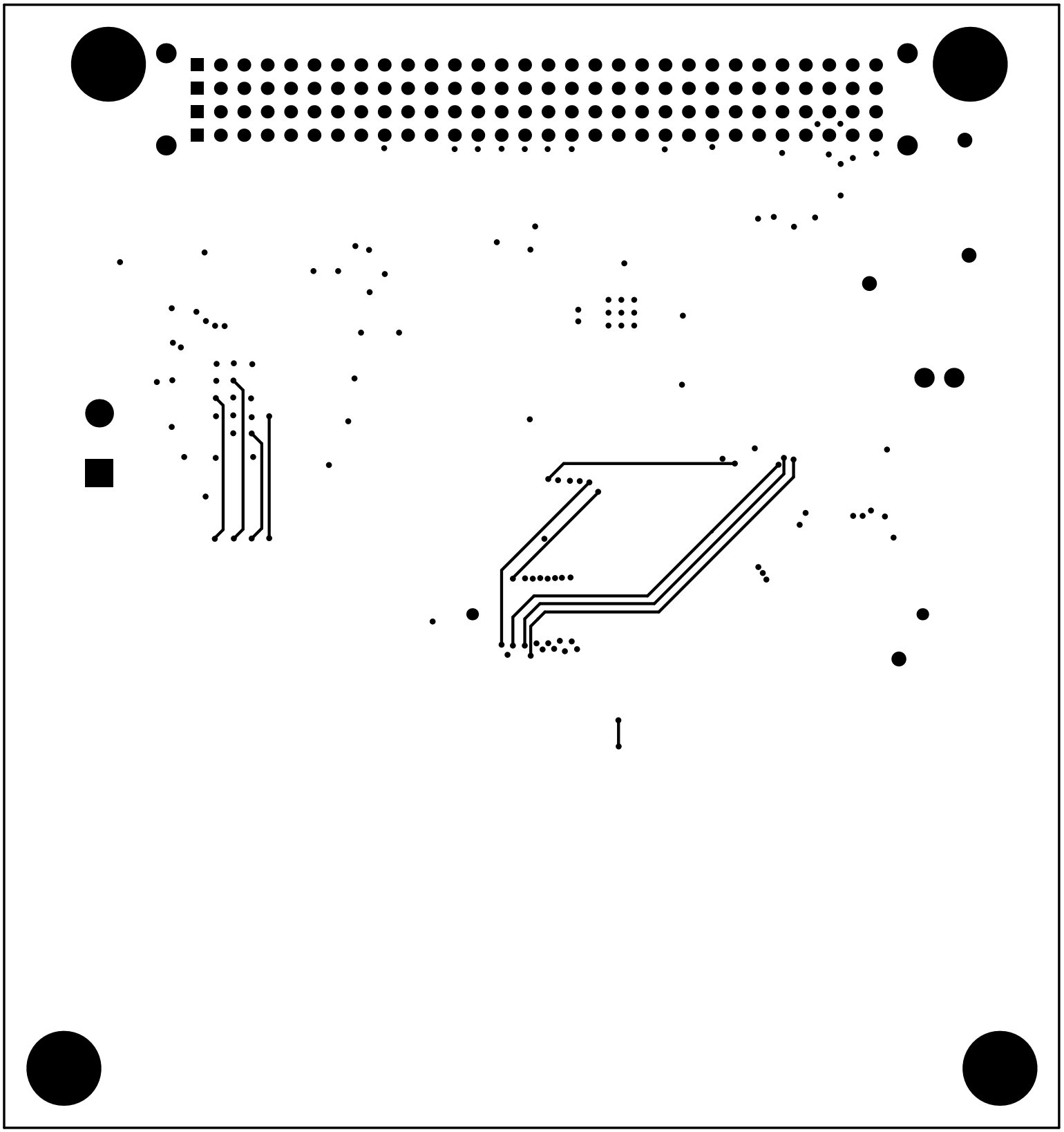
Capa 3



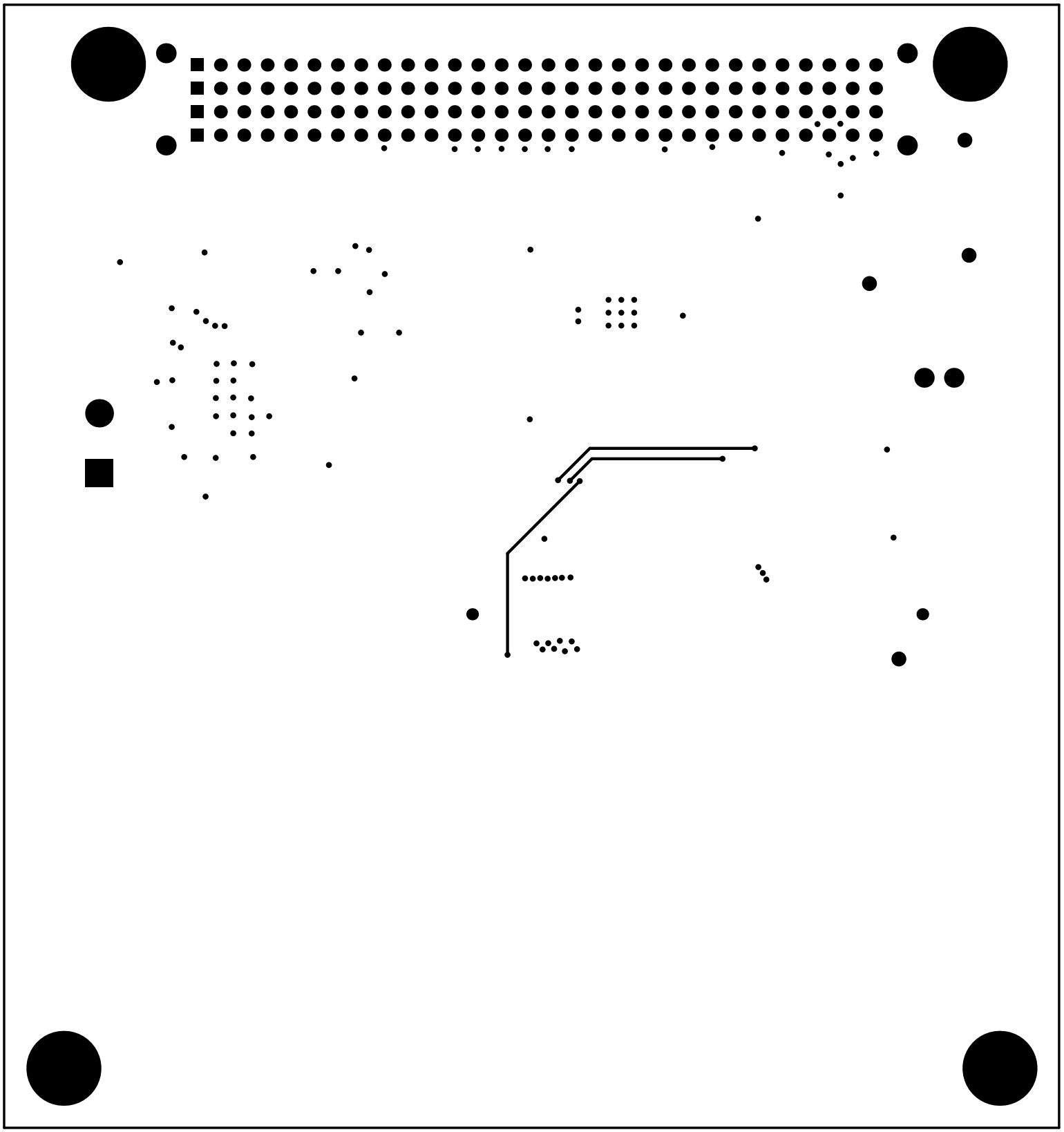
Capa 4



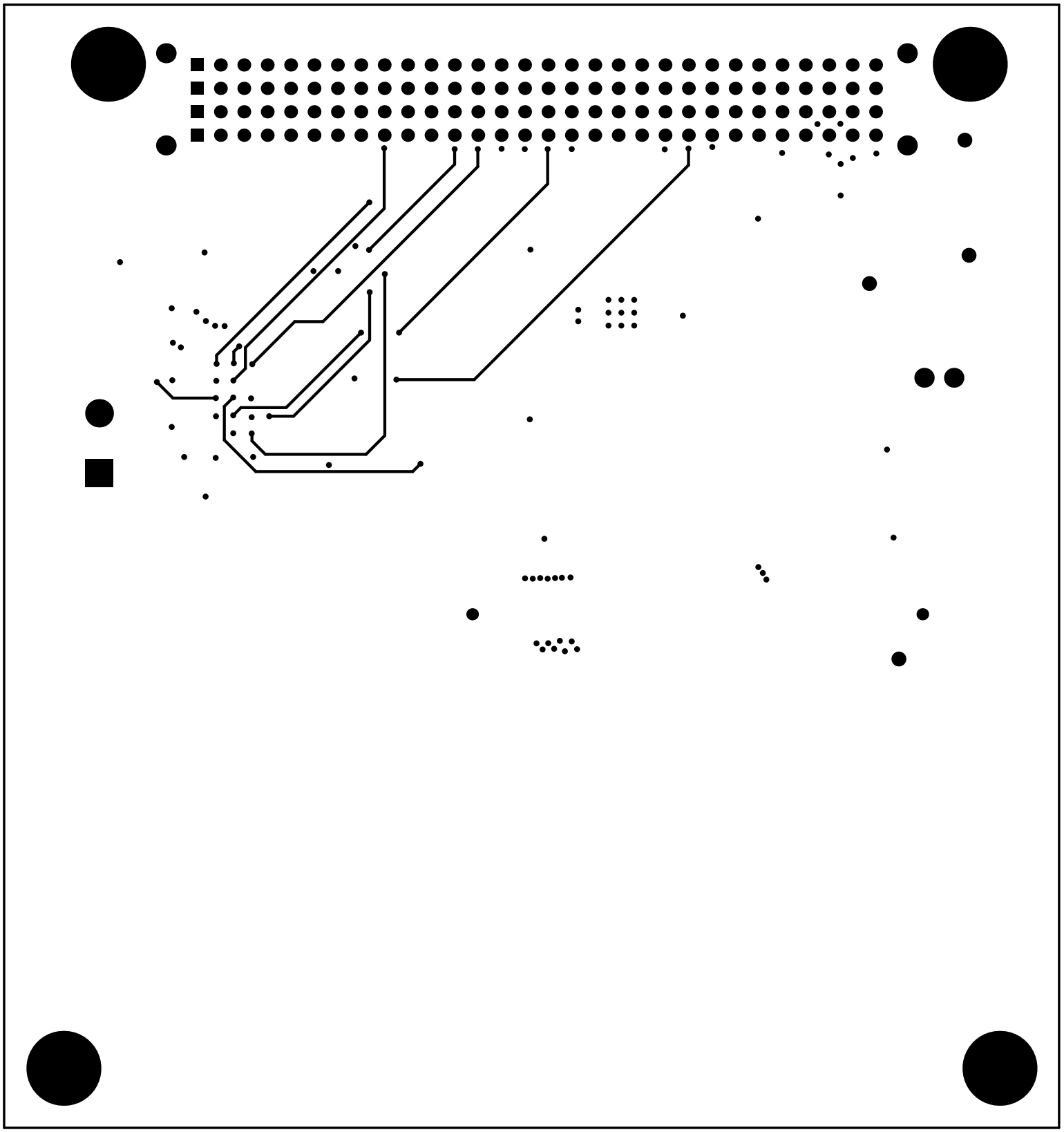
Capa 5



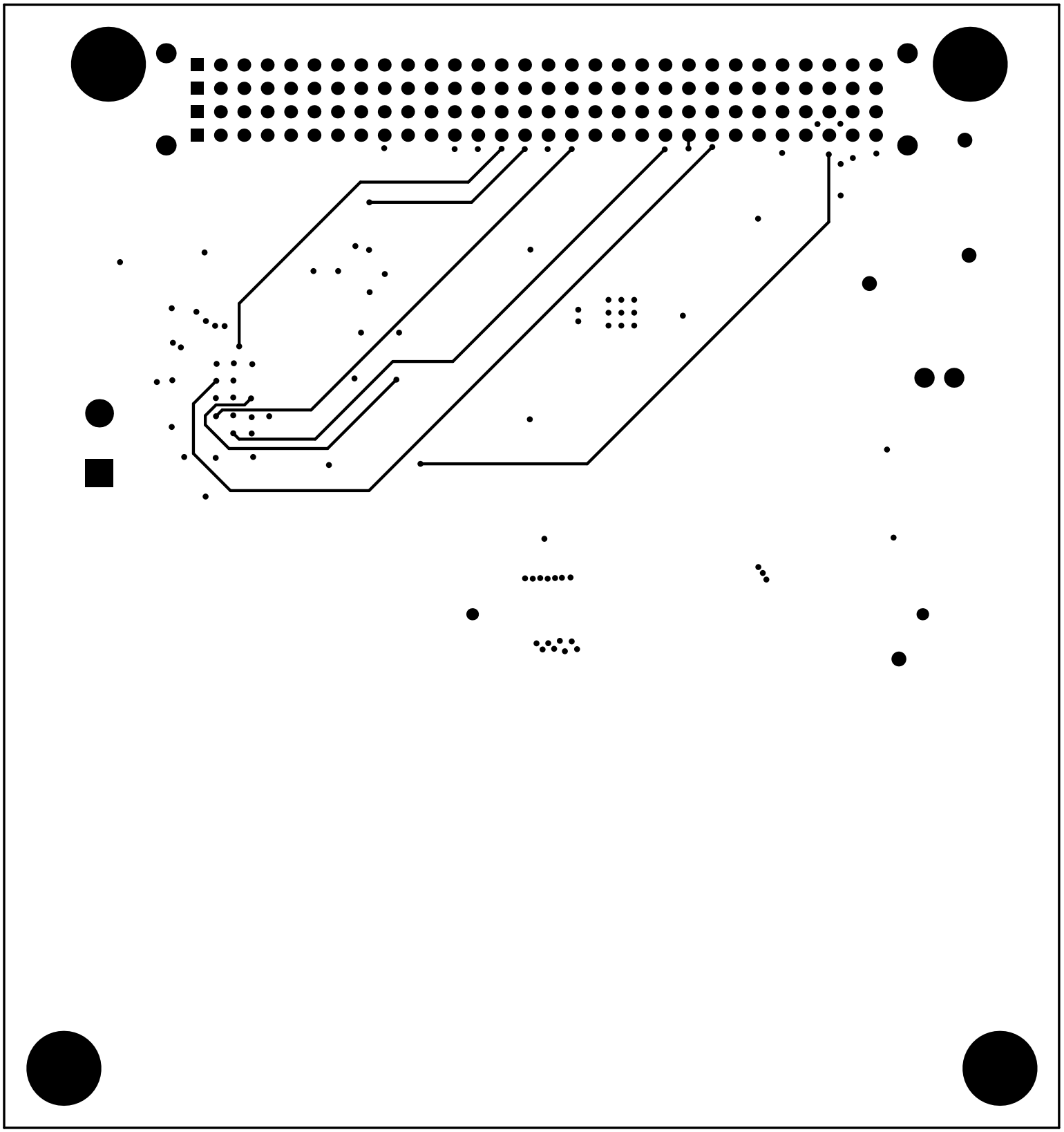
Capa 6



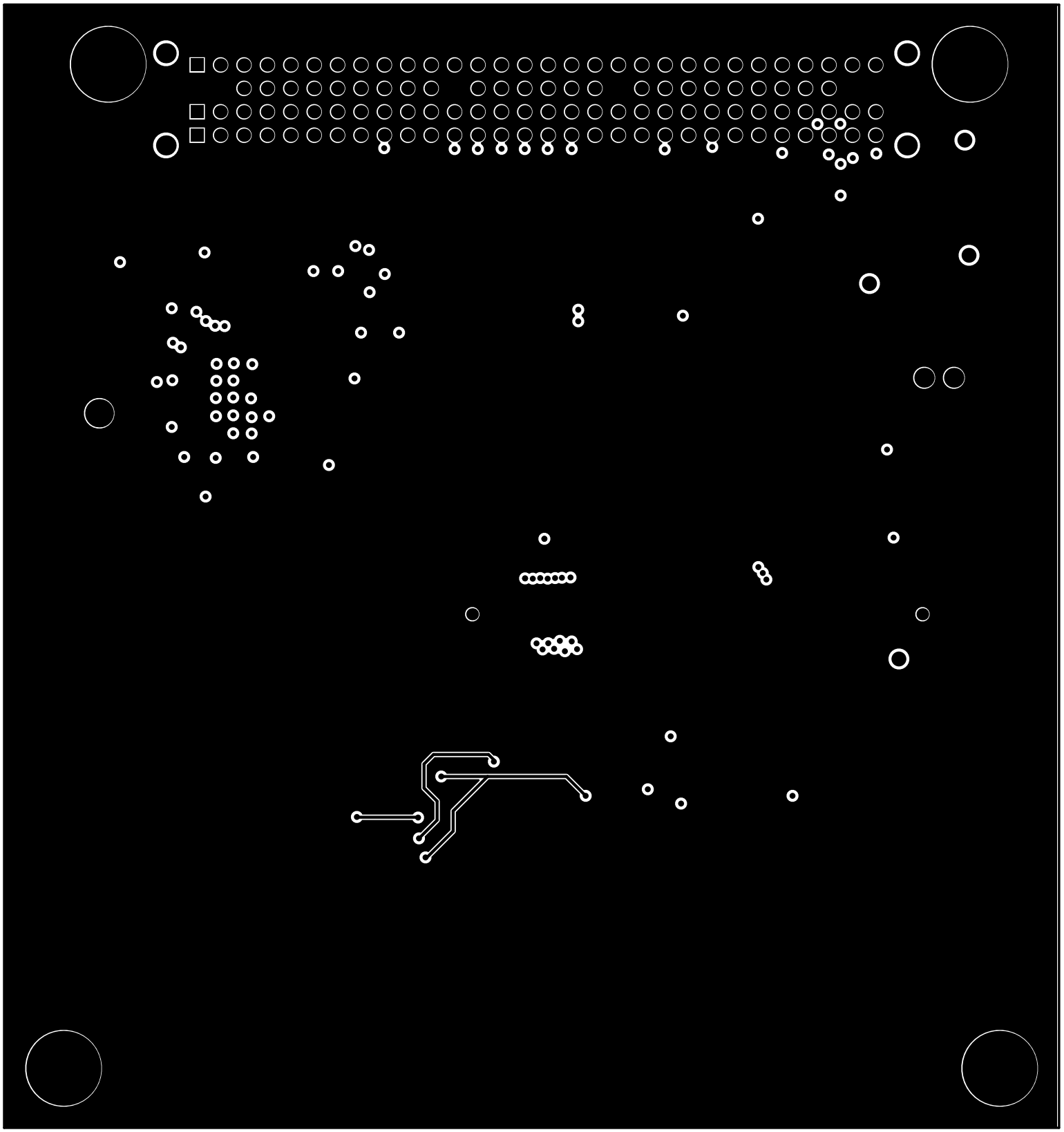
Capa 7



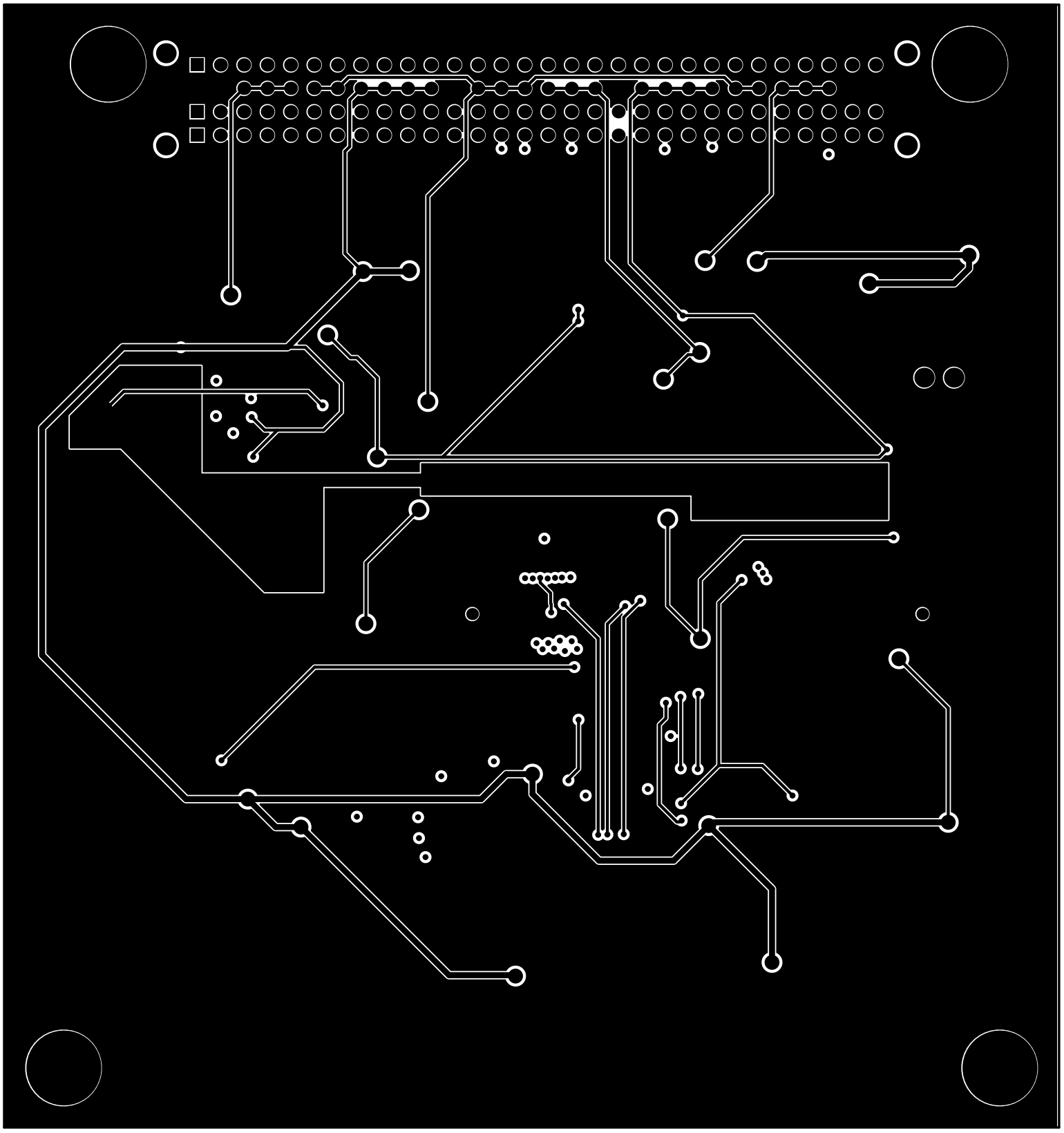
Capa 8



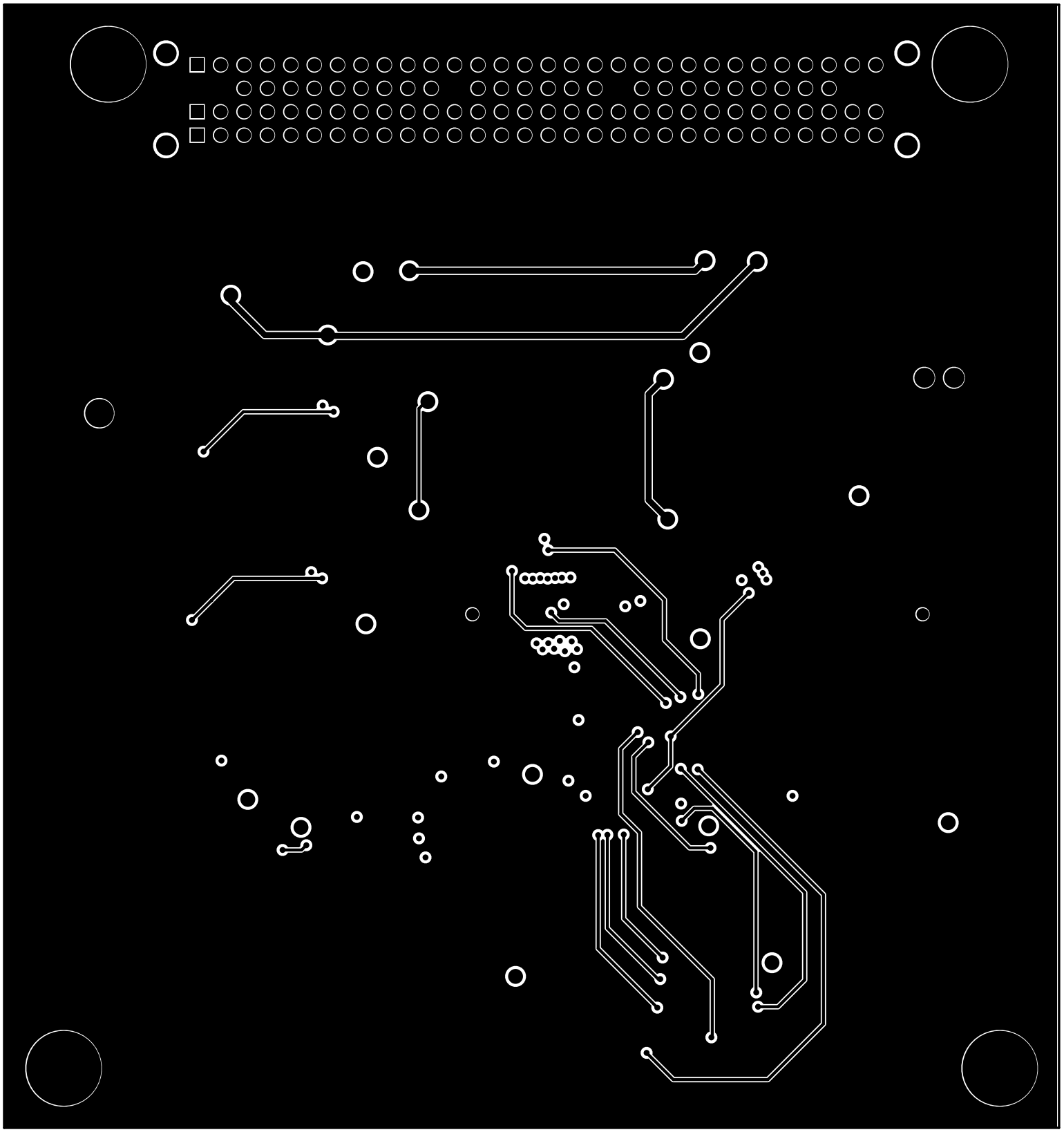
Capa 9



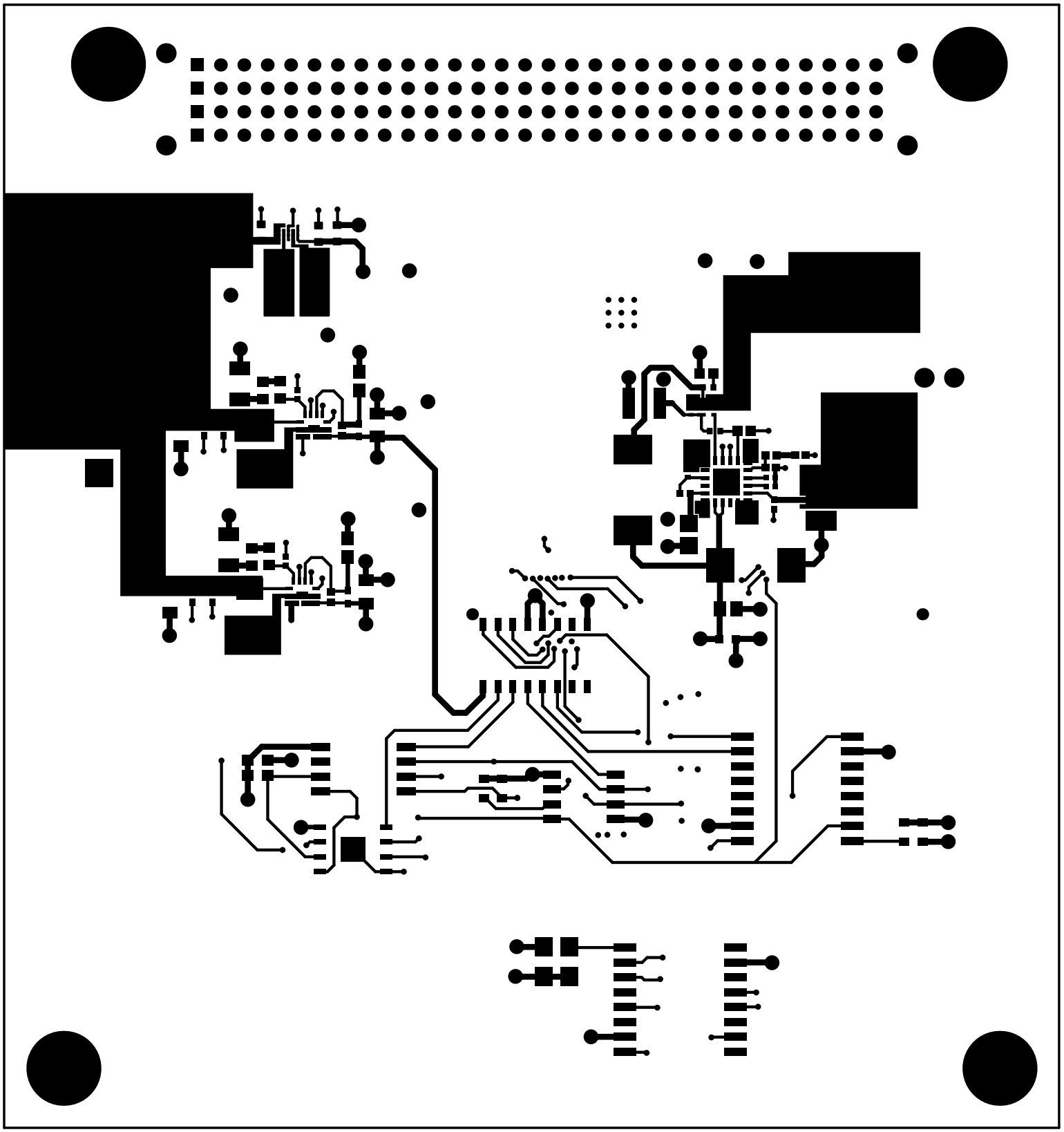
Capa 10



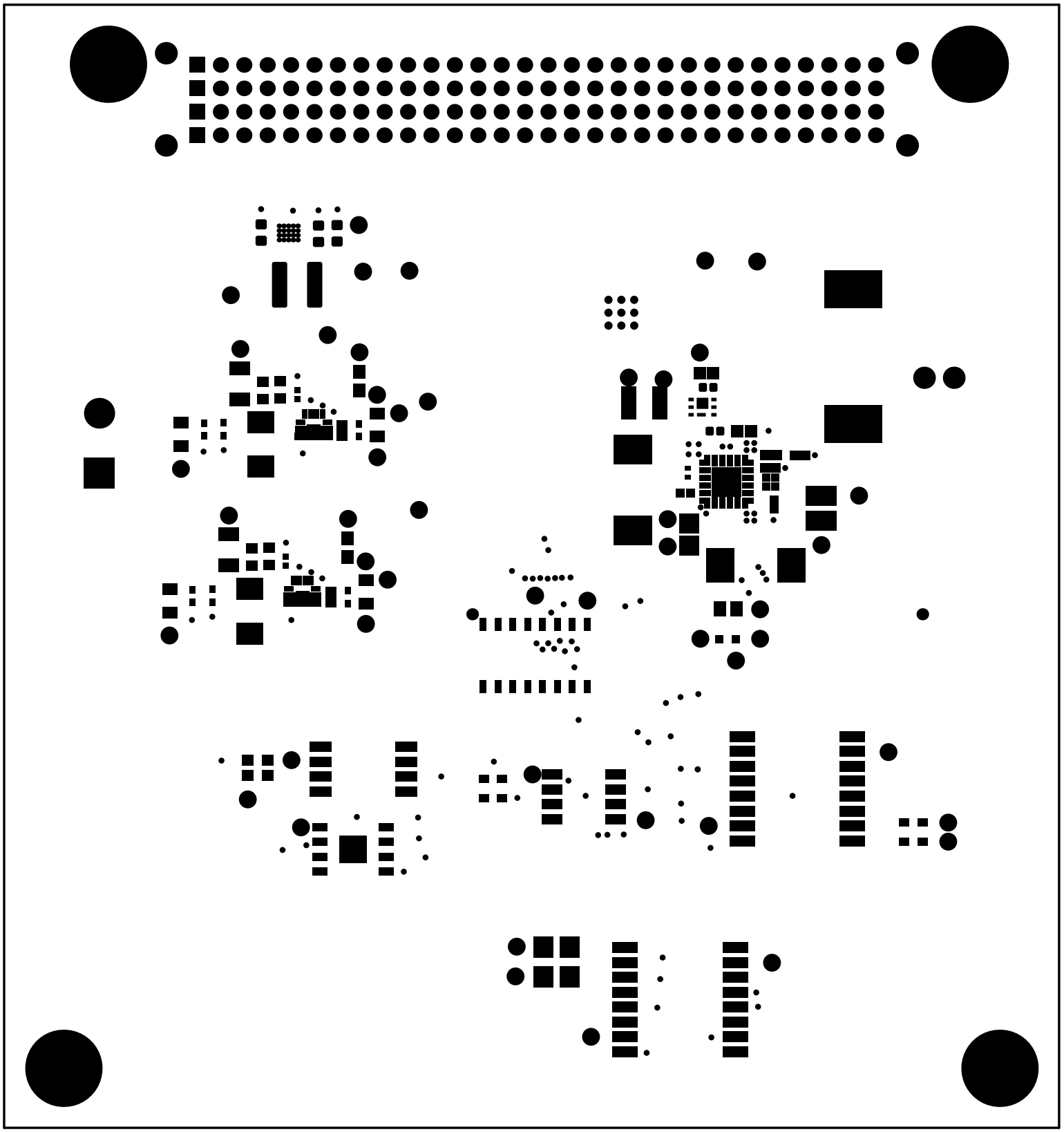
Capa 11



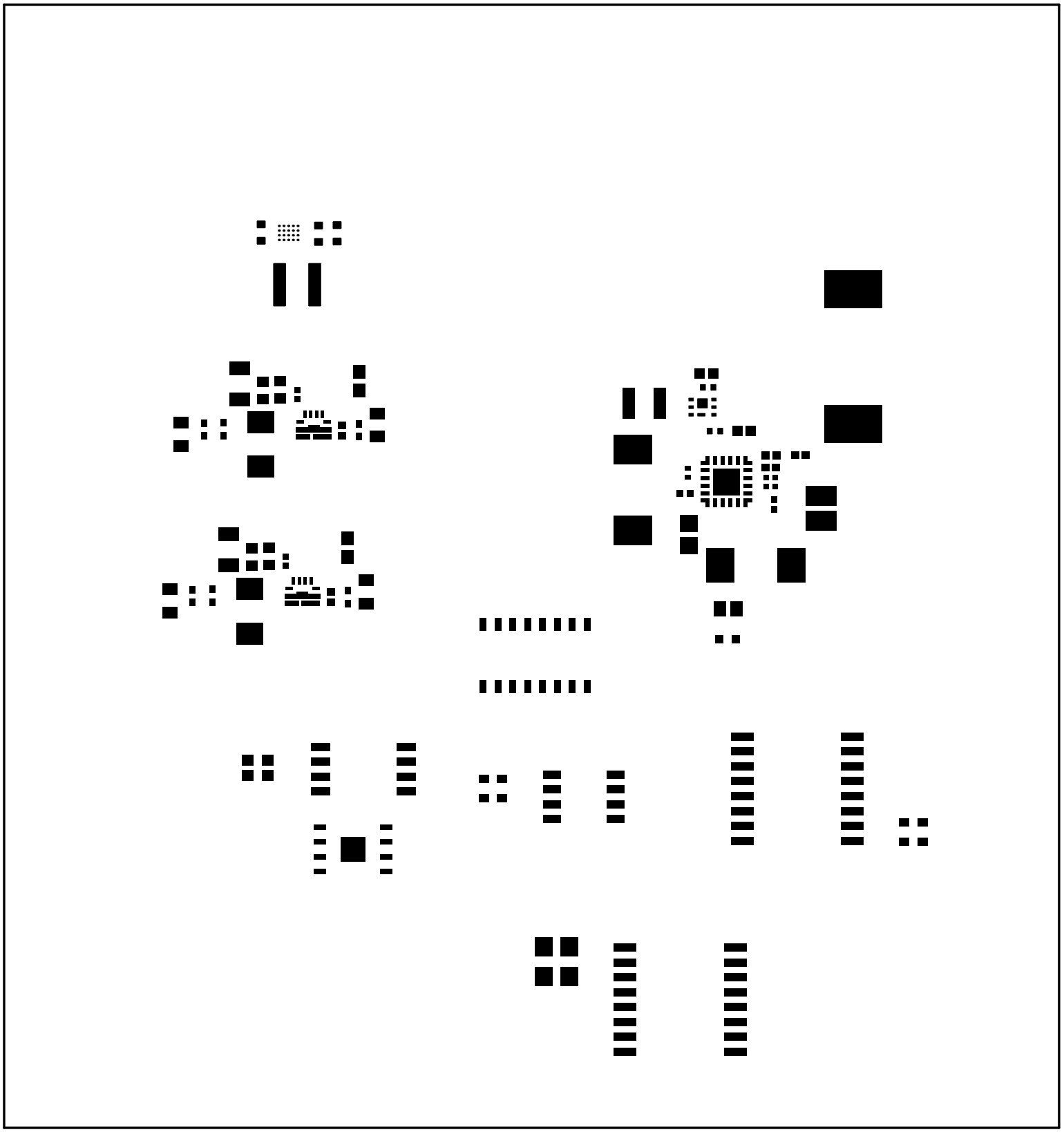
Capa 12



Máscara de soldadura inferior



Pasta de soldadura inferior



Serigrafía inferior

ANEXO IV

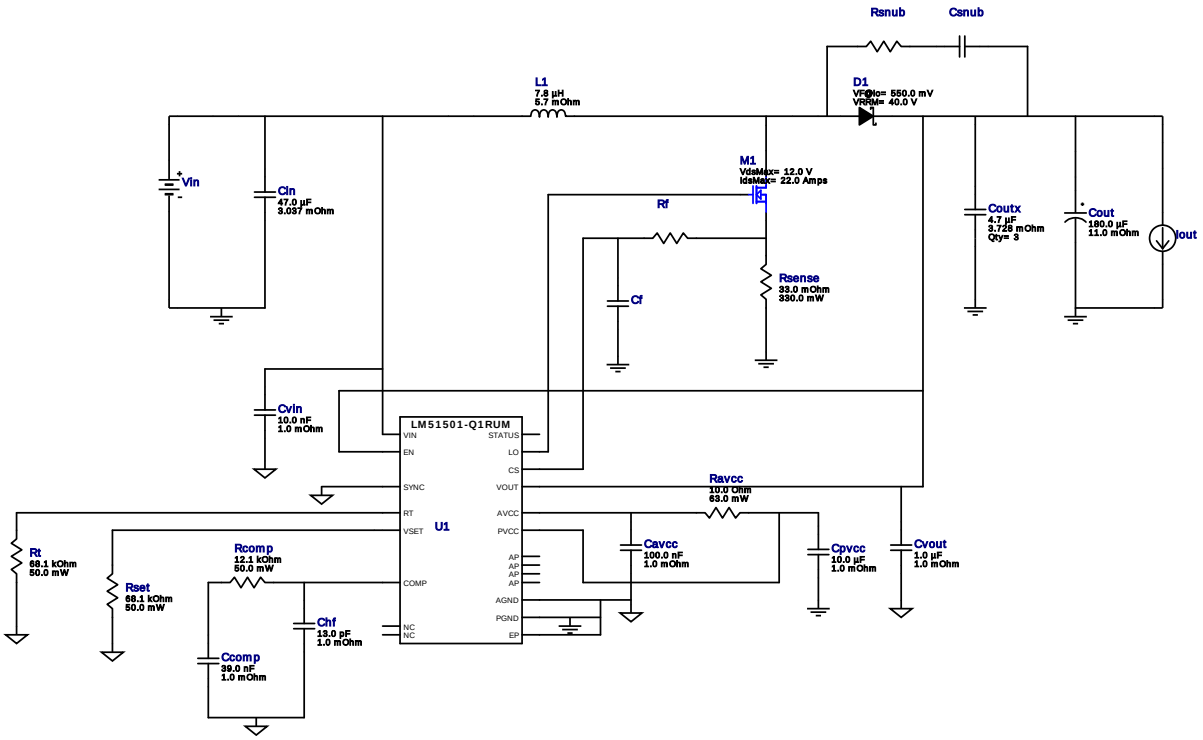
Reportes de la herramienta WEBENCH

VinMin = 2.5V
VinMax = 4.35V
Vout = 6.5V
Iout = 0.8A

Device = LM51501QRUMRQ1
Topology = Boost_PassThrough
Created = 2022-02-12 19:12:58.089
BOM Cost = $4.11
BOM Count = 20
Total Pd = 0.44W

WEBENCH® Design Report

Design : 3 LM51501QRUMRQ1
LM51501QRUMRQ1 2.5V-4.35V to 6.50V @ 0.8A



1. Proper values for Rsnub, Csnub, Rf, and Cf need to be selected by the user based on the input output condition. When Vin is greater than Vout, device operates in Pass Through Mode, where Vout is nearly equal to Vin.

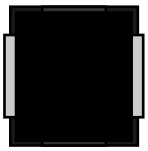
Design Alerts

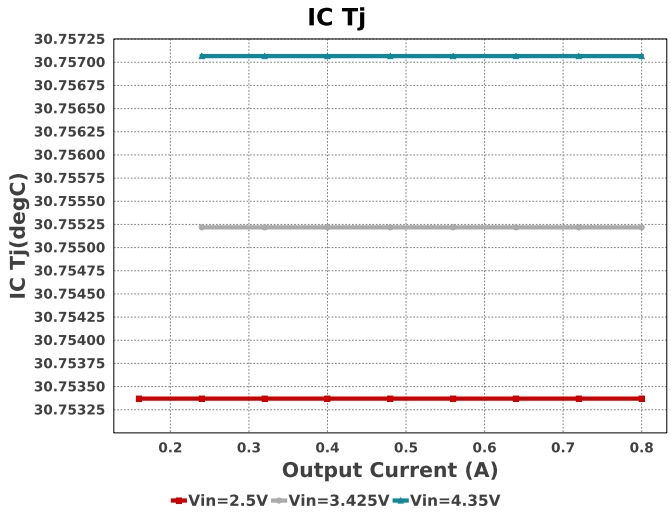
Component Selection Information

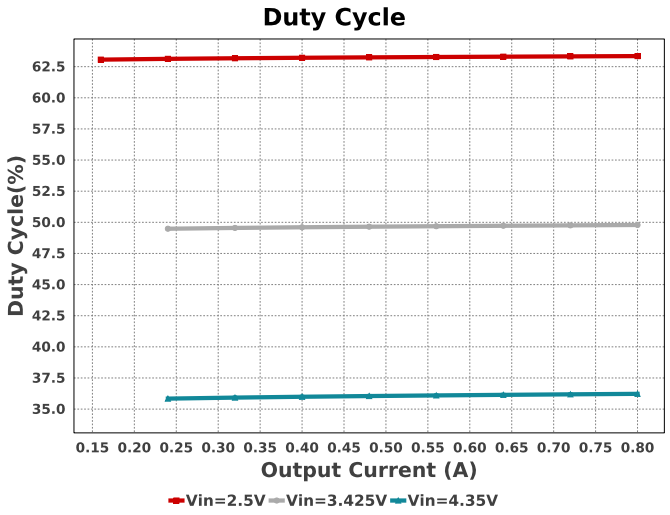
The LM51501-Q1 is qualified for Automotive applications. All passives and other components selected in this design may not be qualified for Automotive applications. The user is required to verify that all components in the design meet the qualification and safety requirements for their specific application. This device requires minimum 5V at VOUT pin to start up. WEBENCH will run the simulation at 5V if the minimum input voltage is less than 5V

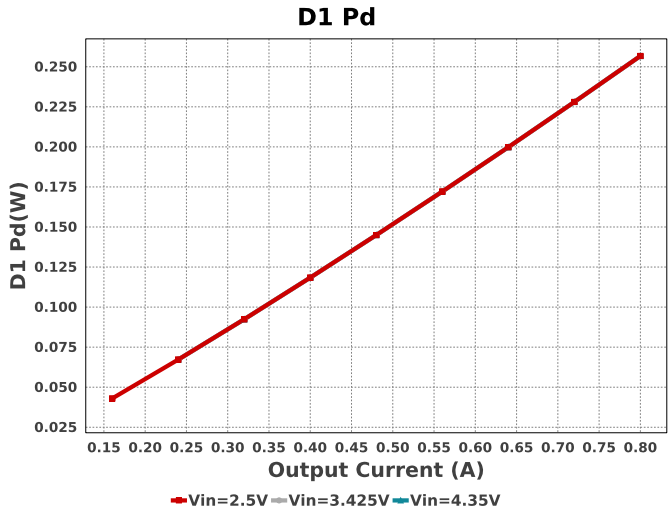
Electrical BOM

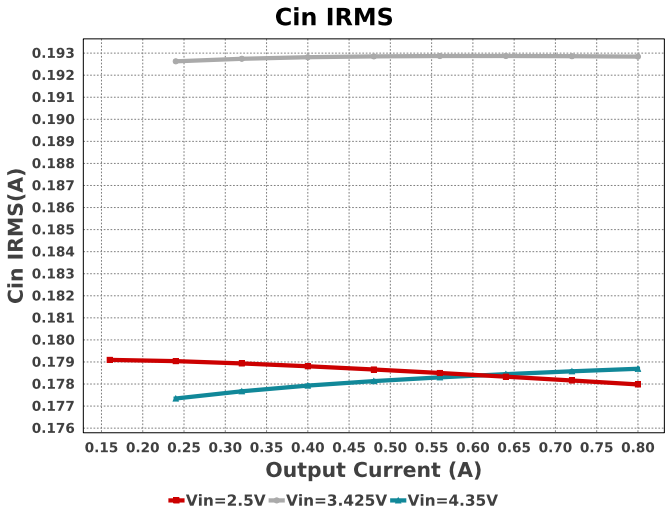
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cavcc	MuRata	GRM155R71C104KA88D Series= X7R	Cap= 100.0 nF ESR= 1.0 mOhm VDC= 16.0 V IRMS= 0.0 A	1	$0.01	0402 3 mm^2
Ccomp	MuRata	GRM155R61A393KA01D Series= X5R	Cap= 39.0 nF ESR= 1.0 mOhm VDC= 10.0 V IRMS= 0.0 A	1	$0.01	0402 3 mm^2
Chf	MuRata	GRM1555C1H130JA01D Series= C0G/NP0	Cap= 13.0 pF ESR= 1.0 mOhm VDC= 50.0 V IRMS= 0.0 A	1	$0.01	0402 3 mm^2
Cin	MuRata	GRM32ER61C476KE15L Series= X5R	Cap= 47.0 uF ESR= 3.037 mOhm VDC= 16.0 V IRMS= 4.59346 A	1	$0.38	1210_280 15 mm^2

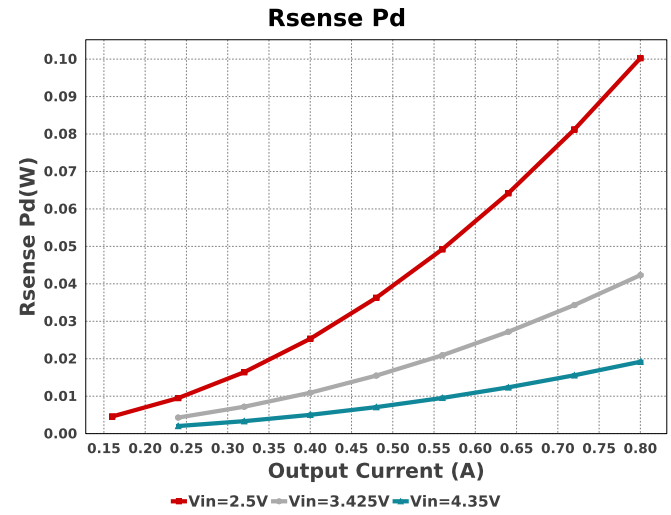
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cout	Panasonic	16SVPE180M Series= SVPE	Cap= 180.0 uF ESR= 11.0 mOhm VDC= 16.0 V IRMS= 4.46 A	1	$0.50	 CAPSMT_62_C10 74 mm²
Coutx	TDK	C1608X7S1A475K080AC Series= X7S	Cap= 4.7 uF ESR= 3.728 mOhm VDC= 10.0 V IRMS= 2.69359 A	3	$0.05	 0603 5 mm²
Cpvcc	Taiyo Yuden	EMK212BJ106KG-T Series= X5R	Cap= 10.0 uF ESR= 1.0 mOhm VDC= 16.0 V IRMS= 0.0 A	1	$0.03	 0805 7 mm²
Cvin	MuRata	GRM155R71C103KA01D Series= X7R	Cap= 10.0 nF ESR= 1.0 mOhm VDC= 16.0 V IRMS= 0.0 A	1	$0.01	 0402 3 mm²
Cvout	Taiyo Yuden	GMK212B7105KG-T Series= X7R	Cap= 1.0 uF ESR= 1.0 mOhm VDC= 35.0 V IRMS= 0.0 A	1	$0.03	 0805 7 mm²
D1	Diodes Inc.	B540C-13-F	VF@Io= 550.0 mV VRRM= 40.0 V	1	$0.17	 SMC 83 mm²
L1	Coiltronics	HC1-7R8-R	L= 7.8 µH 5.7 mOhm	1	$1.74	 HC1 225 mm²
M1	Texas Instruments	CSD13202Q2	VdsMax= 12.0 V IdsMax= 22.0 Amps	1	$0.13	DQK0006C 9 mm²
Ravcc	Vishay-Dale	CRCW040210R0FKED Series= CRCW..e3	Res= 10.0 Ohm Power= 63.0 mW Tolerance= 1.0%	1	$0.01	 0402 3 mm²
Rcomp	Yageo	RC0201FR-0712K1L Series= ?	Res= 12.1 kOhm Power= 50.0 mW Tolerance= 1.0%	1	$0.01	 0201 2 mm²
Rsense	Panasonic	ERJ-L14KF33MU Series= ERJ-L14	Res= 33.0 mOhm Power= 330.0 mW Tolerance= 1.0%	1	$0.11	 1210 15 mm²
Rset	Yageo	RC0201FR-7D68K1L Series= ?	Res= 68.1 kOhm Power= 50.0 mW Tolerance= 1.0%	1	$0.01	 0201 2 mm²
Rt	Yageo	RC0201FR-7D68K1L Series= ?	Res= 68.1 kOhm Power= 50.0 mW Tolerance= 1.0%	1	$0.01	 0201 2 mm²
U1	Texas Instruments	LM51501QRUMRQ1	Switcher	1	$0.79	RUM0016C 25 mm²

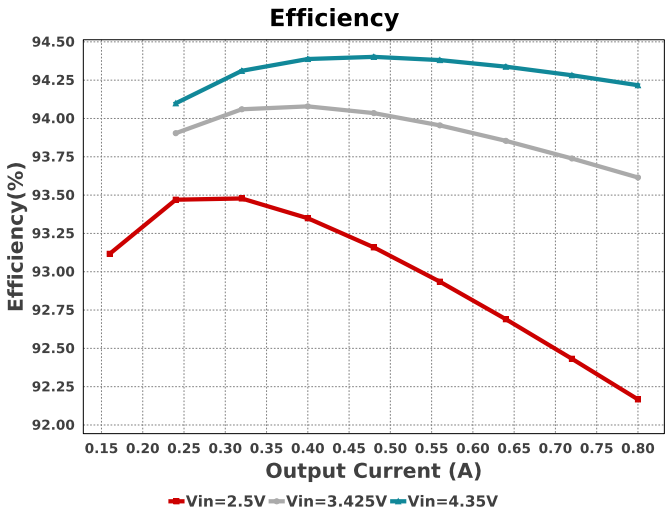


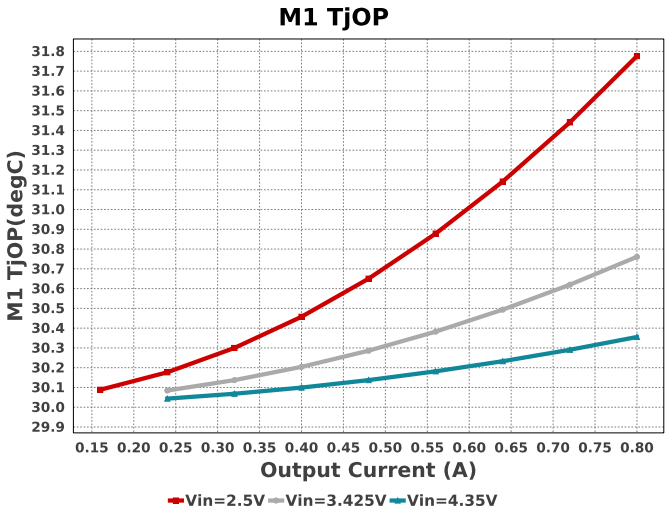


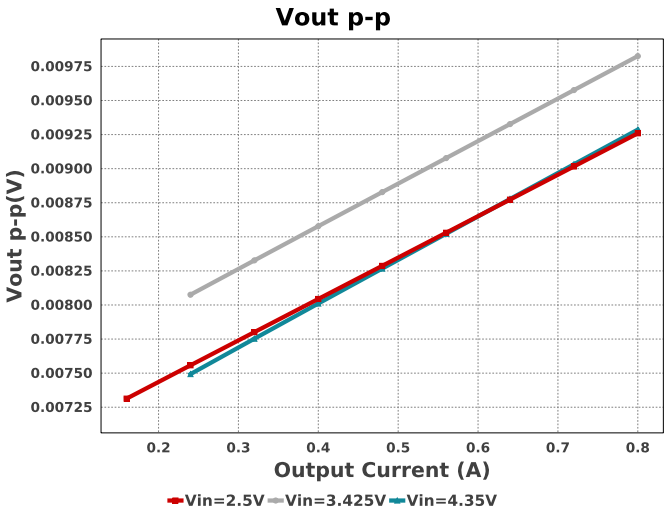


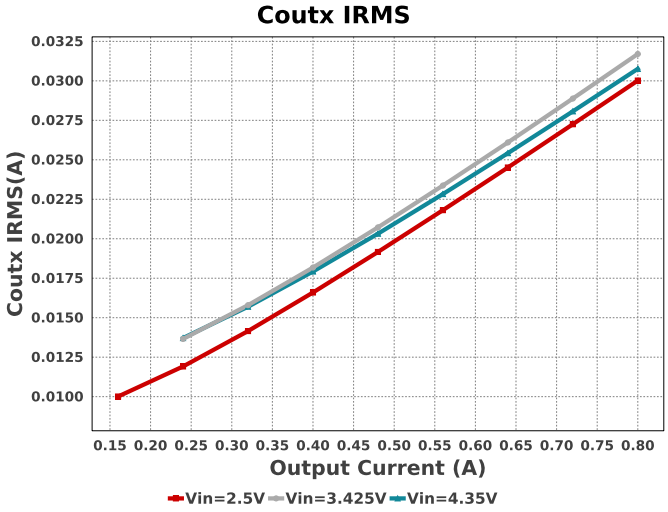


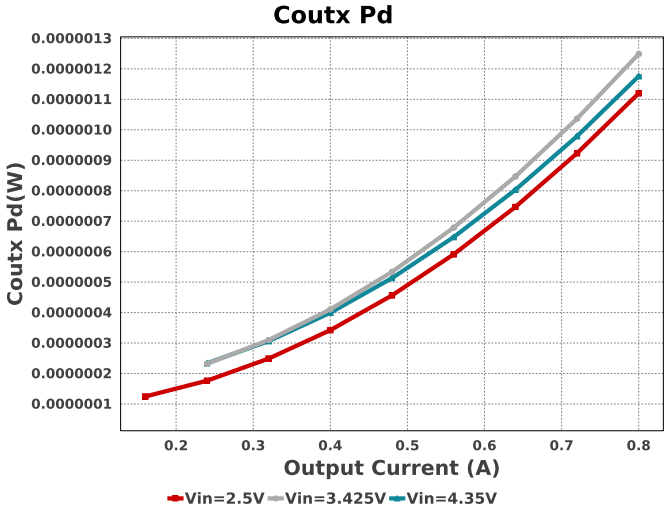


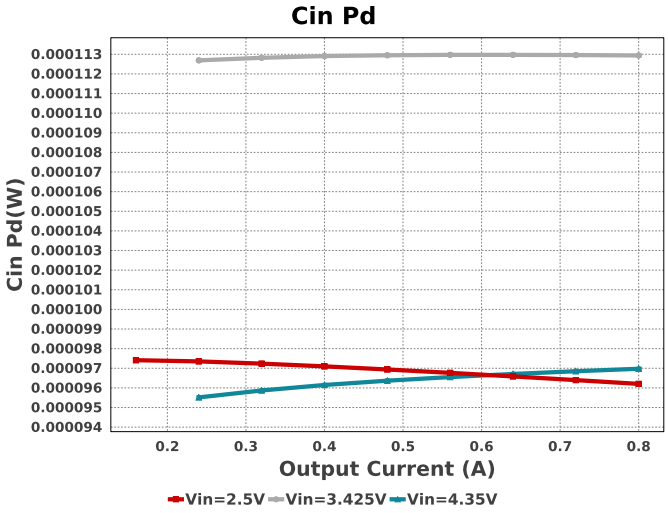


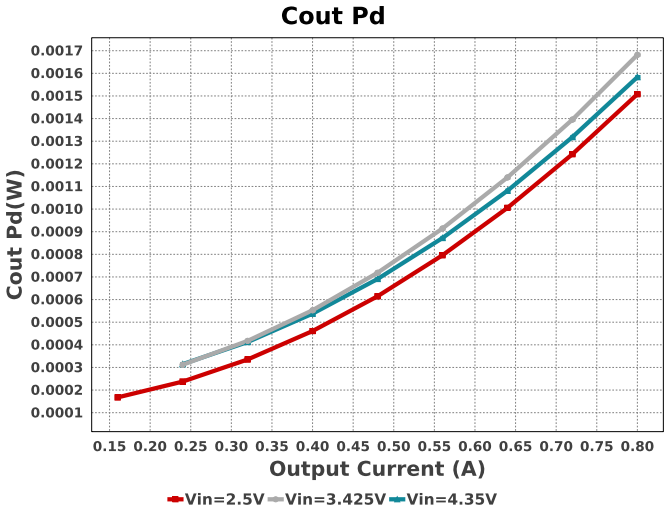


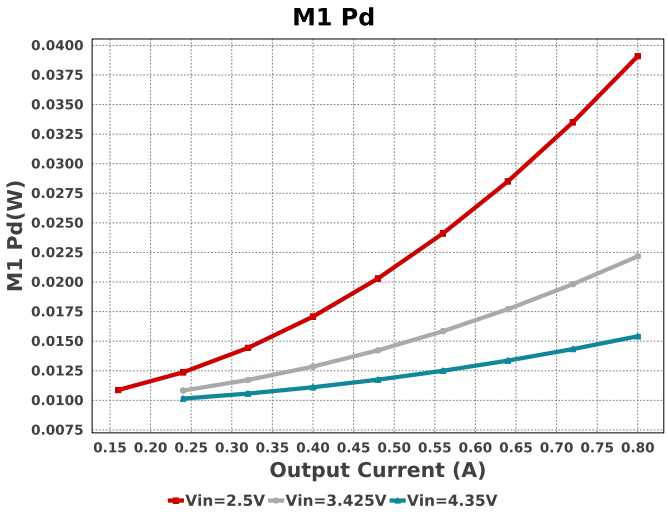


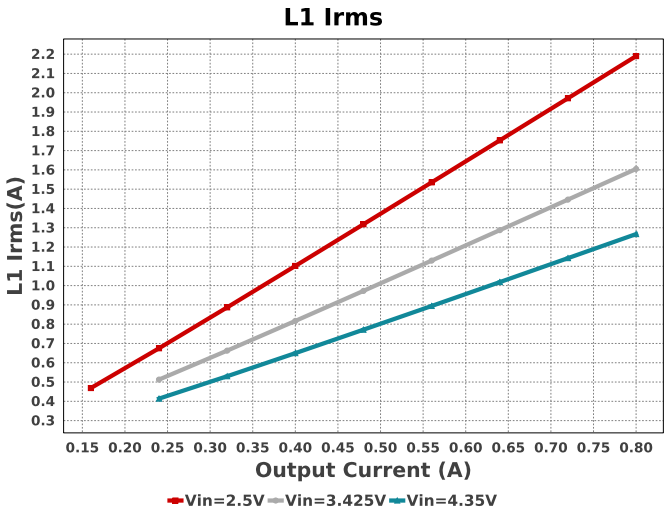


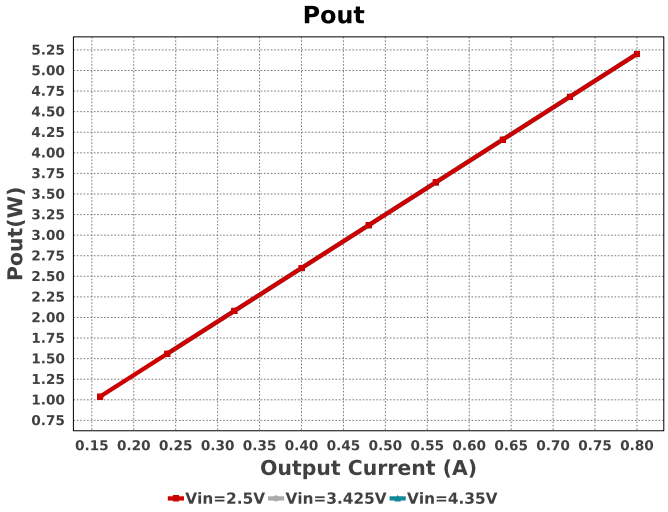


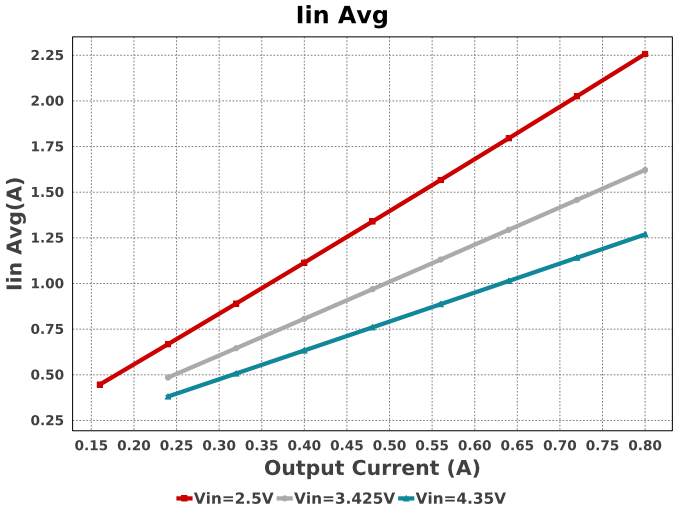


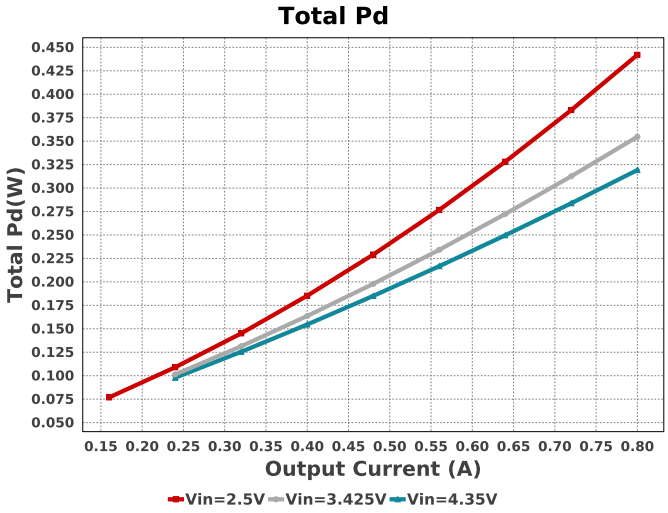


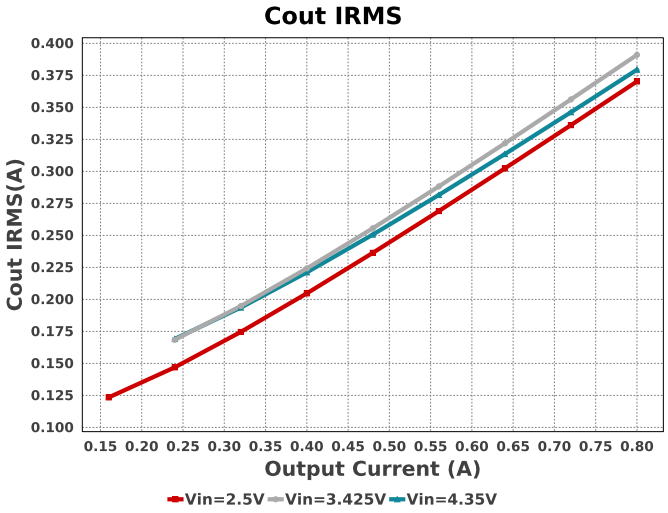


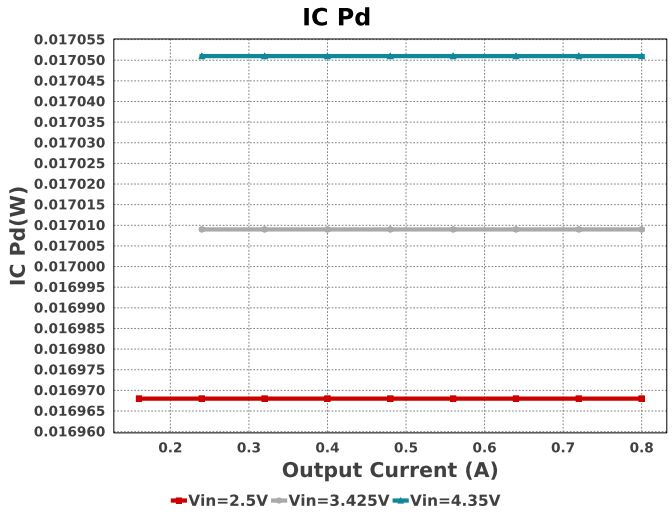


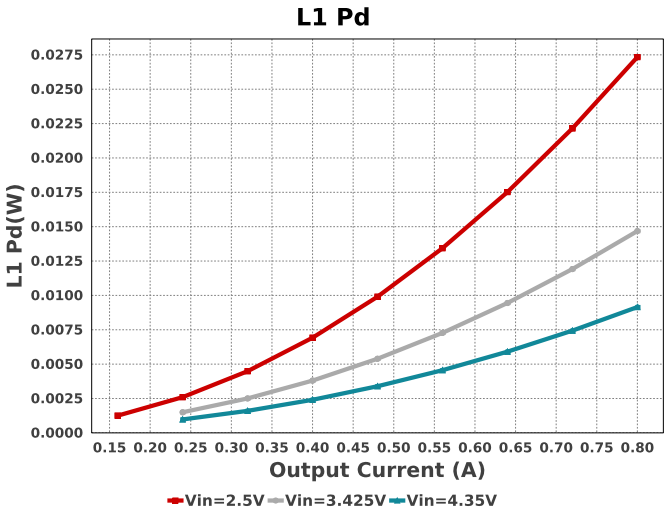


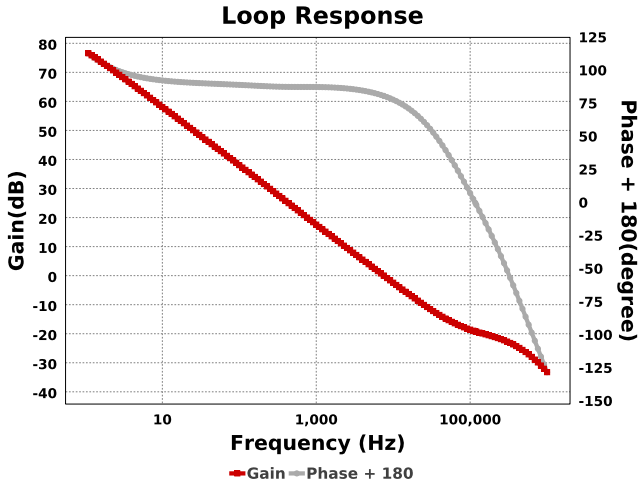












Operating Values

#	Name	Value	Category	Description
1.	Cin IRMS	177.982 mA	Capacitor	Input capacitor RMS ripple current
2.	Cin Pd	96.204 µW	Capacitor	Input capacitor power dissipation
3.	Cout IRMS	370.24 mA	Capacitor	Output capacitor RMS ripple current
4.	Cout Pd	1.508 mW	Capacitor	Output capacitor power dissipation
5.	Coutx IRMS	30.019 mA	Capacitor	Output capacitor_x RMS ripple current
6.	Coutx Pd	1.12 µW	Capacitor	Output capacitor_x power loss
7.	D1 Pd	256.73 mW	Diode	Output Diode Power Dissipation
8.	IC Pd	16.968 mW	IC	IC power dissipation
9.	IC Tj	30.753 degC	IC	IC junction temperature
10.	ICThetaJA	44.4 degC/W	IC	IC junction-to-ambient thermal resistance
11.	Iin Avg	2.257 A	IC	Average input current
12.	L1 Irms	2.19 A	Inductor	Inductor ripple current
13.	L Pd	27.336 mW	Inductor	Power Dissipation in the Inductor
14.	M1 Pd	39.104 mW	Mosfet	M1 MOSFET total power dissipation
15.	M1 TjOP	31.776 degC	Mosfet	M1 MOSFET junction temperature
16.	Cin Pd	96.204 µW	Power	Input capacitor power dissipation
17.	Cout Pd	1.508 mW	Power	Output capacitor power dissipation
18.	Coutx Pd	1.12 µW	Power	Output capacitor_x power loss
19.	D1 Pd	256.73 mW	Power	Output Diode Power Dissipation
20.	IC Pd	16.968 mW	Power	IC power dissipation
21.	L Pd	27.336 mW	Power	Power Dissipation in the Inductor
22.	M1 Pd	39.104 mW	Power	M1 MOSFET total power dissipation
23.	Rsense Pd	100.26 mW	Power	LED Current Rsns Power Dissipation
24.	Total Pd	442.033 mW	Power	Total Power Dissipation
25.	Rsense Pd	100.26 mW	Resistor	LED Current Rsns Power Dissipation
26.	BOM Count	20	System Information	Total Design BOM count
27.	Cross Freq	4.419 kHz	System Information	Bode plot crossover frequency
28.	Duty Cycle	63.348 %	System Information	Duty cycle

#	Name	Value	Category	Description
29.	Efficiency	92.166 %	System Information	Steady state efficiency
30.	FootPrint	494.0 mm^2	System Information	Total Foot Print Area of BOM components
31.	Frequency	324.947 kHz	System Information	Switching frequency
32.	Gain Marg	-12.41 dB	System Information	Bode Plot Gain Margin
33.	Iout	800.0 mA	System Information	Iout operating point
34.	Low Freq Gain	74.84 dB	System Information	Gain at 1Hz
35.	Mode	CCM	System Information	PWM/PFM Mode
36.	Phase Marg	76.971 deg	System Information	Bode Plot Phase Margin
37.	Pout	5.2 W	System Information	Total output power
38.	Total BOM	$4.11	System Information	Total BOM Cost
39.	Vin	2.5 V	System Information	Vin operating point
40.	Vout Act	6.5 V	System Information	Achieved Vout with feedback resistor pair
41.	Vout Actual	6.501 V	System Information	Closest output voltage selected
42.	Vout Tolerance	6.538 %	System Information	Vout Tolerance based on IC Tolerance (no load) and voltage divider resistors if applicable
43.	Vout p-p	9.259 mV	System Information	Peak-to-peak output ripple voltage

Design Inputs

Name	Value	Description
Iout	800.0 m	Maximum Output Current
VinMax	4.35	Maximum input voltage
VinMin	2.5	Minimum input voltage
Vout	6.5	Output Voltage
base_pn	LM51501-Q1	Base Product Number
source	DC	Input Source Type
Ta	30.0	Ambient temperature

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of Cin and Cout, and the inductance and DC resistance of L1 before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

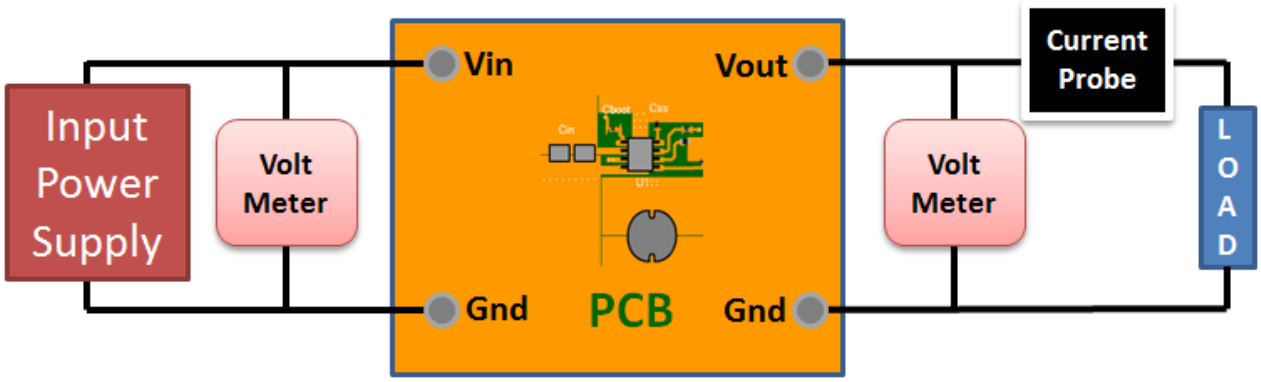
If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab town to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 2.5V and set the input supply's current limit to zero. With the input supply off connect up the input supply to Vin and GND. Connect a digital volt meter and a load if needed to set the minimum Iout of the design from Vout and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between Vin and GND, a load is connected between Vout and GND and a current meter is connected in series between Vout and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.

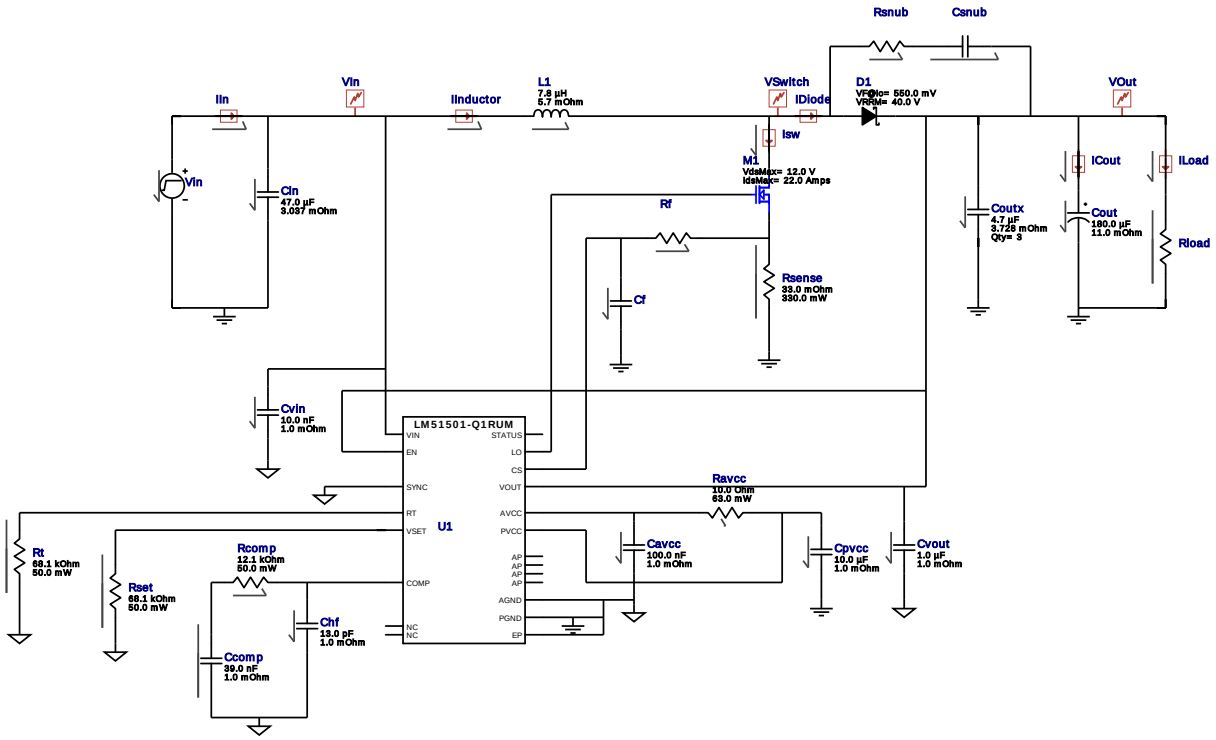


WEBENCH® Electrical Simulation Report

Design Id = 3

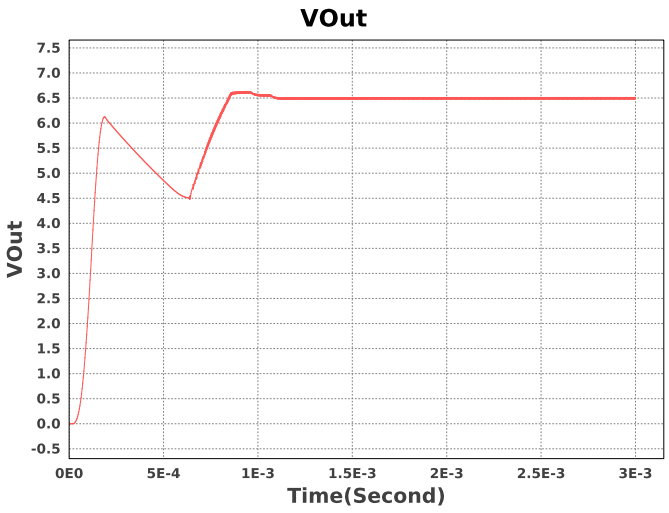
sim_id = 1

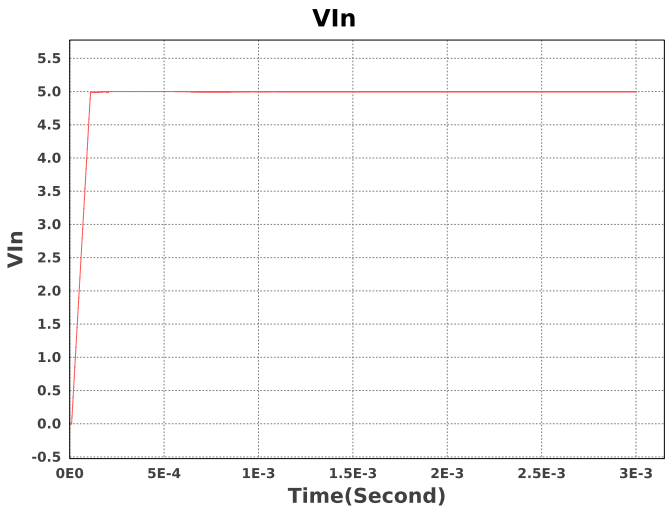
Simulation Type = Startup



Simulation Parameters

#	Name	Parameter Name	Description	Values
1.	Rload	R	Load Resistance	8.125 Ohm

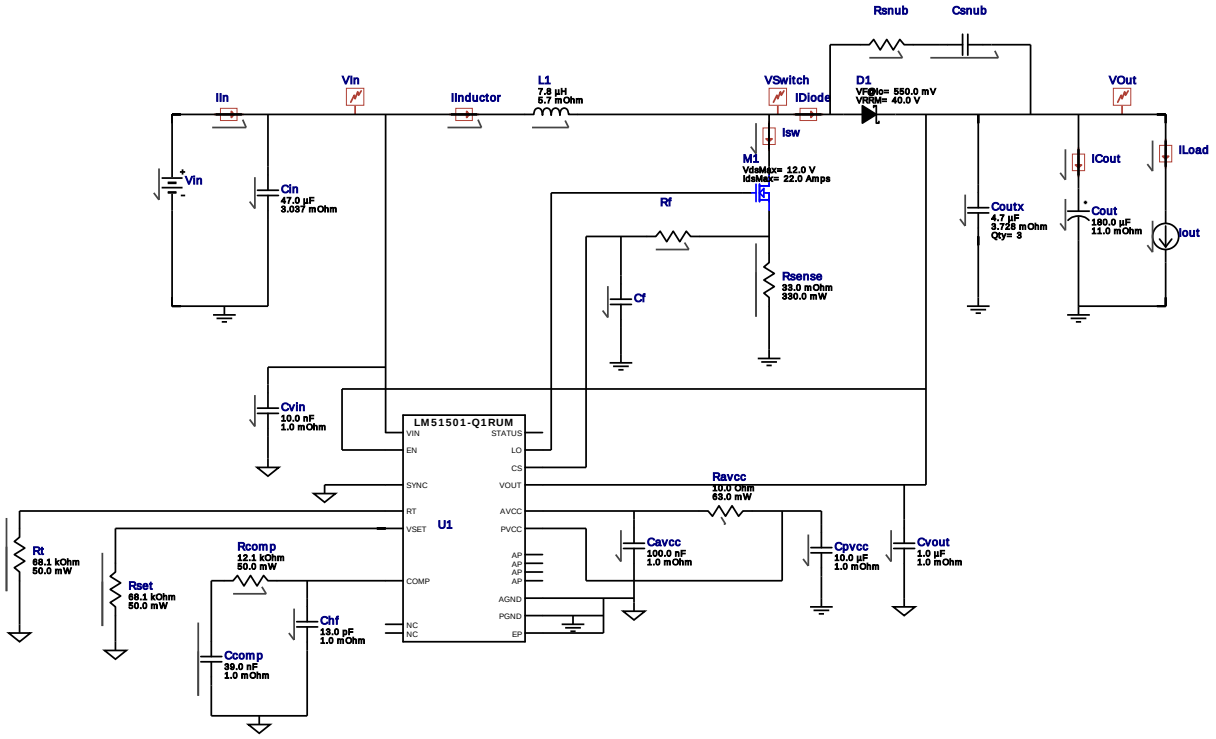




Design Id = 3

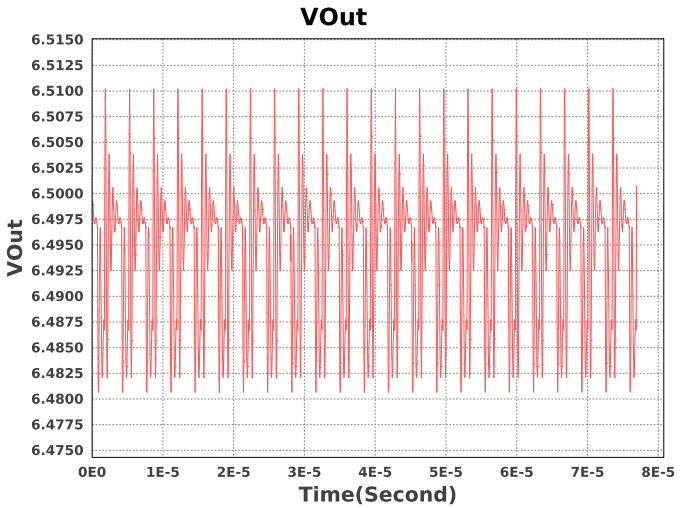
sim_id = 2

Simulation Type = Steady State



Simulation Parameters

#	Name	Parameter Name	Description	Values
1.	Cvout	IC	Initial Voltage	6.5 V
2.	Cout	IC	Initial Voltage	6.5 V
3.	Iout	I	Load Current	0.8 A



Design Assistance

1. Feature Highlights: This is a wide Vin Automotive Low IQ Boost Controller Device will operate in PassThrough Mode When Vin is greater than Vout

2. The LM51501-Q1 is qualified for Automotive applications. All passives and other components selected in this design may not be qualified for Automotive applications. The user is required to verify that all components in the design meet the qualification and safety requirements for their specific application

3. Master key : E45EC124FA155B08[v1]

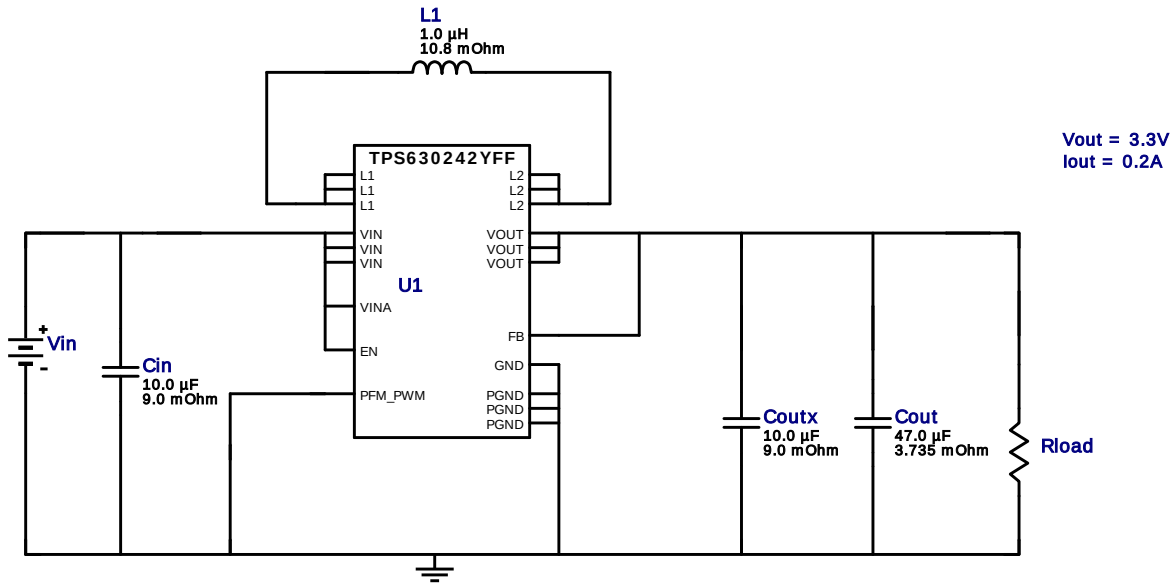
4. **LM51501-Q1** Product Folder : http://www.ti.com/product/LM51501%2DQ1 : contains the data sheet and other resources.

VinMin = 2.5V
VinMax = 4.35V
Vout = 3.3V
Iout = 0.2A

Device = TPS630242YFFR
Topology = Buck_Boost
Created = 2022-03-23 11:07:38.625
BOM Cost = $1.81
BOM Count = 5
Total Pd = 0.04W

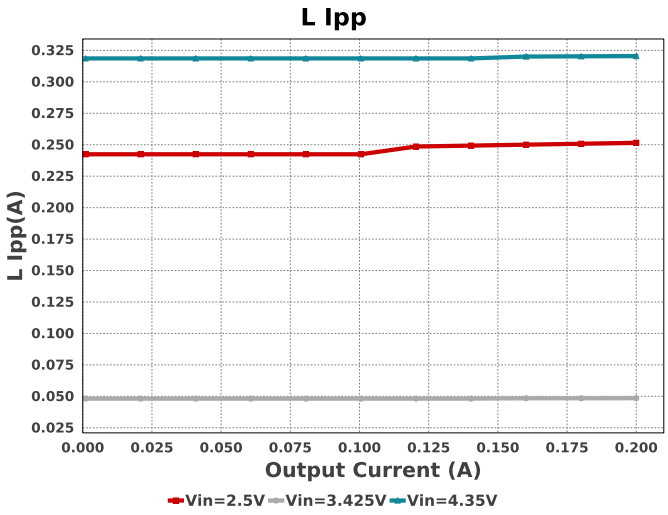
WEBENCH® Design Report

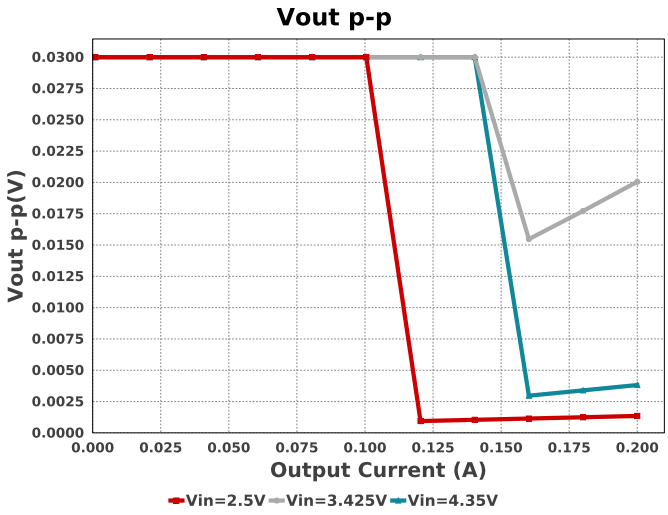
Design : 4 TPS630242YFFR
TPS630242YFFR 2.5V-4.35V to 3.30V @ 0.2A

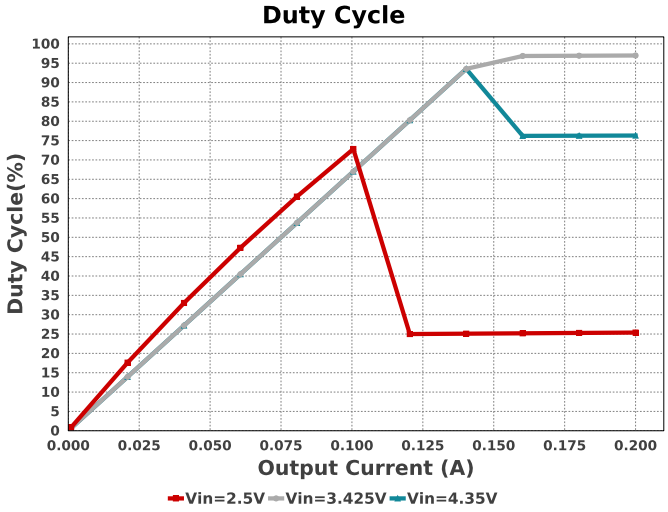


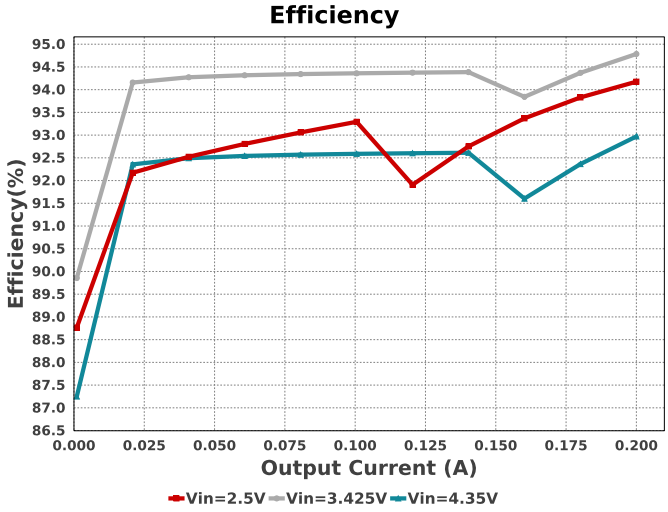
Electrical BOM

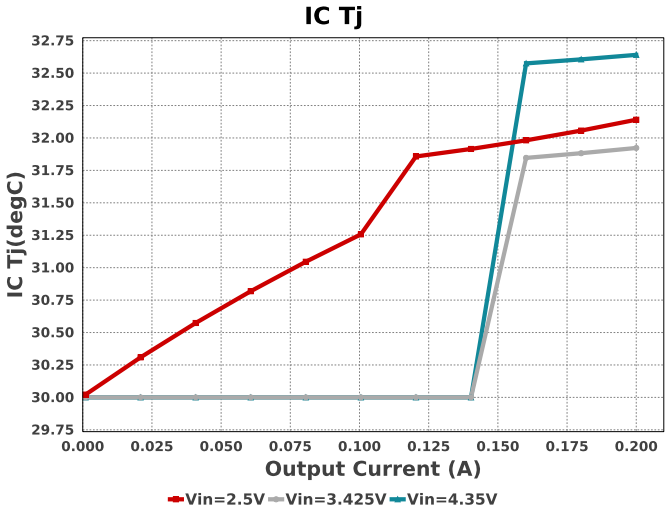
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cin	MuRata	GRM188R60J106ME47D Series= X5R	Cap= 10.0 uF ESR= 9.0 mOhm VDC= 6.3 V IRMS= 2.74 A	1	$0.08	0603 5 mm²
Cout	MuRata	GRM31CC80J476KE18L Series= X6S	Cap= 47.0 uF ESR= 3.735 mOhm VDC= 6.3 V IRMS= 4.0522 A	1	$0.20	1206_190 11 mm²
Coutx	MuRata	GRM188R60J106ME47D Series= X5R	Cap= 10.0 uF ESR= 9.0 mOhm VDC= 6.3 V IRMS= 2.74 A	1	$0.08	0603 5 mm²
L1	Coilcraft	XFL4020-102MEB	L= 1.0 µH 10.8 mOhm	1	$0.61	XFL4020 25 mm²
U1	Texas Instruments	TPS630242YFFR	Switcher	1	$0.84	YFF0020AEBA 9 mm²

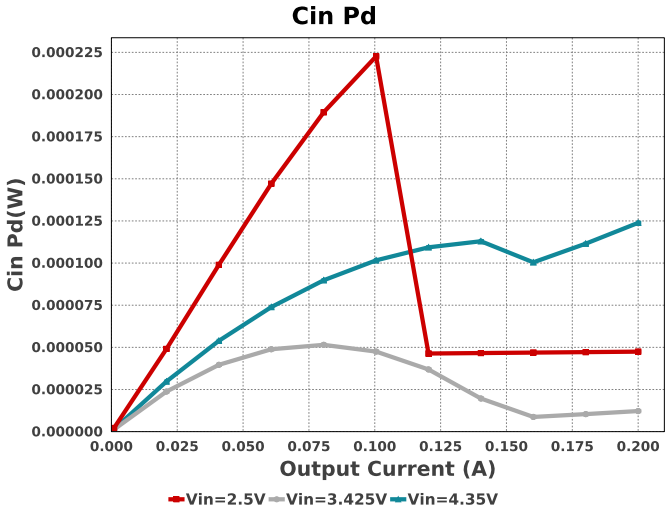


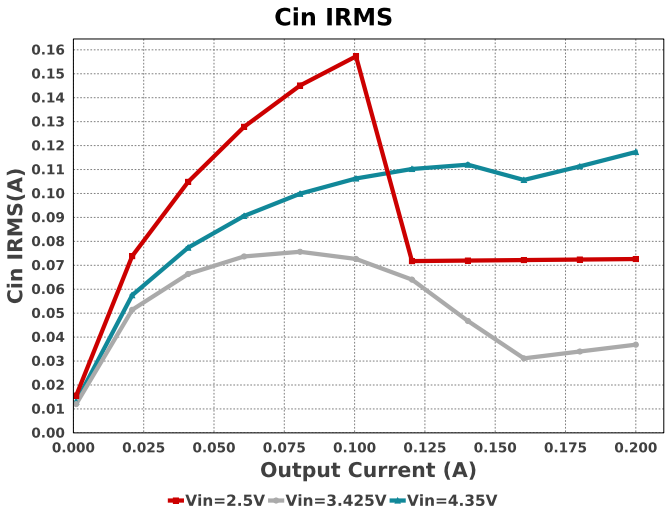


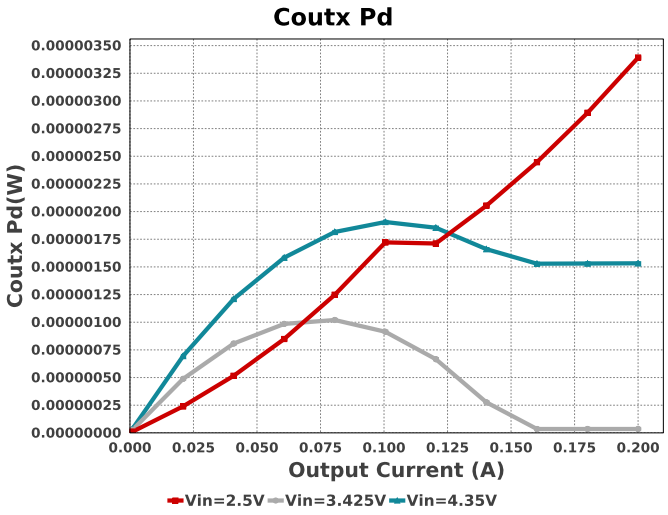


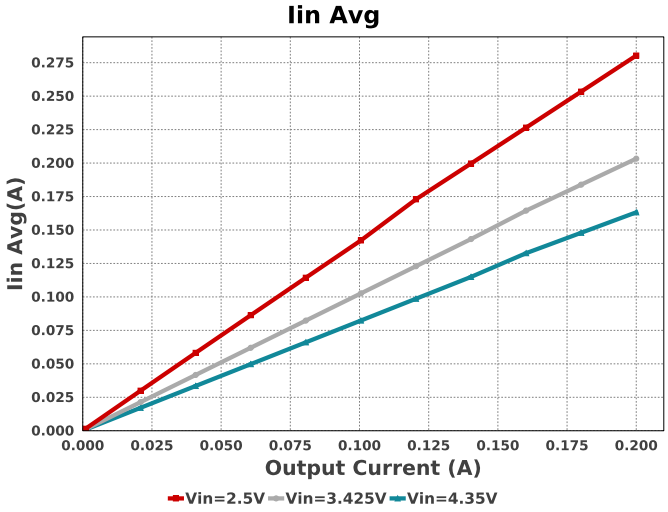


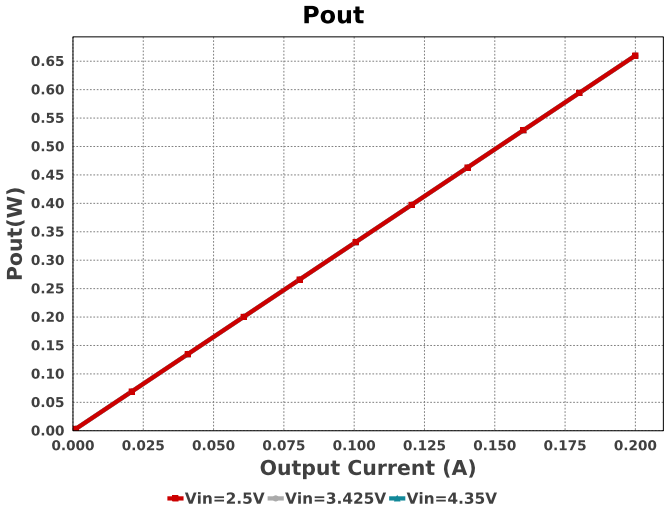


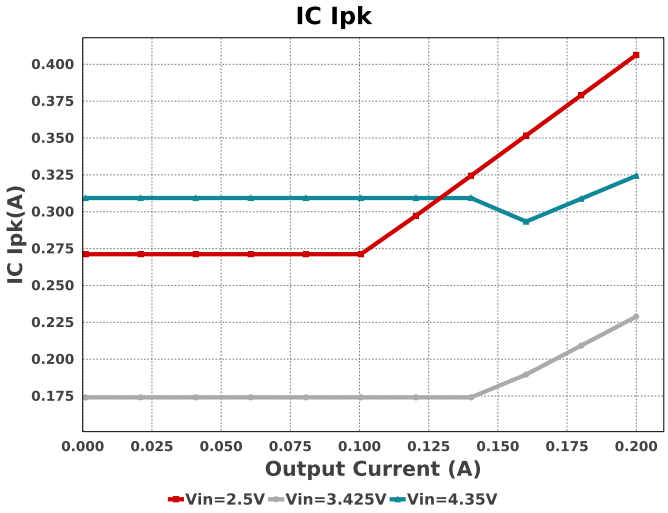


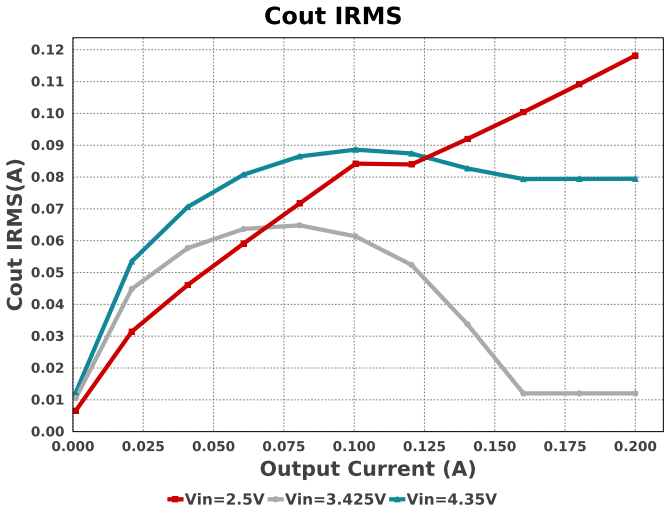


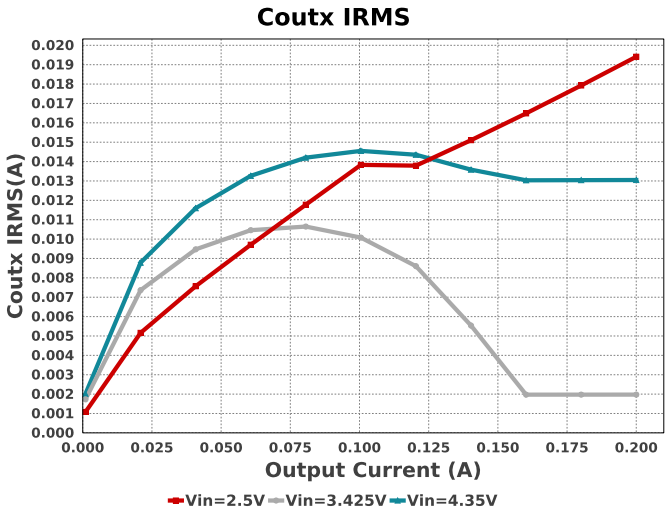


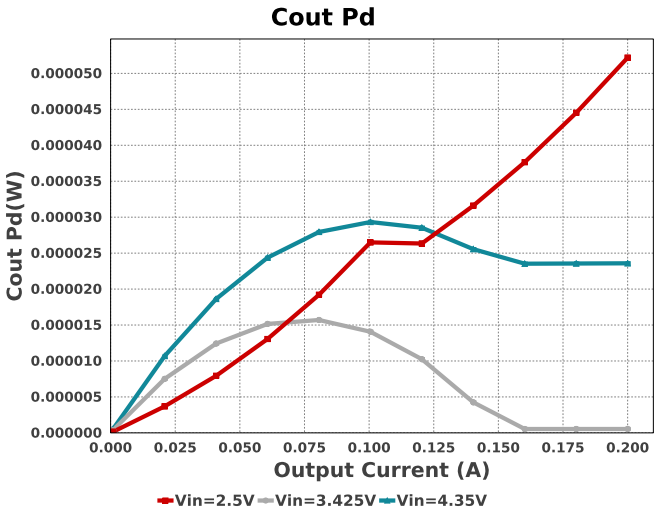


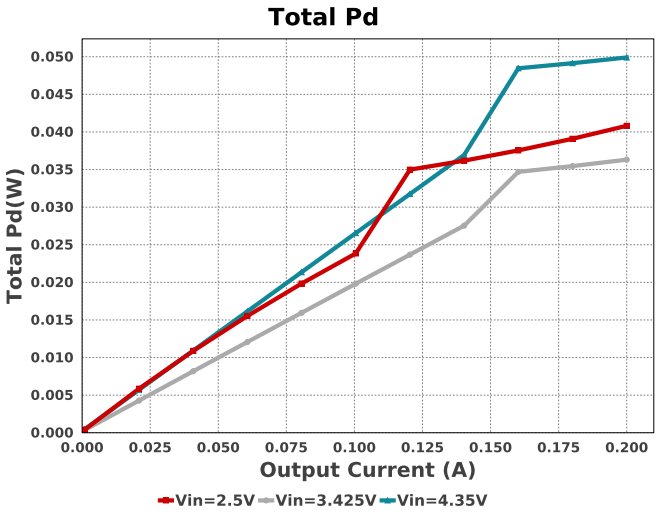


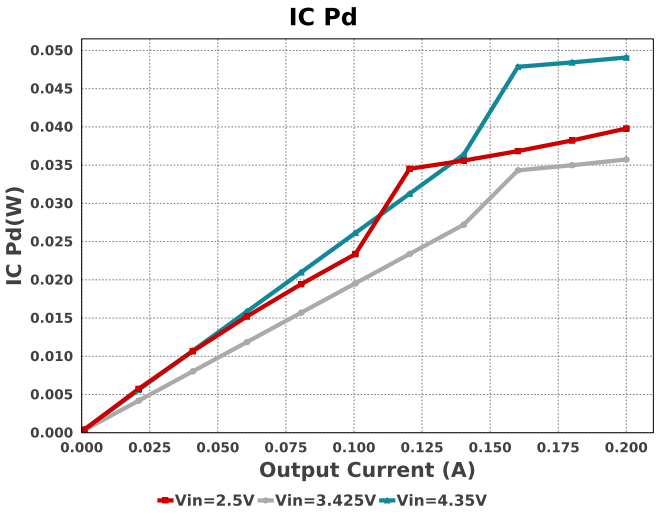


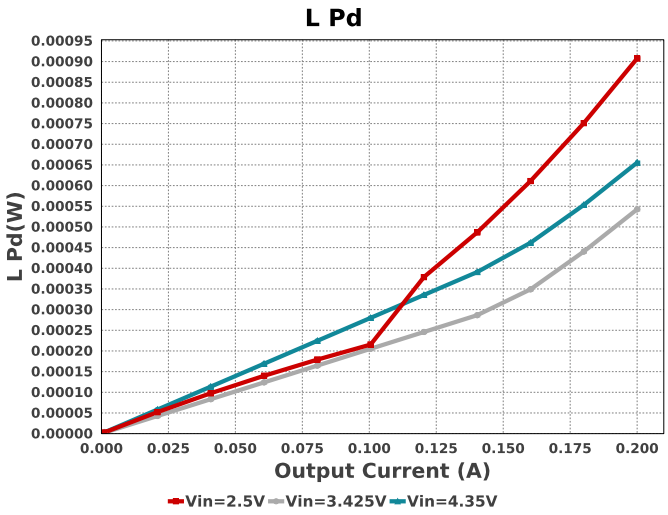


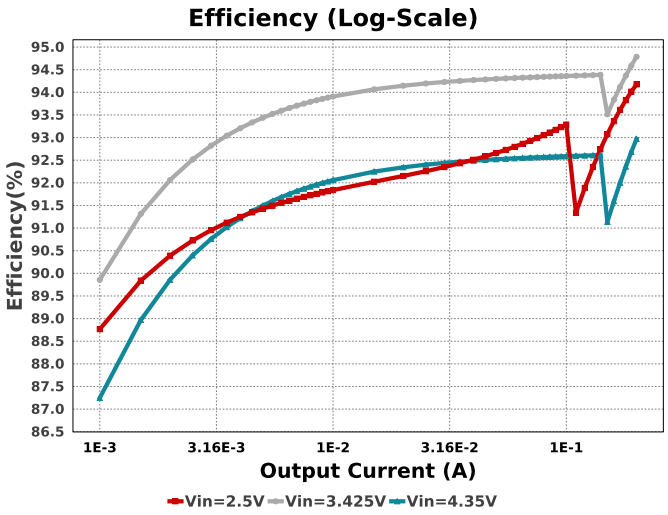












Operating Values

#	Name	Value	Category	Description
1.	Cin IRMS	72.613 mA	Capacitor	Input capacitor RMS ripple current
2.	Cin Pd	47.454 µW	Capacitor	Input capacitor power dissipation
3.	Cout IRMS	118.195 mA	Capacitor	Output capacitor RMS ripple current
4.	Cout Pd	0.0 W	Capacitor	Output capacitor power dissipation
5.	Coutx IRMS	19.409 mA	Capacitor	Output capacitor_x RMS ripple current
6.	Coutx Pd	0.0 W	Capacitor	Output capacitor_x power loss
7.	IC Ipk	406.382 mA	IC	Peak switch current in IC
8.	IC Pd	39.786 mW	IC	IC power dissipation
9.	IC Tj	32.14 degC	IC	IC junction temperature
10.	ICThetaJA	53.8 degC/W	IC	IC junction-to-ambient thermal resistance
11.	Iin Avg	280.3 mA	IC	Average input current

#	Name	Value	Category	Description
12.	L Ipp	251.54 mA	Inductor	Peak-to-peak inductor ripple current
13.	L Pd	907.37 µW	Inductor	Inductor power dissipation
14.	Cin Pd	47.454 µW	Power	Input capacitor power dissipation
15.	Cout Pd	0.0 W	Power	Output capacitor power dissipation
16.	Coutx Pd	0.0 W	Power	Output capacitor_x power loss
17.	IC Pd	39.786 mW	Power	IC power dissipation
18.	L Pd	907.37 µW	Power	Inductor power dissipation
19.	Total Pd	40.756 mW	Power	Total Power Dissipation
20.	BOM Count	5	System Information	Total Design BOM count
21.	Duty Cycle	25.381 %	System Information	Duty cycle
22.	Efficiency	94.184 %	System Information	Steady state efficiency
23.	FootPrint	54.0 mm^2	System Information	Total Foot Print Area of BOM components
24.	Frequency	2.5 MHz	System Information	Switching frequency
25.	Iout	200.0 mA	System Information	Iout operating point
26.	Mode	BOOST PWM CCM	System Information	PWM/PFM Mode
27.	Pout	660.0 mW	System Information	Total output power
28.	Total BOM	$1.81	System Information	Total BOM Cost
29.	Vin	2.5 V	System Information	Vin operating point
30.	Vout p-p	735.538 µV	System Information	Peak-to-peak output ripple voltage

Design Inputs

Name	Value	Description
Iout	200.0 m	Maximum Output Current
VinMax	4.35	Maximum input voltage
VinMin	2.5	Minimum input voltage
Vout	3.3	Output Voltage
base_pn	TPS630242	Base Product Number
source	DC	Input Source Type
Ta	30.0	Ambient temperature

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of Cin and Cout, and the inductance and DC resistance of L1 before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

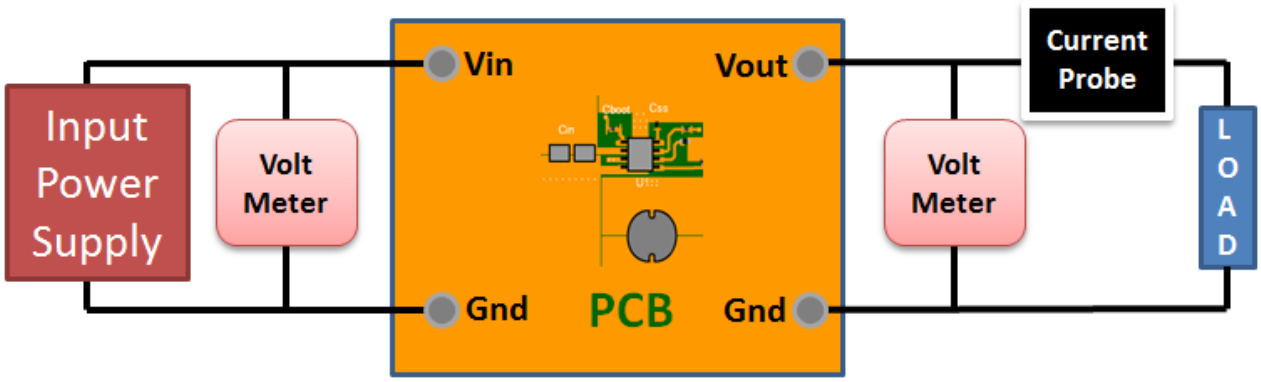
If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab town to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 2.5V and set the input supply's current limit to zero. With the input supply off connect up the input supply to Vin and GND. Connect a digital volt meter and a load if needed to set the minimum Iout of the design from Vout and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between Vin and GND, a load is connected between Vout and GND and a current meter is connected in series between Vout and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.

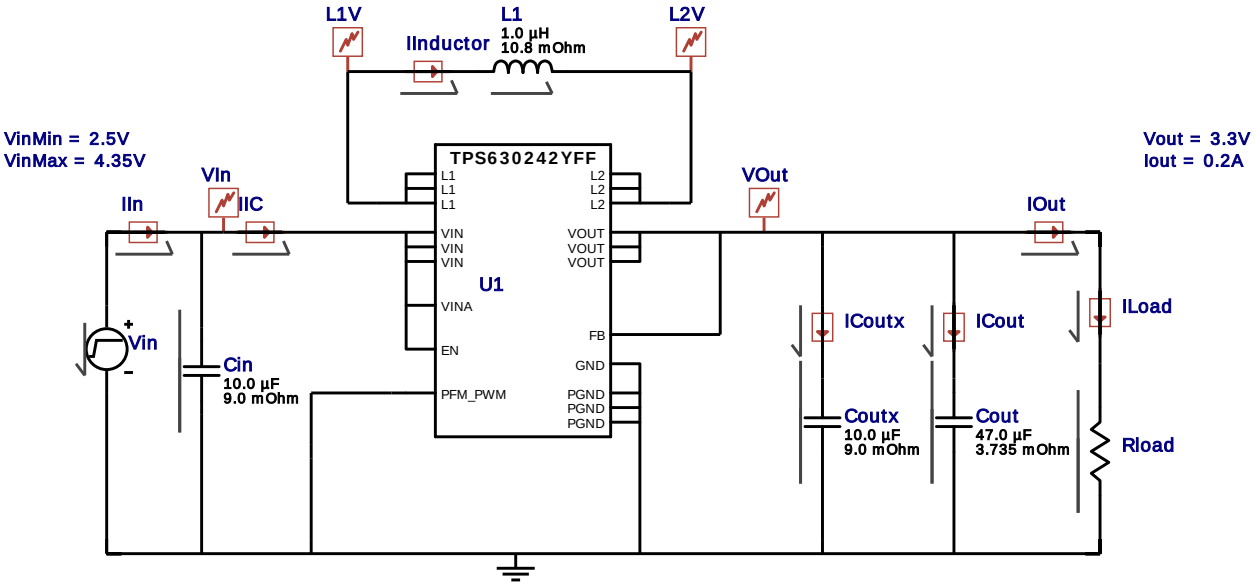


WEBENCH® Electrical Simulation Report

Design Id = 4

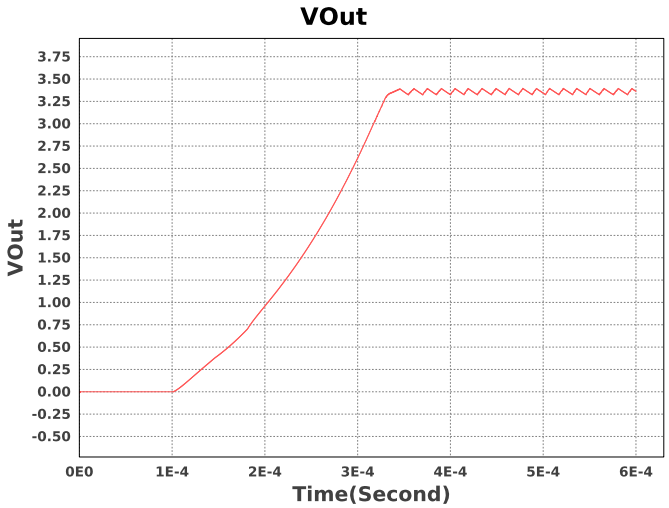
sim_id = 1

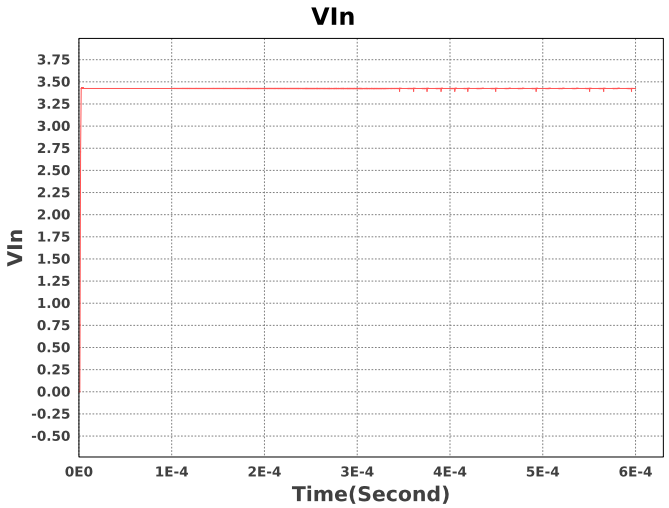
Simulation Type = Startup



Simulation Parameters

#	Name	Parameter Name	Description	Values
1.	Rload	R	Load Resistance	16.499999999999996 Ohm

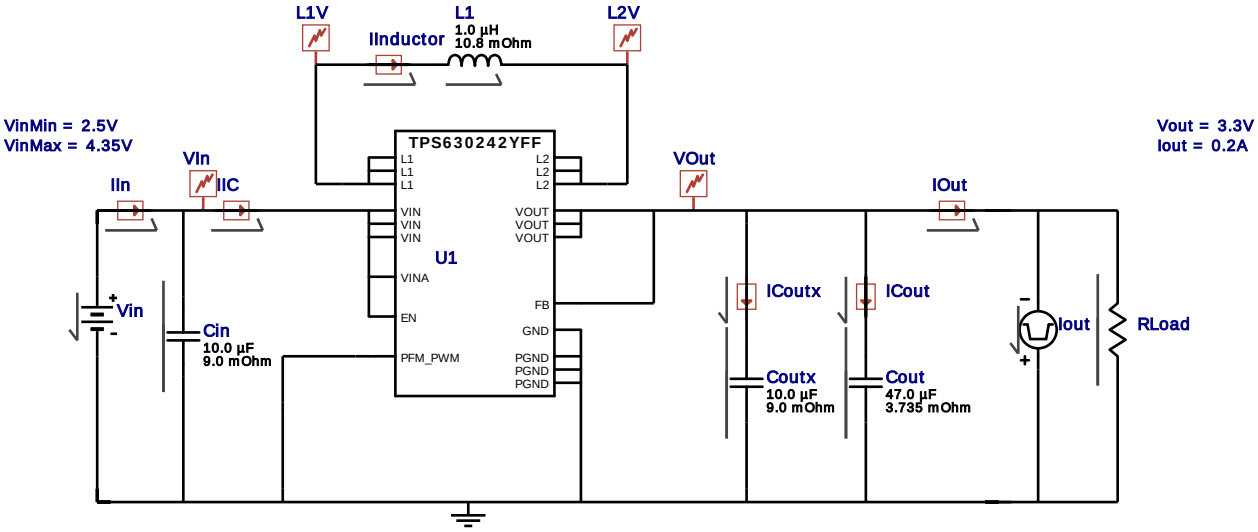




Design Id = 4

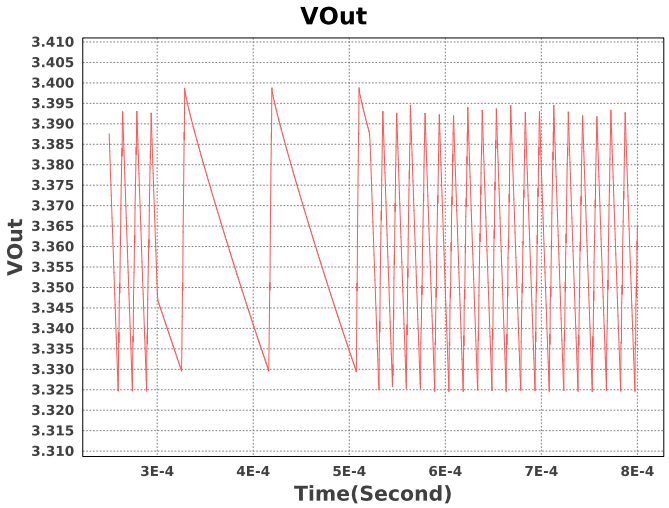
sim_id = 2

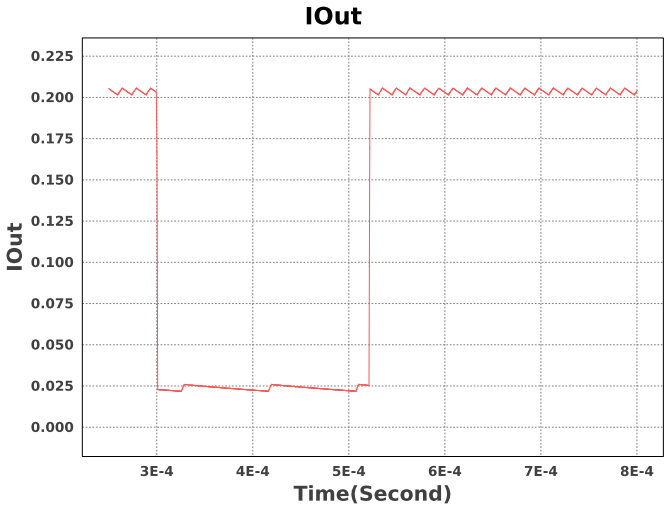
Simulation Type = Load Transient



Simulation Parameters

#	Name	Parameter Name	Description	Values
1.	Cout	IC	Initial Voltage	3.2889999999999997
2.	L1	IC	Initial Current	0.2
3.	Coutx	IC	Initial Condition	3.2889999999999997 V
4.	Iout	signal_type	Signal Type	PULSE
		I1	Initial Current	0
		I2	Final Current	0.18000000000000002
		Td	Initial Time Delay	300u
		Tr	Rise Time	1u
		Tf	Fall Time	1u
		PW	Pulse Width	220u
5.	RLoad	R	Load Resistance	16.499999999999996 ohm

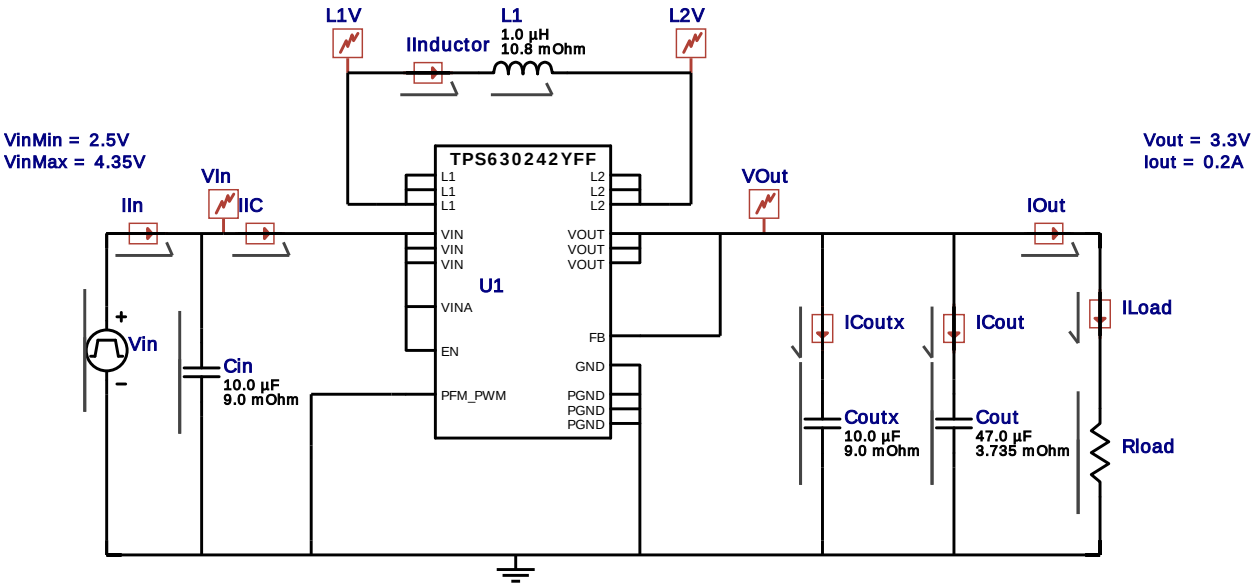




Design Id = 4

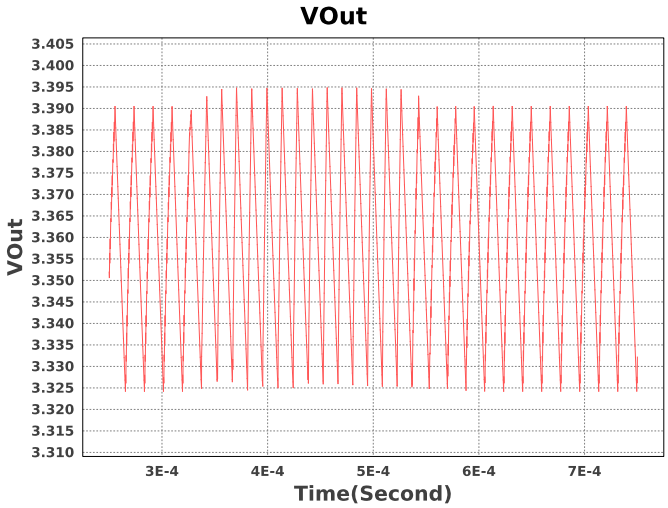
sim_id = 3

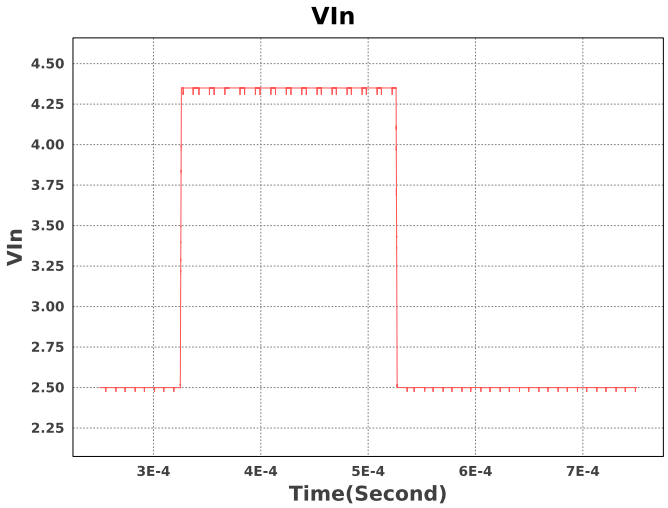
Simulation Type = Input Transient



Simulation Parameters

#	Name	Parameter Name	Description	Values
1.	Cout	IC	Initial Voltage	3.2889999999999997
2.	L1	IC	Initial Current	0.2
3.	Coutx	IC	Initial Voltage	3.2889999999999997
4.	Rload	R	Load Resistance	16.499999999999996 Ohm

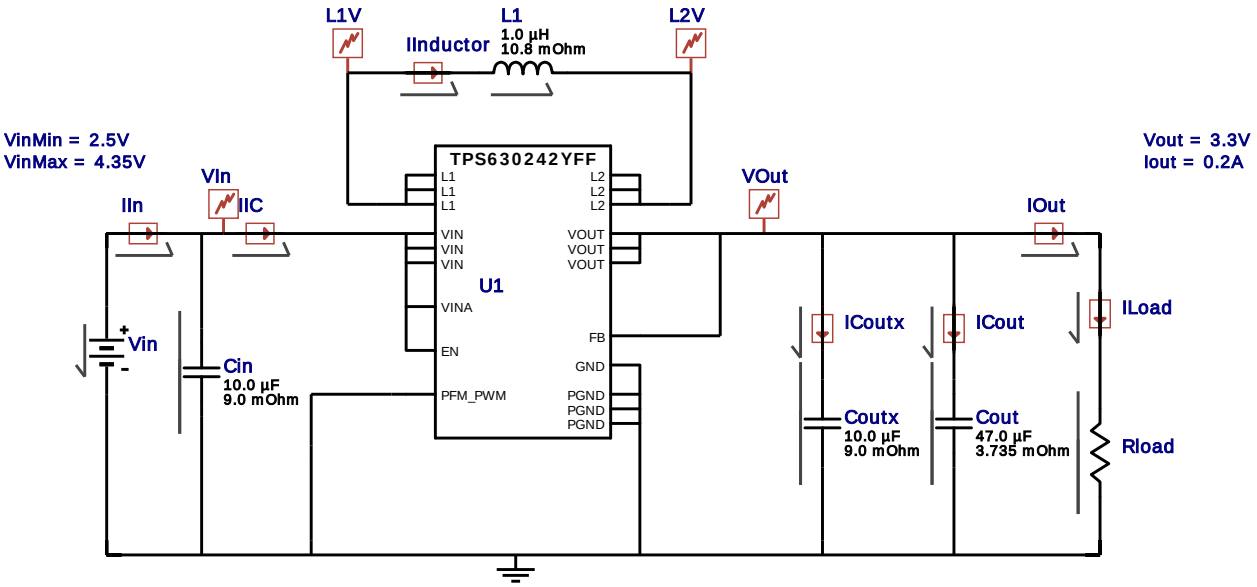




Design Id = 4

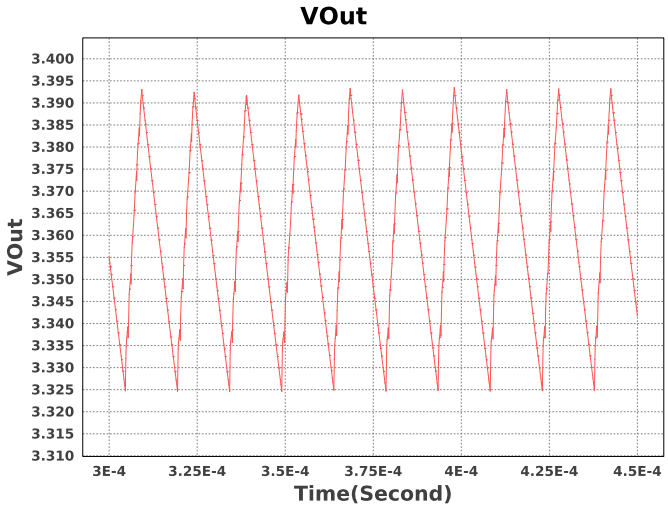
sim_id = 4

Simulation Type = Steady State



Simulation Parameters

#	Name	Parameter Name	Description	Values
1.	Cout	IC	Initial Voltage	3.2889999999999997
2.	L1	IC	Initial Current	0.2
3.	Coutx	IC	Initial Condition	3.2889999999999997 V
4.	Rload	R	Load Resistance	16.499999999999996 Ohm



Design Assistance

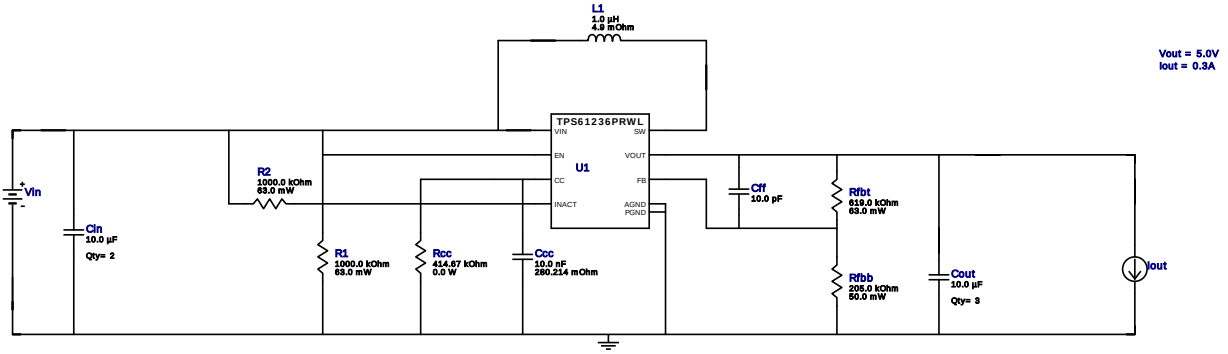
1. Master key : E45EC124FA155B08[v1]
2. **TPS630242** Product Folder : http://www.ti.com/product/TPS630242 : contains the data sheet and other resources.

VinMin = 2.5V
VinMax = 4.35V
Vout = 5.0V
Iout = 0.3A

Device = TPS61236PRWLR
Topology = Boost
Created = 2022-02-12 18:56:06.661
BOM Cost = NA
BOM Count = 14
Total Pd = 0.05W

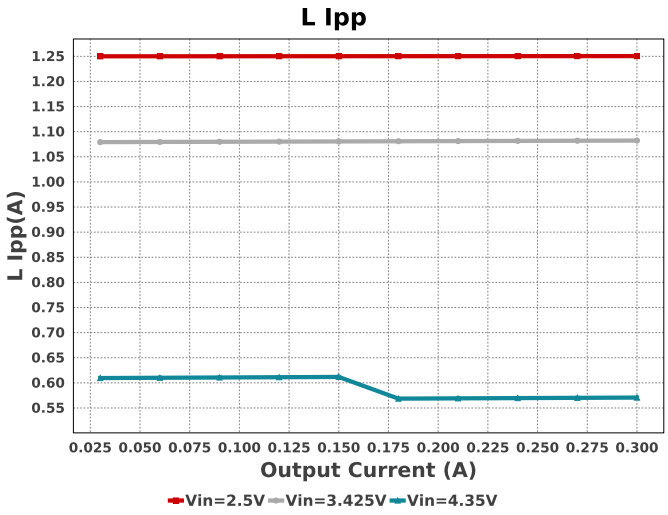
WEBENCH® Design Report

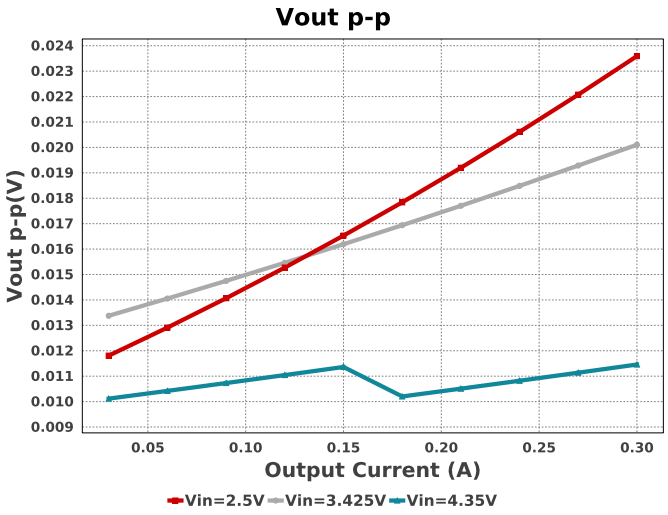
Design : 2 TPS61236PRWLR
TPS61236PRWLR 2.5V-4.35V to 5.00V @ 0.3A

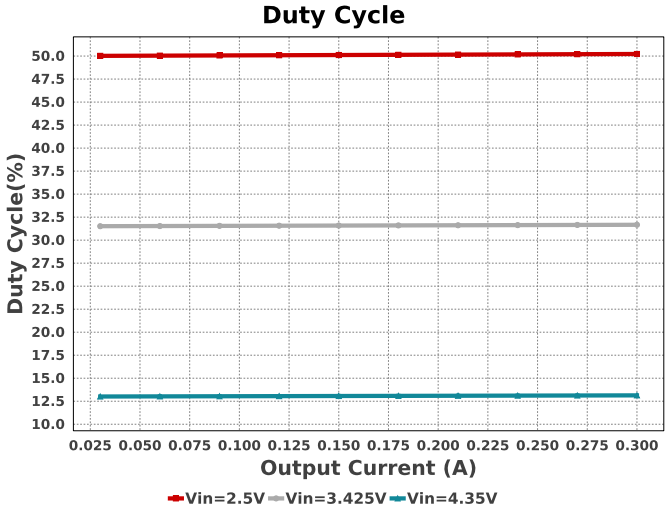


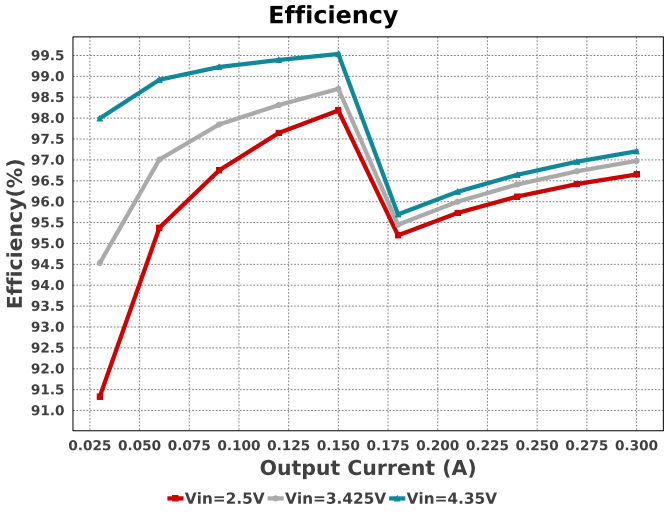
Electrical BOM

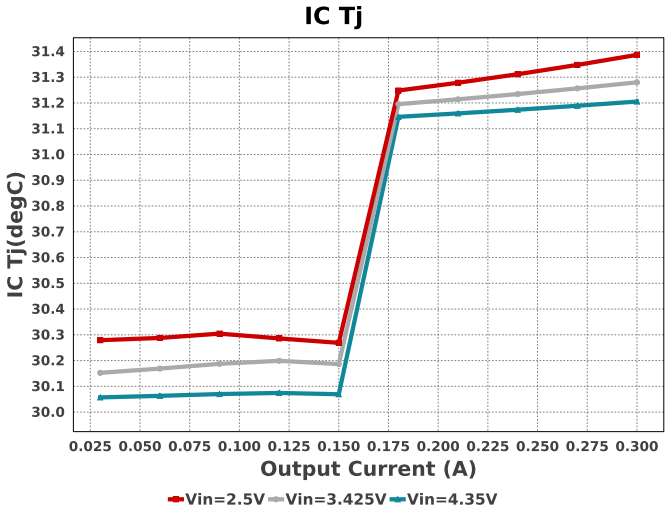
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Ccc	TDK	CGA1A2X7R1A103K030BA Series= X7R	Cap= 10.0 nF ESR= 280.21 mOhm VDC= 10.0 V IRMS= 245.72 mA	1	$0.01	0201_033 2 mm²
Cff	Kemet	C0805C100M4GACTU Series= C0G/NP0	Cap= 10.0 pF VDC= 16.0 V IRMS= 0.0 A	1	$0.01	0805 7 mm²
Cin	TDK	C1608X5R1A106M080AC Series= X5R	Cap= 10.0 uF VDC= 10.0 V IRMS= 0.0 A	2	$0.09	0603 5 mm²
Cout	TDK	C1608X5R1A106M080AC Series= X5R	Cap= 10.0 uF VDC= 10.0 V IRMS= 0.0 A	3	$0.09	0603 5 mm²
L1	Bourns	SRU1028-1R0Y	L= 1.0 µH 4.9 mOhm	1	$0.40	SRU1028 144 mm²
R1	Vishay-Dale	CRCW04021M00FKED Series= CRCW..e3	Res= 1000.0 kOhm Power= 63.0 mW Tolerance= 1.0%	1	$0.01	0402 3 mm²
R2	Vishay-Dale	CRCW04021M00FKED Series= CRCW..e3	Res= 1000.0 kOhm Power= 63.0 mW Tolerance= 1.0%	1	$0.01	0402 3 mm²
Rcc	CUSTOM	CUSTOM Series= ?	Res= 414.67 kOhm Power= 0.0 W Tolerance= 0.0%	1	NA	CUSTOM 0 mm²
Rfbb	Yageo	RC0201FR-07205KL Series= ?	Res= 205.0 kOhm Power= 50.0 mW Tolerance= 1.0%	1	$0.01	0201 2 mm²
Rfbt	Vishay-Dale	CRCW0402619KFKED Series= CRCW..e3	Res= 619.0 kOhm Power= 63.0 mW Tolerance= 1.0%	1	$0.01	0402 3 mm²
U1	Texas Instruments	TPS61236PRWLR	Switcher	1	$0.76	RWL0009A 12 mm²

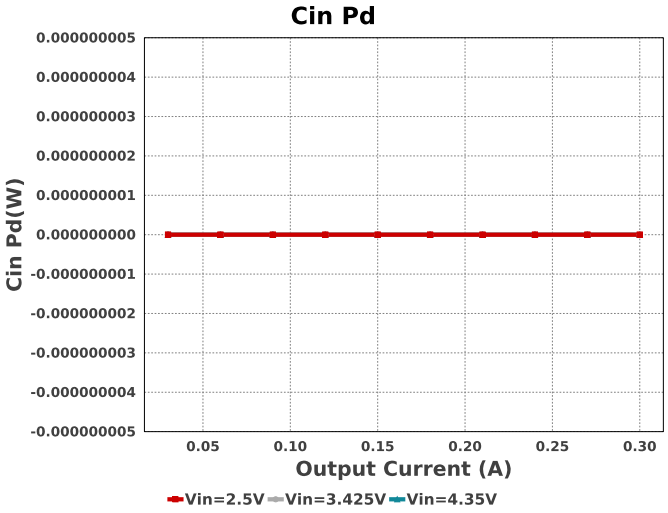


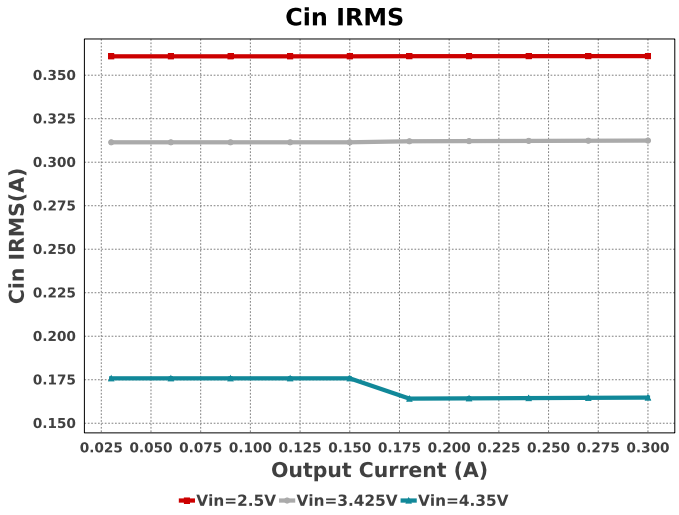


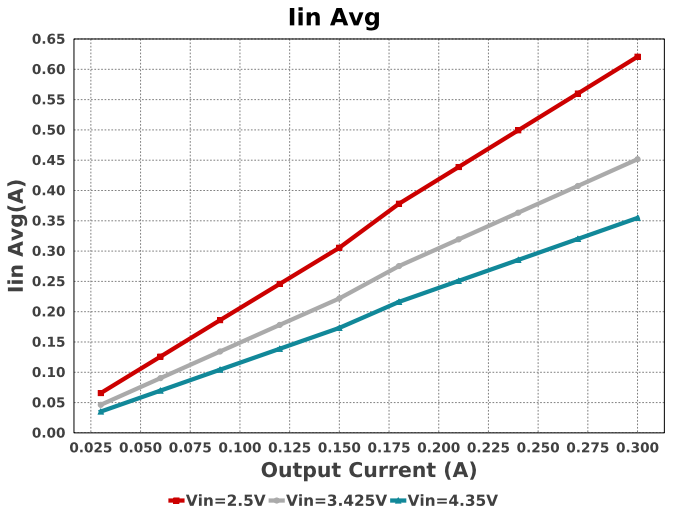


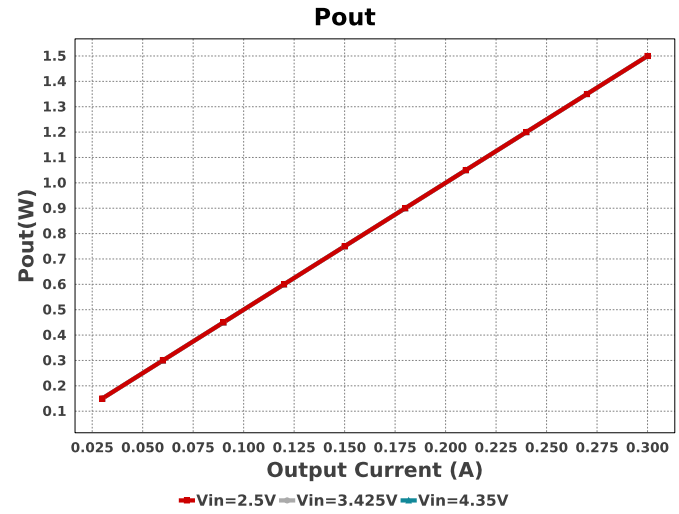


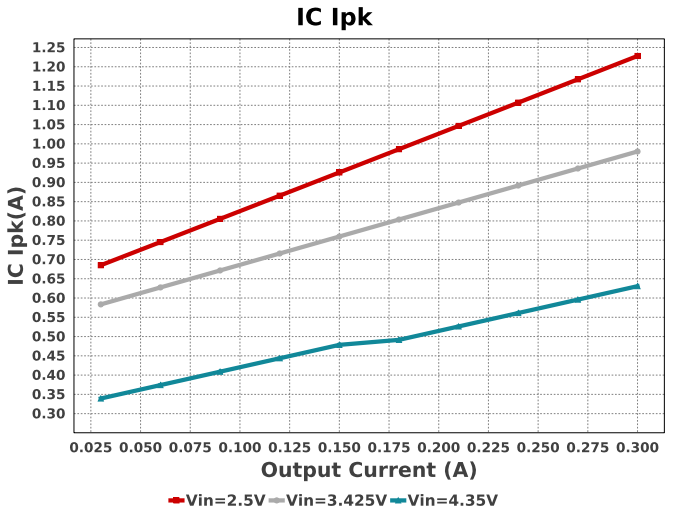


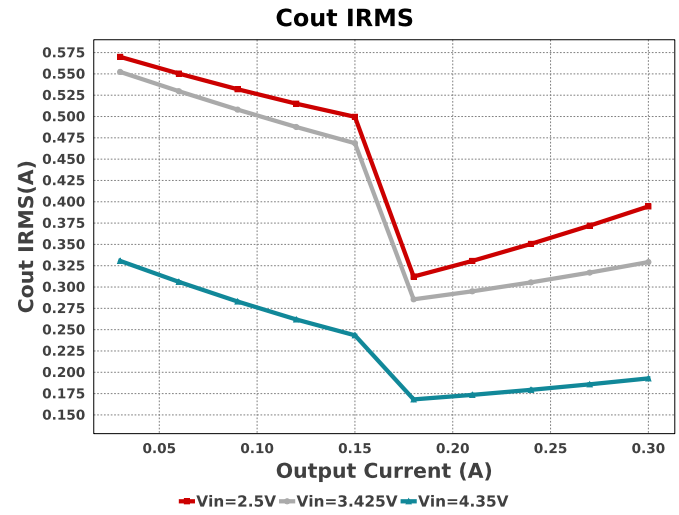


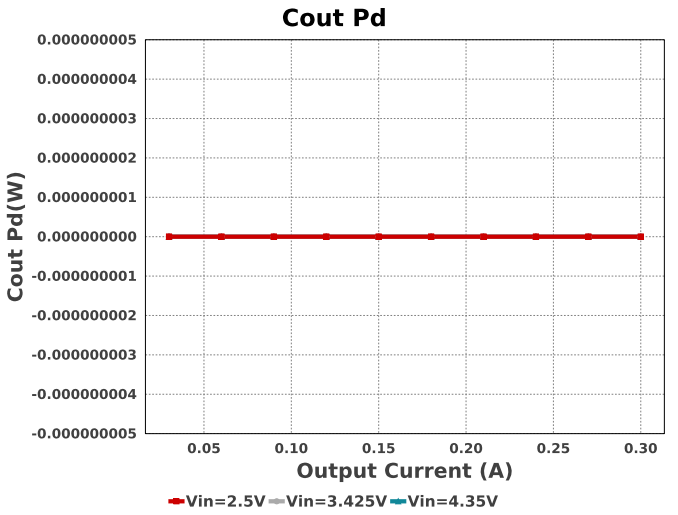


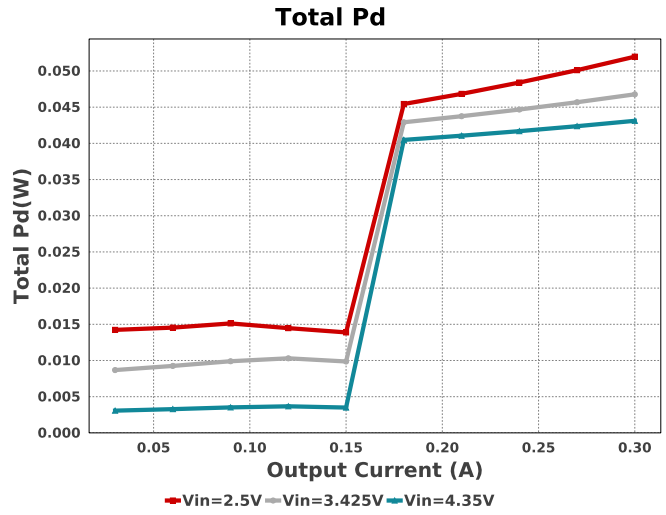


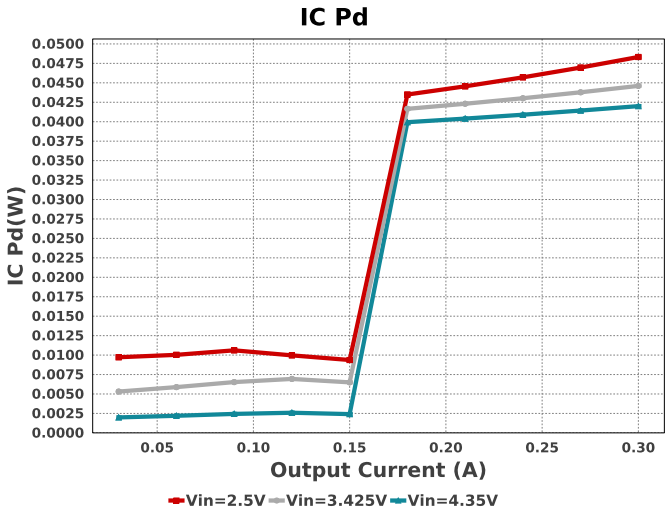


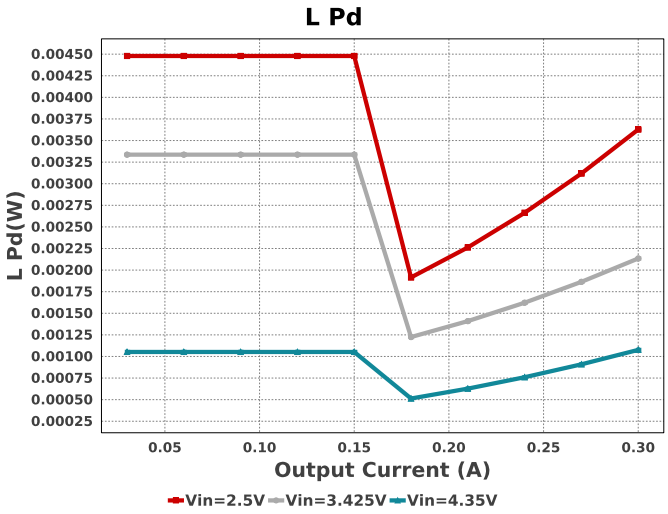


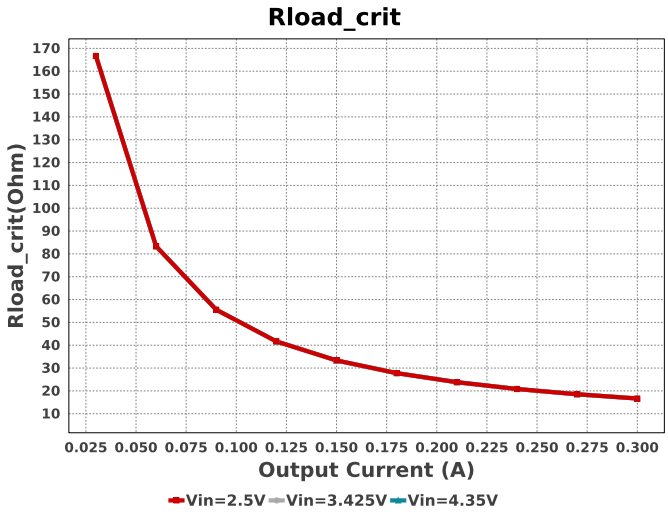












Operating Values

#	Name	Value	Category	Description
1.	BOM Count	14		Total Design BOM count
2.	Total BOM	NA		Total BOM Cost
3.	Cin IRMS	360.976 mA	Capacitor	Input capacitor RMS ripple current
4.	Cin Pd	0.0 W	Capacitor	Input capacitor power dissipation
5.	Cout IRMS	394.542 mA	Capacitor	Output capacitor RMS ripple current
6.	Cout Pd	0.0 W	Capacitor	Output capacitor power dissipation
7.	IC Ipk	1.228 A	IC	Peak switch current in IC
8.	IC Pd	48.32 mW	IC	IC power dissipation
9.	IC Tj	31.387 degC	IC	IC junction temperature
10.	ICThetaJA	28.7 degC/W	IC	IC junction-to-ambient thermal resistance
11.	Iin Avg	620.79 mA	IC	Average input current
12.	L Ipp	1.25 A	Inductor	Peak-to-peak inductor ripple current
13.	L Pd	3.628 mW	Inductor	Inductor power dissipation
14.	Cin Pd	0.0 W	Power	Input capacitor power dissipation
15.	Cout Pd	0.0 W	Power	Output capacitor power dissipation
16.	IC Pd	48.32 mW	Power	IC power dissipation
17.	L Pd	3.628 mW	Power	Inductor power dissipation
18.	Total Pd	51.976 mW	Power	Total Power Dissipation
19.	Duty Cycle	50.226 %	System Information	Duty cycle
20.	Efficiency	96.651 %	System Information	Steady state efficiency
21.	FootPrint	205.0 mm^2	System Information	Total Foot Print Area of BOM components
22.	Frequency	1000.0 kHz	System Information	Switching frequency
23.	Iout	300.0 mA	System Information	Iout operating point
24.	Mode	BOOST PWM CCM	System Information	PWM/PFM Mode
25.	Pout	1.5 W	System Information	Total output power

#	Name	Value	Category	Description
26.	Rload_crit	16.667 Ohm	System Information	Minimum Rload required during Start up
27.	Vin	2.5 V	System Information	Vin operating point
28.	Vout Actual	5.0 V	System Information	Vout Actual calculated based on selected voltage divider resistors
29.	Vout Tolerance	3.15 %	System Information	Vout Tolerance based on IC Tolerance (no load) and voltage divider resistors if applicable
30.	Vout p-p	23.592 mV	System Information	Peak-to-peak output ripple voltage

Design Inputs

Name	Value	Description
Iout	300.0 m	Maximum Output Current
VinMax	4.35	Maximum input voltage
VinMin	2.5	Minimum input voltage
Vout	5.0	Output Voltage
base_pn	TPS61236P	Base Product Number
source	DC	Input Source Type
Ta	30.0	Ambient temperature

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of Cin and Cout, and the inductance and DC resistance of L1 before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

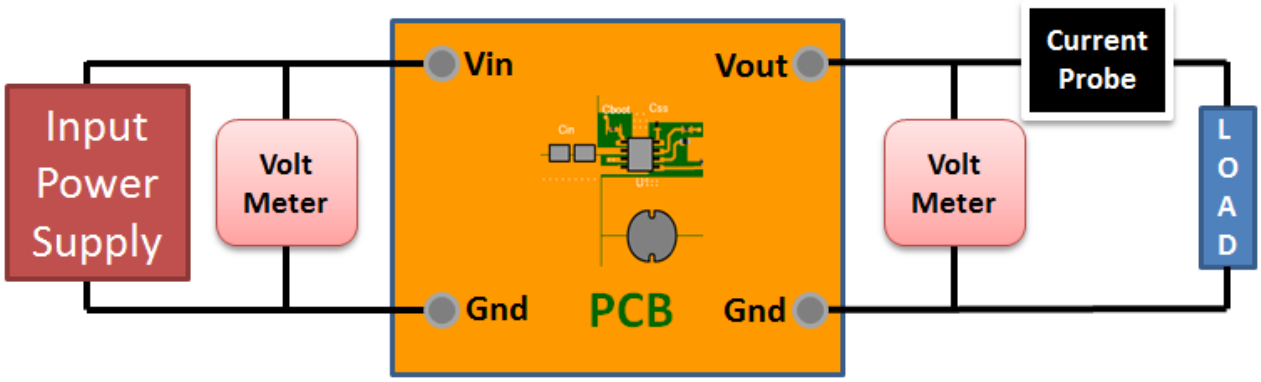
If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab town to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 2.5V and set the input supply's current limit to zero. With the input supply off connect up the input supply to Vin and GND. Connect a digital volt meter and a load if needed to set the minimum Iout of the design from Vout and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between Vin and GND, a load is connected between Vout and GND and a current meter is connected in series between Vout and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.

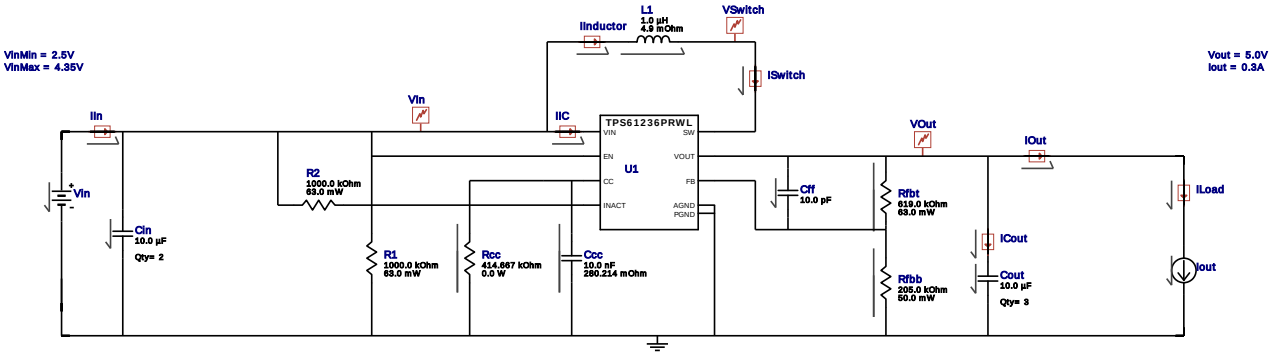


WEBENCH® Electrical Simulation Report

Design Id = 2

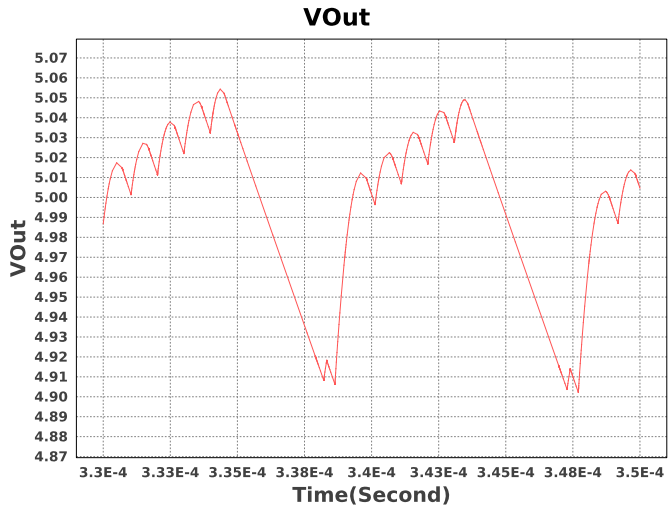
sim_id = 1

Simulation Type = Steady State



Simulation Parameters

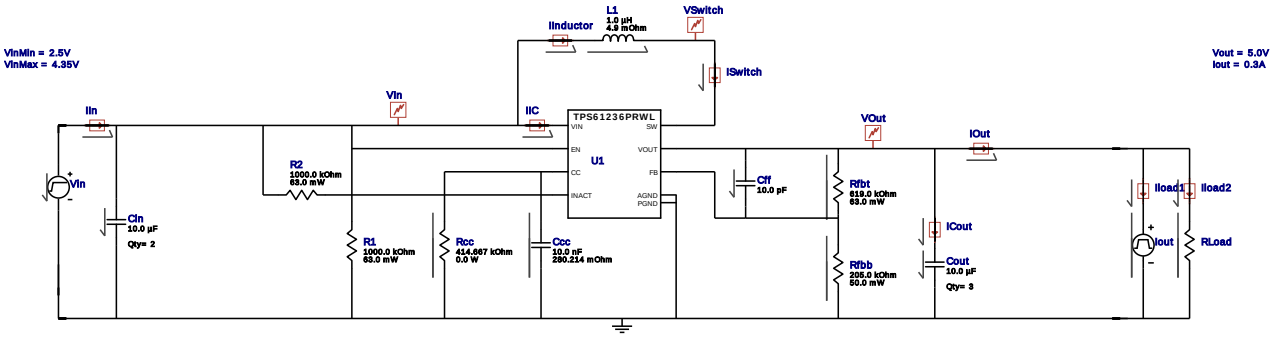
#	Name	Parameter Name	Description	Values
1.	L1	IC	Initial Current	-0.3 A
2.	Iout	I	Load Current	0.3 A



Design Id = 2

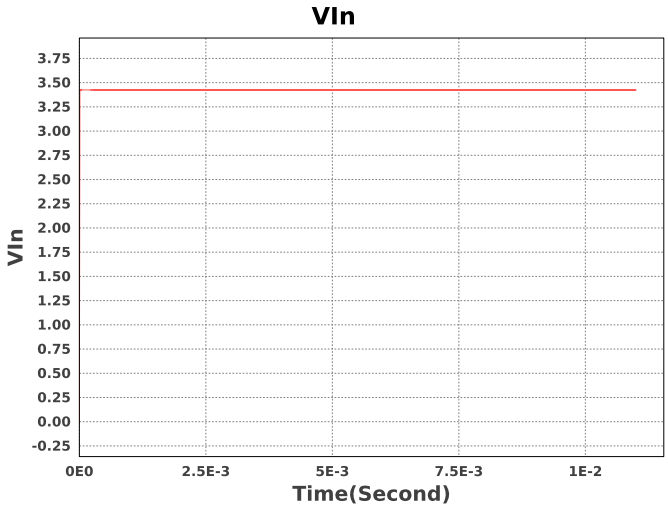
sim_id = 2

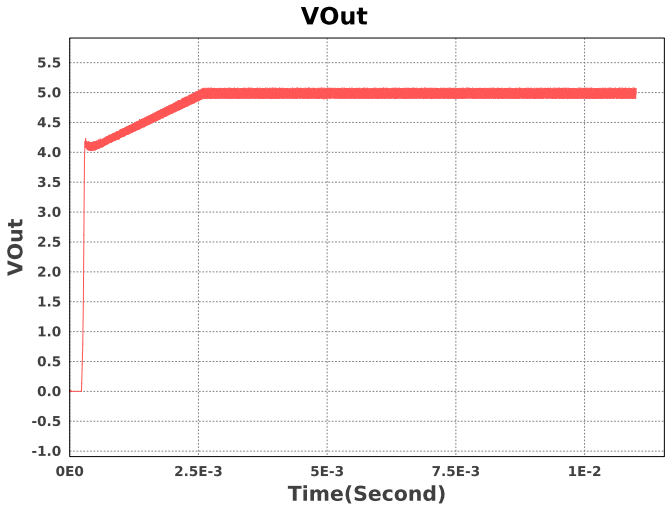
Simulation Type = Startup



Simulation Parameters

#	Name	Parameter Name	Description	Values
1.	Rload	R	Load Resistance	16.666666666666668 Ohm

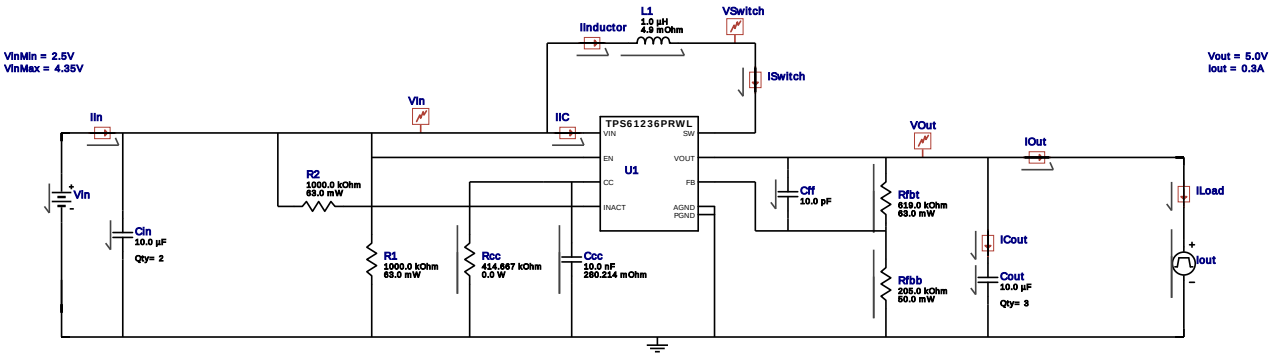




Design Id = 2

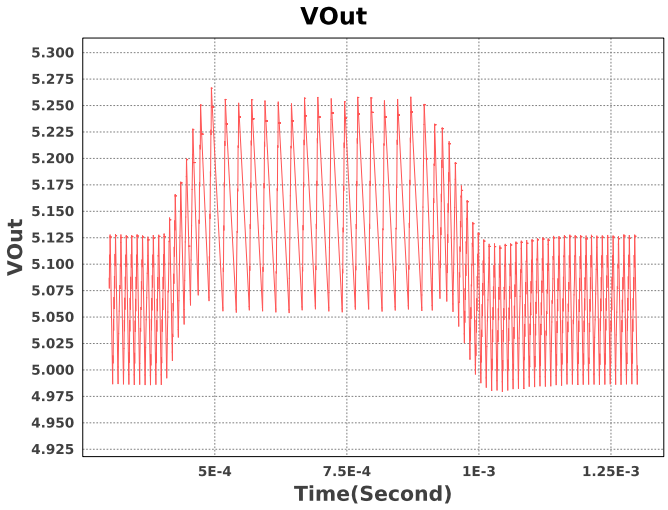
sim_id = 3

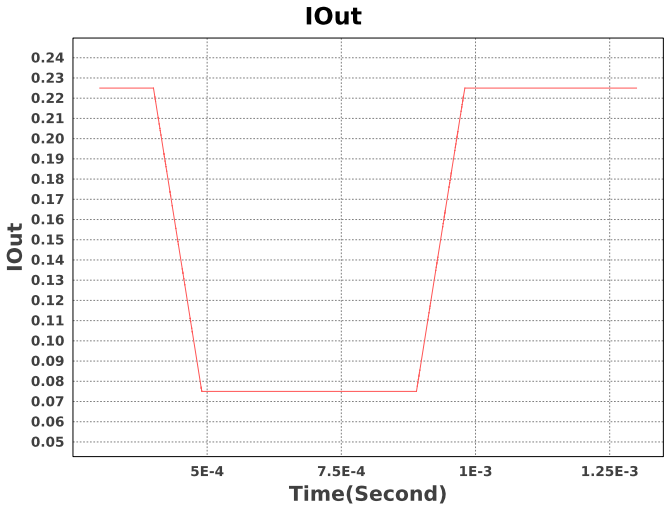
Simulation Type = Load Transient



Simulation Parameters

#	Name	Parameter Name	Description	Values
1.	L1	IC	Initial Current	-0.3 A
2.	Iout	signal_type	Signal type	PULSE
		I1	Initial Load Current	0.22499999999999998 A
		I2	Minimum Load Current	0.075 A
		Td	Initial Time Delay	400u s
		Tf	Fall Time	90u s
		Tr	Rise Time	90u s
		Pw	Pulse Width	400u s





Design Assistance

1. Master key : E45EC124FA155B08[v1]
2. **TPS61236P** Product Folder : http://www.ti.com/product/TPS61236P : contains the data sheet and other resources.

ANEXO V

Datasheets

Atmel

ATmega328P

8-bit AVR Microcontroller with 32K Bytes In-System Programmable Flash

DATASHEET

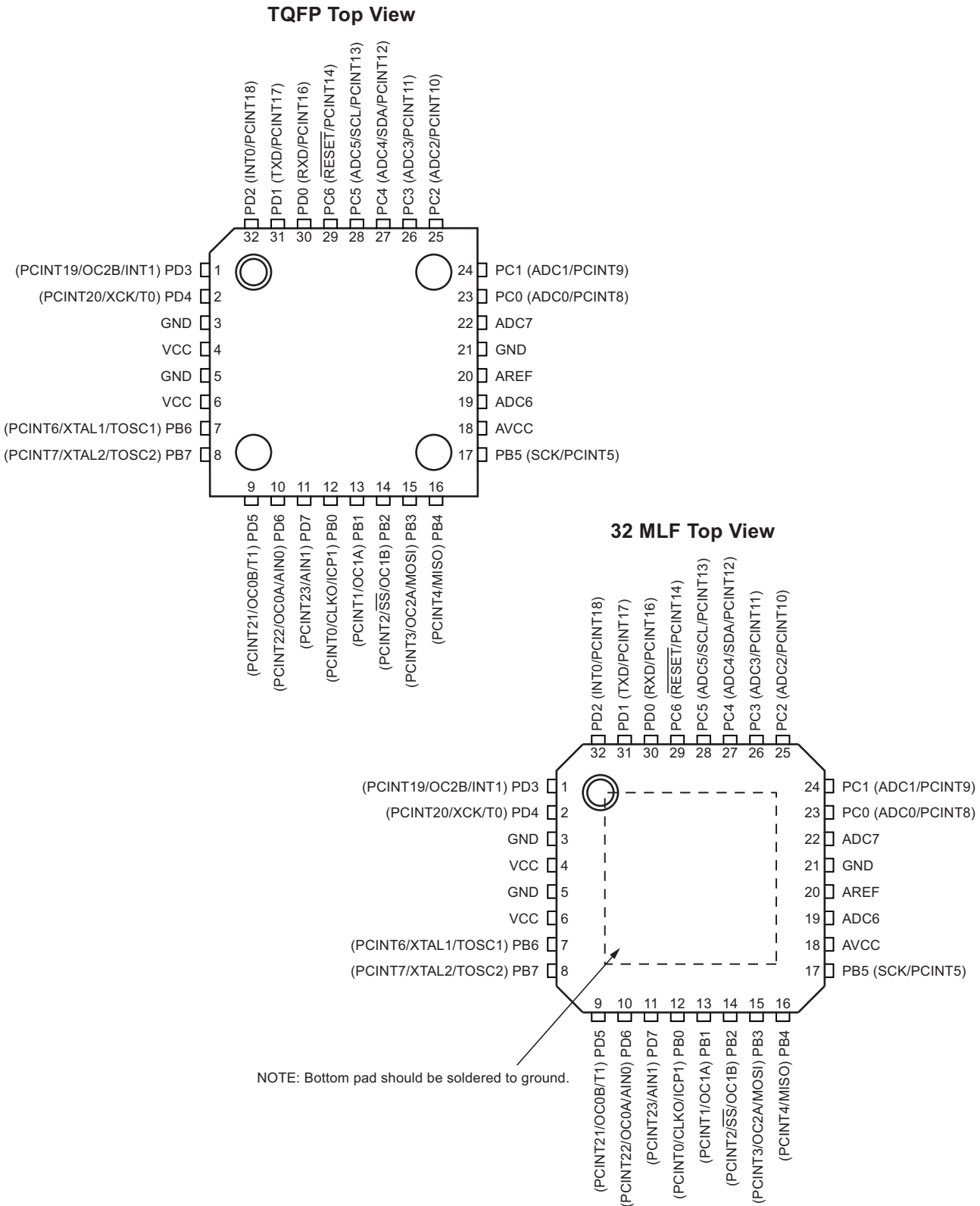
Features

- High performance, low power AVR® 8-bit microcontroller
- Advanced RISC architecture
  - 131 powerful instructions – most single clock cycle execution
  - 32 × 8 general purpose working registers
  - Fully static operation
  - Up to 16MIPS throughput at 16MHz
  - On-chip 2-cycle multiplier
- High endurance non-volatile memory segments
  - 32K bytes of in-system self-programmable flash program memory
  - 1Kbytes EEPROM
  - 2Kbytes internal SRAM
  - Write/erase cycles: 10,000 flash/100,000 EEPROM
  - Optional boot code section with independent lock bits
    - In-system programming by on-chip boot program
    - True read-while-write operation
  - Programming lock for software security
- Peripheral features
  - Two 8-bit Timer/Counters with separate prescaler and compare mode
  - One 16-bit Timer/Counter with separate prescaler, compare mode, and capture mode
  - Real time counter with separate oscillator
  - Six PWM channels
  - 8-channel 10-bit ADC in TQFP and QFN/MLF package
    - Temperature measurement
  - Programmable serial USART
  - Master/slave SPI serial interface
  - Byte-oriented 2-wire serial interface (Phillips I^2C compatible)
  - Programmable watchdog timer with separate on-chip oscillator
  - On-chip analog comparator
  - Interrupt and wake-up on pin change
- Special microcontroller features
  - Power-on reset and programmable brown-out detection
  - Internal calibrated oscillator
  - External and internal interrupt sources
  - Six sleep modes: Idle, ADC noise reduction, power-save, power-down, standby, and extended standby

- I/O and packages
  - 23 programmable I/O lines
  - 32-lead TQFP, and 32-pad QFN/MLF
- Operating voltage:
  - 2.7V to 5.5V for ATmega328P
- Temperature range:
  - Automotive temperature range: –40°C to +125°C
- Speed grade:
  - 0 to 8MHz at 2.7 to 5.5V (automotive temperature range: –40°C to +125°C)
  - 0 to 16MHz at 4.5 to 5.5V (automotive temperature range: –40°C to +125°C)
- Low power consumption
  - Active mode: 1.5mA at 3V - 4MHz
  - Power-down mode: 1µA at 3V

1. Pin Configurations

Figure 1-1. Pinout



1.1 Pin Descriptions

1.1.1 VCC

Digital supply voltage.

1.1.2 GND

Ground.

1.1.3 Port B (PB7:0) XTAL1/XTAL2/TOSC1/TOSC2

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the inverting oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PB7 can be used as output from the inverting oscillator amplifier.

If the internal calibrated RC oscillator is used as chip clock source, PB7..6 is used as TOSC2..1 input for the asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

The various special features of port B are elaborated in Section 13.3.1 “Alternate Functions of Port B” on page 65 and Section 8. “System Clock and Clock Options” on page 24.

1.1.4 Port C (PC5:0)

Port C is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The PC5..0 output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

1.1.5 PC6/$\overline{\text{RESET}}$

If the RSTDISBL fuse is programmed, PC6 is used as an input pin. If the RSTDISBL fuse is unprogrammed, PC6 is used as a reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 28-4 on page 261. Shorter pulses are not guaranteed to generate a reset.

The various special features of port C are elaborated in Section 13.3.2 “Alternate Functions of Port C” on page 68.

1.1.6 Port D (PD7:0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, port D pins that are externally pulled low will source current if the pull-up resistors are activated. The port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

The various special features of port D are elaborated in Section 13.3.3 “Alternate Functions of Port D” on page 70.

1.1.7 AV_{CC}

AV_{CC} is the supply voltage pin for the A/D converter, PC3:0, and ADC7:6. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter. Note that PC6..4 use digital supply voltage, V_{CC}.

1.1.8 AREF

AREF is the analog reference pin for the A/D converter.

1.1.9 ADC7:6 (TQFP and QFN/MLF Package Only)

In the TQFP and QFN/MLF package, ADC7:6 serve as analog inputs to the A/D converter. These pins are powered from the analog supply and serve as 10-bit ADC channels.

1.2 Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of actual ATmega328P AVR® microcontrollers manufactured on the typical process technology. automotive min and max values are based on characterization of actual ATmega328P AVR microcontrollers manufactured on the whole process excursion (corner run).

1.3 Automotive Quality Grade

The ATmega328P have been developed and manufactured according to the most stringent requirements of the international standard ISO-TS-16949. This data sheet contains limit values extracted from the results of extensive characterization (temperature and voltage). The quality and reliability of the ATmega328P have been verified during regular product qualification as per AEC-Q100 grade 1. As indicated in the ordering information paragraph, the products are available in only one temperature.

Table 1-1. Temperature Grade Identification for Automotive Products

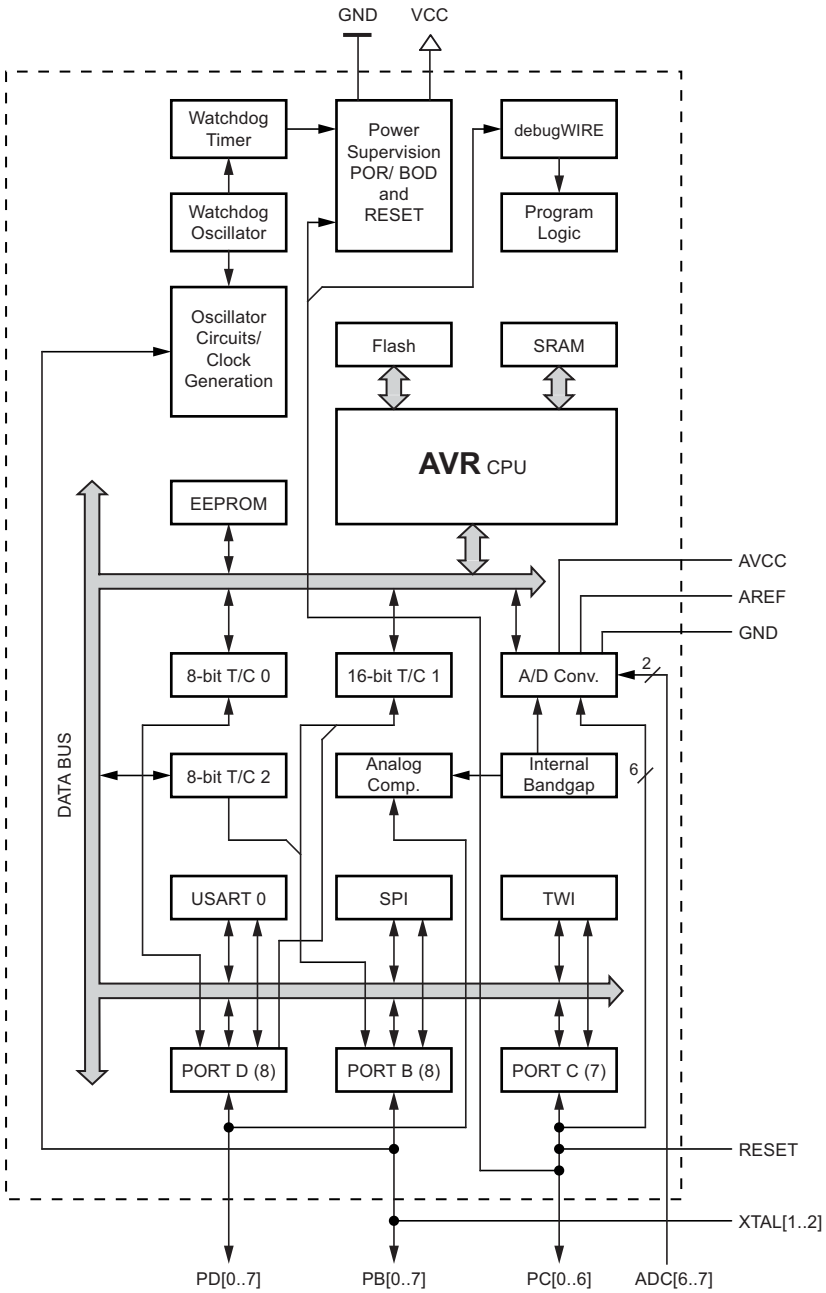
Temperature	Temperature Identifier	Comments
–40°C; +125°C	Z	Full automotive temperature range

2. Overview

The Atmel® ATmega328P is a low-power CMOS 8-bit microcontroller based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega328P achieves throughputs approaching 1MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block Diagram

Figure 2-1. Block Diagram

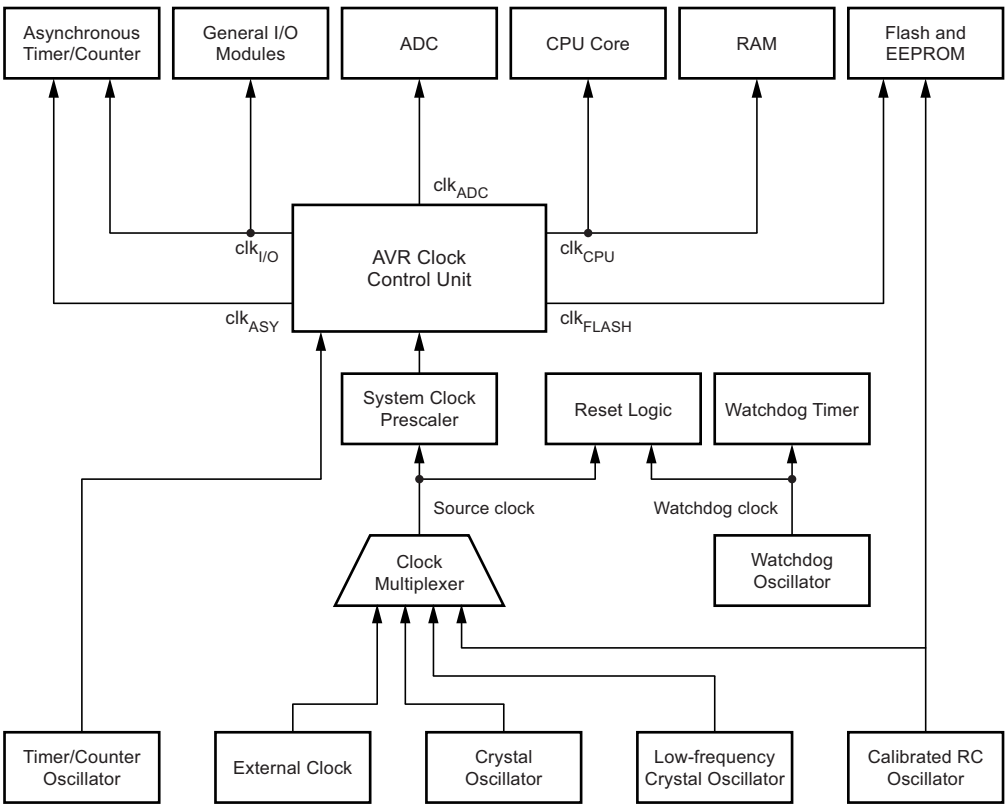


8. System Clock and Clock Options

8.1 Clock Systems and their Distribution

Figure 8-1 presents the principal clock systems in the AVR® and their distribution. All of the clocks need not be active at a given time. In order to reduce power consumption, the clocks to modules not being used can be halted by using different sleep modes, as described in Section 9. “Power Management and Sleep Modes” on page 34. The clock systems are detailed below.

Figure 8-1. Clock Distribution



8.1.1 CPU Clock – clk_{CPU}

The CPU clock is routed to parts of the system concerned with operation of the AVR core. Examples of such modules are the general purpose register file, the status register and the data memory holding the stack pointer. Halting the CPU clock inhibits the core from performing general operations and calculations.

8.1.2 I/O Clock – $clk_{I/O}$

The I/O clock is used by the majority of the I/O modules, like Timer/Counters, SPI, and USART. The I/O clock is also used by the external interrupt module, but note that some external interrupts are detected by asynchronous logic, allowing such interrupts to be detected even if the I/O clock is halted. Also note that start condition detection in the USI module is carried out asynchronously when $clk_{I/O}$ is halted, TWI address recognition in all sleep modes.

8.1.3 Flash Clock – clk_{FLASH}

The flash clock controls operation of the flash interface. The flash clock is usually active simultaneously with the CPU clock.

8.1.4 Asynchronous Timer Clock – clk_{ASY}

The asynchronous timer clock allows the asynchronous Timer/Counter to be clocked directly from an external clock or an external 32kHz clock crystal. The dedicated clock domain allows using this Timer/Counter as a real-time counter even when the device is in sleep mode.

8.1.5 ADC Clock – clk_{ADC}

The ADC is provided with a dedicated clock domain. This allows halting the CPU and I/O clocks in order to reduce noise generated by digital circuitry. This gives more accurate ADC conversion results.

8.2 Clock Sources

The device has the following clock source options, selectable by flash fuse bits as shown below. The clock from the selected source is input to the AVR® clock generator, and routed to the appropriate modules.

Table 8-1. Device Clocking Options Select(1)

Device Clocking Option	CKSEL3..0
Low power crystal oscillator	1111 - 1000
Full swing crystal oscillator	0111 - 0110
Low frequency crystal oscillator	0101 - 0100
Internal 128kHz RC oscillator	0011
Calibrated internal RC oscillator	0010
External clock	0000
Reserved	0001

Note: 1. For all fuses “1” means unprogrammed while “0” means programmed.

8.2.1 Default Clock Source

The device is shipped with internal RC oscillator at 8.0MHz and with the fuse CKDIV8 programmed, resulting in 1.0MHz system clock. The startup time is set to maximum and time-out period enabled. (CKSEL = “0010”, SUT = “10”, CKDIV8 = “0”). The default setting ensures that all users can make their desired clock source setting using any available programming interface.

8.2.2 Clock Startup Sequence

Any clock source needs a sufficient V_{CC} to start oscillating and a minimum number of oscillating cycles before it can be considered stable.

To ensure sufficient V_{CC}, the device issues an internal reset with a time-out delay (t_{TOUT}) after the device reset is released by all other reset sources. Section 10. “System Control and Reset” on page 40 describes the start conditions for the internal reset. The delay (t_{TOUT}) is timed from the watchdog oscillator and the number of cycles in the delay is set by the SUTx and CKSELx fuse bits. The selectable delays are shown in Table 8-2. The frequency of the watchdog oscillator is voltage dependent as shown in Section 29. “Typical Characteristics” on page 268.

Table 8-2. Number of Watchdog Oscillator Cycles

Typ Time-out (V_{CC} = 5.0V)	Typ Time-out (V_{CC} = 3.0V)	Number of Cycles
0ms	0ms	0
4.1ms	4.3ms	512
65ms	69ms	8K (8,192)

Main purpose of the delay is to keep the AVR in reset until it is supplied with minimum V_{CC}. The delay will not monitor the actual voltage and it will be required to select a delay longer than the V_{CC} rise time. If this is not possible, an internal or external brown-out detection circuit should be used. A BOD circuit will ensure sufficient V_{CC} before it releases the reset, and the time-out delay can be disabled. Disabling the time-out delay without utilizing a brown-out detection circuit is not recommended.

The oscillator is required to oscillate for a minimum number of cycles before the clock is considered stable. An internal ripple counter monitors the oscillator output clock, and keeps the internal reset active for a given number of clock cycles. The reset is then released and the device will start to execute. The recommended oscillator start-up time is dependent on the clock type, and varies from 6 cycles for an externally applied clock to 32K cycles for a low frequency crystal.

The start-up sequence for the clock includes both the time-out delay and the start-up time when the device starts up from reset. When starting up from power-save or power-down mode, V_{CC} is assumed to be at a sufficient level and only the start-up time is included.

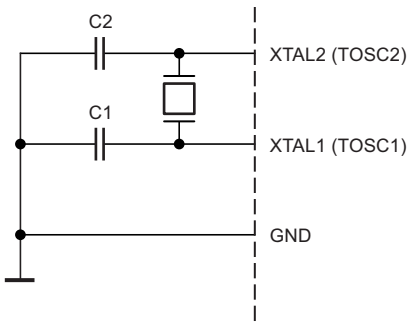
8.3 Low Power Crystal Oscillator

Pins XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 8-2. Either a quartz crystal or a ceramic resonator may be used.

This crystal oscillator is a low power oscillator, with reduced voltage swing on the XTAL2 output. It gives the lowest power consumption, but is not capable of driving other clock inputs, and may be more susceptible to noise in noisy environments. In these cases, refer to the Section 8.4 “Full Swing Crystal Oscillator” on page 27.

C1 and C2 should always be equal for both crystals and resonators. The optimal value of the capacitors depends on the crystal or resonator in use, the amount of stray capacitance, and the electromagnetic noise of the environment. Some initial guidelines for choosing capacitors for use with crystals are given in Table 8-3. For ceramic resonators, the capacitor values given by the manufacturer should be used.

Figure 8-2. Crystal Oscillator Connections



The low power oscillator can operate in three different modes, each optimized for a specific frequency range. The operating mode is selected by the fuses CKSEL3..1 as shown in Table 8-3.

Table 8-3. Low Power Crystal Oscillator Operating Modes(2)

Frequency Range (MHz)	Recommended Range for Capacitors C1 and C2 (pF)	CKSEL3..1
0.4 to 0.9	–	100(1)
0.9 to 3.0	12 to 22	101
3.0 to 8.0	12 to 22	110
8.0 to 16.0	12 to 22	111

Notes:
1. .This option should not be used with crystals, only with ceramic resonators.
2. If 8MHz frequency exceeds the specification of the device (depends on V_{CC}), the CKDIV8 fuse can be programmed in order to divide the internal frequency by 8. It must be ensured that the resulting divided clock meets the frequency specification of the device.

The CKSEL0 fuse together with the SUT1..0 fuses select the start-up times as shown in Table 8-4.

Table 8-4. Start-up Times for the Low Power Crystal Oscillator Clock Selection

Oscillator Source / Power Conditions	Start-up Time from Power-down and Power-save	Additional Delay from Reset (V_{CC} = 5.0V)	CKSEL0	SUT1..0
Ceramic resonator, fast rising power	258CK	14CK + 4.1ms(1)	0	00
Ceramic resonator, slowly rising power	258CK	14CK + 65ms(1)	0	01
Ceramic resonator, BOD enabled	1KCK	14CK(2)	0	10
Ceramic resonator, fast rising power	1KCK	14CK + 4.1ms(2)	0	11
Ceramic resonator, slowly rising power	1KCK	14CK + 65ms(2)	1	00
Crystal oscillator, BOD enabled	16KCK	14CK	1	01
Crystal oscillator, fast rising power	16KCK	14CK + 4.1ms	1	10
Crystal oscillator, slowly rising power	16KCK	14CK + 65ms	1	11

Notes:
1. These options should only be used when not operating close to the maximum frequency of the device, and only if frequency stability at start-up is not important for the application. These options are not suitable for crystals.
2. These options are intended for use with ceramic resonators and will ensure frequency stability at start-up. They can also be used with crystals when not operating close to the maximum frequency of the device, and if frequency stability at start-up is not important for the application.

8.4 Full Swing Crystal Oscillator

Pins XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 8-2 on page 26. Either a quartz crystal or a ceramic resonator may be used.

This crystal oscillator is a full swing oscillator, with rail-to-rail swing on the XTAL2 output. This is useful for driving other clock inputs and in noisy environments. The current consumption is higher than the Section 8.3 “Low Power Crystal Oscillator” on page 26. Note that the full swing crystal oscillator will only operate for V_{CC} = 2.7 to 5.5V.

C1 and C2 should always be equal for both crystals and resonators. The optimal value of the capacitors depends on the crystal or resonator in use, the amount of stray capacitance, and the electromagnetic noise of the environment. Some initial guidelines for choosing capacitors for use with crystals are given in Table 8-6 on page 28. For ceramic resonators, the capacitor values given by the manufacturer should be used.

The operating mode is selected by the fuses CKSEL3..1 as shown in Table 8-5.

Table 8-5. Full Swing Crystal Oscillator operating modes(2)

Frequency Range(1) (MHz)	Recommended Range for Capacitors C1 and C2 (pF)	CKSEL3..1
0.4 - 16	12 - 22	011

Notes:
1. The frequency ranges are preliminary values. Actual values are TBD.
2. If 8MHz frequency exceeds the specification of the device (depends on V_{CC}), the CKDIV8 fuse can be programmed in order to divide the internal frequency by 8. It must be ensured that the resulting divided clock meets the frequency specification of the device.

Figure 8-3. Crystal Oscillator Connections

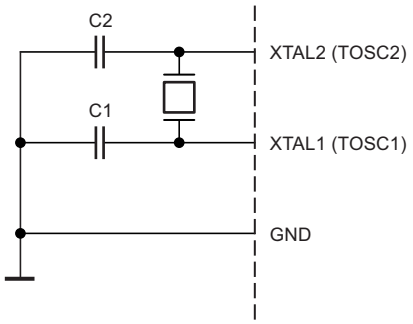


Table 8-6. Start-up Times for the Full Swing Crystal Oscillator Clock Selection

Oscillator Source / Power Conditions	Start-up Time from Power-down and Power-save	Additional Delay from Reset (V_{CC} = 5.0V)	CKSEL0	SUT1..0
Ceramic resonator, fast rising power	258CK	14CK + 4.1ms[1]	0	00
Ceramic resonator, slowly rising power	258CK	14CK + 65ms[1]	0	01
Ceramic resonator, BOD enabled	1KCK	14CK[2]	0	10
Ceramic resonator, fast rising power	1KCK	14CK + 4.1ms[2]	0	11
Ceramic resonator, slowly rising power	1KCK	14CK + 65ms[2]	1	00
Crystal oscillator, BOD enabled	16KCK	14CK	1	01
Crystal oscillator, fast rising power	16KCK	14CK + 4.1ms	1	10
Crystal oscillator, slowly rising power	16KCK	14CK + 65ms	1	11

Notes:
1. These options should only be used when not operating close to the maximum frequency of the device, and only if frequency stability at start-up is not important for the application. These options are not suitable for crystals.
2. These options are intended for use with ceramic resonators and will ensure frequency stability at start-up. They can also be used with crystals when not operating close to the maximum frequency of the device, and if frequency stability at start-up is not important for the application.

8.5 Low Frequency Crystal Oscillator

The low-frequency crystal oscillator is optimized for use with a 32.768kHz watch crystal. When selecting crystals, load capacitance and crystal's equivalent series resistance, ESR must be taken into consideration. Both values are specified by the crystal vendor. ATmega328P oscillator is optimized for very low power consumption, and thus when selecting crystals, see Table 8-7 for maximum ESR recommendations on 6.5pF, 9.0pF and 12.5pF crystals

Table 8-7. Maximum ESR Recommendation for 32.768 kHz Crystal

Crystal CL (pF)	Max ESR [kΩ](1)
6.5	75
9.0	65
12.5	30

Note: 1. Maximum ESR is typical value based on characterization

The low-frequency crystal oscillator provides an internal load capacitance of typical 6pF at each TOSC pin. The external capacitance (C) needed at each TOSC pin can be calculated by using:

$$C = 2 \times CL - C_S$$

where CL is the load capacitance for a 32.768kHz crystal specified by the crystal vendor and C_S is the total stray capacitance for one TOSC pin.

Crystals specifying load capacitance (CL) higher than 6pF, require external capacitors applied as described in Figure 8-2 on page 26.

The low-frequency crystal oscillator must be selected by setting the CKSEL fuses to "0110" or "0111", as shown in Table 8-9. Start-up times are determined by the SUT fuses as shown in Table 8-8.

Table 8-8. Start-up Times for the Low-frequency Crystal Oscillator Clock Selection

SUT1..0	Additional Delay from Reset (V_{CC} = 5.0V)	Recommended Usage
00	4CK	Fast rising power or BOD enabled
01	4CK + 4.1ms	Slowly rising power
10	4CK + 65ms	Stable frequency at start-up
11	Reserved	

Table 8-9. Start-up Times for the Low-frequency Crystal Oscillator Clock Selection

CKSEL3..0	Start-up Time from Power-down and Power-save	Recommended Usage
0100(1)	1KCK	
0101	32KCK	Stable frequency at start-up

Note: 1. This option should only be used if frequency stability at start-up is not important for the application

8.6 Calibrated Internal RC Oscillator

By default, the internal RC oscillator provides an approximate 8.0MHz clock. Though voltage and temperature dependent, this clock can be very accurately calibrated by the user. See Table 28-1 on page 260 for more details. The device is shipped with the CKDIV8 fuse programmed. See Section 8.11 "System Clock Prescaler" on page 32 for more details.

This clock may be selected as the system clock by programming the CKSEL fuses as shown in Table 8-10 on page 30. If selected, it will operate with no external components. During reset, hardware loads the pre-programmed calibration value into the OSCCAL register and thereby automatically calibrates the RC oscillator. The accuracy of this calibration is shown as factory calibration in Table 28-1 on page 260.

By changing the OSCCAL register from SW, see Section 8.12.1 “OSCCAL – Oscillator Calibration Register” on page 32, it is possible to get a higher calibration accuracy than by using the factory calibration. The accuracy of this calibration is shown as User calibration in Table 28-1 on page 260.

When this oscillator is used as the chip clock, the watchdog oscillator will still be used for the watchdog timer and for the reset time-out. For more information on the pre-programmed calibration value, see Section 27.4 “Calibration Byte” on page 244.

Table 8-10. Internal Calibrated RC Oscillator Operating Modes(1)(2)

Nominal Frequency (MHz)	CKSEL3..0
8	0010

Notes: 1. The device is shipped with this option selected.
2. If 8MHz frequency exceeds the specification of the device (depends on V_{CC}), the CKDIV8 fuse can be programmed in order to divide the internal frequency by 8.

When this oscillator is selected, start-up times are determined by the SUT fuses as shown in Table 8-11.

Table 8-11. Start-up Times for the Internal calibrated RC Oscillator Clock Selection

Power Conditions	Start-up Time from Power-down and Power-save	Additional Delay from Reset (V_{CC} = 5.0V)	SUT1..0
BOD enabled	6CK	14CK(1)	00
Fast rising power	6CK	14CK + 4.1ms	01
Slowly rising power	6CK	14CK + 65ms(2)	10
Reserved			11

Notes: 1. If the RSTDISBL fuse is programmed, this start-up time will be increased to 14CK + 4.1ms to ensure programming mode can be entered.
2. The device is shipped with this option selected.

8.7 128 kHz Internal Oscillator

The 128kHz internal oscillator is a low power oscillator providing a clock of 128kHz. The frequency is nominal at 3V and 25°C. This clock may be select as the system clock by programming the CKSEL fuses to “11” as shown in Table 8-12.

.

Table 8-12. 128kHz Internal Oscillator Operating Modes

Nominal Frequency	CKSEL3..0
128kHz	0011

When this clock source is selected, start-up times are determined by the SUT fuses as shown in Table 8-13.

Table 8-13. Start-up Times for the 128 kHz Internal Oscillator

Power Conditions	Start-up Time from Power-down and Power-save	Additional Delay from Reset	SUT1..0
BOD enabled	6CK	14CK(1)	00
Fast rising power	6CK	14CK + 4ms	01
Slowly rising power	6CK	14CK + 64ms	10
Reserved			11

Note: 1. If the RSTDISBL fuse is programmed, this start-up time will be increased to 14CK + 4.1ms to ensure programming mode can be entered.

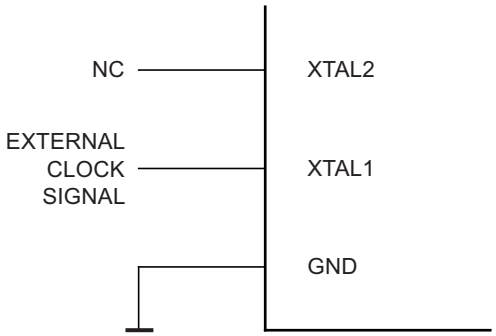
8.8 External Clock

To drive the device from an external clock source, XTAL1 should be driven as shown in Figure 8-4. To run the device on an external clock, the CKSEL fuses must be programmed to “0000” (see Table 8-14).

Table 8-14. Crystal Oscillator Clock Frequency

Frequency	CKSEL3..0
0 to 16MHz	0000

Figure 8-4. External Clock Drive Configuration



When this clock source is selected, start-up times are determined by the SUT fuses as shown in Table 8-15.

Table 8-15. Start-up Times for the External Clock Selection

Power Conditions	Start-up Time from Power-down and Power-save	Additional Delay from Reset (V_{CC} = 5.0V)	SUT1..0
BOD enabled	6CK	14CK	00
Fast rising power	6CK	14CK + 4.1ms	01
Slowly rising power	6CK	14CK + 65ms	10
Reserved			11

When applying an external clock, it is required to avoid sudden changes in the applied clock frequency to ensure stable operation of the MCU. A variation in frequency of more than 2% from one clock cycle to the next can lead to unpredictable behavior. If changes of more than 2% is required, ensure that the MCU is kept in reset during the changes.

Note that the system clock prescaler can be used to implement run-time changes of the internal clock frequency while still ensuring stable operation. Refer to Section 8.11 “System Clock Prescaler” on page 32 for details.

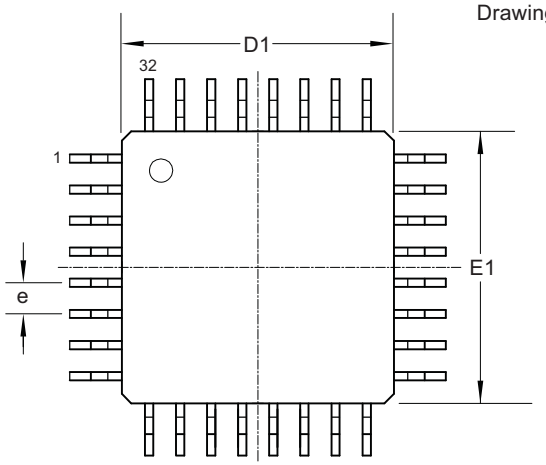
8.9 Clock Output Buffer

The device can output the system clock on the CLKO pin. To enable the output, the CKOUT fuse has to be programmed. This mode is suitable when the chip clock is used to drive other circuits on the system. The clock also will be output during reset, and the normal operation of I/O pin will be overridden when the fuse is programmed. Any clock source, including the internal RC oscillator, can be selected when the clock is output on CLKO. If the system clock prescaler is used, it is the divided system clock that is output.

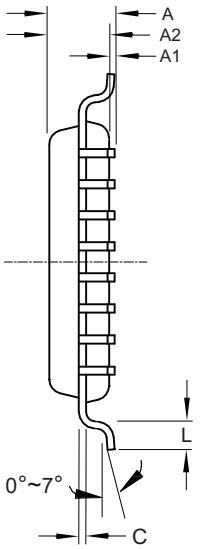
33. Packaging Information

33.1 MA

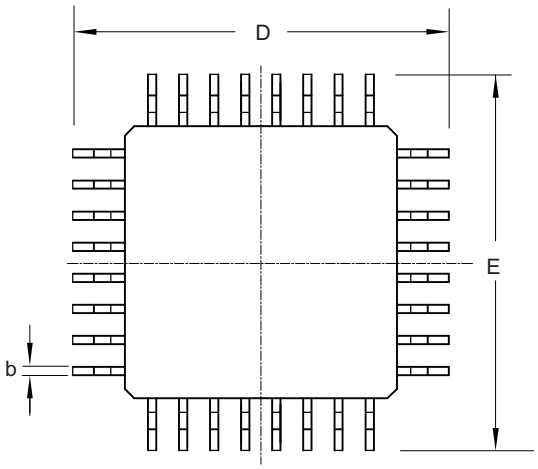
Drawings not scaled



Top View



Side View



Bottom View

COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A	----	----	1.20	
A1	0.05	----	0.15	
A2	0.95	1.00	1.05	
D/E	8.75	9.00	9.25	
D1/E1	6.90	7.00	7.10	2
C	0.09	----	0.20	
L	0.45	----	0.75	
b	0.30	----	0.45	
e	0.80 TYP.			
n	32			

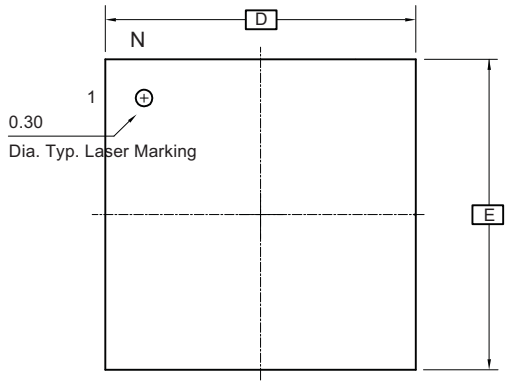
Notes: 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

02/29/12

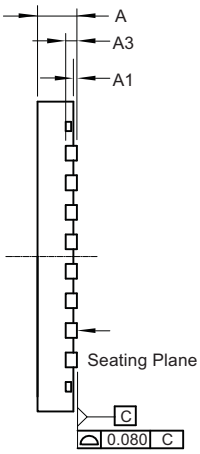
Atmel **Package Drawing Contact:** packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	MA, 32 Lds - 0.80mm Pitch, 7x7x1.00mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	AUT	MA	C

33.2 PN

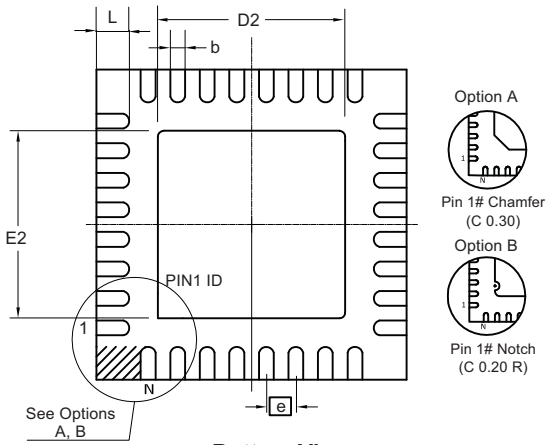
Drawings not scaled



Top View



Side View



Bottom View

COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A	0.80	0.85	0.90	
A1	0.00	----	0.05	
A3		0.20 REF		
D/E		5.00 BSC		
D2/E2	3.00	3.10	3.20	
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	2
e		0.50 BSC		
n		32		

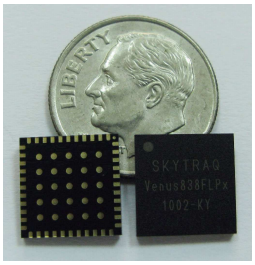
Notes: 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VHHD-2, for proper dimensions, tolerances, datums, etc.
2. Dimensions b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optical radius on the other end of the terminal, the dimensions should not be measured in that radius area.

01/31/12

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	PN, 32 Leads - 0.50mm Pitch, 5x5mm Very Thin Quad Flat no Lead Package (VQFN) Sawn	ZMF	PN	I

Venus838FLPx GPS Receiver

Data Sheet



10mmx 10mm

Venus838FLPx-L / Venus838FLPx-D

FEATURES

- 50Hz maximum update rate
- -148dBm cold start sensitivity
- -165dBm tracking sensitivity
- 29 second cold start TTFF
- 3.5 second TTFF with AGPS
- 1 second hot start
- 2.5m accuracy
- Multipath detection and suppression
- Jamming detection and mitigation
- QZSS and SBAS support
- 7-day extended ephemeris AGPS
- Self-aided ephemeris estimation
- 74mW full power navigation
- Works directly with active or passive antenna
- Supports external SPI flash memory data logging
- Complete receiver in 10mm x 10mm x 1.3mm size
- Contains LNA, SAW Filter, TCXO, RTC Xtal, LDO
- Pb-free RoHS compliant

Venus838FLPx is a high performance, low cost, single chip GPS receiver targeting mobile consumer and cellular handset applications. It offers very low power consumption, high sensitivity, and best in class signal acquisition and time-to-first-fix performance.

Venus838FLPx contains all the necessary components of a complete GPS receiver, includes 1.2dB cascaded system NF RF front-end, GPS baseband signal processor, 0.5ppm TCXO, 32.768kHz RTC crystal, RTC LDO regulator, and passive components. It requires very low external component count and takes up only 100mm^2 PCB footprint.

Dedicated massive-correlator signal parameter search engine within the baseband enables rapid search of all the available satellites and acquisition of very weak signal. An advanced track engine allows weak signal tracking and positioning in harsh environments such as urban canyons and under deep foliage.

The self-contained architecture keeps GPS processing off the host and allows integration into applications with very little resource.

Venus838FLPx is very easy to use, minimizes RF layout design issues and offers very fast time to market.

Product Series	**Product Description**
Venus838FLPx-L	Flash version GPS receiver (internal 1.2V LDO version) Suitable for lower cost application using internal 1.2V supply
Venus838FLPx-D	Flash version GPS receiver (external 1.2V version) Suitable for lower power application using external 1.2V supply

TECHNICAL SPECIFICATIONS

Receiver Type	L1 C/A code GPS QZSS SBAS 65-channel architecture 167 channel Venus 8 engine
Accuracy	Position 2.5m CEP Velocity 0.1m/sec Timing 10ns
Open Sky TTFF	29 second cold start 3.5 second with AGPS 1 second hot start
Reacquisition	< 1s
Sensitivity	-165dBm tracking -148dBm cold start
Update Rate	1 / 2 / 4 / 5 / 8 / 10 / 20 / 25 / 40 / 50 Hz (default 1Hz)
Dynamics	4G
Operational Limits	Altitude < 18,000m[*1], Velocity < 515m/s[*1]
Datum	Default WGS-84
Interface	UART LVTTL level
Baud Rate	4800 / 9600 / 38400 / 115200
Protocol	NMEA-0183 V3.01, GGA, GLL, GSA, GSV, RMC, VTG, ZDA SkyTraq Binary
Main Supply Voltage	2.8V ~ 3.6V (Venus838FLPx-L) 2.8V ~ 3.6V, 1.08V ~ 1.32V (Venus838FLPx-D)
Backup Voltage	2.5V ~ 3.6V

Current Consumption (3.3V)

	Acquisition				Tracking
Number of Search Engine	2	4	6*	8	
Venus838FLPx-L	39mA	45mA	51mA	59mA	33mA
Venus838FLPx-D**	20mA	23mA	26mA	30mA	16mA

* default 6 search engine used
** higher efficiency 3.3V-to-1.2V switch-mode regulator is used

Operating Temperature	-40 ~ +85 deg-C
Storage Temperature	-40 ~ +125 deg-C
Package	LGA69 10mm x 10mm x 1.3mm, 0.8mm pitch
Weight	0.3g

*1: COCOM limit, either may be exceeded but not both

BLOCK DIAGRAM

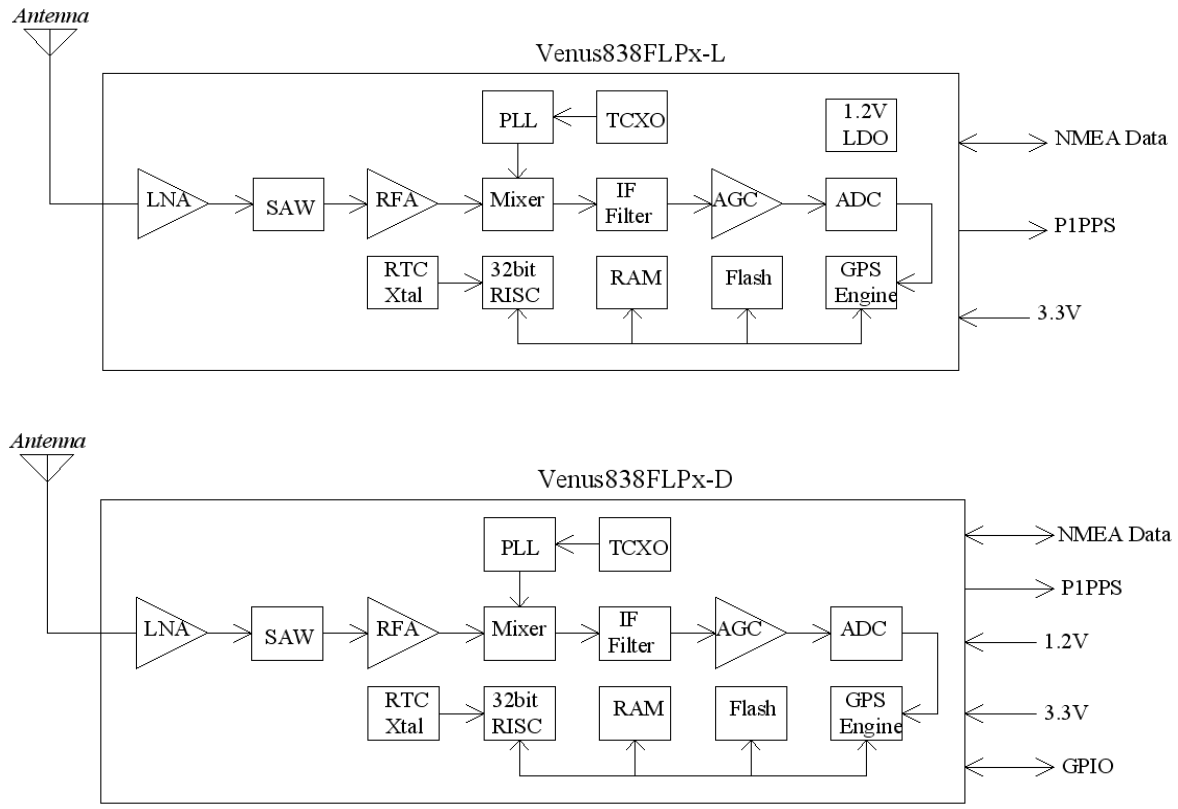


Figure-1 GPS Receiver based on Venus838FLPx

Venus838FLPx PIN-OUT DIAGRAM

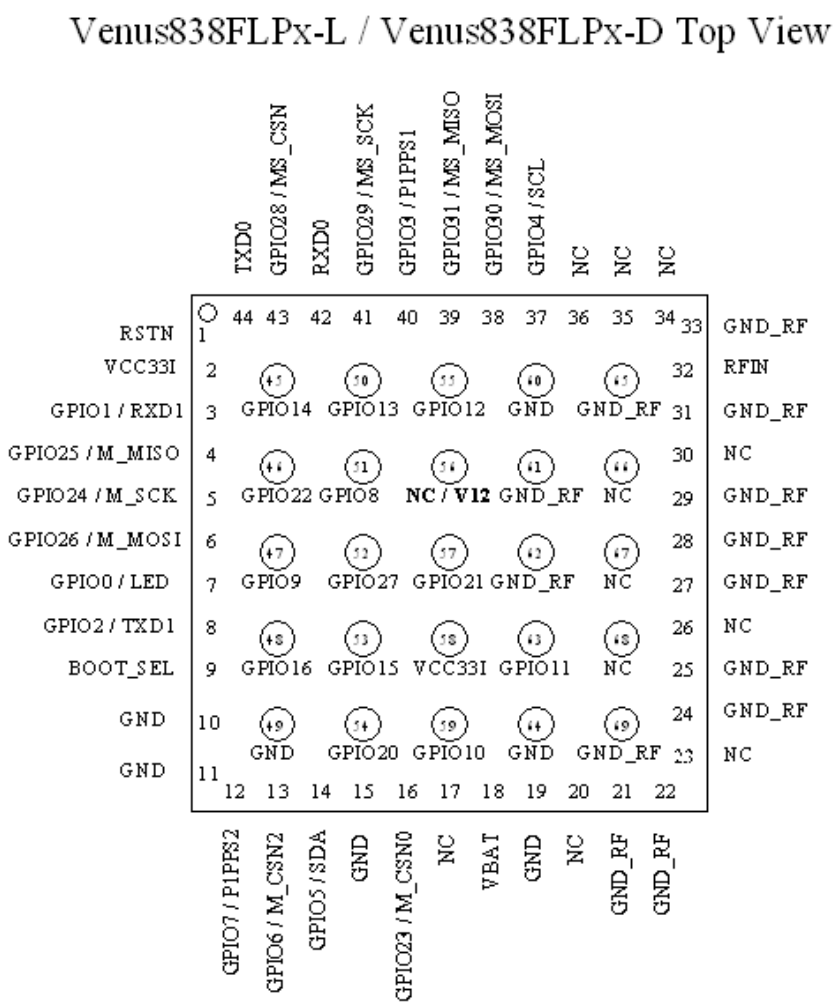


Figure-2 Venus838FLPx Pin-Out Diagram

Venus838FLPx PIN DEFINITION

Pin Number	Signal Name	Type	Description
1	RSTN	Input	Active LOW reset input, 3.3V LVTTL
2	VCC33I	Power Input	Main voltage supply input, 2.8V ~ 3.6V
3	GPIO1 / RXD1	Bidir	General purpose I/O pin, 3.3V LVTTL Or receive input of the asynchronous UART port Default not used
4	GPIO25 / M_MISO	Bidir	General purpose I/O pin, 3.3V LVTTL Or SPI master input Default not used
5	GPIO24 / M_SCK	Bidir	General purpose I/O pin, 3.3V LVTTL Or SPI master clock Default not used
6	GPIO26 / M_MOSI	Bidir	General purpose I/O pin, 3.3V LVTTL Or SPI master output Default not used
7	LED / GPIO0	Bidir	Navigation status indicator (default) Or General purpose I/O. 3.3V LVTTL
8	GPIO2 / TXD1	Bidir	General purpose I/O pin. 3.3V LVTTL Or transmit output of the asynchronous UART port Default not used

9	BOOT_SEL	Bidir	Boot mode selection. Pull-high or pull-low 1: execute from internal Flash 0: execute from internal ROM This is opposite of Venus638FLPx
10	GND	Power	System ground
11	GND	Power	System ground
12	GPIO7 / P1PPS2	Bidir	General purpose I/O pin, 3.3V LVTTL Second P1PPS output Default unused
13	GPIO6 / M_CSN2	Bidir	General purpose I/O pin, 3.3V LVTTL Or SPI master chip select #2 Default not used
14	GPIO5 / SDA	Bidir	General purpose I/O pin, 3.3V LVTTL Or I2C serial data Default not used
15	GND	Power	System ground
16	GPIO23 / M_CSN0	Bidir	General purpose I/O pin, 3.3V LVTTL Or SPI master chip select #0 Default not used
17	NC		Not connected, empty pin
18	VBAT	Power Input	Supply voltage for internal RTC and backup SRAM, 2.5V ~ 3.6V. VBAT should be powered by non-volatile supply voltage to have optimal performance. Maximum VBAT current draw when VCC33I is removed is 35uA. If VBAT is connected to VCC33I, powered off as VCC33I power is removed, then it'll cold start every time. For applications that do not care lesser performance cold starting every time, this pin can be connected to VCC33I. Must not be left unconnected.
19	GND	Power	System ground
20	NC		Not connected, empty pin
21	GND_RF	Power	RF section system ground
22	GND_RF	Power	RF section system ground
23	NC		Not connected, empty pin
24	GND_RF	Power	RF section system ground
25	GND_RF	Power	RF section system ground
26	NC		Not connected, empty pin
27	GND_RF	Power	RF section system ground
28	GND_RF	Power	RF section system ground
29	GND_RF	Power	RF section system ground
30	NC		Not connected, empty pin
31	GND_RF	Power	RF section system ground
32	RFIN	Input	GPS signal input, connect to GPS antenna.
33	GND_RF	Power	RF section system ground
34	NC		Not connected, empty pin
35	NC		Not connected, empty pin
36	NC		Not connected, empty pin
37	GPIO4 / SCL	Bidir	General purpose I/O pin, 3.3V LVTTL Or I2C SCL clock Default not used
38	GPIO30 / MS_MOSI	Bidir	General purpose I/O pin, 3.3V LVTTL Or SPI master/slave data output Default not used
39	GPIO31 / MS_MISO	Bidir	General purpose I/O pin, 3.3V LVTTL Or SPI master/slave data input Default not used
40	P1PPS / GPIO3	bidir	1 pulse per second output. Active after position fix; goes HIGH for about 4msec, 3.3V LVTTL (default) Or general purpose I/O pin
41	GPIO29 / MS_SCK	Output	General purpose output pin, 3.3V LVTTL Or SPI master/slave clock Default not used
42	RXD0	Input	Received input of the asynchronous UART port. Used to input binary command to the GPS receiver. 3.3V LVTTL
43	GPIO28 / MS_CSN	Bidir	General purpose I/O pin, 3.3V LVTTL Or SPI master/slave chip select Default not used

44	TXD0	Output	Transmit output of the asynchronous UART port. Used to output standard NMEA-0183 sentence or response to input binary command. 3.3V LVTTL
45	GPIO14	Bidir	General purpose I/O pin, 3.3V LVTTL Default not used
46	GPIO22 / M_CSN1	Bidir	General purpose I/O pin, 3.3V LVTTL Or SPI master chip select #1 Default not used
47	GPIO9	Bidir	General purpose I/O pin, 3.3V LVTTL Default not used
48	GPIO16	Bidir	General purpose I/O pin, 3.3V LVTTL Default not used
49	GND		System ground
50	GPIO13	Bidir	General purpose I/O pin, 3.3V LVTTL Default not used
51	GPIO8	Bidir	General purpose I/O pin, 3.3V LVTTL Default not used
52	GPIO27	Input	General purpose I/O pin, 3.3V LVTTL Default not used
53	GPIO15	Bidir	General purpose I/O pin, 3.3V LVTTL Default not used
54	GPIO20 / PWM0	Bidir	General purpose I/O pin, 3.3V LVTTL Or PWM output #0 Default not used
55	GPIO12	Bidir	General purpose I/O pin, 3.3V LVTTL Default not used
56	NC / V12		NC pin for Venus838FLPx-L 1.2V supply input pin for Venus838FLPx-D
57	GPIO21 / PWM1	Output	General purpose I/O pin, 3.3V LVTTL Or PWM output #1 Default not used
58	VCC33I	Power Input	Main voltage supply input, 2.8V ~ 3.6V
59	GPIO10	Bidir	General purpose I/O pin, 3.3V LVTTL Default not used
60	GND	Power	System ground
61	GND_RF	Power	RF section system ground
62	GND_RF	Power	RF section system ground
63	GPIO11	Bidir	General purpose I/O pin, 3.3V LVTTL Default not used
64	GND	Power	System ground
65	GND_RF	Power	RF section system ground
66,67,68	NC		Not connected, empty pin
69	GND_RF	Power	RF section system ground

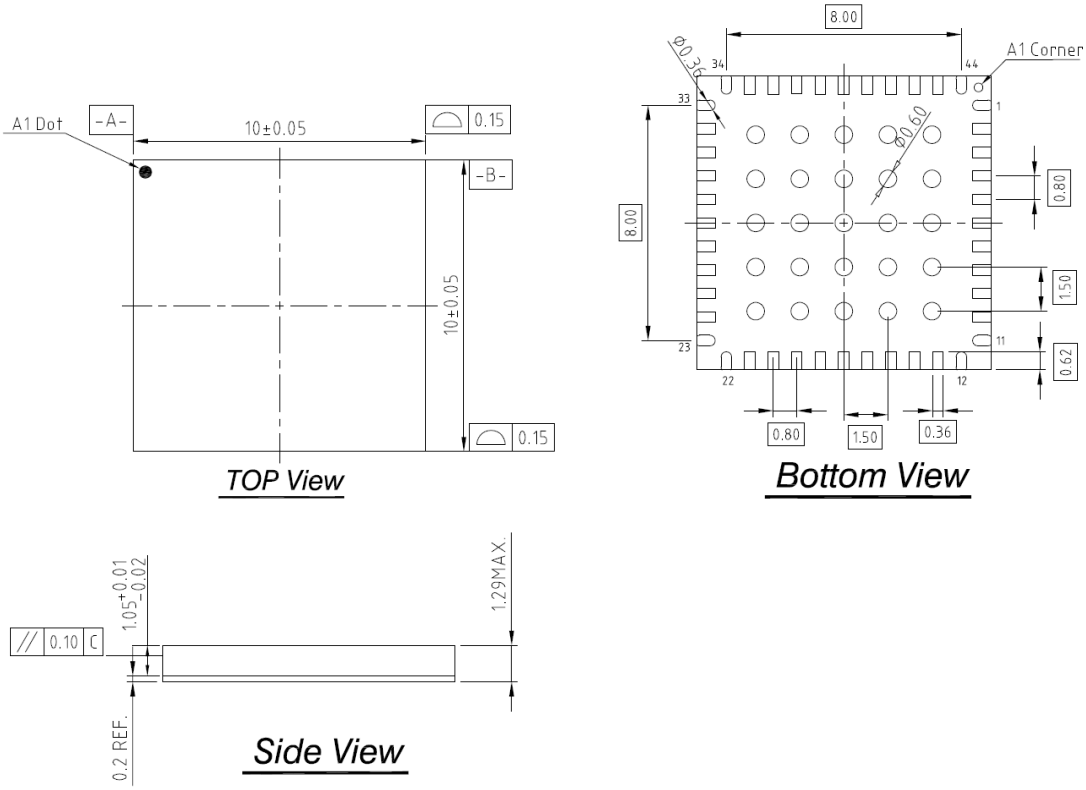
When using Venus838FLPx-L to replace Venus634FLPx, pin-45 ~ pin-69 can all be left unconnected.
When using Venus838FLPx-D, 1.2V need to be supplied at pin-56
The NC pins are to be left unconnected.

DC CHARACTERISTICS OF DIGITAL INTERFACE

Below is when VCC3I is at nominally 3.3V

Parameter	**Min.**	**Typ.**	**Max.**	**Units**
Input Low Voltage			0.8	Volt
Input High Voltage	2.0			Volt
Output Low Voltage, Iol = 4 ~ 7.8mA			0.4	Volt
Output High Voltage, Ioh = 4.6 ~ 15.4mA	2.4			Volt

MECHANICAL DIMENSION



RECOMMENDED PCB FOOTPRINT

Package size = 10 mm x 10mm x1.3 mm
Package Pad = 15 x 21 mil
Package Pitch= 0.8 mm

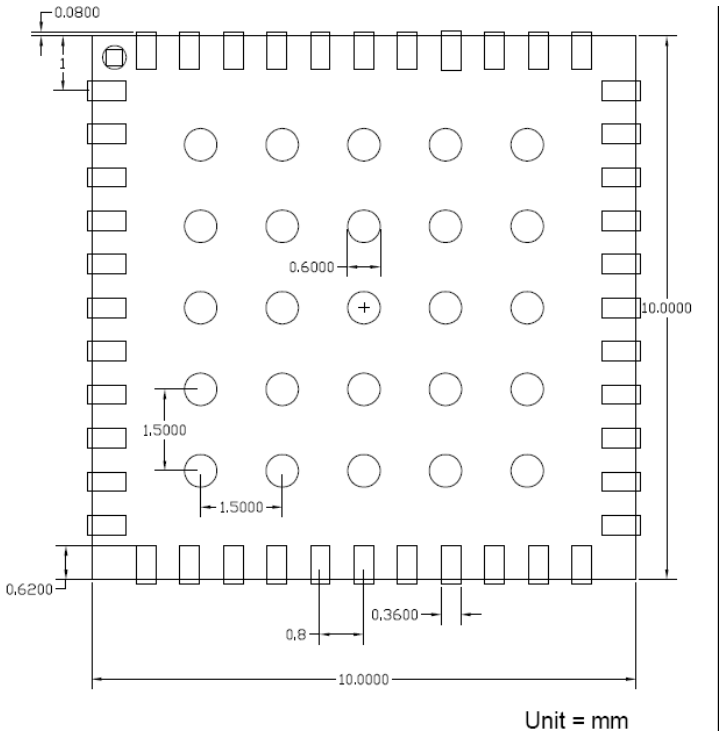
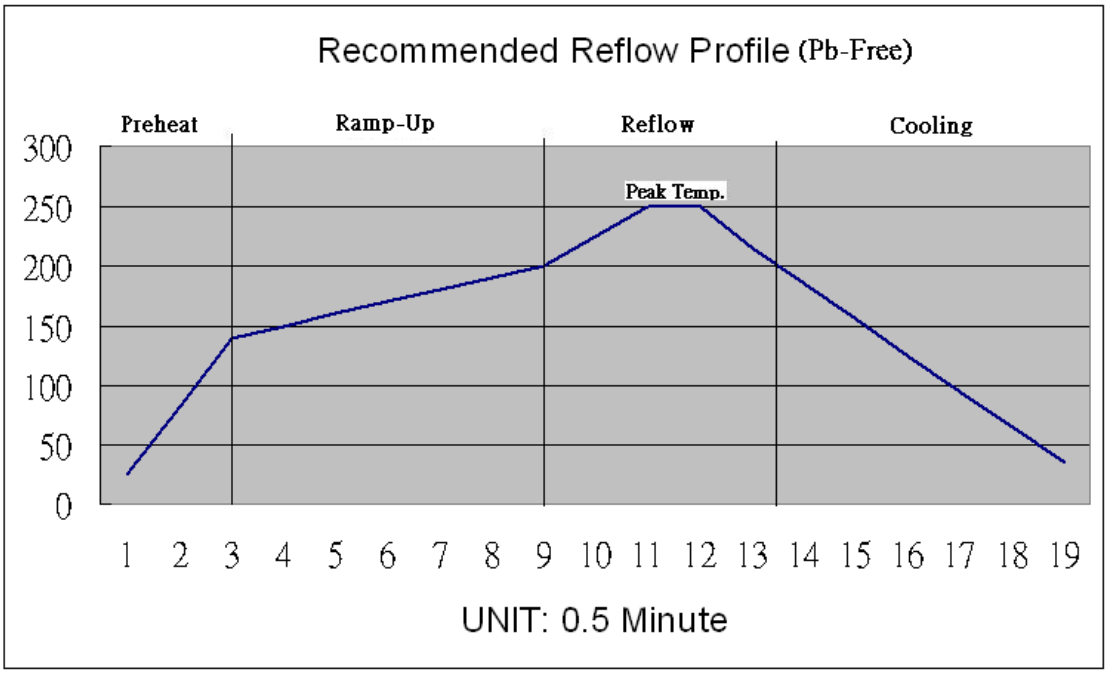


Figure-3 Recommended PCB Footprint.

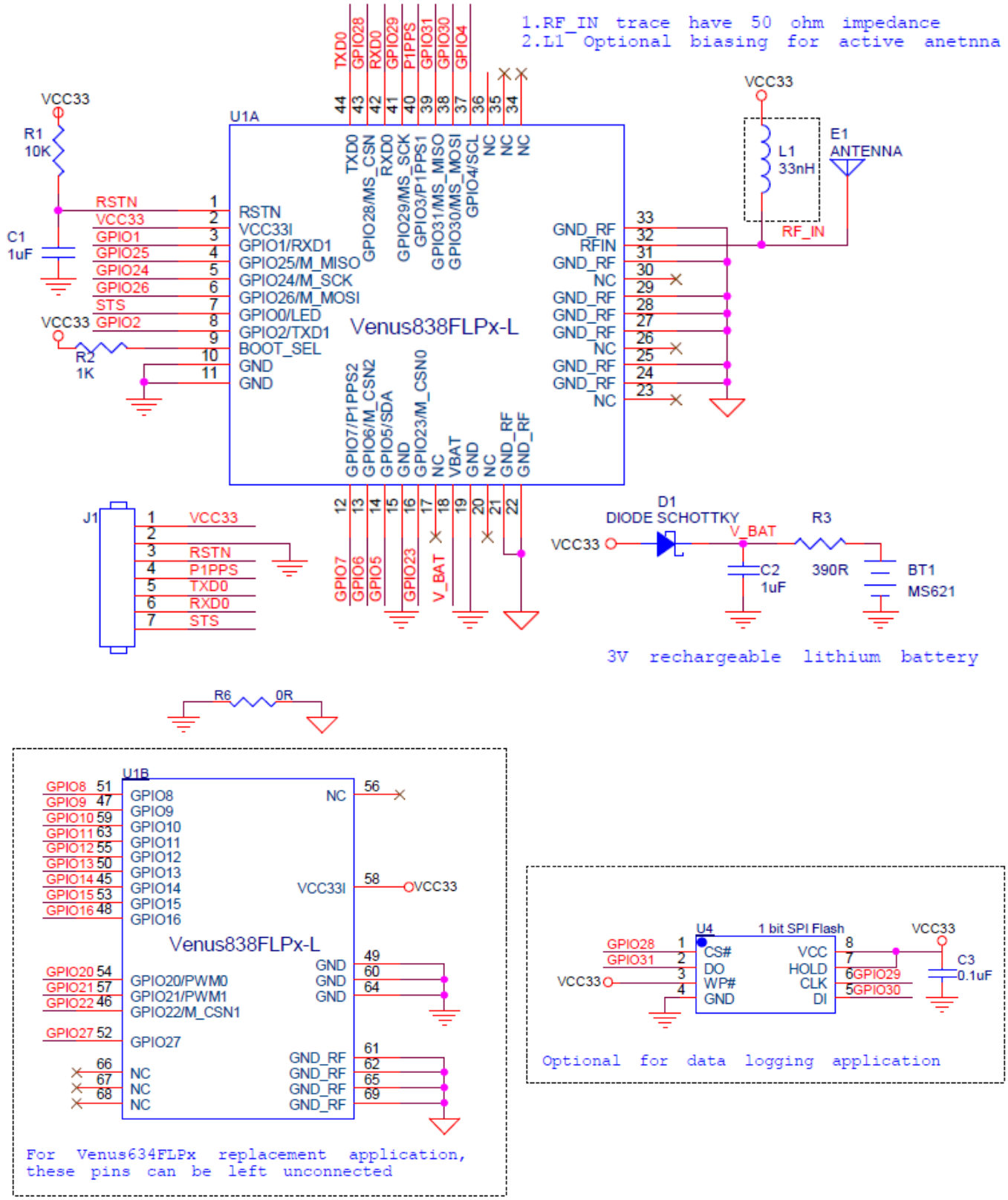
RECOMMENDED REFLOW PROFILE



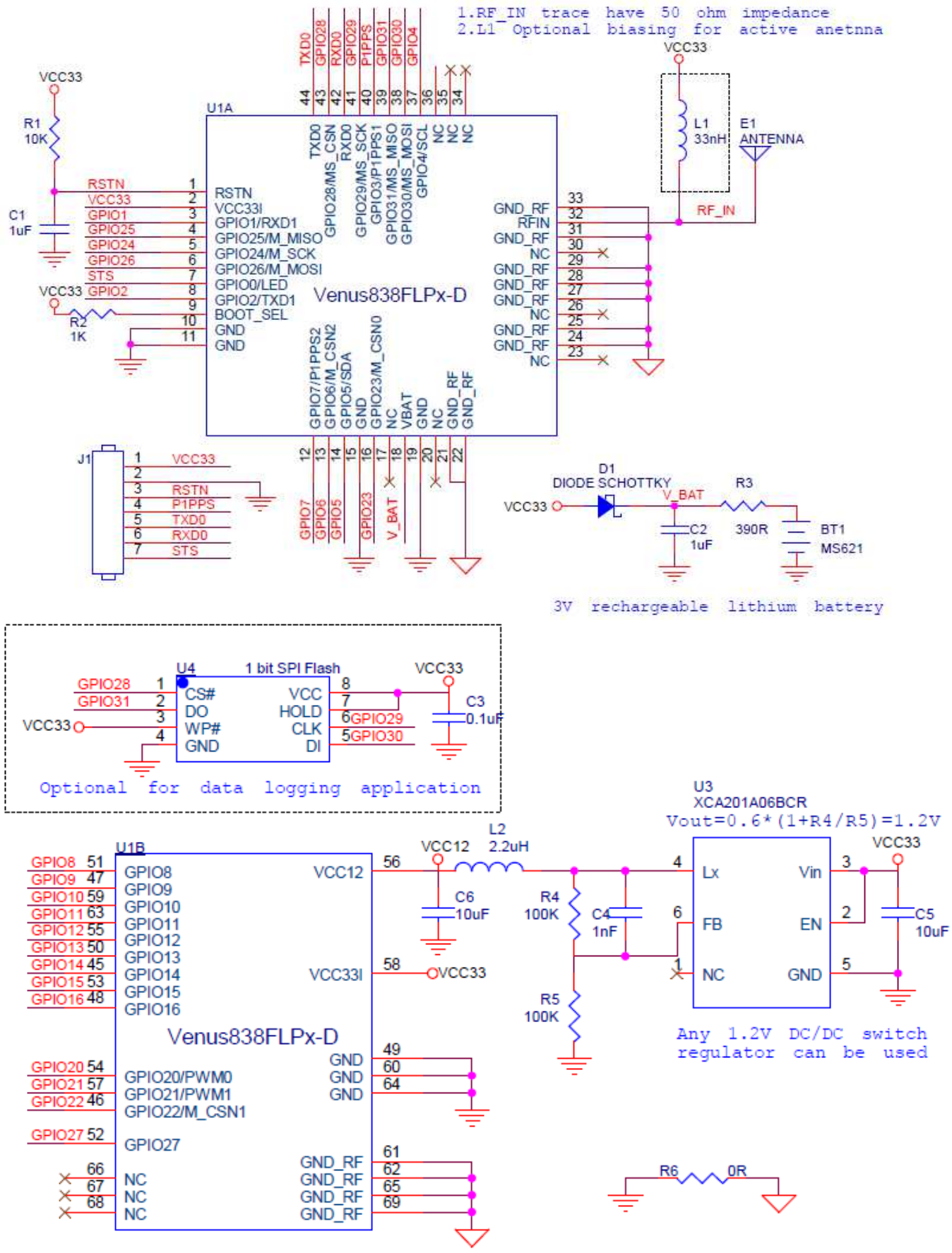
Temperature (℃)	25	82.5	140	150	160	170	180	190	200	225	250	250	215	185	155	125	95	65	35
Time(minute)	0	0.5	1	1.5	2	2.5	3	3.5	4	4.5	5	5.5	6	6.5	7	7.5	8	8.5	9

Profile Description	SnPb Eutectic Process	Lead Free Process
Preheat		
Maximum Temperature	100+/-10 ℃	140+/-10 ℃
Time(ΔT)	40~60s	50~70s
Ramp-Up		
Ramp-Up Rate	1 ℃/s Max.	1 ℃/s Max.
Time(ΔT)	120~150s	160~200s
Reflow		
Maximum Temperature	Peak Temp.	Peak Temp.
Minimum Temperature	180+/-5℃	200+/-10℃
Peak Temperature	220+/-2℃	250+/-2℃
Time(ΔT) during Peak Temp.+/-2℃	10~30s	20~40s
Reflow Time(ΔT)	120~150s	120~150s
Cooling		
Cooling Rate	1.5 ℃/s Max	1.5 ℃/s Max
Time(ΔT)	60~120s	150~180s

VENUS838FLPx-L APPLICATION CIRCUIT



VENUS838FLPx-D APPLICATION CIRCUIT



APPLICATION CIRCUIT INTERFACE SIGNALS

STS:	Signal to indicate GPS position status, 3.3V LVTTL. Active low for no-fix, toggle every second after position fix.
P1PPS:	1 pulse per second time-mark (3.3V LVTTL)
RSTN:	Active low reset input
VCC33:	3.3V power input
RXD0:	UART input (3.3V LVTTL)
TXD0:	UART output (3.3V LVTTL)

APPLICATION INFORMATION

1. For fast-rising power supply, a simple series R/C reset delay to pin-1, RSTN, as indicated in the application circuit is suitable. For system having slow-rising power supply, a reset IC providing 2~5ms reset duration may be necessary.

2. The RF input of Venus838FLPx is already matched to 50-ohm. Passive antenna matched to 50-ohm can be directly applied.

3. For using Venus838FLPx with active antenna, one with gain in range of 10~30dB and noise figure < 2dB can be used. Power to the active antenna needs to be applied externally.

4. Pin-18 VBAT supplies backup power to the real-time clock and backup SRAM for fast startup. For portable applications where there is battery with voltage in range of 2.5V ~ 3.6V as the main source, the VBAT pin can be directly connected to it. If VBAT is connected to main power as pin-2, no supply voltage as Venus838FLPx is powered off, then it'll cold start every time and GPS performance will not be optimal.

5. Like BGA device, the Venus838FLPx is moisture sensitive. It needs to be handled with care to void damage from moisture absorption and SMT re-flow. The device should be baked for 24 hours at 125-degC before mounting for SMT re-flow if it has been removed from the protective seal for more than 48[*1] hours.

6. If hot plug/remove power and UART serial interface, add at least 1K-ohm series resistor to pin-42 RXD0 and pin-44 TXD0 to improve ESD protection.

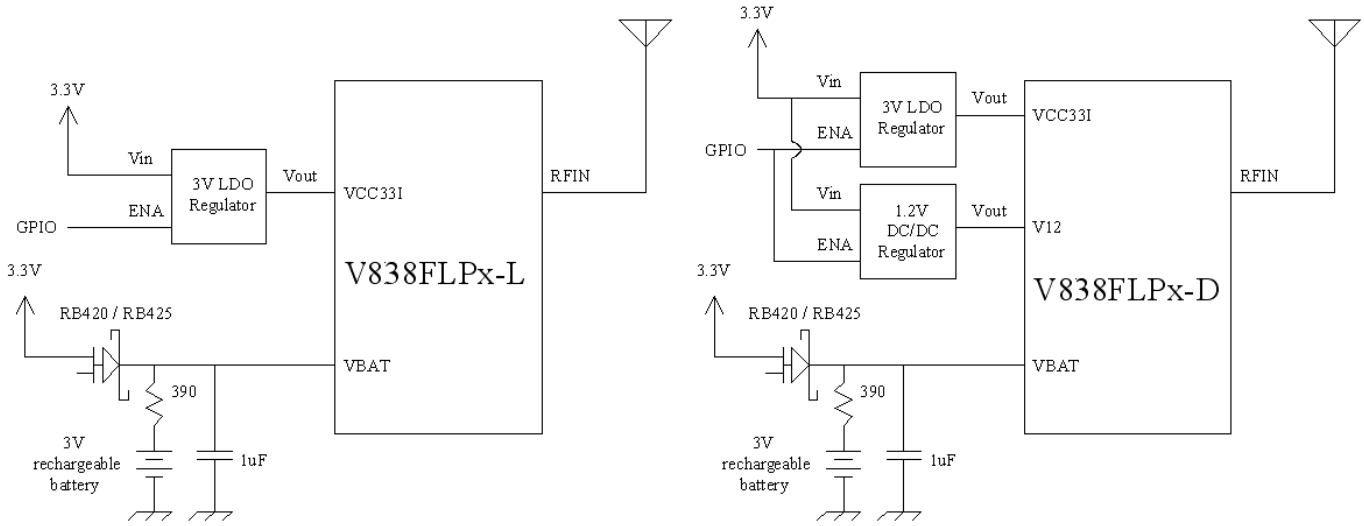
7. The supported SPI Flash memory verified for data logging application are:

Manufacturer	Device ID	Size
EON	EN25F040	4Mbit
EON	EN25F080	8Mbit
MXIC	MX25L400	4Mbit
MXIC	MX25L800	8Mbit
MXIC	MX25L1605	16Mbit
MXIC	MX25L3205	32Mbit
MXIC	MX25L6405	64Mbit
WINBOND	W25X40	4Mbit
WINBOND	W25X80	8Mbit
WINBOND	W25X16	16Mbit
WINBOND	W25X32	32Mbit
WINBOND	W25X64	64Mbit
SST	SST25LF040	4Mbit
SST	SST25LF080	8Mbit
SST	SST25VF016	16Mbit
SST	SST 25VF032	32Mbit

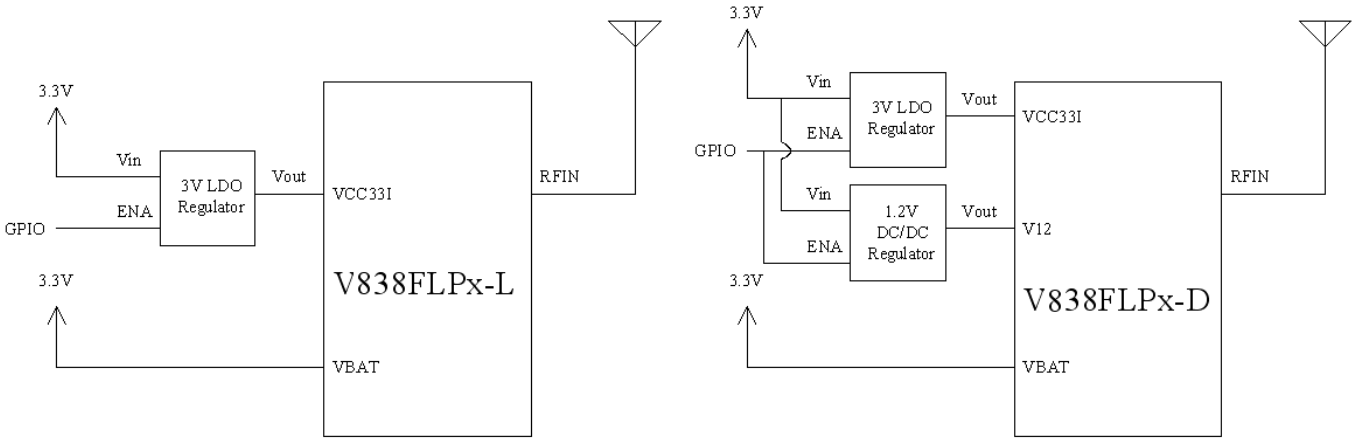
*1: Actual will be longer, moisture sensitivity level still undergoing verification.

SLEEP MODE

For application requiring sleep mode, it can be implemented using regulator with enable control as below figure shows. To put Venus838FLPx to sleep, the power to Venus838FLPx is cut off by disabling the regulator via host processor GPIO pin. In sleep mode, VBAT consume less than 40uA. Fast start up operation is provided by keeping supply voltage to VBAT constant, retaining the internal data and keep RTC running while Venus838FLPx is put to sleep or when supply 3.3V power is removed.

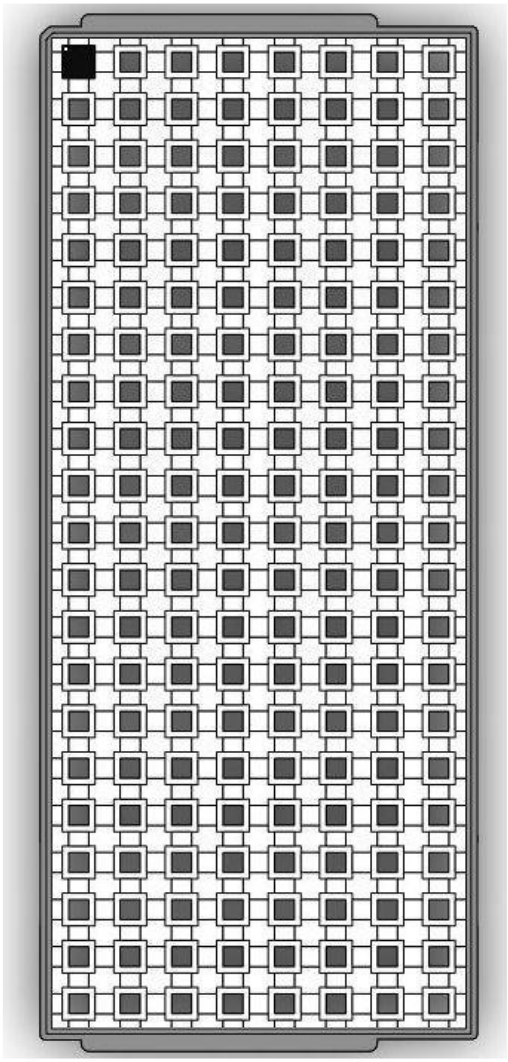


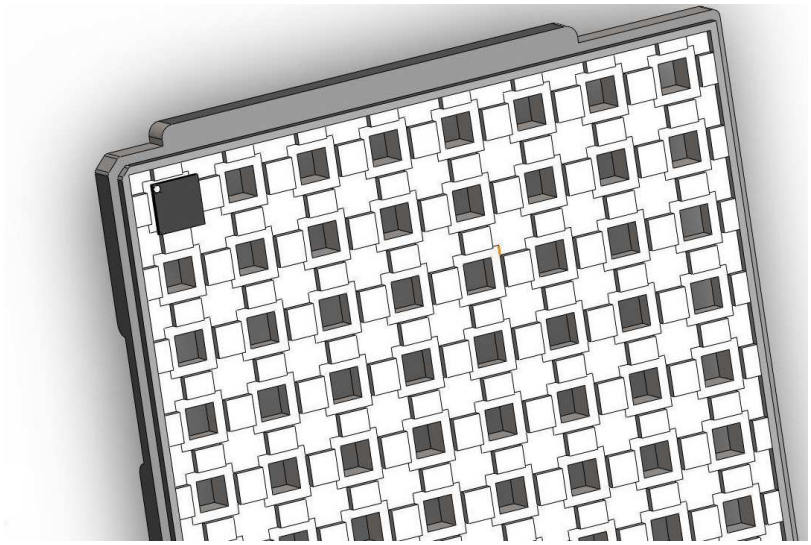
For applications needing sleep mode but cannot have extra cost of adding a rechargeable backup supply battery, it can be implemented as below figure shows. It will provide fast start up when Venus838FLPx is put to sleep and awakened, but will cold start every time when the 3.3V supply voltage is removed and re-applied again.



When using sleep mode, add 10K ~ 20K series resistor on pin-42 RXD0 to reduce leakage current.

PACKAGE





NMEA MESSAGES

The full descriptions of supported NMEA messages are provided at the following paragraphs.

GGA - Global Positioning System Fix Data

Time, position and fix related data for a GPS receiver.

Structure:

$GPGGA,hhmmss.sss,ddmm.mmmm,a,dddmm.mmmm,a,x,xx,x.x,x.x,M,,,,xxxx*hh<CR><LF>

1 2 3 4 5 6 7 8 9 10 11

Example:

$GPGGA,111636.932,2447.0949,N,12100.5223,E,1,11,0.8,118.2,M,,,,0000*02<CR><LF>

Field	Name	Example	Description
1	UTC Time	111636.932	UTC of position in hhmmss.sss format, (000000.000 ~ 235959.999)
2	Latitude	2447.0949	Latitude in ddmm.mmmm format Leading zeros transmitted
3	N/S Indicator	N	Latitude hemisphere indicator, 'N' = North, 'S' = South
4	Longitude	12100.5223	Longitude in dddmm.mmmm format Leading zeros transmitted
5	E/W Indicator	E	Longitude hemisphere indicator, 'E' = East, 'W' = West
6	GPS quality indicator	1	GPS quality indicator 0: position fix unavailable 1: valid position fix, SPS mode 2: valid position fix, differential GPS mode 3: GPS PPS Mode, fix valid 4: Real Time Kinematic. System used in RTK mode with fixed integers 5: Float RTK. Satellite system used in RTK mode. Floating integers 6: Estimated (dead reckoning) Mode 7: Manual Input Mode 8: Simulator Mode
7	Satellites Used	11	Number of satellites in use, (00 ~ 12)
8	HDOP	0.8	Horizontal dilution of precision, (00.0 ~ 99.9)
9	Altitude	108.2	mean sea level (geoid), (-9999.9 ~ 17999.9)
10	DGPS Station ID	0000	Differential reference station ID, 0000 ~ 1023 NULL when DGPS not used
11	Checksum	02	

GLL – Latitude/Longitude

Latitude and longitude of current position, time, and status.

Structure:

$GPGLL,ddmm.mmmm,a,dddmm.mmmm,a,hhmmss.sss,A,a*hh<CR><LF>

1 2 3 4 5 6 7 8

Example:

$GPGLL,2447.0944,N,12100.5213,E,112609.932,A,A*57<CR><LF>

Field	Name	Example	Description
1	Latitude	2447.0944	Latitude in ddmm.mmmm format Leading zeros transmitted
2	N/S Indicator	N	Latitude hemisphere indicator 'N' = North 'S' = South
3	Longitude	12100.5213	Longitude in dddmm.mmmm format Leading zeros transmitted
4	E/W Indicator	E	Longitude hemisphere indicator 'E' = East 'W' = West
5	UTC Time	112609.932	UTC time in hhmmss.sss format (000000.000 ~ 235959.999)
6	Status	A	Status, 'A' = Data valid, 'V' = Data not valid
7	Mode Indicator	A	Mode indicator 'N' = Data not valid 'A' = Autonomous mode 'D' = Differential mode 'E' = Estimated (dead reckoning) mode 'M' = Manual input mode 'S' = Simulator mode
8	Checksum	57	

GSA – GNSS DOP and Active Satellites

GPS receiver operating mode, satellites used in the navigation solution reported by the GGA or GNS sentence and DOP values.

Structure:

$GPGSA,A,x,xx,xx,xx,xx,xx,xx,xx,xx,xx,xx,xx,xx,x.x,x.x,x.x*hh<CR><LF>

1 2 3 3 3 3 3 3 3 3 3 3 3 3 4 5 6 7

Example:

$GPGSA,A,3,05,12,21,22,30,09,18,06,14,01,31,,1.2,0.8,0.9*36<CR><LF>

Field	Name	Example	Description
1	Mode	A	Mode 'M' = Manual, forced to operate in 2D or 3D mode 'A' = Automatic, allowed to automatically switch 2D/3D
2	Mode	3	Fix type 1 = Fix not available 2 = 2D 3 = 3D
3	Satellite used 1~12	05,12,21,22,30,09,18,06,14,01,31,,	Satellite ID number, 01 to 32, of satellite used in solution, up to 12 transmitted
4	PDOP	1.2	Position dilution of precision (00.0 to 99.9)
5	HDOP	0.8	Horizontal dilution of precision (00.0 to 99.9)
6	VDOP	0.9	Vertical dilution of precision (00.0 to 99.9)
7	Checksum	36	

GSV – GNSS Satellites in View

Number of satellites (SV) in view, satellite ID numbers, elevation, azimuth, and SNR value. Four satellites maximum per transmission.

Structure:

$GPGSV,x,x,xx,xx,xx,xxx,xx,…,xx,xx,xxx,xx *hh<CR><LF>

1 2 3 4 5 6 7 4 5 6 7 8

Example:

$GPGSV,3,1,12,05,54,069,45,12,44,061,44,21,07,184,46,22,78,289,47*72<CR><LF>

$GPGSV,3,2,12,30,65,118,45,09,12,047,37,18,62,157,47,06,08,144,45*7C<CR><LF>

$GPGSV,3,3,12,14,39,330,42,01,06,299,38,31,30,256,44,32,36,320,47*7B<CR><LF>

Field	Name	Example	Description
1	Number of message	3	Total number of GSV messages to be transmitted (1-3)
2	Sequence number	1	Sequence number of current GSV message
3	Satellites in view	12	Total number of satellites in view (00 ~ 12)
4	Satellite ID	05	Satellite ID number, GPS: 01 ~ 32, SBAS: 33 ~ 64 (33 = PRN120)
5	Elevation	54	Satellite elevation in degrees, (00 ~ 90)
6	Azimuth	069	Satellite azimuth angle in degrees, (000 ~ 359)
7	SNR	45	C/No in dB (00 ~ 99) Null when not tracking
8	Checksum	72	

RMC – Recommended Minimum Specific GNSS Data

Time, date, position, course and speed data provided by a GNSS navigation receiver.

Structure:

$GPRMC,hhmmss.sss,A,dddmm.mmmm,a,dddmm.mmmm,a,x.x,x.x,ddmmyy,,,a*hh<CR><LF>

1 2 3 4 5 6 7 8 9 10 11

Example:

$GPRMC,111636.932,A,2447.0949,N,12100.5223,E,000.0,000.0,030407,,,A*61<CR><LF>

Field	Name	Example	Description
1	UTC time	0111636.932	UTC time in hhmmss.sss format (000000.00 ~ 235959.999)
2	Status	A	Status 'V' = Navigation receiver warning 'A' = Data Valid
3	Latitude	2447.0949	Latitude in dddmm.mmmm format Leading zeros transmitted
4	N/S indicator	N	Latitude hemisphere indicator 'N' = North 'S' = South
5	Longitude	12100.5223	Longitude in dddmm.mmmm format Leading zeros transmitted
6	E/W Indicator	E	Longitude hemisphere indicator 'E' = East 'W' = West
7	Speed over ground	000.0	Speed over ground in knots (000.0 ~ 999.9)
8	Course over ground	000.0	Course over ground in degrees (000.0 ~ 359.9)
9	UTC Date	030407	UTC date of position fix, ddmmyy format
10	Mode indicator	A	Mode indicator 'N' = Data not valid 'A' = Autonomous mode 'D' = Differential mode 'E' = Estimated (dead reckoning) mode 'M' = Manual input mode 'S' = Simulator mode
11	checksum	61	

VTG – Course Over Ground and Ground Speed

The Actual course and speed relative to the ground.

Structure:

GPVTG,x.x,T,,M,x.x,N,x.x,K,a*hh<CR><LF>

1 2 3 4 5

Example:

$GPVTG, 000.0,T,,M,000.0,N,0000.0,K,A*3D<CR><LF>

Field	Name	Example	Description
1	Course	000.0	True course over ground in degrees (000.0 ~ 359.9)
2	Speed	000.0	Speed over ground in knots (000.0 ~ 999.9)
3	Speed	0000.0	Speed over ground in kilometers per hour (0000.0 ~ 1800.0)
4	Mode	A	Mode indicator 'N' = not valid 'A' = Autonomous mode 'D' = Differential mode 'E' = Estimated (dead reckoning) mode 'M' = Manual input mode 'S' = Simulator mode
5	Checksum	3D	

ZDA – Time & Date

UTC, day, month, year and local time zone.

Structure:

$GPZDA,hhmmss.sss,xx,xx,xxxx,xx,xx*hh<CR><LF>

1 2 3 4 5 6 7

Example:

$GPZDA,052633.376,13,07,2012,00,00*51<CR><LF>

Field	Name	Example	Description
1	UTC time	0111636.932	UTC time in hhmmss.sss format (000000.000 ~ 235959.999)
2	Day	13	Day, 01 to 31
3	Month	07	Month, 01 to 12
4	Year	2012	Year in yyyy format
5	Local zone hours	00	Local zone hours, 00 to +/- 13 hrs
6	Local zone minutes	00	Local zone minutes, 00 to +59
7	checksum	51	

ORDERING INFORMATION

Part Number	Description
Venus838FLPx-L	Flash version GPS receiver (internal 1.2V LDO version)
Venus838FLPx-D	Flash version GPS receiver (external 1.2V version)

SkyTraq Technology, Inc.
4F, No.26, Minsiang Street, Hsinchu, Taiwan, 300
Phone: +886 3 5678650
Fax: +886 3 5678680
Email: info@skytraq.com.tw

Change Log

Version 0.5, April 16, 2014

1. Updated current consumption number with respect to number of search engine used.

Version 0.4, March 7, 2014

2. Pin-36 changed to NC

Version 0.3, February 24, 2014

3. Updated DC characteristics
4. Added ZDA

Version 0.2, February 19, 2014

1. Fixed RF input schematic error
2. Updated VBAT description

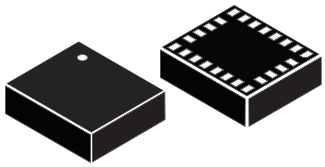
Version 0.1, December 25, 2013

1. Initial release

LSM9DS1

iNEMO inertial module: 3D accelerometer, 3D gyroscope, 3D magnetometer

Datasheet - production data



LGA-24L (3.5x3x1.0 mm)

Features

- 3 acceleration channels, 3 angular rate channels, 3 magnetic field channels
- ±2/±4/±8/±16 *g* linear acceleration full scale
- ±4/±8/±12/±16 gauss magnetic full scale
- ±245/±500/±2000 dps angular rate full scale
- 16-bit data output
- SPI / I^2C serial interfaces
- Analog supply voltage 1.9 V to 3.6 V
- “Always-on” eco power mode down to 1.9 mA
- Programmable interrupt generators
- Embedded temperature sensor
- Embedded FIFO
- Position and motion detection functions
- Click/double-click recognition
- Intelligent power saving for handheld devices
- ECOPACK®, RoHS and “Green” compliant

Applications

- Indoor navigation
- Smart user interfaces
- Advanced gesture recognition
- Gaming and virtual reality input devices
- Display/map orientation and browsing

Description

The LSM9DS1 is a system-in-package featuring a 3D digital linear acceleration sensor, a 3D digital angular rate sensor, and a 3D digital magnetic sensor.

The LSM9DS1 has a linear acceleration full scale of ±2*g*/±4*g*/±8/±16 *g,* a magnetic field full scale of ±4/±8/±12/±16 gauss and an angular rate of ±245/±500/±2000 dps.

The LSM9DS1 includes an I^2C serial bus interface supporting standard and fast mode (100 kHz and 400 kHz) and an SPI serial standard interface.

Magnetic, accelerometer and gyroscope sensing can be enabled or set in power-down mode separately for smart power management.

The LSM9DS1 is available in a plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Part number	Temperature range [°C]	Package	Packing
LSM9DS1	-40 to +85	LGA-24L	Tray
LSM9DS1TR	-40 to +85	LGA-24L	Tape and reel

Contents

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List of figures

1 Pin description

Figure 1. Pin connections

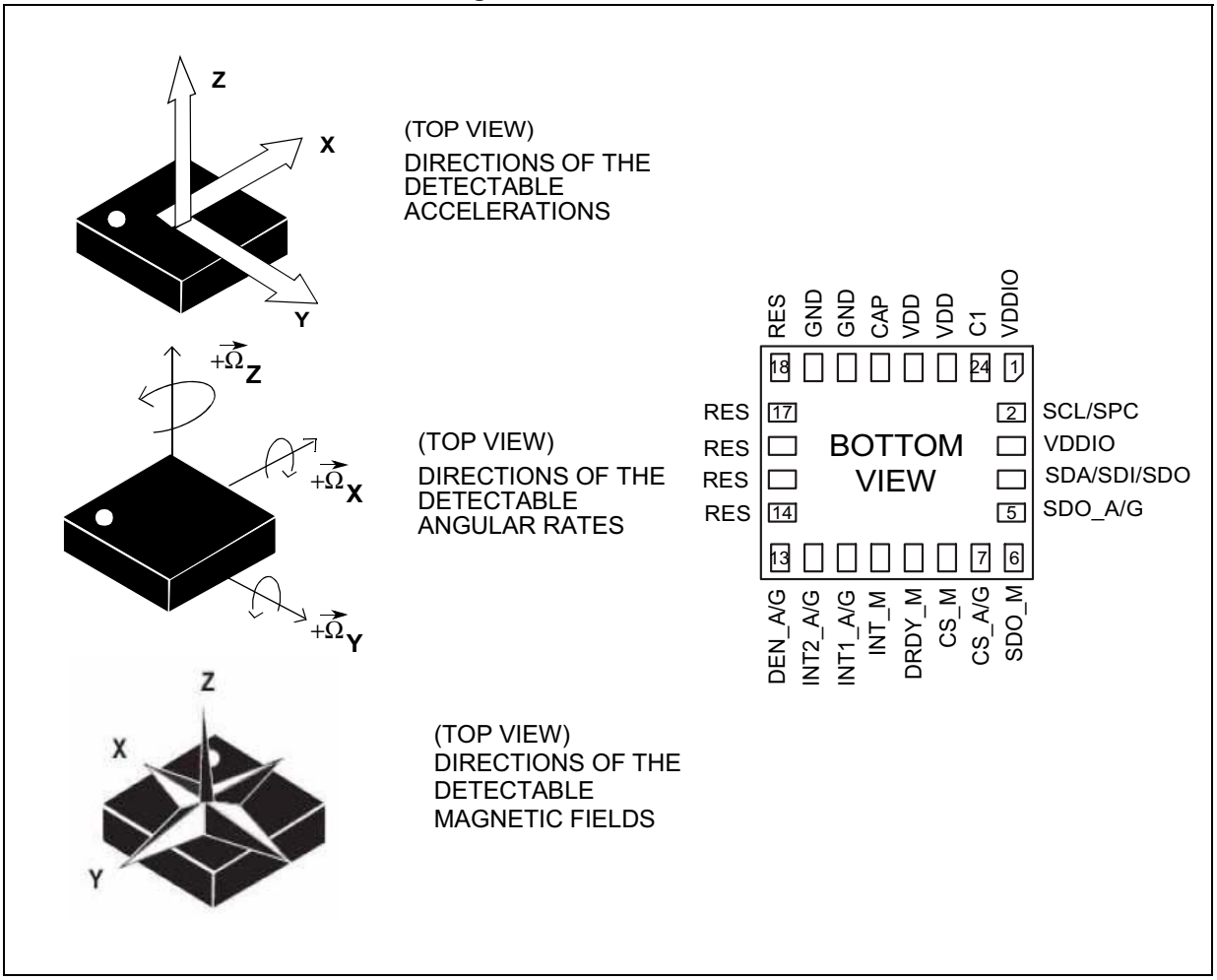


Table 2. Pin description

Pin #	Name	Function
1	VDDIO(1)	Power supply for I/O pins
2	SCL/SPC	I^2C serial clock (SCL) / SPI serial port clock (SPC)
3	VDDIO(2)	Power supply for I/O pins
4	SDA/SDI/SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	SDO_A/G	SPI serial data output (SDO) for the accelerometer and gyroscope I^2C least significant bit of the device address (SA0) for the accelerometer and gyroscope
6	SDO_M	SPI serial data output (SDO) for the magnetometer I^2C least significant bit of the device address (SA0) for the magnetometer
7	CS_A/G	SPI enable I^2C/SPI mode selection for the accelerometer and gyroscope (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
8	CS_M	SPI enable I^2C/SPI mode selection for the magnetometer (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
9	DRDY_M	Magnetic sensor data ready
10	INT_M	Magnetic sensor interrupt
11	INT1_A/G	Accelerometer and gyroscope interrupt 1
12	INT2_A/G	Accelerometer and gyroscope interrupt 2
13	DEN_A/G	Accelerometer and gyroscope data enable
14	RES	Reserved. Connected to GND.
15	RES	Reserved. Connected to GND.
16	RES	Reserved. Connected to GND.
17	RES	Reserved. Connected to GND.
18	RES	Reserved. Connected to GND.
19	GND	0 V supply
20	GND	0 V supply
21	CAP	Connected to GND with ceramic capacitor(3)
22	VDD(4)	Power supply
23	VDD(5)	Power supply
24	C1	Capacitor connection (C1 = 100 nF)

1. Recommended 100 nF filter capacitor.
2. Recommended 100 nF filter capacitor.
3. 10 nF (±10%), 16 V. 1 nF minimum value has to be guaranteed under 11 V bias condition.
4. Recommended 100 nF plus 10 µF capacitors.
5. Recommended 100 nF plus 10 µF capacitors.

2 Module specifications

2.1 Sensor characteristics

@ Vdd = 2.2 V, T = 25 °C unless otherwise noted[a]

Table 3. Sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range			±2		*g*
				±4		
				±8		
				±16		
M_FS	Magnetic measurement range			±4		gauss
				±8		
				±12		
				±16		
G_FS	Angular rate measurement range			±245		dps
				±500		
				±2000		
LA_So	Linear acceleration sensitivity	Linear acceleration FS = ±2 *g*		0.061		m*g*/LSB
		Linear acceleration FS = ±4 *g*		0.122		
		Linear acceleration FS = ±8 *g*		0.244		
		Linear acceleration FS = ±16 *g*		0.732		
M_GN	Magnetic sensitivity	Magnetic FS = ±4 gauss		0.14		mgauss/ LSB
		Magnetic FS = ±8 gauss		0.29		
		Magnetic FS = ±12 gauss		0.43		
		Magnetic FS = ±16 gauss		0.58		
G_So	Angular rate sensitivity	Angular rate FS = ±245 dps		8.75		mdps/ LSB
		Angular rate FS = ±500 dps		17.50		
		Angular rate FS = ±2000 dps		70		
LA_TyOff	Linear acceleration typical zero-g level offset accuracy[2]	FS = ±8 *g*		±90		m*g*
M_TyOff	Zero-gauss level [3]	FS = ±4 gauss		±1		gauss
G_TyOff	Angular rate typical zero-rate level [4]	FS = ±2000 dps		±30		dps
M_DF	Magnetic disturbance field	Zero-gauss offset starts to degrade			50	gauss
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed
2. Typical zero-*g* level offset value after soldering
3. Typical zero-gauss level value after test and trimming
4. Typical zero rate level offset value after MSL3 preconditioning

a. The product is factory calibrated at 2.2 V. The operational power supply range is from 1.9 V to 3.6 V.

2.2 Electrical characteristics

@ Vdd = 2.2 V, T = 25 °C unless otherwise noted[b]

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		1.9		3.6	V
Vdd_IO	Module power supply for I/O		1.71		Vdd+0.1	
Idd_XM	Current consumption of the accelerometer and magnetic sensor in normal mode (2)			600		µA
Idd_G	Gyroscope current consumption in normal mode(3)			4.0		mA
Top	Operating temperature range		-40		+85	°C
Trise	Time for power supply rising(4)		0.01		100	ms
Twait	Time delay between Vdd_IO and Vdd(4)		0		10	ms

1. Typical specifications are not guaranteed
2. Magnetic sensor in high-resolution mode (ODR = 20 Hz), accelerometer sensor in normal mode, gyroscope in power-down mode
3. Accelerometer and magnetic sensor in power-down mode
4. Please refer to *Section 2.2.1: Recommended power-up sequence* for more details.

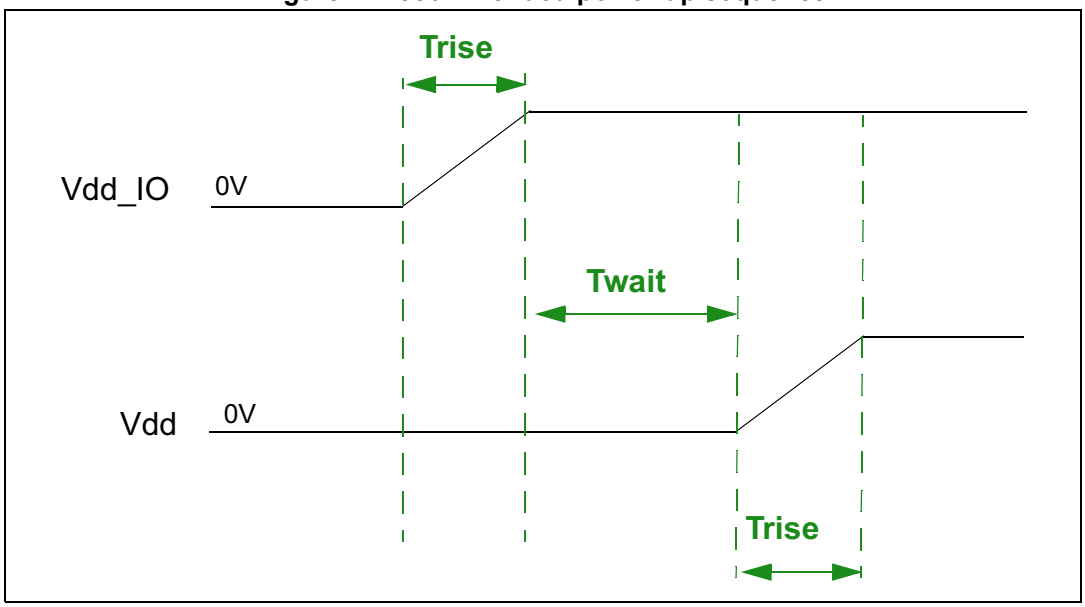
b. LSM9DS1 is factory calibrated at 2.2 V.

2.2.1 Recommended power-up sequence

For the power-up sequence please refer to the following figure, where:

- Trise is the time for the power supply to rise from 10% to 90% of its final value
- Twait is the delay between the end of the Vdd_IO ramp (90% of its final value) and the start of the Vdd ramp

Figure 2. Recommended power-up sequence



2.3 Temperature sensor characteristics

@ Vdd = 2.2 V, T = 25 °C unless otherwise noted [c]

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
TODR	Temperature refresh rate	Gyro OFF(2)		50		Hz
		Gyro ON		59.5		
TSen	Temperature sensitivity(3)			16		LSB/°C
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. When the accelerometer ODR is set to 10 Hz and the gyroscope part is turned off, the TODR value is 10 Hz.
3. The output of the temperature sensor is 0 (typ.) at 25 °C

c. The product is factory calibrated at 2.2 V.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

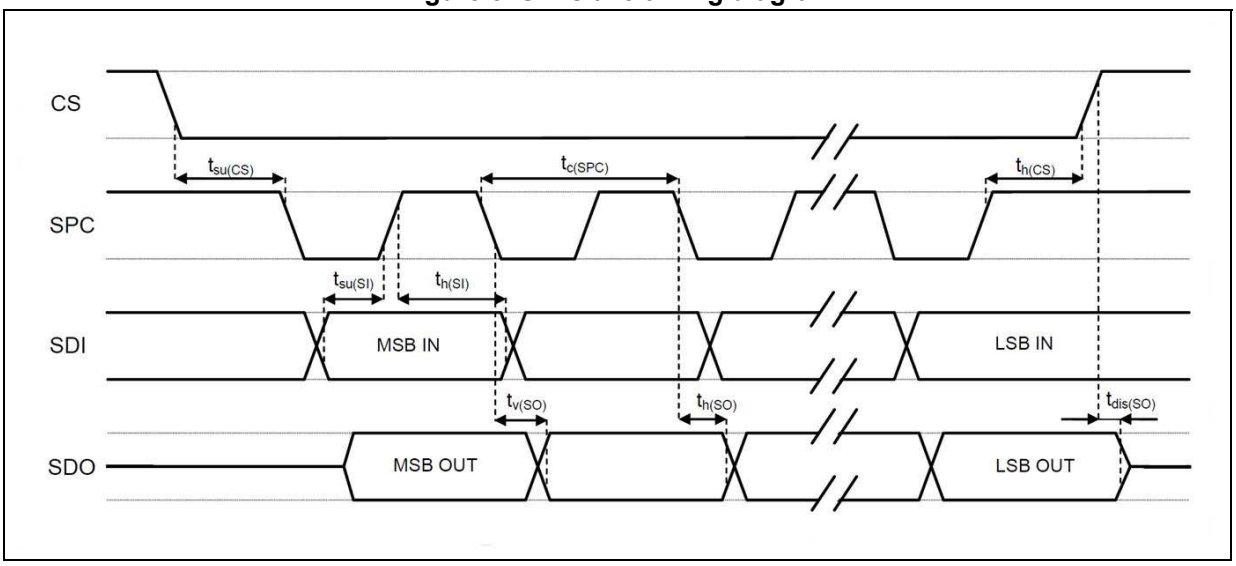
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

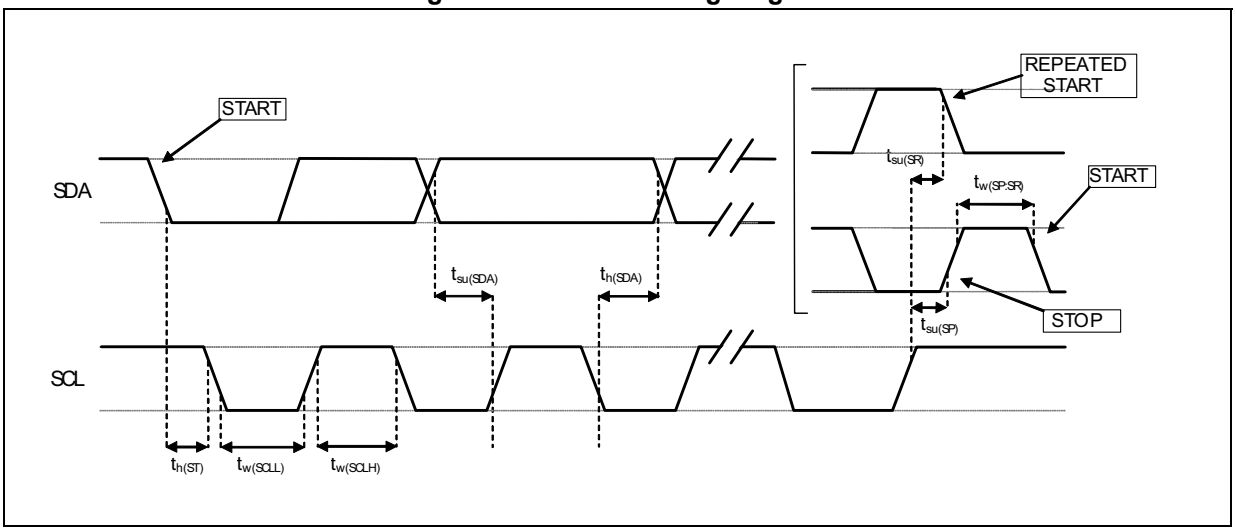
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C Standard mode(1)		I²C Fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports

2.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (including CS_A/G, CS_M, SCL/SPC, SDA/SDI/SDO, SDO_A/G, SDO_M)	0.3 to Vdd_IO +0.3	V
A_{UNP}	Acceleration (any axis)	3,000 for 0.5 ms	g
		10,000 for 0.1 ms	g
M_{EF}	Maximum exposed field	1000	gauss
ESD	Electrostatic discharge protection (HBM)	2	kV
T_{STG}	Storage temperature range	-40 to +125	°C

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

2.6 Terminology

2.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors.

An angular rate gyroscope is device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

Magnetic sensor sensitivity describes the gain of the sensor and can be determined, for example, by applying a magnetic field of 1 *gauss* to it.

2.6.2 Zero-*g*, zero-rate and zero-*gauss* level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on both the X-axis and Y-axis, whereas the Z-axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in *Table 3*. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

Zero-*g*auss level offset (M_TyOff) describes the deviation of an actual output signal from the ideal output if no magnetic field is present.

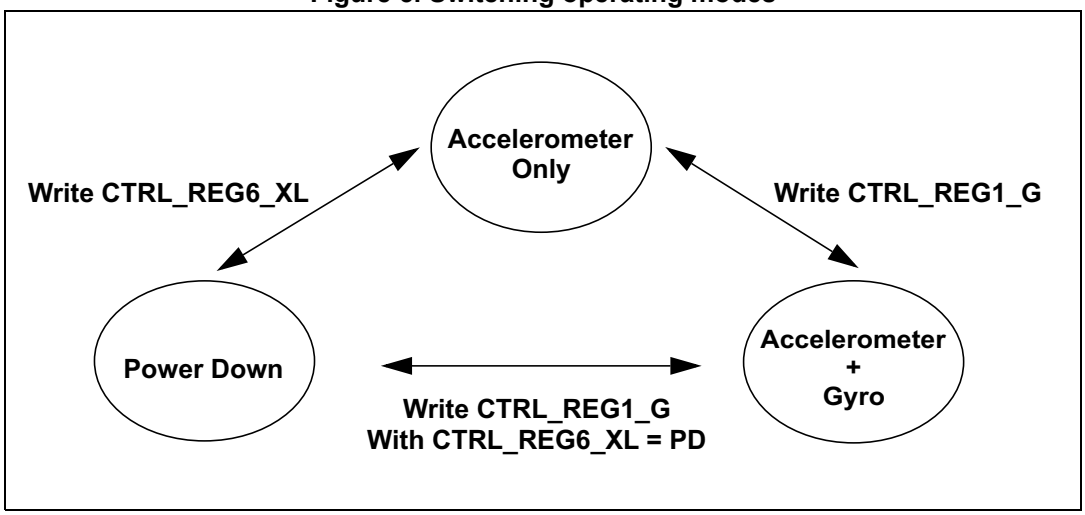
3 LSM9DS1 functionality

3.1 Operating modes

In the LSM9DS1 the accelerometer and gyroscope have two operating modes available: only accelerometer active and gyroscope in power down or both accelerometer and gyroscope sensors active at the same ODR. Switching from one mode to the other requires one write operation: writing to *CTRL_REG6_XL (20h)*, the accelerometer operates in normal mode and the gyroscope is powered down, writing to *CTRL_REG1_G (10h)* both accelerometer and gyroscope are activated at the same ODR.

Figure 5 depicts both modes of operation from power down.

Figure 5. Switching operating modes



The magnetic sensor has three operating modes available: power-down (default), continuous-conversion mode and single-conversion mode. Switching from power-down to the other modes requires one write operation to *CTRL_REG3_M (22h)*, setting values in the MD[1:0] bits. For the output of the magnetic data compensated by temperature, the TEMP_COMP bit in *CTRL_REG1_M (20h)* must be set to '1'.

3.2 Gyroscope power modes

In the LSM9DS1, the gyroscope can be configured in three different operating modes: power-down, low-power and normal mode.

Low-power mode is available for lower ODR (14.9, 59.5, 119 Hz) while for greater ODR (238, 476, 952 Hz) the device is automatically in normal mode. *Table* summarizes the ODR configuration (ODR_G[2:0] bits set in *CTRL_REG1_G (10h)*) and corresponding power modes.

To enable low-power mode, the LP_mode bit in *CTRL_REG3_G (12h)* has to be set to '1'.

Low-power mode allows reaching low power consumption while maintaining the device always on, refer to *Table 10*.

Table 9. Gyroscope operating modes

ODR_G [2:0]	ODR [Hz]	Power mode
000	Power down	Power-down
001	14.9	Low-power/Normal mode
010	59.5	Low-power/Normal mode
011	119	Low-power/Normal mode
100	238	Normal mode
101	476	Normal mode
110	952	Normal mode

Table 10. Operating mode current consumption

ODR [Hz]	Power mode	Current consumption(1) [mA]
14.9	Low-power	1.9
59.5	Low-power	2.4
119	Low-power	3.1
238	Normal mode	4.3
476	Normal mode	4.3
952	Normal mode	4.3

1. Typical values of gyroscope and accelerometer current consumption are based on characterization data.

Table 11. Accelerometer turn-on time

ODR [Hz]	BW = 400 Hz(1)	BW = 200 Hz(1)	BW = 100 Hz(1)	BW = 50 Hz(1)
14.9	0	0	0	0
59.5	0	0	0	0
119	1	1	1	2
238	1	1	2	4
476	1	2	4	7
952	2	4	7	14

1. The table contains the number of samples to be discarded after switching between power-down mode and normal mode.

Table 12. Gyroscope turn-on time

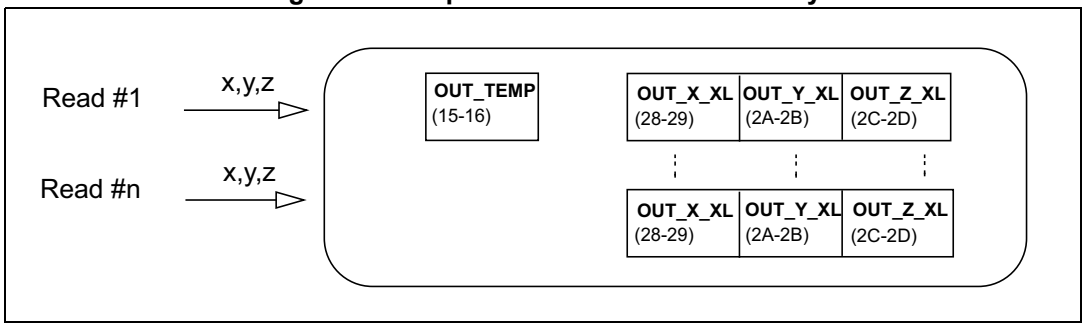
ODR [Hz]	LPF1 only(1)	LPF1 and LPF2(1)
14.9	2	LPF2 not available
59.5 or 119	3	13
238	4	14
476	5	15
952	8	18

1. The table contains the number of samples to be discarded after switching between low-power mode and normal mode.

3.3 Accelerometer and gyroscope multiple reads (burst)

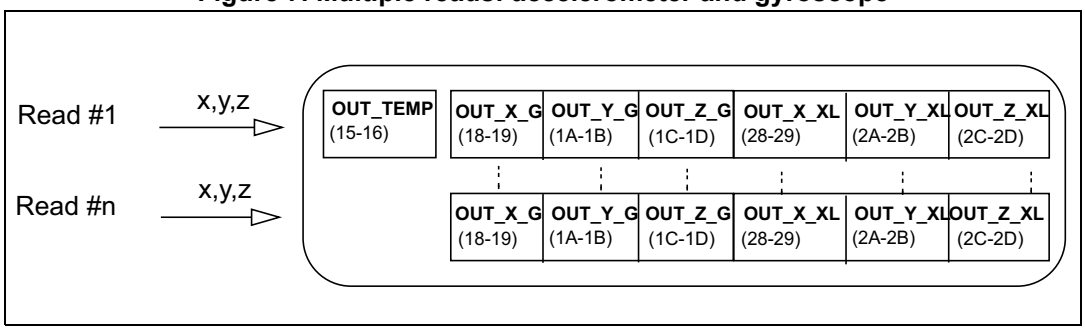
When only accelerometer is activated and the gyroscope is in power down, starting from *OUT_X_XL (28h - 29h)* multiple reads can be performed. Once *OUT_Z_XL (2Ch - 2Dh)* is read, the system automatically restarts from *OUT_X_XL (28h - 29h)* (see *Figure 6*).

Figure 6. Multiple reads: accelerometer only



When both accelerometer and gyroscope sensors are activated at the same ODR, starting from *OUT_X_G (18h - 19h)* multiple reads can be performed. Once *OUT_Z_XL (2Ch - 2Dh)* is read, the system automatically restarts from *OUT_X_G (18h - 19h)* (see *Figure 7*).

Figure 7. Multiple reads: accelerometer and gyroscope



3.4 Block diagram

Figure 8. Accelerometer and gyroscope digital block diagram

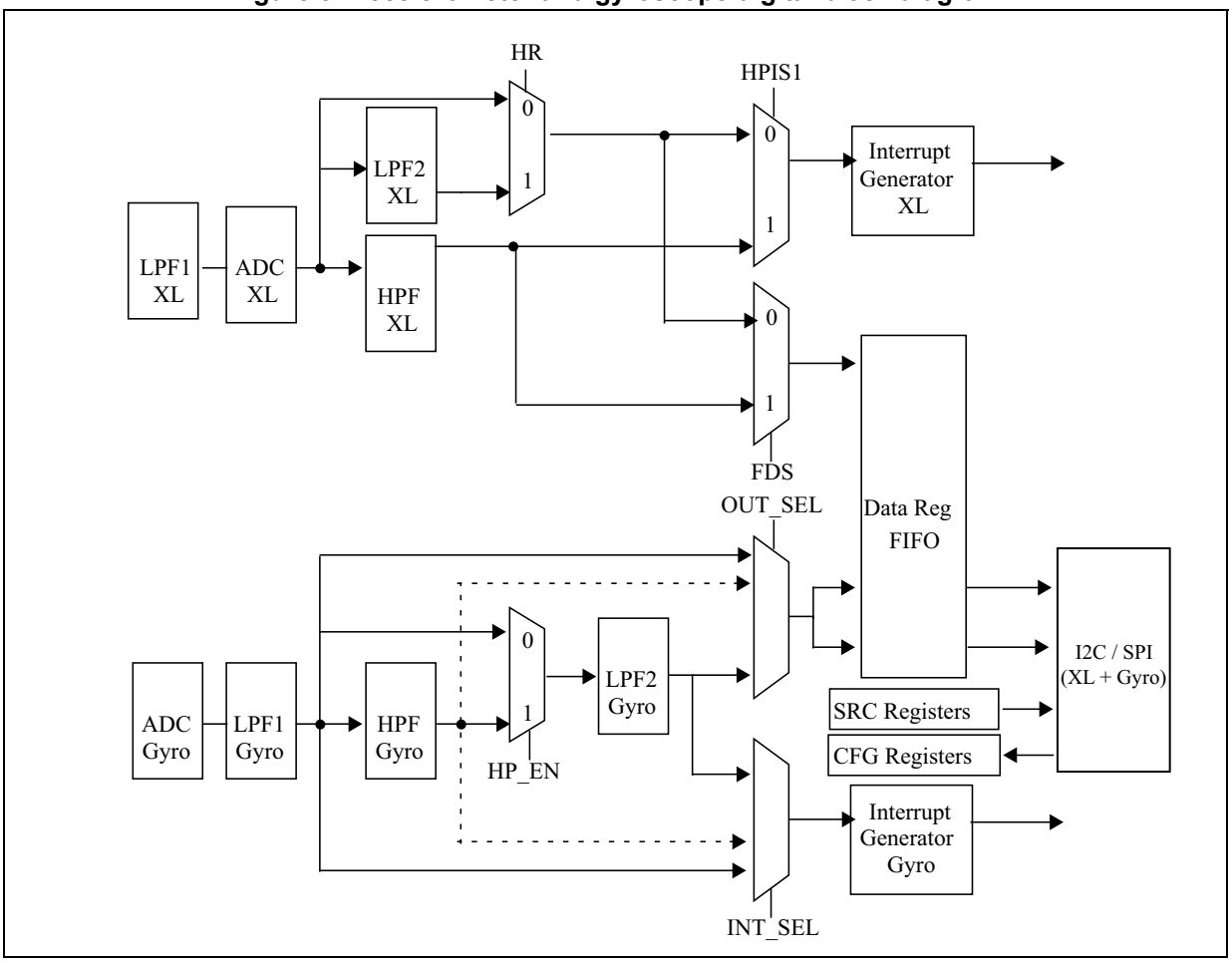
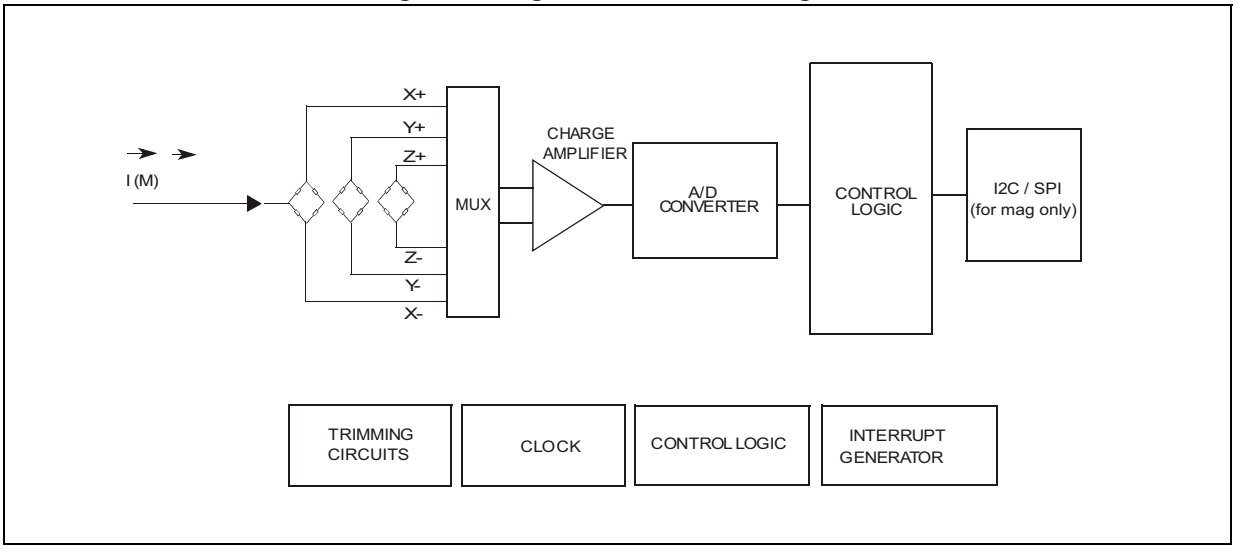


Figure 9. Magnetometer block diagram



3.5 Accelerometer and gyroscope FIFO

The LSM9DS1 embeds 32 slots of 16-bit data FIFO for each of the gyroscope's three output channels, yaw, pitch and roll, and 16-bit data FIFO for each of the accelerometer's three output channels, X, Y and Z. This allows consistent power saving for the system since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly to five different modes: Bypass mode, FIFO-mode, Continuous mode, Continuous-to-FIFO mode and Bypass-to-Continuous. Each mode is selected by the FMODE [2:0] bits in the *FIFO_CTRL (2Eh)* register. Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the *FIFO_SRC (2Fh)* register and can be set to generate dedicated interrupts on the INT1_A/G pin in the *INT1_CTRL (0Ch)* register and on the INT2_A/G pin in the *INT2_CTRL (0Dh)* register.

FIFO_SRC (2Fh)(FTH) goes to '1' when the number of unread samples (*FIFO_SRC (2Fh)* (FSS5:0)) is greater than or equal to FTH [4:0] in *FIFO_CTRL (2Eh)*. If *FIFO_CTRL (2Eh)* (FTH[4:0]) is equal to 0, *FIFO_SRC (2Fh)*(FTH) goes to '0'.

FIFO_SRC (2Fh)(OVRN) is equal to '1' if a FIFO slot is overwritten.

FIFO_SRC (2Fh)(FSS [5:0]) contains stored data levels of unread samples. When FSS [5:0] is equal to '000000' FIFO is empty, when FSS [5:0] is equal to '100000' FIFO is full and the unread samples are 32.

The FIFO feature is enabled by writing '1' in *CTRL_REG9 (23h)* (FIFO_EN).

To guarantee the correct acquisition of data during the switching into and out of FIFO mode, the first sample acquired must be discarded.

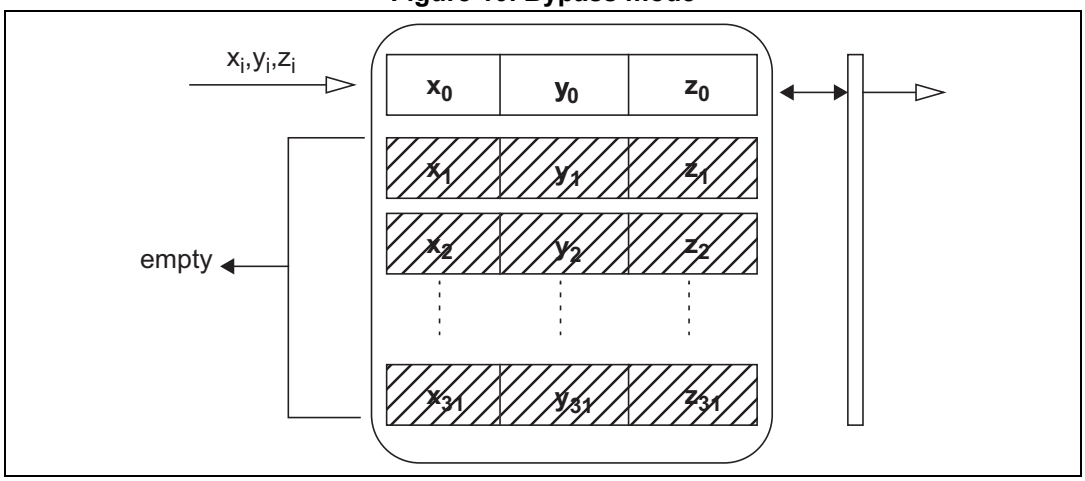
3.5.1 Bypass mode

In Bypass mode (*FIFO_CTRL (2Eh)*(FMODE [2:0]= 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

As described in *Figure 10*, for each channel only the first address is used. When new data is available the old data is overwritten.

Figure 10. Bypass mode



3.5.2 FIFO mode

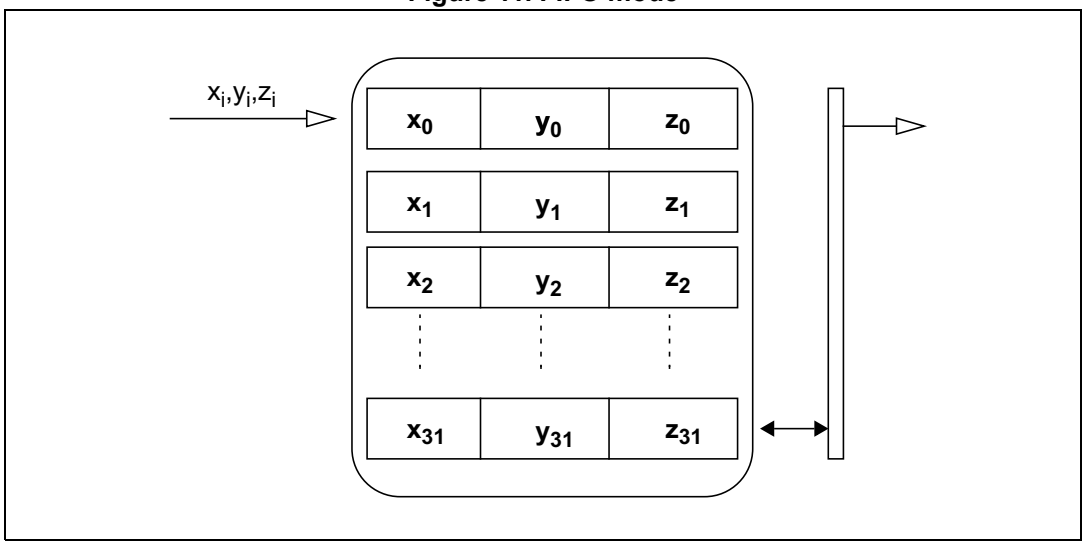
In FIFO mode (*FIFO_CTRL (2Eh)* (FMODE [2:0] = 001) data from the output channels are stored in the FIFO until it is overwritten.

To reset FIFO content, Bypass mode should be selected by writing *FIFO_CTRL (2Eh)* (FMODE [2:0]) to '000'. After this reset command, it is possible to restart FIFO mode by writing *FIFO_CTRL (2Eh)* (FMODE [2:0]) to '001'.

The FIFO buffer memorizes 32 levels of data but the depth of the FIFO can be resized by setting the STOP_ON_FTH bit in *CTRL_REG9 (23h)*. If the STOP_ON_FTH bit is set to '1', FIFO depth is limited to *FIFO_CTRL (2Eh)*(FTH [4:0]) + 1 data.

A FIFO threshold interrupt can be enabled (INT_OVR bit in *INT1_CTRL (0Ch)*) in order to be raised when the FIFO is filled to the level specified by the FTH[4:0] bits of *FIFO_CTRL (2Eh)*. When a FIFO threshold interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

Figure 11. FIFO mode



3.5.3 Continuous mode

Continuous mode (*FIFO_CTRL (2Eh)*(FMODE[2:0] = 110) provides continuous FIFO update: as new data arrives the older is discarded.

A FIFO threshold flag *FIFO_SRC (2Fh)*(FTH) is asserted when the number of unread samples in FIFO is greater than or equal to *FIFO_CTRL (2Eh)*(FTH4:0).

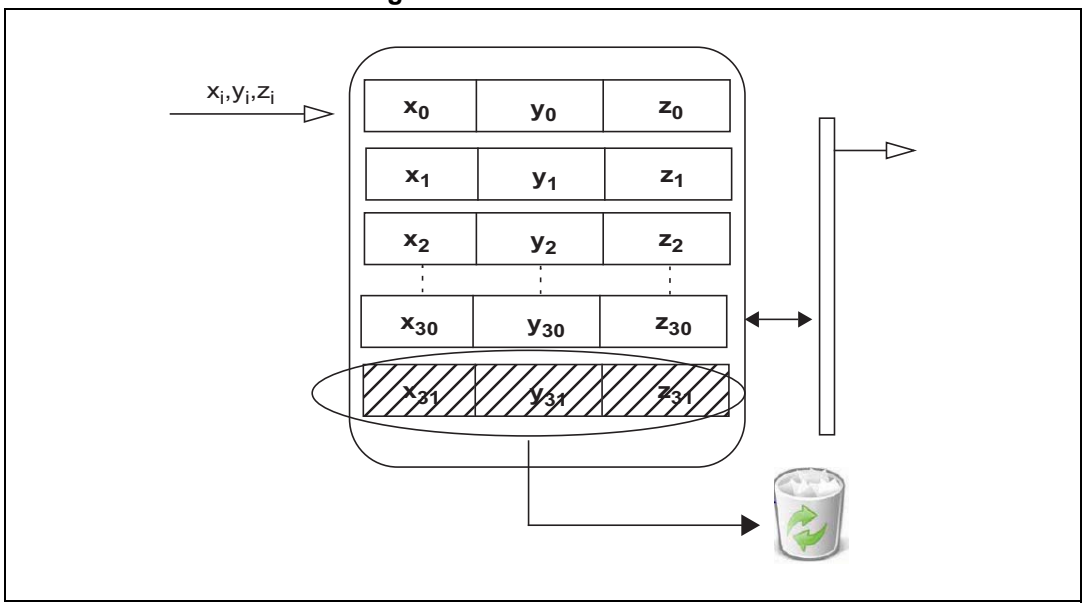
It is possible to route *FIFO_SRC (2Fh)*(FTH) to the INT1_A/G pin by writing in register *INT1_CTRL (0Ch)* (INT1_FTH) = '1', or to the INT2_A/G pin by writing in register *INT2_CTRL (0Dh)* (INT2_FTH) = '1'.

A full-flag interrupt can be enabled, (*INT1_CTRL (0Ch)* (INT_ FSS5)= '1') when the FIFO becomes saturated and in order to read the contents all at once.

If an overrun occurs, the oldest sample in FIFO is overwritten and the OVRN flag in *FIFO_SRC (2Fh)* is asserted.

In order to empty the FIFO before it is full it is also possible to pull from FIFO the number of unread samples available in *FIFO_SRC (2Fh)* (FSS[5:0]).

Figure 12. Continuous mode



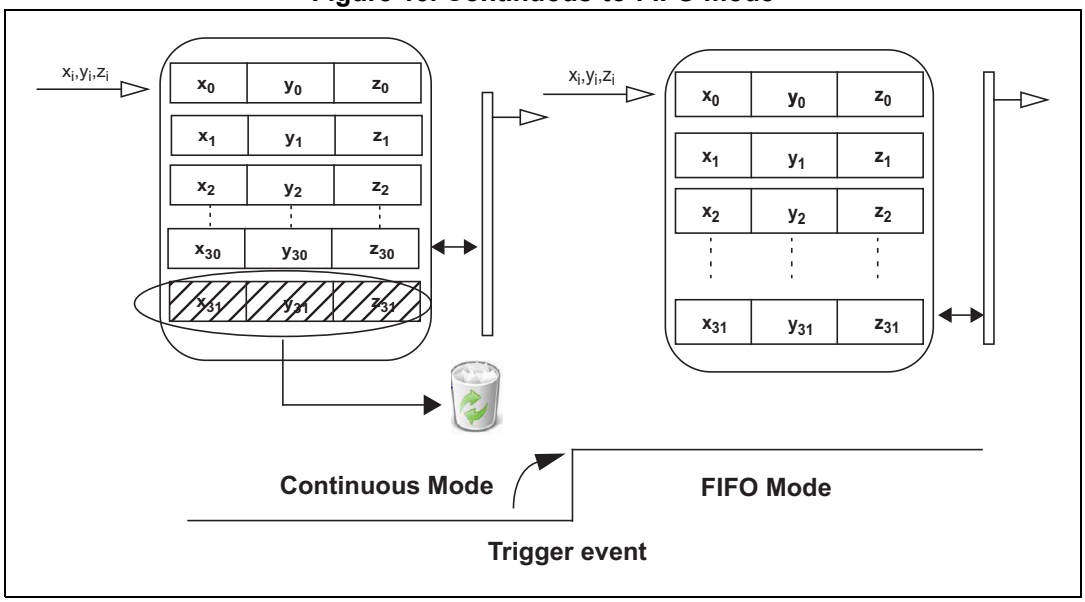
3.5.4 Continuous-to-FIFO mode

In Continuous-to-FIFO mode (*FIFO_CTRL (2Eh)*(FMODE [2:0] = 011), FIFO behavior changes according to the *INT_GEN_SRC_XL (26h)*(IA_XL) bit. When the *INT_GEN_SRC_XL (26h)*(IA_XL) bit is equal to '1', FIFO operates in FIFO-mode, when the *INT_GEN_SRC_XL (26h)*(IA_XL) bit is equal to '0', FIFO operates in Continuous mode.

The interrupt generator should be set to the desired configuration by means of *INT_GEN_CFG_XL (06h)*, *INT_GEN_THS_X_XL (07h)*, *INT_GEN_THS_Y_XL (08h)* and *INT_GEN_THS_Z_XL (09h)*.

The *CTRL_REG4 (1Eh)*(LIR_XL) bit should be set to '1' in order to have latched interrupt.

Figure 13. Continuous-to-FIFO mode



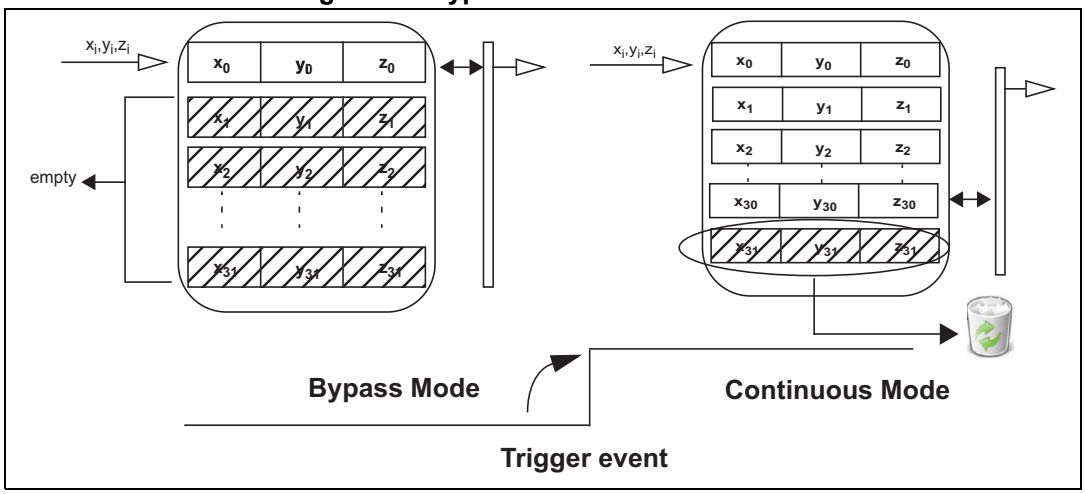
3.5.5 Bypass-to-Continuous mode

In Bypass-to-Continuous mode (*FIFO_CTRL (2Eh)*(FMODE[2:0] = '100'), data measurement storage inside FIFO operates in Continuous mode when *INT_GEN_SRC_XL (26h)*(IA_XL) is equal to '1', otherwise FIFO content is reset (Bypass mode).

The interrupt generator should be set to the desired configuration by means of *INT_GEN_CFG_XL (06h)*, *INT_GEN_THS_X_XL (07h)*, *INT_GEN_THS_Y_XL (08h)* and *INT_GEN_THS_Z_XL (09h)*.

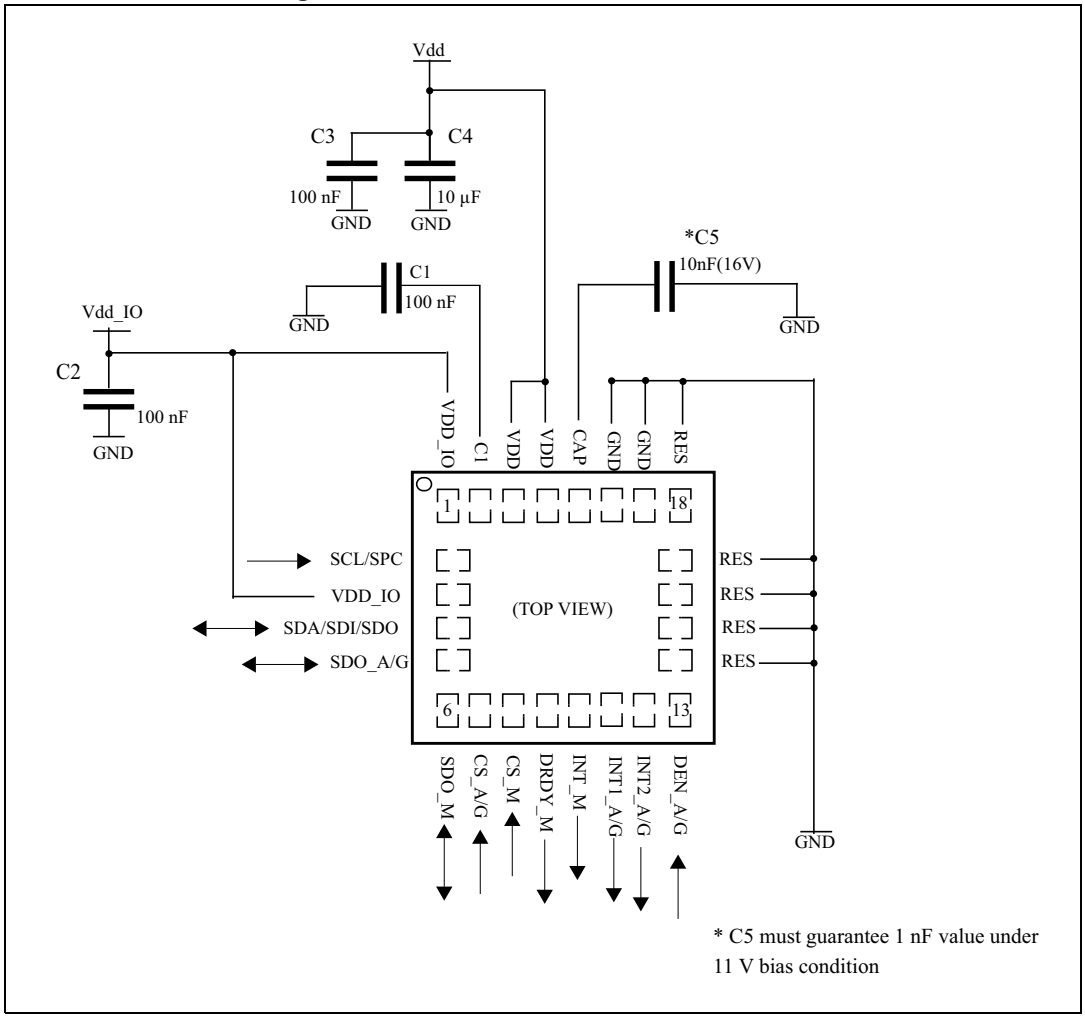
The *CTRL_REG4 (1Eh)*(LIR_XL) bit should be set to '1' in order to have latched interrupt.

Figure 14. Bypass-to-Continuous mode



4 Application hints

Figure 15. LSM9DS1 electrical connections



4.1 External capacitors

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C2, C3 = 100 *nF* ceramic, C4 = 10 *µF* Al) should be placed as near as possible to the supply pin of the device (common design practice). Capacitor C1 (100 nF) should be a capacitor with low ESR value and should be placed as near as possible to the C1 pin.

All voltage and ground supplies must be present at the same time to achieve proper behavior of the IC (refer to *Figure 15*).

5 Digital interfaces

The registers embedded inside the LSM9DS1 may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I^2C interface, the CS line must be tied high (i.e connected to Vdd_IO).

Table 13. Serial interface pin description

Pin name	Pin description
CS_A/G, CS_M	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL/SPC	I^2C Serial Clock (SCL) SPI Serial Port Clock (SPC)
SDA/SDI/SDO	I^2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
SDO_A/G, SDO_M	SPI Serial Data Output (SDO) I^2C less significant bit of the device address

5.1 I^2C serial interface

The LSM9DS1 I^2C is a bus slave. The I^2C is employed to write the data to the registers, whose content can also be read back.

The relevant I^2C terminology is provided in the table below.

Table 14. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the Serial DAta line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I^2C interface is implemented with fast mode (400 kHz) I^2C standards as well as with the standard mode.

In order to disable the I^2C block for accelerometer and gyroscope the I2C_DISABLE bit must be written to ‘1’ in *CTRL_REG9 (23h)*, while for magnetometer the I2C_DISABLE bit must be written to ‘1’ in *CTRL_REG3_M (22h)*.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM9DS1 behaves like a slave device and the following protocol must be adhered to. In the I²C of the accelerometer and gyroscope sensor, after the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The 7 LSb represent the actual register address while the *CTRL_REG8 (22h)* (IF_ADD_INC) bit defines the address increment. In the I²C of the magnetometer sensor, after the START condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The 7 LSb represent the actual register address while the MSB enables the address auto increment. The SUB (register address) is automatically increased to allow multiple data read/write.

Table 15. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 16. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 17. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 18. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed

some other function, it can hold the clock line, SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA line while the SCL line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

Default address:

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes. If the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 19* and *Table 20* explain how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 19. Accelerometer and gyroscope SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Table 20. Magnetic sensor SAD+Read/Write patterns

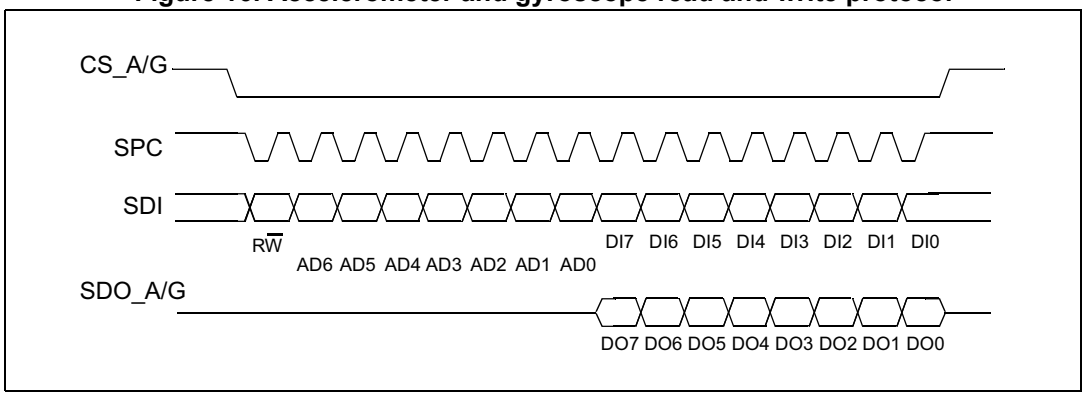
Command	SAD[6:2]	SAD[1] = SDO/SA1	SAD[0]	R/W	SAD+R/W
Read	00111	0	0	1	00111001 (39h)
Write	00111	0	0	0	00111000 (38h)
Read	00111	1	0	1	00111101 (3Dh)
Write	00111	1	0	0	00111100 (3Ch)

5.2 Accelerometer and gyroscope SPI bus interface

The LSM9DS1 accelerometer and gyroscope SPI is a bus slave. The SPI allows to write and read the registers of the device.

The Serial Interface connects to applications using 4 wires: **CS_A/G**, **SPC**, **SDI** and **SDO_A/G**.

Figure 16. Accelerometer and gyroscope read and write protocol



CS_A/G is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS_A/G** is high (no transmission). **SDI** and **SDO_A/G** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS_A/G** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS_A/G**.

bit 0: $\overline{RW}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO_A/G** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

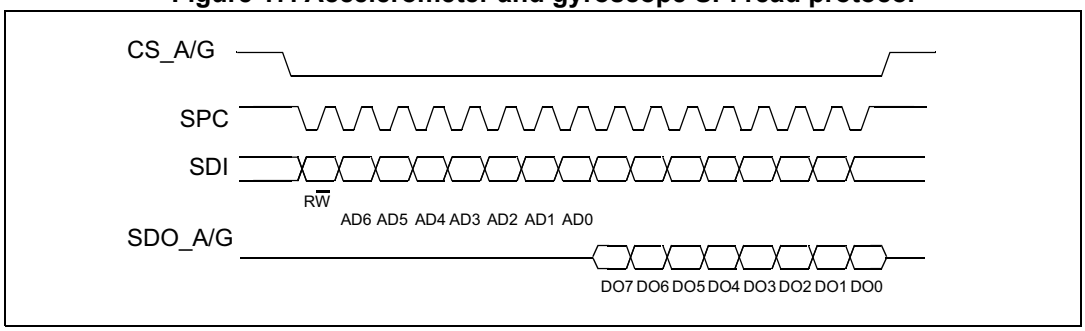
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the *CTRL_REG8 (22h)* (IF_ADD_INC) bit is '0' the address used to read/write data remains the same for every block. When the *CTRL_REG8 (22h)*(IF_ADD_INC) bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO_A/G** remain unchanged.

5.2.1 SPI read

Figure 17. Accelerometer and gyroscope SPI read protocol



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

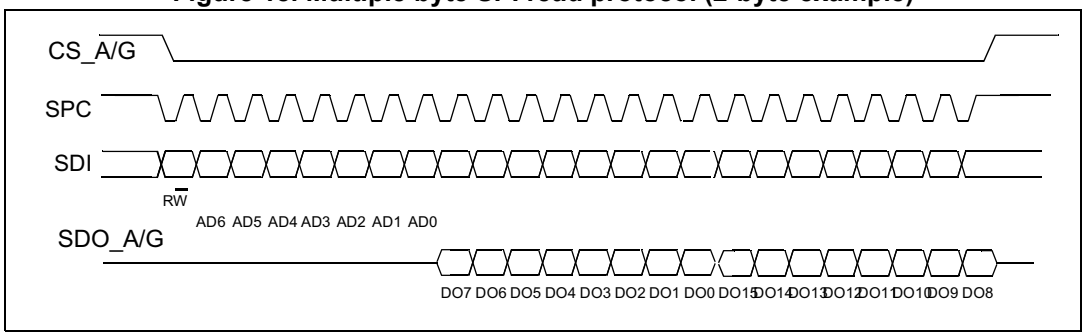
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

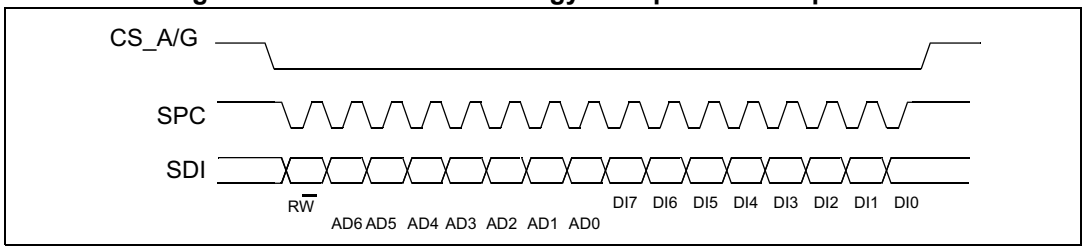
bit 16-... : data DO(...-8). Further data in multiple byte reads.

Figure 18. Multiple byte SPI read protocol (2-byte example)



5.2.2 SPI write

Figure 19. Accelerometer and gyroscope SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

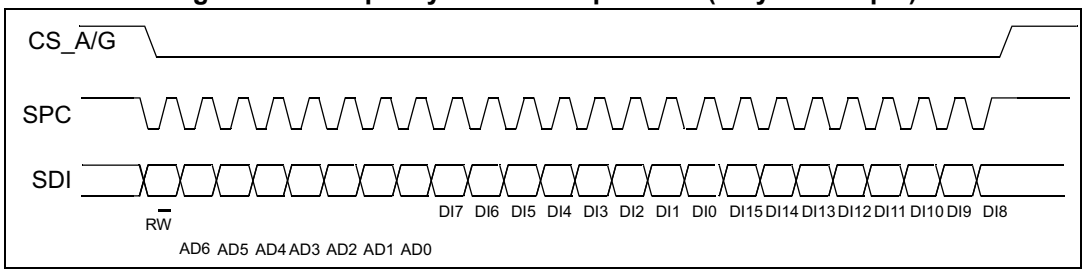
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

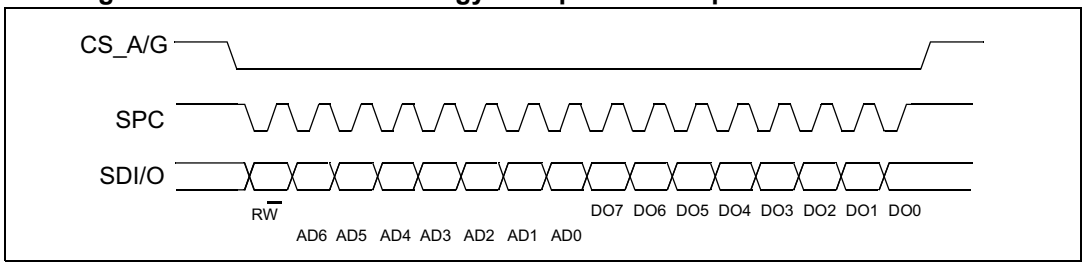
Figure 20. Multiple byte SPI write protocol (2-byte example)



5.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the *CTRL_REG8 (22h)*(SIM) bit equal to ‘1’ (SPI serial interface mode selection).

Figure 21. Accelerometer and gyroscope SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

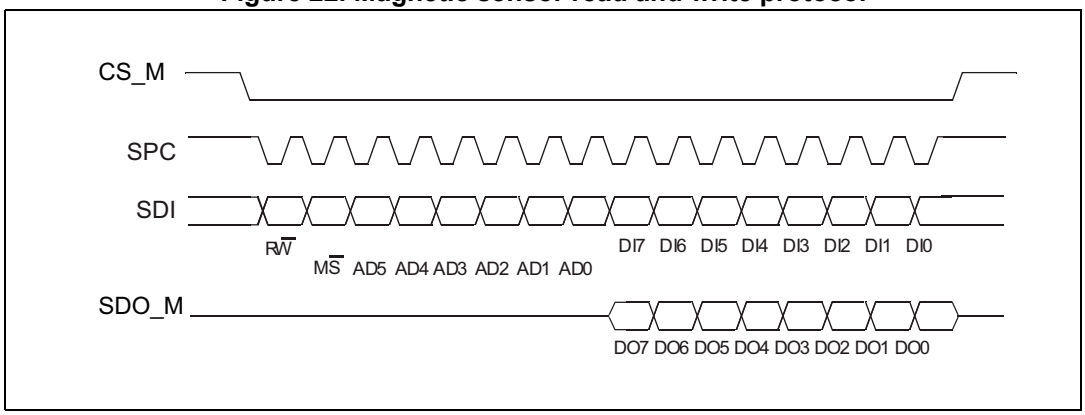
A multiple read command is also available in 3-wire mode.

5.3 Magnetic sensor SPI bus interface

The LSM9DS1 magnetic sensor SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface connects to applications using 4 wires: **CS_M**, **SPC**, **SDI** and **SDO_M**.

Figure 22. Magnetic sensor read and write protocol



CS_M is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS_M** is high (no transmission). **SDI** and **SDO_M** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS_M** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS_M**.

bit 0: $\overline{RW}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO_M** at the start of bit 8.

bit 1: $\overline{MS}$ bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address is auto-incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

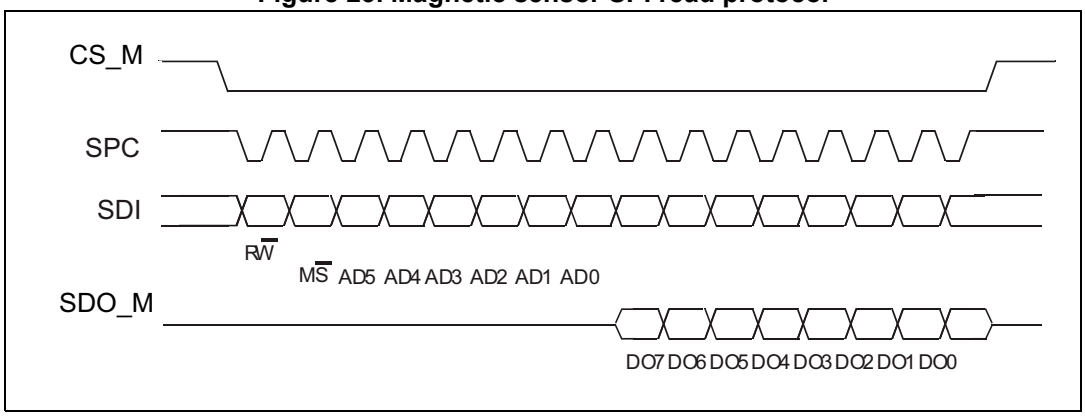
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the $\overline{MS}$ bit is '0', the address used to read/write data remains the same for every block. When the $\overline{MS}$ bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO_M** remain unchanged.

5.3.1 SPI read

Figure 23. Magnetic sensor SPI read protocol



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

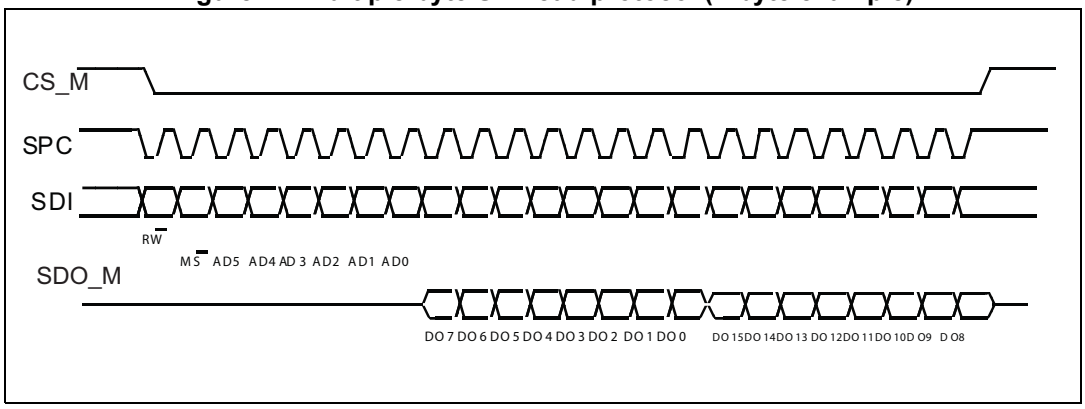
bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

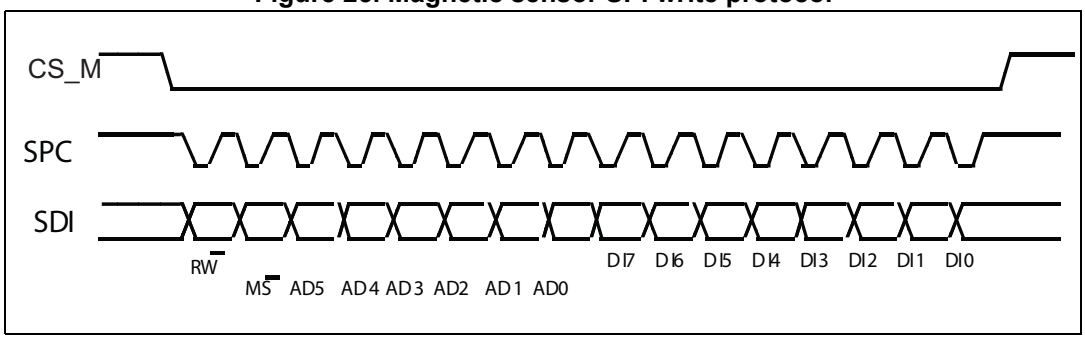
bit 16-... : data DO(...-8). Further data in multiple byte reads.

Figure 24. Multiple byte SPI read protocol (2-byte example)



5.3.2 SPI write

Figure 25. Magnetic sensor SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

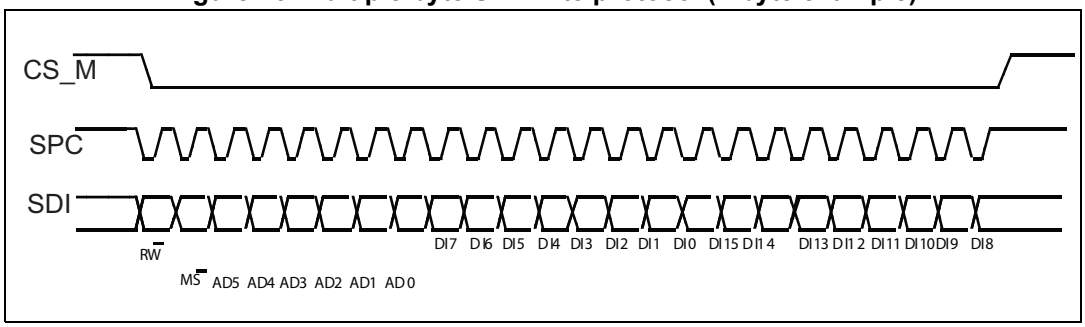
bit 1: $\overline{MS}$ bit. When 0, does not increment the address; when 1, increments the address in multiple writes.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

Figure 26. Multiple byte SPI write protocol (2-byte example)

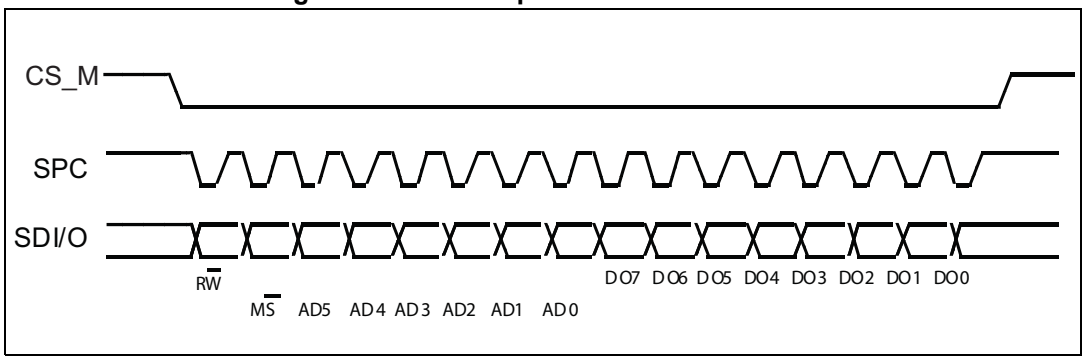


5.3.3 SPI read in 3-wire mode

3-wire mode is entered by setting the SIM bit to '1' (SPI serial interface mode selection) in *CTRL_REG3_M (22h)*.

When 3-wire mode is used, the SDO_M pin has to be connected to GND or Vdd_IO.

Figure 27. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: $\overline{MS}$ bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

6 Register mapping

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

Table 21. Accelerometer and gyroscope register address map

Name	Type	Register address		Default	Note
		Hex	Binary		
Reserved	--	00-03	--	--	Reserved
ACT_THS	r/w	04	00000100	00000000	
ACT_DUR	r/w	05	00000101	00000000	
INT_GEN_CFG_XL	r/w	06	00000110	00000000	
INT_GEN_THS_X_XL	r/w	07	00000111	00000000	
INT_GEN_THS_Y_XL	r/w	08	00001000	00000000	
INT_GEN_THS_Z_XL	r/w	09	00001001	00000000	
INT_GEN_DUR_XL	r/w	0A	00001010	00000000	
REFERENCE_G	r/w	0B	00001011	00000000	
INT1_CTRL	r/w	0C	00001100	00000000	
INT2_CTRL	r/w	0D	00001101	00000000	
Reserved	--	0E	--	--	Reserved
WHO_AM_I	r	0F	00001111	01101000	
CTRL_REG1_G	r/w	10	00010000	00000000	
CTRL_REG2_G	r/w	11	00010001	00000000	
CTRL_REG3_G	r/w	12	00010010	00000000	
ORIENT_CFG_G	r/w	13	00010011	00000000	
INT_GEN_SRC_G	r	14	00010100	output	
OUT_TEMP_L	r	15	00010101	output	
OUT_TEMP_H	r	16	00010110	output	
STATUS_REG	r	17	00010111	output	
OUT_X_L_G	r	18	00011000	output	
OUT_X_H_G	r	19	00011001	output	
OUT_Y_L_G	r	1A	00011010	output	
OUT_Y_H_G	r	1B	00011011	output	
OUT_Z_L_G	r	1C	00011100	output	
OUT_Z_H_G	r	1D	00011101	output	
CTRL_REG4	r/w	1E	00011110	00111000	
CTRL_REG5_XL	r/w	1F	00011111	00111000	

Table 21. Accelerometer and gyroscope register address map (continued)

Name	Type	Register address		Default	Note
		Hex	Binary		
CTRL_REG6_XL	r/w	20	00100000	00000000	
CTRL_REG7_XL	r/w	21	00100001	00000000	
CTRL_REG8	r/w	22	00100010	00000100	
CTRL_REG9	r/w	23	00100011	00000000	
CTRL_REG10	r/w	24	00100100	00000000	
Reserved	--	25	--	--	Reserved
INT_GEN_SRC_XL	r	26	00100110	output	
STATUS_REG	r	27	00100111	output	
OUT_X_L_XL	r	28	00101000	output	
OUT_X_H_XL	r	29	00101001	output	
OUT_Y_L_XL	r	2A	00101010	output	
OUT_Y_H_XL	r	2B	00101011	output	
OUT_Z_L_XL	r	2C	00101100	output	
OUT_Z_H_XL	r	2D	00101101	output	
FIFO_CTRL	r/w	2E	00101110	00000000	
FIFO_SRC	r	2F	00101111	output	
INT_GEN_CFG_G	r/w	30	00110000	00000000	
INT_GEN_THS_XH_G	r/w	31	00110001	00000000	
INT_GEN_THS_XL_G	r/w	32	00110010	00000000	
INT_GEN_THS_YH_G	r/w	33	00110011	00000000	
INT_GEN_THS_YL_G	r/w	34	00110100	00000000	
INT_GEN_THS_ZH_G	r/w	35	00110101	00000000	
INT_GEN_THS_ZL_G	r/w	36	00110110	00000000	
INT_GEN_DUR_G	r/w	37	00110111	00000000	
Reserved	r	38-7F	--	--	Reserved

Table 22. Magnetic sensor register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved		00 - 04	--	--	Reserved
OFFSET_X_REG_L_M	r/w	05		00000000	Offset in order to compensate environmental effects
OFFSET_X_REG_H_M	r/w	06		00000000	
OFFSET_Y_REG_L_M	r/w	07		00000000	
OFFSET_Y_REG_H_M	r/w	08		00000000	
OFFSET_Z_REG_L_M	r/w	09		00000000	
OFFSET_Z_REG_H_M	r/w	0A		00000000	
Reserved		0B - 0E	--	--	Reserved
WHO_AM_I_M	r	0F	0000 1111	00111101	Magnetic Who I am ID
Reserved		10 - 1F	--	--	Reserved
CTRL_REG1_M	r/w	20	0010 0000	00010000	Magnetic control registers
CTRL_REG2_M	r/w	21	0010 0001	00000000	
CTRL_REG3_M	r/w	22	0010 0010	00000011	
CTRL_REG4_M	r/w	23	0010 0011	00000000	
CTRL_REG5_M	r/w	24	0010 0100	00000000	
Reserved		25 - 26	--	--	Reserved
STATUS_REG_M	r	27	0010 0111	Output	
OUT_X_L_M	r	28	0010 1000	Output	Magnetic output registers
OUT_X_H_M	r	29	0010 1001	Output	
OUT_Y_L_M	r	2A	0010 1010	Output	
OUT_Y_H_M	r	2B	0010 1011	Output	
OUT_Z_L_M	r	2C	0010 1100	Output	
OUT_Z_H_M	r	2D	0010 1101	Output	
Reserved	r	2E-2F	--	--	Reserved
INT_CFG_M	rw	30	00110000	00001000	Magnetic interrupt configuration register
INT_SRC_M	r	31	00110001	00000000	Magnetic interrupt generator status register
INT_THS_L_M	r	32	00110010	00000000	Magnetic interrupt generator threshold
INT_THS_H_M	r	33	00110011	00000000	

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

To guarantee proper behavior of the device, all registers addresses not listed in the above table must not be accessed and the content stored on those registers must not be changed.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

7 Accelerometer and gyroscope register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

7.1 ACT_THS (04h)

Activity threshold register.

Table 23. ACT_THS register

SLEEP_ON _INACT_EN	ACT_THS 6	ACT_THS 5	ACT_THS 4	ACT_THS 3	ACT_THS 2	ACT_TH S1	ACT_THS 0

Table 24. ACT_THS register description

SLEEP_ON_ INACT_EN	Gyroscope operating mode during inactivity. Default value: 0 (0: gyroscope in power-down; 1: gyroscope in sleep mode)
ACT_THS [6:0]	Inactivity threshold. Default value: 000 0000

7.2 ACT_DUR (05h)

Inactivity duration register.

Table 25. ACT_DUR register

ACT_DUR 7	ACT_DUR 6	ACT_DUR 5	ACT_DUR 4	ACT_DUR 3	ACT_DUR 2	ACT_DUR 1	ACT_DUR 0

Table 26. ACT_DUR register description

ACT_DUR [7:0]	Inactivity duration. Default value: 0000 0000

7.3 INT_GEN_CFG_XL (06h)

Linear acceleration sensor interrupt generator configuration register.

Table 27. INT_GEN_CFG_XL register

AOI_XL	6D	ZHIE_XL	ZLIE_XL	YHIE_XL	YLIE_XL	XHIE_XL	XLIE_XL

Table 28. INT_GEN_CFG_XL register description

AOI_XL	AND/OR combination of accelerometer's interrupt events. Default value: 0 (0: OR combination; 1: AND combination)
6D	6-direction detection function for interrupt. Default value: 0 (0: disabled; 1: enabled)
ZHIE_XL	Enable interrupt generation on accelerometer's Z-axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
ZLIE_XL	Enable interrupt generation on accelerometer's Z-axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value lower than preset threshold)
YHIE_XL	Enable interrupt generation on accelerometer's Y-axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
YLIE_XL	Enable interrupt generation on accelerometer's Y-axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value lower than preset threshold)
XHIE_XL	Enable interrupt generation on accelerometer's X-axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold)
XLIE_XL	Enable interrupt generation on accelerometer's X-axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured acceleration value lower than preset threshold)

7.4 INT_GEN_THS_X_XL (07h)

Linear acceleration sensor interrupt threshold register.

Table 29. INT_GEN_THS_X_XL register

THS_XL_X7	THS_XL_X6	THS_XL_X5	THS_XL_X4	THS_XL_X3	THS_XL_X2	THS_XL_X1	THS_XL_X0

Table 30. INT_GEN_THS_X_XL register description

THS_XL_X [7:0]	X-axis interrupt threshold. Default value: 0000 0000

7.5 INT_GEN_THS_Y_XL (08h)

Linear acceleration sensor interrupt threshold register.

Table 31. INT_GEN_THS_Y_XL register

THS_XL_Y7	THS_XL_Y6	THS_XL_Y5	THS_XL_Y4	THS_XL_Y3	THS_XL_Y2	THS_XL_Y1	THS_XL_Y0

Table 32. INT_GEN_THS_Y_XL register description

THS_XL_Y [7:0]	Y-axis interrupt threshold. Default value: 0000 0000

7.6 INT_GEN_THS_Z_XL (09h)

Linear acceleration sensor interrupt threshold register.

Table 33. INT_GEN_THS_Z_XL register

THS_XL_Z 7	THS_XL_Z 6	THS_XL_Z 5	THS_XL_Z 4	THS_XL_Z 3	THS_XL_Z 2	THS_XL_Z 1	THS_XL_Z 0

Table 34. INT_GEN_THS_Z_XL register description

THS_XL_Z [7:0]	Z-axis interrupt threshold. Default value: 0000 0000

7.7 INT_GEN_DUR_XL (0Ah)

Linear acceleration sensor interrupt duration register.

Table 35. INT_GEN_DUR_XL register

WAIT_XL	DUR_XL6	DUR_XL5	DUR_XL4	DUR_XL3	DUR_XL2	DUR_XL1	DUR_XL0

Table 36. INT_GEN_DUR_XL register description

WAIT_XL	Wait function enabled on duration counter. Default value: 0 (0: wait function off; 1: wait for DUR_XL [6:0] samples before exiting interrupt)
DUR_XL [6:0]	Enter/exit interrupt duration value. Default value: 000 0000

7.8 REFERENCE_G (0Bh)

Angular rate sensor reference value register for digital high-pass filter (r/w).

Table 37. REFERENCE_G register

REF7_G	REF6_G	REF5_G	REF4_G	REF3_G	REF2_G	REF1_G	REF0_G

Table 38. REFERENCE_G register description

REF_G [7:0]	Reference value for gyroscope's digital high-pass filter (r/w). Default value: 0000 0000

7.9 INT1_CTRL (0Ch)

INT1_A/G pin control register.

Table 39. INT1_CTRL register

INT1_IG _G	INT1_IG_ XL	INT1_ FSS5	INT1_OVR	INT1_FTH	INT1_ Boot	INT1_ DRDY_G	INT1_ DRDY_XL

Table 40. INT1_CTRL register description

INT1_IG_G	Gyroscope interrupt enable on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT_ IG_XL	Accelerometer interrupt generator on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT_ FSS5	FSS5 interrupt enable on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT_OVR	Overrun interrupt on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT_FTH	FIFO threshold interrupt on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT_ Boot	Boot status available on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT_DRDY_G	Gyroscope data ready on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT_DRDY_XL	Accelerometer data ready on INT 1_A/G pin. Default value: 0 (0: disabled; 1: enabled)

7.10 INT2_CTRL (0Dh)

INT2_A/G pin control register.

Table 41. INT2_CTRL register

INT2_IN ACT	0	INT2_ FSS5	INT2_OVR	INT2_FTH	INT2_ DRDY_ TEMP	INT2_ DRDY_G	INT2_ DRDY_XL

Table 42. INT2_CTRL register description

INT2_INACT	Inactivity interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
INT2_ FSS5	FSS5 interrupt enable on INT2_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT2_OVR	Overrun interrupt on INT2_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT2_FTH	FIFO threshold interrupt on INT2_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT2_ DRDY_TEMP	Temperature data ready on INT2_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_G	Gyroscope data ready on INT2_A/G pin. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_XL	Accelerometer data ready on INT2_A/G pin. Default value: 0 (0: disabled; 1: enabled)

7.11 WHO_AM_I (0Fh)

Who_AM_I register.

Table 43. WHO_AM_I register

0	1	1	0	1	0	0	0

7.12 CTRL_REG1_G (10h)

Angular rate sensor Control Register 1.

Table 44. CTRL_REG1_G register

ODR_G2	ODR_G1	ODR_G0	FS_G1	FS_G0	0(1)	BW_G1	BW_G0

1. This bit must be set to '0' for the correct operation of the device.

Table 45. CTRL_REG1_G register description

ODR_G [2:0]	Gyroscope output data rate selection. Default value: 000 (Refer to *Table 46* and *Table 47*)
FS_G [1:0]	Gyroscope full-scale selection. Default value: 00 (00: 245 dps; 01: 500 dps; 10: Not Available; 11: 2000 dps)
BW_G [1:0]	Gyroscope bandwidth selection. Default value: 00

ODR_G [2:0] are used to set ODR selection when both the accelerometer and gyroscope are activated. BW_G [1:0] are used to set gyroscope bandwidth selection.

The following table summarizes all frequencies available for each combination of the ODR_G / BW_G bits after LPF1 (see *Table 46*) and LPF2 (see *Table 47*) when both the accelerometer and gyroscope are activated. For more details regarding signal processing please refer to *Figure 28*.

Table 46. ODR and BW configuration setting (after LPF1)

ODR_G2	ODR_G1	ODR_G0	ODR [Hz]	Cutoff [Hz](1)
0	0	0	Power-down	n.a.
0	0	1	14.9	5
0	1	0	59.5	19
0	1	1	119	38
1	0	0	238	76
1	0	1	476	100
1	1	0	952	100
1	1	1	n.a.	n.a.

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

Table 47. ODR and BW configuration setting (after LPF2)

ODR_G [2:0]	BW_G [1:0]	ODR [Hz]	Cutoff [Hz](1)
000	00	Power-down	n.a.
000	01	Power-down	n.a.
000	10	Power-down	n.a.
000	11	Power-down	n.a.
001	00	14.9	n.a.
001	01	14.9	n.a.
001	10	14.9	n.a.
001	11	14.9	n.a.
010	00	59.5	16
010	01	59.5	16
010	10	59.5	16
010	11	59.5	16
011	00	119	14
011	01	119	31
011	10	119	31
011	11	119	31
100	00	238	14
100	01	238	29
100	10	238	63
100	11	238	78
101	00	476	21
101	01	476	28
101	10	476	57
101	11	476	100
110	00	952	33
110	01	952	40
110	10	952	58
110	11	952	100
111	00	n.a.	n.a.
111	01	n.a.	n.a.
111	10	n.a.	n.a.
111	11	n.a.	n.a.

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

7.13 CTRL_REG2_G (11h)

Angular rate sensor Control Register 2.

Table 48. CTRL_REG2_G register

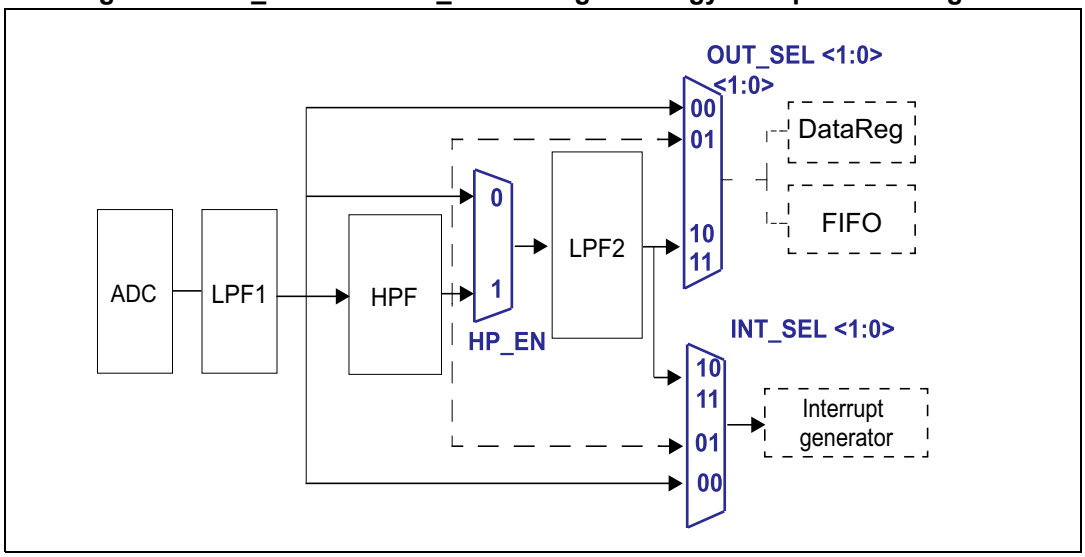
0(1)	0(1)	0(1)	0(1)	INT_SEL1	INT_SEL0	OUT_SEL1	OUT_SEL0

1. These bits must be set to '0' for the correct operation of the device

Table 49. CTRL_REG2_G register description

INT_SEL [1:0]	INT selection configuration. Default value: 00 (Refer to *Figure 28*)
OUT_SEL [1:0]	Out selection configuration. Default value: 00 (Refer to *Figure 28*)

Figure 28. INT_SEL and OUT_SEL configuration gyroscope block diagram



7.14 CTRL_REG3_G (12h)

Angular rate sensor Control Register 3.

Table 50. CTRL_REG3_G register

LP_mode	HP_EN	0(1)	0(1)	HPCF3_G	HPCF2_G	HPCF1_G	HPCF0_G

1. These bits must be set to '0' for the correct operation of the device

Table 51. CTRL_REG3_G register description

LP_mode	Low-power mode enable. Default value: 0 (0: Low-power disabled; 1: Low-power enabled)
HP_EN	High-pass filter enable. Default value: 0 (0: HPF disabled; 1: HPF enabled, refer to *Figure 28*)
HPCF_G [3:0]	Gyroscope high-pass filter cutoff frequency selection. Default value: 0000 Refer to *Table 52*.

Table 52. Gyroscope high-pass filter cutoff frequency configuration [Hz](1)

HPCF_G [3:0]	ODR= 14.9 Hz	ODR= 59.5 Hz	ODR= 119 Hz	ODR= 238 Hz	ODR= 476 Hz	ODR= 952 Hz
0000	1	4	8	15	30	57
0001	0.5	2	4	8	15	30
0010	0.2	1	2	4	8	15
0011	0.1	0.5	1	2	4	8
0100	0.05	0.2	0.5	1	2	4
0101	0.02	0.1	0.2	0.5	1	2
0110	0.01	0.05	0.1	0.2	0.5	1
0111	0.005	0.02	0.05	0.1	0.2	0.5
1000	0.002	0.01	0.02	0.05	0.1	0.2
1001	0.001	0.005	0.01	0.02	0.05	0.1

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

7.15 ORIENT_CFG_G (13h)

Angular rate sensor sign and orientation register.

Table 53. ORIENT_CFG_G register

0(1)	0(1)	SignX_G	SignY_G	SignZ_G	Orient_2	Orient_1	Orient_0

1. These bits must be set to ‘0’ for the correct operation of the device.

Table 54. ORIENT_CFG_G register description

SignX_G	Pitch axis (X) angular rate sign. Default value: 0 (0: positive sign; 1: negative sign)
SignY_G	Roll axis (Y) angular rate sign. Default value: 0 (0: positive sign; 1: negative sign)
SignZ_G	Yaw axis (Z) angular rate sign. Default value: 0 (0: positive sign; 1: negative sign)
Orient [2:0]	Directional user orientation selection. Default value: 000

7.16 INT_GEN_SRC_G (14h)

Angular rate sensor interrupt source register.

Table 55. INT_GEN_SRC_G register

0	IA_G	ZH_G	ZL_G	YH_G	YL_G	XH_G	XL_G

Table 56. INT_GEN_SRC_G register description

IA_G	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH_G	Yaw (Z) high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL_G	Yaw (Z) low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH_G	Roll (Y) high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL_G	Roll (Y) low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH_G	Pitch (X) high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL_G	Pitch (X) low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

7.17 OUT_TEMP_L (15h), OUT_TEMP_H (16h)

Temperature data output register. L and H registers together express a 16-bit word in two's complement right-justified.

Table 57. OUT_TEMP_L register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 58. OUT_TEMP_H register

Temp11	Temp11	Temp11	Temp11	Temp11	Temp10	Temp9	Temp8

Table 59. OUT_TEMP register description

Temp [11:0]	Temperature sensor output data. The value is expressed as two's complement sign extended on the MSB.

7.18 STATUS_REG (17h)

Status register.

Table 60. STATUS_REG register

0	IG_XL	IG_G	INACT	BOOT_ STATUS	TDA	GDA	XLDA

Table 61. STATUS_REG register description

IG_XL	Accelerometer interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
IG_G	Gyroscope interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
INACT	Inactivity interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
BOOT_ STATUS	Boot running flag signal. Default value: 0 (0: no boot running; 1: boot running)
TDA	Temperature sensor new data available. Default value: 0 (0: new data is not yet available; 1: new data is available)
GDA	Gyroscope new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
XLDA	Accelerometer new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)

7.19 OUT_X_G (18h - 19h)

Angular rate sensor pitch axis (X) angular rate output register. The value is expressed as a 16-bit word in two's complement.

7.20 OUT_Y_G (1Ah - 1Bh)

Angular rate sensor roll axis (Y) angular rate output register. The value is expressed as a 16-bit word in two's complement.

7.21 OUT_Z_G (1Ch - 1Dh)

Angular rate sensor Yaw axis (Z) angular rate output register. The value is expressed as a 16-bit word in two's complement.

7.22 CTRL_REG4 (1Eh)

Control register 4.

Table 62. CTRL_REG4 register

0(1)	0(1)	Zen_G	Yen_G	Xen_G	0(1)	LIR_XL1	4D_XL1

1. These bits must be set to '0' for the correct operation of the device.

Table 63. CTRL_REG4 register description

Zen_G	Gyroscope's Yaw axis (Z) output enable. Default value: 1 (0: Z-axis output disabled; 1: Z-axis output enabled)
Yen_G	Gyroscope's roll axis (Y) output enable. Default value: 1 (0: Y-axis output disabled; 1: Y-axis output enabled)
Xen_G	Gyroscope's pitch axis (X) output enable. Default value: 1 (0: X -xis output disabled; 1: X-axis output enabled)
LIR_XL1	Latched Interrupt. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
4D_XL1	4D option enabled on Interrupt. Default value: 0 (0: interrupt generator uses 6D for position recognition; 1: interrupt generator uses 4D for position recognition)

7.23 CTRL_REG5_XL (1Fh)

Linear acceleration sensor Control Register 5.

Table 64. CTRL_REG5_XL register

DEC_1	DEC_0	Zen_XL	Yen_XL	Xen_XL	0(1)	0(1)	0(1)

1. These bits must be set to '0' for the correct operation of the device.

Table 65. CTRL_REG5_XL register description

DEC_ [0:1]	Decimation of acceleration data on OUT REG and FIFO. Default value: 00 (00: no decimation; 01: update every 2 samples; 10: update every 4 samples; 11: update every 8 samples)
Zen_XL	Accelerometer's Z-axis output enable. Default value: 1 (0: Z-axis output disabled; 1: Z-axis output enabled)
Yen_XL	Accelerometer's Y-axis output enable. Default value: 1 (0: Y-axis output disabled; 1: Y-axis output enabled)
Xen_XL	Accelerometer's X-axis output enable. Default value: 1 (0: X-axis output disabled; 1: X-axis output enabled)

7.24 CTRL_REG6_XL (20h)

Linear acceleration sensor Control Register 6.

Table 66. CTRL_REG6_XL register

ODR_XL2	ODR_XL1	ODR_XL0	FS1_XL	FS0_XL	BW_SCAL_ODR	BW_XL1	BW_XL0

Table 67. CTRL_REG6_XL register description

ODR_XL [2:0]	Output data rate and power mode selection. default value: 000 (see *Table 68*)
FS_XL [1:0]	Accelerometer full-scale selection. Default value: 00 (00: ±2*g*; 01: ±16 *g;* 10: ±4 *g*; 11: ±8 *g*)
BW_SCAL_ ODR	Bandwidth selection. Default value: 0 (0: bandwidth determined by ODR selection: - BW = 408 Hz when ODR = 952 Hz, 50 Hz, 10 Hz; - BW = 211 Hz when ODR = 476 Hz; - BW = 105 Hz when ODR = 238 Hz; - BW = 50 Hz when ODR = 119 Hz; 1: bandwidth selected according to BW_XL [2:1] selection)
BW_XL [1:0]	Anti-aliasing filter bandwidth selection. Default value: 00 (00: 408 Hz; 01: 211 Hz; 10: 105 Hz; 11: 50 Hz)

ODR_XL [2:0] is used to set power mode and ODR selection. *Table 68* indicates all the frequencies available when only the accelerometer is activated.

Table 68. ODR register setting (accelerometer only mode)

ODR_XL2	ODR_XL1	ODR_XL0	ODR selection [Hz]
0	0	0	Power-down
0	0	1	10 Hz
0	1	0	50 Hz
0	1	1	119 Hz
1	0	0	238 Hz
1	0	1	476 Hz
1	1	0	952 Hz
1	1	1	n.a.

7.25 CTRL_REG7_XL (21h)

Linear acceleration sensor Control Register 7.

Table 69. CTRL_REG7_XL register

HR	DCF1	DCF0	0(1)	0(1)	FDS	0(1)	HPIS1

1. These bits must be set to ‘0’ for the correct operation of the device

Table 70. CTRL_REG7_XL register description

HR	High resolution mode for accelerometer enable. Default value: 0 (0: disabled; 1: enabled). Refer to *Table 71*
DCF[1:0]	Accelerometer digital filter (high pass and low pass) cutoff frequency selection: the band-width of the high-pass filter depends on the selected ODR. Refer to *Table 71*
FDS	Filtered data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
HPIS1	High-pass filter enabled for acceleration sensor interrupt function on Interrupt. Default value: 0 (0: filter bypassed; 1: filter enabled)

Table 71. Low pass cutoff frequency in high resolution mode (HR = 1)

HR	CTRL_REG7 (DCF [1:0])	LP cutoff freq. [Hz]
1	00	ODR/50
1	01	ODR/100
1	10	ODR/9
1	11	ODR/400

7.26 CTRL_REG8 (22h)

Control register 8.

Table 72. CTRL_REG8 register

BOOT	BDU	H_LACTIVE	PP_OD	SIM	IF_ADD_INC	BLE	SW_RESET

Table 73. CTRL_REG8 register description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content(1))
BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB read)
H_LACTIVE	Interrupt activation level. Default value: 0 (0: interrupt output pins active high; 1: interrupt output pins active low)
PP_OD	Push-pull/open-drain selection on the INT1_A/G pin and INT2_A/G pin. Default value: 0 (0: push-pull mode; 1: open-drain mode)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).
IF_ADD_INC	Register address automatically incremented during a multiple byte access with a serial interface (I^2C or SPI). Default value: 1 (0: disabled; 1: enabled)
BLE	Big/Little Endian data selection. Default value 0 (0: data LSB @ lower address; 1: data MSB @ lower address)
SW_RESET	Software reset. Default value: 0 (0: normal mode; 1: reset device) This bit is cleared by hardware after next flash boot.

1. Boot request is executed as soon as internal oscillator is turned-on. It is possible to set bit while in power-down mode, in this case it will be served at the next normal mode or sleep mode.

7.27 CTRL_REG9 (23h)

Control register 9.

Table 74. CTRL_REG9 register

0(1)	SLEEP_G	0(1)	FIFO_ TEMP_EN	DRDY_ mask_bit	I2C_DISAB LE	FIFO_EN	STOP_ON _FTH

1. These bits must be set to '0' for the correct operation of the device

Table 75. CTRL_REG9 register description

SLEEP_G	Gyroscope sleep mode enable. Default value: 0 (0: disabled; 1: enabled)
FIFO_TEMP_EN	Temperature data storage in FIFO enable. Default value: 0 (0: temperature data not stored in FIFO; 1: temperature data stored in FIFO)
DRDY_mask_bit	Data available enable bit. Default value: 0 (0: DA timer disabled; 1: DA timer enabled)
I2C_DISABLE	Disable I^2C interface. Default value: 0 (0: both I^2C and SPI enabled; 1: I^2C disabled, SPI only)
FIFO_EN	FIFO memory enable. Default value: 0 (0: disabled; 1: enabled)
STOP_ON_FTH	Enable FIFO threshold level use. Default value: 0 (0: FIFO depth is not limited; 1: FIFO depth is limited to threshold level)

7.28 CTRL_REG10 (24h)

Control register 10.

Table 76. CTRL_REG10 register

0(1)	0(1)	0(1)	0(1)	0(1)	ST_G	0(1)	ST_XL

1. These bits must be set to '0' for the correct operation of the device

Table 77. CTRL_REG10 register description

ST_G	Angular rate sensor self-test enable. Default value: 0 (0: Self-test disabled; 1: Self-test enabled)
ST_XL	Linear acceleration sensor self-test enable. Default value: 0 (0: Self-test disabled; 1: Self-test enabled)

7.29 INT_GEN_SRC_XL (26h)

Linear acceleration sensor interrupt source register.

Table 78. INT_GEN_SRC_XL register

0	IA_XL	ZH_XL	ZL_XL	YH_XL	YL_XL	XH_XL	XL_XL

Table 79. INT_GEN_SRC_XL register description

IA_XL	Interrupt active. Default value: 0. (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH_XL	Accelerometer's Z high event. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL_XL	Accelerometer's Z low event. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH_XL	Accelerometer's Y high event. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL_XL	Accelerometer's Y low event. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH_XL	Accelerometer's X high event. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL_XL	Accelerometer's X low. event. Default value: 0 (0: no interrupt, 1: X low event has occurred)

7.30 STATUS_REG (27h)

Status register.

Table 80. STATUS_REG register

0	IG_XL	IG_G	INACT	BOOT_ STATUS	TDA	GDA	XLDA

Table 81. STATUS_REG register description

IG_XL	Accelerometer interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
IG_G	Gyroscope interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
INACT	Inactivity interrupt output signal. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
BOOT_ STATUS	Boot running flag signal. Default value: 0 (0: no boot running; 1: boot running)
TDA	Temperature sensor new data available. Default value: 0 (0: a new data is not yet available; 1: a new data is available)
GDA	Gyroscope new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
XLDA	Accelerometer new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)

7.31 OUT_X_XL (28h - 29h)

Linear acceleration sensor X-axis output register. The value is expressed as a 16-bit word in two's complement.

7.32 OUT_Y_XL (2Ah - 2Bh)

Linear acceleration sensor Y-axis output register. The value is expressed as a 16-bit word in two's complement.

7.33 OUT_Z_XL (2Ch - 2Dh)

Linear acceleration sensor Z-axis output register. The value is expressed as a 16-bit word in two's complement.

7.34 FIFO_CTRL (2Eh)

FIFO control register.

Table 82. FIFO_CTRL register

FMODE2	FMODE1	FMODE0	FTH4	FTH3	FTH2	FTH1	FTH0

Table 83. FIFO_CTRL register description

FMODE [2:0]	FIFO mode selection bits. Default value: 000 For further details refer to *Table 84*.
FTH [4:0]	FIFO threshold level setting. Default value: 0 0000

Table 84. FIFO mode selection

FMODE2	FMODE1	FMODE0	Mode
0	0	0	Bypass mode. FIFO turned off
0	0	1	FIFO mode. Stops collecting data when FIFO is full.
0	1	0	Reserved
0	1	1	Continuous mode until trigger is deasserted, then FIFO mode.
1	0	0	Bypass mode until trigger is deasserted, then Continuous mode.
1	1	0	Continuous mode. If the FIFO is full, the new sample over-writes the older sample.

7.35 FIFO_SRC (2Fh)

FIFO status control register.

Table 85. FIFO_SRC register

FTH	OVRN	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0

Table 86. FIFO_SRC register description

FTH	FIFO threshold status. (0: FIFO filling is lower than threshold level; 1: FIFO filling is equal or higher than threshold level
OVRN	FIFO overrun status. (0: FIFO is not completely filled; 1: FIFO is completely filled and at least one samples has been overwritten) For further details refer to *Table 87*.
FSS [5:0]	Number of unread samples stored into FIFO. (000000: FIFO empty; 100000: FIFO full, 32 unread samples) For further details refer to *Table 87*.

Table 87. FIFO_SRC example: OVR/FSS details

FTH	OVRN	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0	Description
0	0	0	0	0	0	0	0	FIFO empty
--(1)	0	0	0	0	0	0	1	1 unread sample
...								
--(1)	0	1	0	0	0	0	0	32 unread samples
1	1	1	0	0	0	0	0	At least one sample has been overwritten

1. When the number of unread samples in FIFO is greater than the threshold level set in register *FIFO_CTRL (2Eh)*, FTH value is '1'.

7.36 INT_GEN_CFG_G (30h)

Angular rate sensor interrupt generator configuration register.

Table 88. INT_GEN_CFG_G register

AOI_G	LIR_G	ZHIE_G	ZLIE_G	YHIE_G	YLIE_G	XHIE_G	XLIE_G

Table 89. INT_GEN_CFG_G register description

AOI_G	AND/OR combination of gyroscope's interrupt events. Default value: 0 (0: OR combination; 1: AND combination)
LIR_G	Latch Gyroscope interrupt request. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
ZHIE_G	Enable interrupt generation on gyroscope's yaw (Z) axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value higher than preset threshold)
ZLIE_G	Enable interrupt generation on gyroscope's yaw (Z) axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value lowerthan preset threshold)
YHIE_G	Enable interrupt generation on gyroscope's roll (Y) axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value higher than preset threshold)
YLIE_G	Enable interrupt generation on gyroscope's roll (Y) axis low event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value lower than preset threshold)
XHIE_G	Enable interrupt generation on gyroscope's pitch (X) axis high event. Default value: 0 (0: disable interrupt request; 1: interrupt request on measured angular rate value higher than preset threshold)
XLIE_G	Enable interrupt generation on gyroscope's pitch (X) axis low event. Default value: 0. (0: disable interrupt request; 1: interrupt request on measured angular rate value lower than preset threshold)

7.37 INT_GEN_THS_X_G (31h - 32h)

Angular rate sensor interrupt generator threshold registers. The value is expressed as a 15-bit word in two's complement.

Table 90. INT_GEN_THS_XH_G register

DCRM_G	THS_G_X14	THS_G_X13	THS_G_X12	THS_G_X11	THS_G_X10	THS_G_X9	THS_G_X8

Table 91. INT_GEN_THS_XL_G register

THS_G_X7	THS_G_X6	THS_G_X5	THS_G_X4	THS_G_X3	THS_G_X2	THS_G_X1	THS_G_X0

Table 92. INT_GEN_THS_X_G register description

DCRM_G	Decrement or reset counter mode selection. Default value: 0 (0: Reset; 1: Decrement, as per counter behavior in *Figure 29* and *Figure 30*)
THS_G_X [14:0]	Angular rate sensor interrupt threshold on pitch (X) axis. Default value: 0000000 00000000

7.38 INT_GEN_THS_Y_G (33h - 34h)

Angular rate sensor interrupt generator threshold registers. The value is expressed as a 15-bit word in two's complement.

Table 93. INT_GEN_THS_YH_G register

0(1)	THS_G_Y14	THS_G_Y13	THS_G_Y12	THS_G_Y11	THS_G_Y10	THS_G_Y9	THS_G_Y8

1. This bit must be set to '0' for the correct operation of the device.

Table 94. INT_GEN_THS_YL_G register

THS_G_Y7	THS_G_Y6	THS_G_Y5	THS_G_Y4	THS_G_Y3	THS_G_Y2	THS_G_Y1	THS_G_Y0

Table 95. INT_GEN_THS_Y_G register description

THS_G_Y [14:0]	Angular rate sensor interrupt threshold on roll (Y) axis. Default value: 0000000 00000000.

7.39 INT_GEN_THS_Z_G (35h - 36h)

Angular rate sensor interrupt generator threshold registers. The value is expressed as a 15-bit word in two's complement.

Table 96. INT_GEN_THS_ZH_G register

0(1)	THS_G_Z14	THS_G_Z13	THS_G_Z12	THS_G_Z11	THS_G_Z10	THS_G_Z9	THS_G_Z8

1. This bit must be set to '0' for the correct operation of the device.

Table 97. INT_GEN_THS_ZL_G register

THS_G_Z7	THS_G_Z6	THS_G_Z5	THS_G_Z4	THS_G_Z3	THS_G_Z2	THS_G_Z1	THS_G_Z0

Table 98. INT_GEN_THS_Z_G register description

THS_G_Z [14:0]	Angular rate sensor interrupt thresholds on yaw (Z) axis. Default value: 0000000 00000000.

7.40 INT_GEN_DUR_G (37h)

Angular rate sensor interrupt generator duration register.

Table 99. INT_GEN_DUR_G register

WAIT_G	DUR_G6	DUR_G5	DUR_G4	DUR_G3	DUR_G2	DUR_G1	DUR_G0

Table 100. INT_GEN_DUR_G register description

WAIT_G	Exit from interrupt wait function enable. Default value: 0 (0: wait function off; 1: wait for DUR_G [6:0] samples before exiting interrupt)
DUR_G [6:0]	Enter/exit interrupt duration value. Default Value: 000 0000

The **DUR_G [6:0]** bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

The **WAIT_G** bit has the following meaning:

'0': the interrupt falls immediately if the signal crosses the selected threshold

'1': if the signal crosses the selected threshold, the interrupt falls after a number of samples equal to the value of the duration counter register.

For further details refer to *Figure 29* and *Figure 30*.

Figure 29. Wait bit disabled

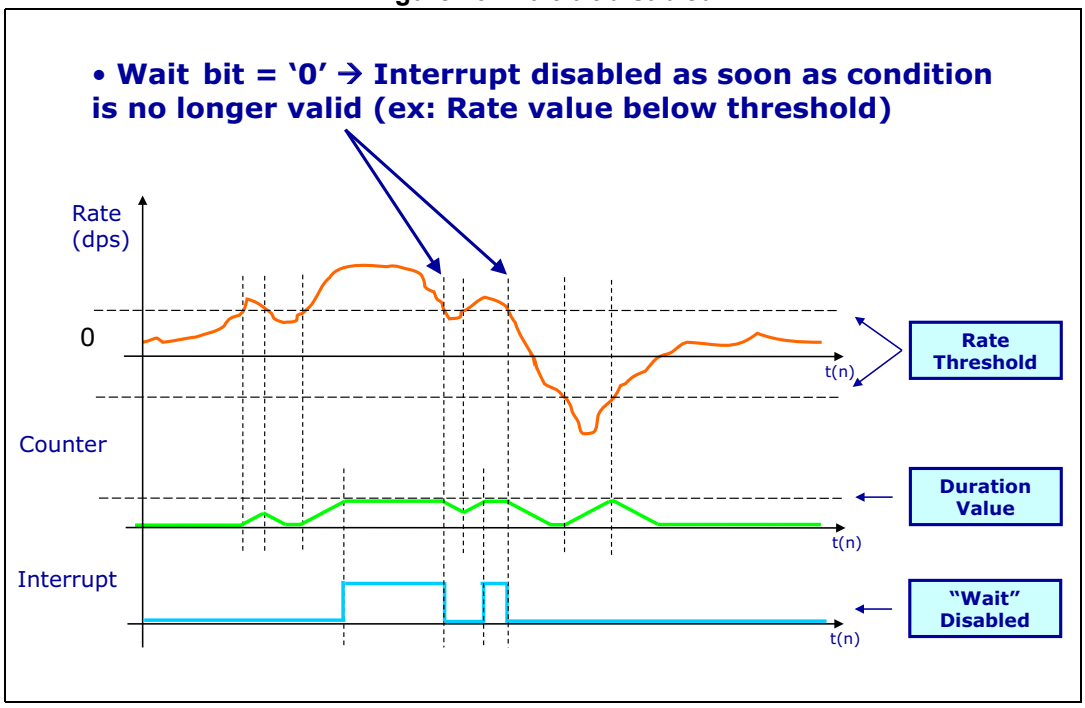
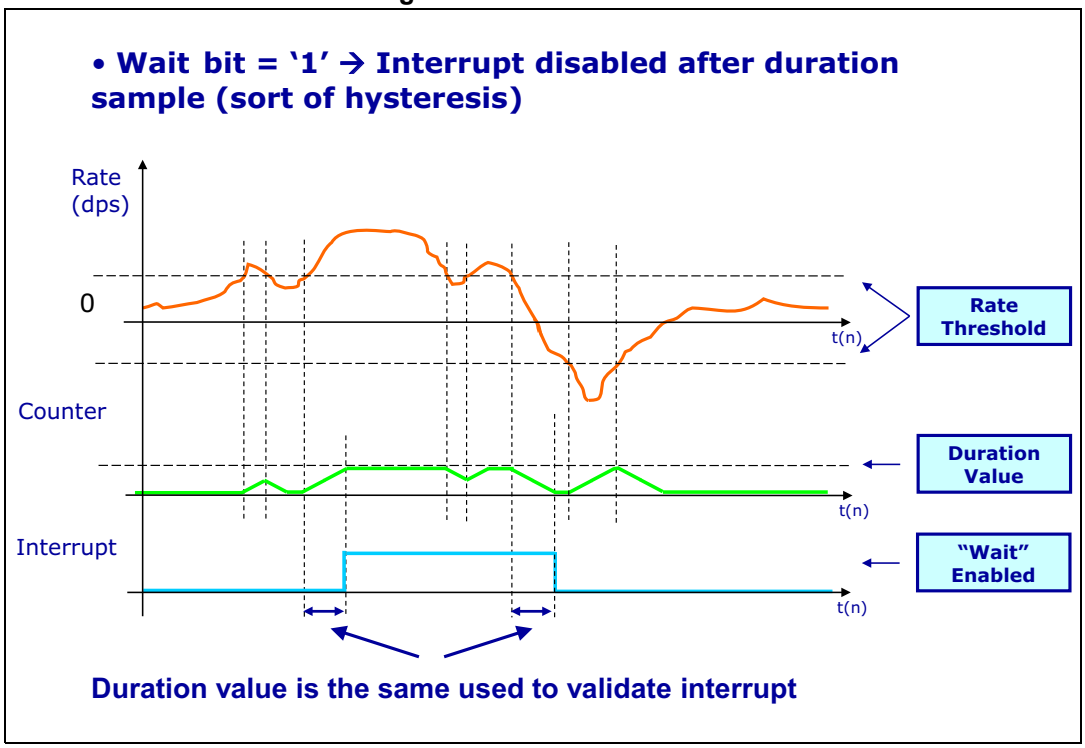


Figure 30. Wait bit enabled



8 Magnetometer register description

8.1 OFFSET_X_REG_L_M (05h), OFFSET_X_REG_H_M (06h)

This register is a 16-bit register and represents the X offset used to compensate environmental effects (data is expressed as two's complement). This value acts on the magnetic output data value in order to subtract the environmental offset.

Default value: 0

Table 101. OFFSET_X_REG_L_M register

OFXM7	OFXM6	OFXM5	OFXM4	OFXM3	OFXM2	OFXM1	OFXM0

Table 102. OFFSET_X_REG_H_M register

OFXM15	OFXM14	OFXM13	OFXM12	OFXM11	OFXM10	OFXM9	OFXM8

8.2 OFFSET_Y_REG_L_M (07h), OFFSET_Y_REG_H_M (08h)

This register is a 16-bit register and represents the Y offset used to compensate environmental effects (data is expressed as two's complement). This value acts on the magnetic output data value in order to subtract the environmental offset.

Default value: 0

Table 103. OFFSET_Y_REG_L_M register

OFYM7	OFYM6	OFYM5	OFYM4	OFYM3	OFYM2	OFYM1	OFYM0

Table 104. OFFSET_Y_REG_H_M register

OFYM15	OFYM14	OFYM13	OFYM12	OFYM11	OFYM10	OFYM9	OFYM8

8.3 OFFSET_Z_REG_L_M (09h), OFFSET_Z_REG_H_M (0Ah)

This register is a 16-bit register and represents the Z offset used to compensate environmental effects (data is expressed as two's complement). This value acts on the magnetic output data value in order to subtract the environmental offset.

Default value: 0.

Table 105. OFFSET_Z_REG_L_M register

OFZM7	OFZM6	OFZM5	OFZM4	OFZM3	OFZM2	OFZM1	OFZM0

Table 106. OFFSET_Z_REG_H_M register

OFZM15	OFZM14	OFZM13	OFZM12	OFZM11	OFZM10	OFZM9	OFZM8

8.4 WHO_AM_I_M (0Fh)

Device identification register.

Table 107. WHO_AM_I_M register

0	0	1	1	1	1	0	1

8.5 CTRL_REG1_M (20h)

Table 108. CTRL_REG1_M register

TEMP_ COMP	OM1	OM0	DO2	DO1	DO0	FAST_ODR	ST

Table 109. CTRL_REG1_M register description

TEMP_COMP	Temperature compensation enable. Default value: 0 (0: temperature compensation disabled; 1: temperature compensation enabled)
OM[1:0]	X and Y axes operative mode selection. Default value: 00 (Refer to *Table 110*)
DO[2:0]	Output data rate selection. Default value: 100 (Refer to *Table 111*)
FAST_ODR	FAST_ODR enables data rates higher than 80 Hz. Default value: 0 (0: Fast_ODR disabled; 1: FAST_ODR enabled)
ST	Self-test enable. Default value: 0 (0: self-test disabled; 1: self-test enabled)

Table 110. X and Y axes operative mode selection

OM1	OM0	Operative mode for X and Y axes
0	0	Low-power mode
0	1	Medium-performance mode
1	0	High-performance mode
1	1	Ultra-high performance mode

Table 111. Output data rate configuration

DO2	DO1	DO0	ODR [Hz]
0	0	0	0.625
0	0	1	1.25
0	1	0	2.5
0	1	1	5
1	0	0	10
1	0	1	20
1	1	0	40
1	1	1	80

8.6 CTRL_REG2_M (21h)

Table 112. CTRL_REG2_M register

0(1)	FS1	FS0	0(1)	REBOOT	SOFT_RST	0(1)	0(1)

1. These bits must be set to '0' for the correct operation of the device.

Table 113. CTRL_REG2_M register description

FS[1:0]	Full-scale configuration. Default value: 00 Refer to *Table 114*
REBOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
SOFT_RST	Configuration registers and user register reset function. (0: default value; 1: reset operation)

Table 114. Full-scale selection

FS1	FS0	Full scale
0	0	± 4 gauss
0	1	± 8 gauss
1	0	± 12 gauss
1	1	± 16 gauss

8.7 CTRL_REG3_M (22h)

Table 115. CTRL_REG3_M register

I2C_ DISABLE	0(1)	LP	0(1)	0(1)	SIM	MD1	MD0

1. These bits must be set to '0' for the correct operation of the device.

Table 116. CTRL_REG3_M register description

I2C_DISABLE	Disable I^2C interface. Default value 0. (0: I^2C enable; 1: I^2C disable)
LP	Low-power mode configuration. Default value: 0 If this bit is '1', the DO[2:0] is set to 0.625 Hz and the system performs, for each channel, the minimum number of averages. Once the bit is set to '0', the magnetic data rate is configured by the DO bits in the *CTRL_REG1_M (20h)* register.
SIM	SPI Serial Interface mode selection. Default value: 0 (0: SPI only write operations enabled; 1: SPI read and write operations enable).
MD[1:0]	Operating mode selection. Default value: 11 Refer to *Table 117.*

Table 117. System operating mode selection

MD1	MD0	Mode
0	0	Continuous-conversion mode
0	1	Single-conversion mode
1	0	Power-down mode
1	1	Power-down mode

8.8 CTRL_REG4_M (23h)

Table 118. CTRL_REG4_M register

0(1)	0(1)	0(1)	0(1)	OMZ1	OMZ0	BLE	0(1)

1. These bits must be set to '0' for the correct operation of the device

Table 119. CTRL_REG4_M register description

OMZ[1:0]	Z-axis operative mode selection. Default value: 00. Refer to *Table 120.*
BLE	Big/Little Endian data selection. Default value: 0 (0: data LSb at lower address; 1: data MSb at lower address)

Table 120. Z-axis operative mode selection

OMZ1	OMZ0	Operative mode for Z-axis
0	0	Low-power mode
0	1	Medium-performance mode
1	0	High-performance mode
1	1	Ultra-high performance mode

8.9 CTRL_REG5_M (24h)

Table 121. CTRL_REG5_M register

FAST_READ	BDU	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)

1. These bits must be set to '0' for the correct operation of the device.

Table 122. CTRL_REG5_M register description

FAST_READ	FAST_READ allows reading the high part of DATA OUT only in order to increase reading efficiency. Default value: 0 (0: FAST_READ disabled; 1: FAST_READ enabled)
BDU	Block data update for magnetic data. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)

8.10 STATUS_REG_M (27h)

Table 123. STATUS_REG_M register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 124. STATUS_REG_M register description

ZYXOR	X, Y and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous set)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X, Y and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X-axis new data available. Default value: 0 (0: a new data for the X-axis is not yet available; 1: a new data for the X-axis is available)

8.11 OUT_X_L_M (28h), OUT_X_H_M(29h)

Magnetometer X-axis data output. The value of the magnetic field is expressed as two’s complement.

8.12 OUT_Y_L_M (2Ah), OUT_Y_H_M (2Bh)

Magnetometer Y-axis data output. The value of the magnetic field is expressed as two’s complement.

8.13 OUT_Z_L_M (2Ch), OUT_Z_H_M (2Dh)

Magnetometer Z-axis data output. The value of the magnetic field is expressed as two’s complement.

8.14 INT_CFG_M (30h)

Table 125. INT_CFG_M register

XIEN	YIEN	ZIEN	0(1)	0(1)	IEA	IEL	IEN

1. This bit must be set to '0' for the correct operation of the device.

Table 126. INT_CFG_M register description

XIEN	Enable interrupt generation on X-axis. Default value: 0 0: disable interrupt request; 1: enable interrupt request
YIEN	Enable interrupt generation on Y-axis. Default value: 0 0: disable interrupt request; 1: enable interrupt request
ZIEN	Enable interrupt generation on Z-axis. Default value: 0 0: disable interrupt request; 1: enable interrupt request
IEA	Interrupt active configuration on INT_MAG. Default value: 0 0: low; 1: high
IEL	Latch interrupt request. Default value: 0 0: interrupt request latched; 1: interrupt request not latched) Once latched, the INT_M pin remains in the same state until *INT_SRC_M (31h)*) is read.
IEN	Interrupt enable on the INT_M pin. Default value: 0 0: disable; 1: enable

8.15 INT_SRC_M (31h)

Table 127. INT_SRC_M register

PTH_X	PTH_Y	PTH_Z	NTH_X	NTH_Y	NTH_Z	MROI(1)	INT

1. This functionality can be enabled only if the IEN bit in *INT_CFG_M (30h)* is enabled.

Table 128. INT_SRC_M register description

PTH_X	Value on X-axis exceeds the threshold on the positive side. Default value: 0
PTH_Y	Value on Y-axis exceeds the threshold on the positive side. Default value: 0
PTH_Z	Value on Z-axis exceeds the threshold on the positive side. Default value: 0
NTH_X	Value on X-axis exceeds the threshold on the negative side. Default value: 0
NTH_Y	Value on Y-axis exceeds the threshold on the negative side. Default value: 0
NTH_Z	Value on Z-axis exceeds the threshold on the negative side. Default value: 0
MROI	Internal measurement range overflow on magnetic value. Default value: 0
INT	This bit signals when the interrupt event occurs.

8.16 INT_THS_L(32h), INT_THS_H(33h)

Interrupt threshold. Default value: 0.

The value is expressed in 15-bit unsigned.

Even if the threshold is expressed in absolute value, the device detects both positive and negative thresholds.

Table 129. INT_THS_L_M register

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 130. INT_THS_H_M register

0(1)	THS14	THS13	THS12	THS11	THS10	THS9	THS8

1. This bit must be set to ‘0’ for the correct operation of the device.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

9.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

9.2 LGA package information

Figure 31. LGA (3.5x3x1 mm) 24-lead package outline

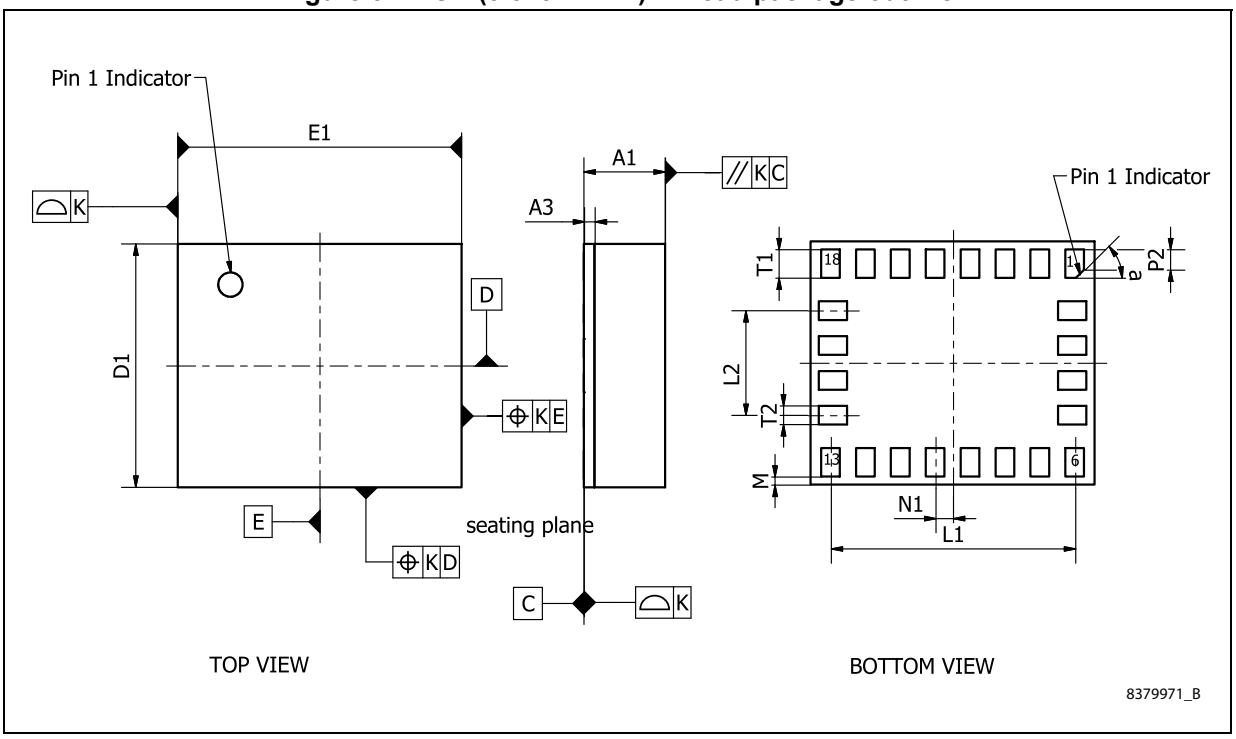


Table 131. LGA (3.5x3x1 mm) 24-lead package mechanical data

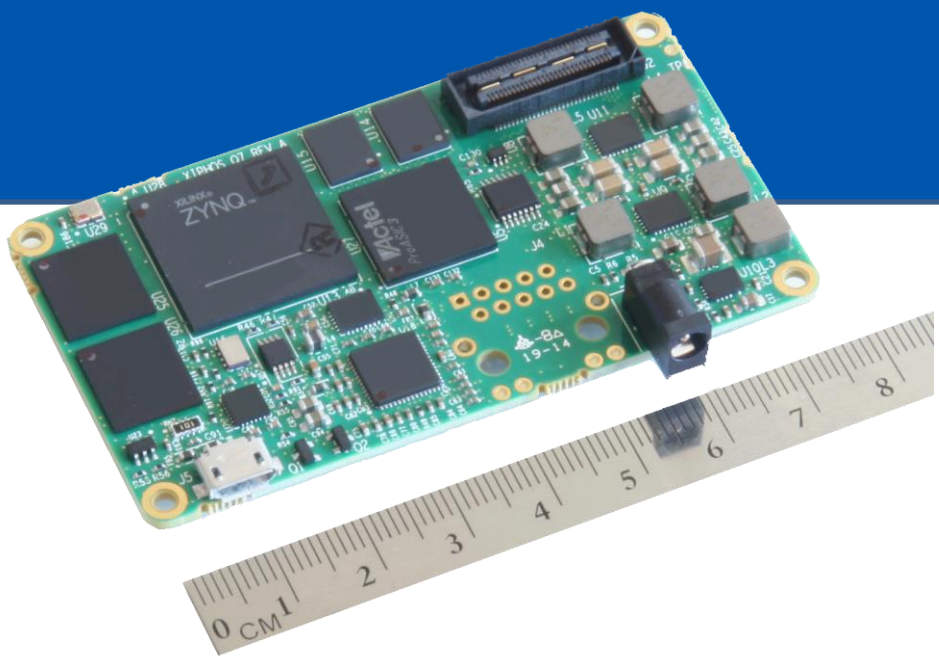
Dim.	mm		
	Min.	Typ.	Max.
A1		1.000	1.027
A3		0.130	
D1	2.850	3.000	3.150
E1	3.350	3.500	3.650
L1	2.960	3.010	3.060
L2	1.240	1.290	1.340
N1	0.165	0.215	0.265
P2	0.200	0.250	0.300
a		45°	
T1	0.300	0.350	0.400
T2	0.180	0.230	0.280
K		0.050	
M		0.100	

10 Revision history

Table 132. Document revision history

Date	Revision	Changes
18-Dec-2013	1	Initial release
05-Nov-2014	2	Datasheet status promoted from preliminary to production data Added ±16 *g* linear acceleration full scale throughout datasheet Corrected typo in footnote *3*, *4* and *5* of *Table 2: Pin description* Updated *Figure 15: LSM9DS1 electrical connections* and *Section 4.1: External capacitors* Updated *Table 117: System operating mode selection*
12-Mar-2015	3	Added FAST_ODR bit to *CTRL_REG1_M (20h)* Added FAST_READ bit to *CTRL_REG5_M (24h)*

Q7S SPECIFICATIONS



Q7S

FEATURE HIGHLIGHTS

Industry-Leading Performance	The Q7S features an All-Programmable System-on-Chip (AP SoC), including multi-core CPUs supported by massive programmable logic resources and a wide array of hardware interfaces.
Low Mass, Volume, Power	The Q7S measures 78 mm x 43 mm x 9 mm, has a mass of 24 g (excluding connectors) and consumes 2 W for typical applications. Its small size, low mass and power consumption make the Q7 ideal for aerospace applications.
Flexible Interfacing	The Q7S provides Gigabit Ethernet networking through its RJ45 connector and USB 2.0 OTG. The Q7S also provides multiple digital I/O lines, including up to 24 LVDS pairs, and selectable RS-232/422/485 through its mezzanine connectors.

Q7S features for robustness in space:

Radiation Tolerance	The Q7S has been tested beyond 25 krad (TID).
TMR Logic	TMR (Triple Mode Redundancy) can prevent errors in the firmware from propagating and in some cases, correct them.
EDAC for RAM	EDAC (Error Detection and Correction) logic and software can detect and correct errors and scrub the RAM
Health Monitoring	The Q7S can detect error events and failures, monitor system statistics and report these as telemetry.
And several others…	Other features based on years of flight heritage, such as low power modes, multiple firmware and software images, and Zynq logic scrubbing.

OVERVIEW

The Q7S is the latest in the Xiphos Q-Card family of low-cost, embedded nodes for control, processing and interface applications, primarily for aerospace markets. Q-Cards combine a small form factor with broad networking, processing and I/O capabilities.

The Q7S consists of a Q7 card which is specially equipped with space-ready software and firmware, and rigorously tested.

At the core of each Q7S is a hybrid environment of powerful CPUs and reprogrammable logic, providing consistent, reliable performance. The library of logic and software functions is augmented by onboard analog and digital I/O.

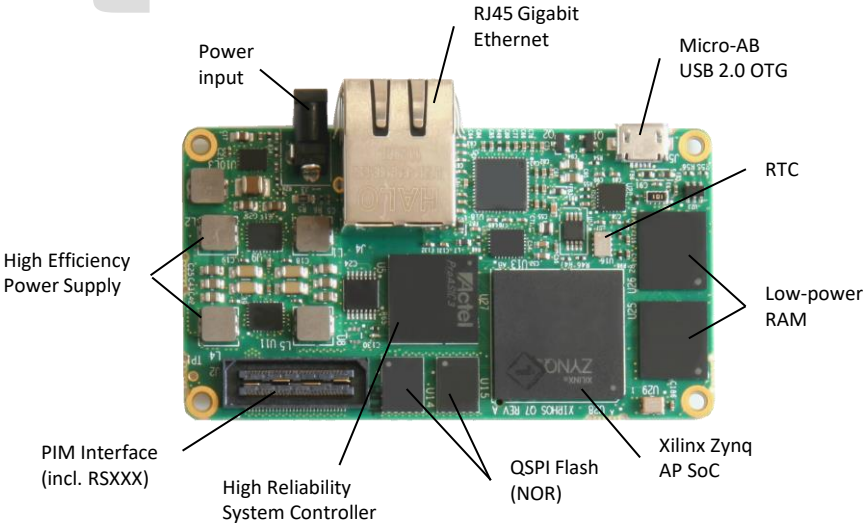
FLIGHT HERITAGE

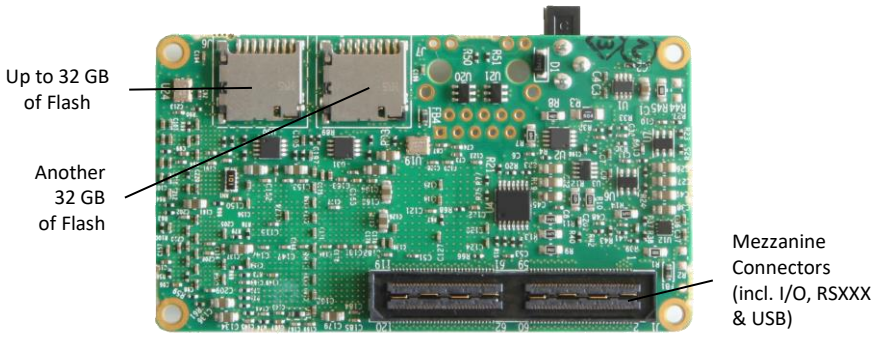
- The Q7S has been operating in orbit since June 2016. The Q7S is certified for manned space flight and is used on the International Space Station (ISS).
- The Q6 was first flown in August 2011, with almost 100 units delivered to customers worldwide. The Q6 was also certified for manned space flight and used on the ISS.
- The Q5 was first flown in June 2004.
- The Q4 was first flown in December 2002, and was also certified for manned space flight and used on the ISS.

Xiphos Technologies

Q7S

Front & Back





Product Integration Module (PIM)
Each Q7S is delivered with a detachable PIM, to facilitate development. The PIM provides standard commercial interfaces (e.g. CAN, JTAG, 4 analog input, 1-wire) , debug LEDs and other lab development features.

Software Development
Xiphos provides an Application Development Kit with standard Linux libraries for C/C++ to support software development on Linux workstations. ***Code previously developed for Linux desktop and server applications can be easily ported to the Q7S.*** Q7S hardware and logic interfaces are all accessible through either standard Linux and Xilinx kernel drivers or custom drivers provided by Xiphos.

Logic Development
Logic development uses standard Xilinx development tools. Xiphos, Xilinx and many third-party vendors also provide a wide range of compatible reusable logic cores for Xilinx FPGAs.

Xiphos Technologies

Characteristics

Memory
- Independent 1x512 MB (256 MB with ECC) and 1x256 MB LPDDR2 RAM chips
- 2 MicroSD slots (max. 32 GB each) on independent buses / power control
- 2x128 MB QSPI Flash (NOR)
- External mass memory interface

All-Programmable System-on-Chip
- Xilinx Zynq-7020
- ARM dual-core Cortex-A9 MPCore processors each up to 766 MHz
- 106,400 flip-flops (FF), 53,200 look-up tables (LUT), and 220 DSP slices

Control FPGA
- Microsemi ProASIC3

Operating System
- Linux 4.14 LTS
- Robot Operating System (ROS)

Real Time Clock
- RTC with sleep & wake-up on alarm/interrupt
- Dedicated power pin for external battery

Power
- Scalable, typ. 2 W
- 6 V to 15 V (5 V to 28 V option)
- Power modes (including deep sleep)
- Overcurrent detection and protection

Mass
- 32 g with RJ45 connector
- 24 g without RJ45 connector

Form Factor
- 78 mm x 43 mm x 19 mm (with RJ45 connector)
- 78 mm x 43 mm x 9 mm (without connectors)

Environmental
- Operating Temperature -40 to +60ºC
- TVAC, shock and vibe, TID > 25 krad

Interfaces
- Gigabit Ethernet (RJ45)
- USB 2.0 (Micro-AB)
- Factory-selectable RS232/422/485
- CAN Bus controller
- 90 I/O, with up to 24 LVDS pairs (mezzanine connector)

Space-Qualified Software and Logic
- Triple-mode redundancy
- EDAC-protected RAM
- Upset and multi-current monitoring
- FPGA bit-stream scrubbing
- Software robustness / watchdog

www.xiphos.com

MR20H40 - 50MHz/20ns ^{t}SCK 4Mb SPI Interface MRAM
MR25H40 - 40MHz/25ns ^{t}SCK 4Mb SPI Interface MRAM
For more information on product options, see **"Table 16 – Ordering Part Numbers" on page 25**.

FEATURES

- No write delays
- Unlimited write endurance
- Data retention greater than 20 years
- Automatic data protection on power loss
- Fast, simple SPI interface, up to 50 MHz clock rate with MR20H40.
- 3.0 to 3.6 Volt power supply range
- Low-current sleep mode
- Commercial (0 to 70°C), Industrial (-40 to 85°C), Extended (-40 to 105°C), and AEC-Q100 Grade 1 (-40 to 125°C) temperature range options.
- Available in 8-pin DFN or 8-pin DFN Small Flag, RoHS-compliant packages.
- Direct replacement for serial EEPROM, Flash, and FeRAM
- MSL Level 3

8-DFN

8-DFN Small Flag

RoHS

DESCRIPTION

MR2xH40 is a family of 4,194,304-bit magnetoresistive random access memory (MRAM) devices organized as 524,288 words of 8 bits. They are the ideal memory solution for applications that must store and retrieve data and programs quickly using a small number of I/O pins. They have serial EEPROM and serial Flash compatible read/write timing with no write delays and unlimited read/write endurance. Unlike other serial memories, with the MR2xH40 family both reads and writes can occur randomly in memory with no delay between writes.

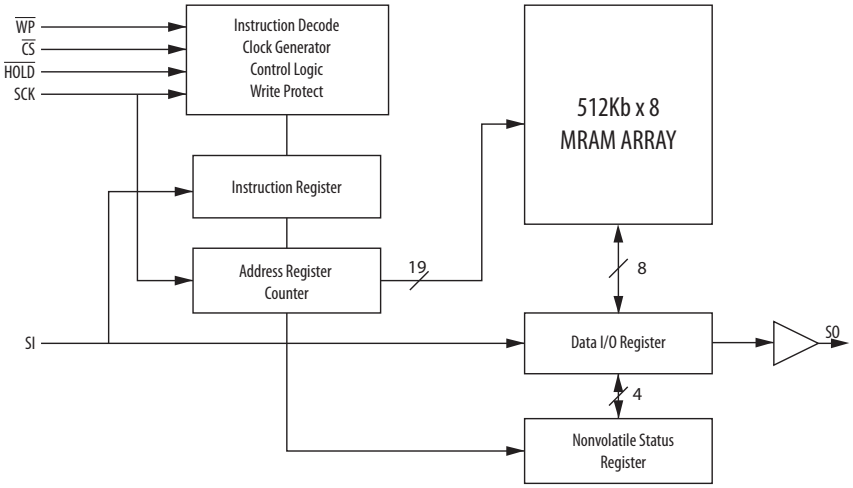
The MR2xH40 family provides highly reliable data storage over a wide range of temperatures. The MR20H40 (50MHz) is offered with Industrial (-40° to 85 °C) range. The MR25H40 (40MHz) is offered with Commercial (0 to 70°C), Industrial (-40° to 85 °C), Extended (-40 to 105°C), and AEC-Q100 Grade 1 (-40°C to 125 °C) operating temperature range options.

Both are available in a 5 x 6mm, 8-pin DFN package. The pinout is compatible with serial SRAM, EEPROM, Flash, and FeRAM products.

OVERVIEW

The MR2xH40 family is an SPI interface MRAM family with a memory array logically organized as 512Kx8 using the four pin interface of chip select ($\overline{CS}$), serial input (SI), serial output (SO) and serial clock (SCK) of the serial peripheral interface (SPI) bus. The MRAM implements a subset of commands common to SPI EEPROM and SPI Flash components. This allows the SPI MRAM to replace these components in the same socket and interoperate on a shared SPI bus. The SPI MRAM offers superior write speed, unlimited endurance, low standby & operating power, and simple, reliable data retention compared to other serial memory alternatives.

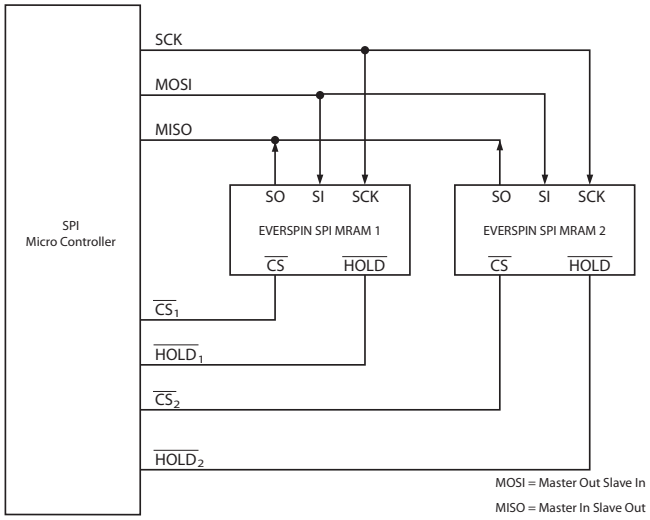
Figure 1 – Block Diagram



System Configuration

Single or multiple devices can be connected to the bus as shown in Figure 2. Pins SCK, SO and SI are common among devices. Each device requires $\overline{CS}$ and $\overline{HOLD}$ pins to be driven separately.

Figure 2 – System Configuration



Pin Functions

Figure 3 – DFN Package Pin Diagram (Top View)

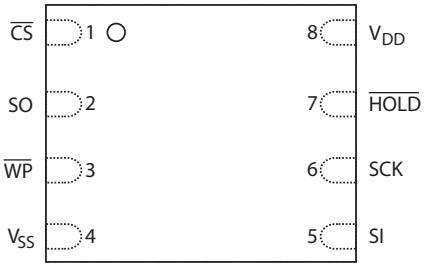


Table 1 – Pin Functions

Signal Name	Pin	I/O	Function	Description
$\overline{CS}$	1	Input	Chip Select	An active low chip select for the serial MRAM. When chip select is high, the memory is powered down to minimize standby power, inputs are ignored and the serial output pin is Hi-Z. Multiple serial memories can share a common set of data pins by using a unique chip select for each memory.
SO	2	Output	Serial Output	The data output pin is driven during a read operation and remains Hi-Z at all other times. SO is Hi-Z when HOLD is low. Data transitions on the data output occur on the falling edge of SCK.
$\overline{WP}$	3	Input	Write Protect	A low on the write protect input prevents write operations to the Status Register.
V_{SS}	4	Reference	Ground	Power supply ground pin.
SI	5	Input	Serial Input	All data is input to the device through this pin. This pin is sampled on the rising edge of SCK and ignored at other times. SI can be tied to SO to create a single bidirectional data bus if desired.
SCK	6	Input	Serial Clock	Synchronizes the operation of the MRAM. The clock can operate up to 50 MHz to shift commands, address, and data into the memory. Inputs are captured on the rising edge of clock. Data outputs from the MRAM occur on the falling edge of clock. The serial MRAM supports both SPI Mode 0 (CPOL=0, CPHA=0) and Mode 3 (CPOL=1, CPHA=1). In Mode 0, the clock is normally low. In Mode 3, the clock is normally high. Memory operation is static so the clock can be stopped at any time.
$\overline{HOLD}$	7	Input	Hold	A low on the Hold pin interrupts a memory operation for another task. When $\overline{HOLD}$ is low, the current operation is suspended. The device will ignore transitions on the $\overline{CS}$ and SCK when $\overline{HOLD}$ is low. All transitions of $\overline{HOLD}$ must occur while $\overline{CS}$ is low.
V_{DD}	8	Supply	Power Supply	Power supply voltage from +3.0 to +3.6 volts.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 6 – Absolute Maximum Ratings

Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

Symbol	Parameter	Conditions	Value	Unit
V_{DD}	Supply voltage [2]		-0.5 to 4.0	V
V_{IN}	Voltage on any pin [2]		-0.5 to V_{DD} + 0.5	V
I_{OUT}	Output current per pin		±20	mA
P_D	Package power dissipation [3]		0.600	W
T_{BIAS}	Temperature under bias	Commercial	-10 to 85	°C
		Industrial	-45 to 95	°C
		Extended	-45 to 115	°C
		AEC-Q100 Grade 1	-45 to 135	°C
T_{stg}	Storage Temperature		-55 to 150	°C
T_{Lead}	Lead temperature during solder (3 minute max)		260	°C
H_{max_write}	Maximum magnetic field during write	Write	12,000	A/m
H_{max_read}	Maximum magnetic field during read or standby	Read or Standby	12,000	A/m

Notes:

1. All voltages are referenced to V_{SS}. The DC value of V_{IN} must not exceed actual applied V_{DD} by more than 0.5V. The AC value of V_{IN} must not exceed applied V_{DD} by more than 2V for 10ns with I_{IN} limited to less than 20mA.
2. Power dissipation capability depends on package characteristics and use environment.

Table 7 – Operating Conditions

Symbol	Parameter	Temp Grade	Min	Max	Unit
V_{DD}	Power supply voltage		3.0	3.6	V
V_{IH}	Input high voltage		2.2	V_{DD} + 0.3	V
V_{IL}	Input low voltage		-0.5	0.8	V
T_A	Ambient temperature under bias	Commercial	0	70	°C
		Industrial	-40	85	°C
		Extended	-40	105	°C
		AEC-Q100 Grade 1 [1]	-40	125	°C

Notes:

1. AEC-Q100 Grade 1 temperature profile assumes 10 percent duty cycle at maximum temperature (2 years out of 20-year life.)

Table 8 – DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
I_{LI}	Input leakage current		-	±1	µA
I_{LO}	Output leakage current		-	±1	µA
V_{OL}	Output low voltage	I_{OL} = +4 mA	-	0.4	V
		I_{OL} = +100 µA	-	V_{SS} + 0.2v	V
V_{OH}	Output high voltage	I_{OH} = -4 mA	2.4	-	V
		I_{OH} = -100 µA	V_{DD} - 0.2	-	V

Table 9 – Power Supply Characteristics

Symbol	Parameter	Conditions	Typical	Max	Unit
I_{DDR}	Active Read Current	@ 1 MHz	5.0	11	mA
		@ 40 MHz	12	17	mA
		@ 50MHz	13.8	18.5	mA
I_{DDW}	Active Write Current	@ 1 MHz	9.0	25	mA
		@ 40 MHz	28	42	mA
		@ 50 MHz	33	46.5	mA
I_{SB1}	AC Standby Current (CS High)	@ 40 MHz	250	400	µA
		@ 50 MHz	650	750	µA
I_{SB2}	CMOS Standby Current (CS High)		90	180	µA
I_{ZZ}	Standby Sleep Mode Current (CS High)		15	40	µA

TIMING SPECIFICATIONS

Capacitance

Table 10 – Capacitance

Symbol	Parameter	Typical	Max	Unit
C_{In}	Control input capacitance [1]	-	6	pF
$C_{I/O}$	Input/Output capacitance [1]	-	8	pF

Notes:

1. f = 1.0 MHz, dV = 3.0 V, T_A = 25 °C, periodically sampled rather than 100% tested.

AC Measurement Conditions

Table 11 – AC Measurement Conditions

Parameter	Value	Unit
Logic input timing measurement reference level	1.5	V
Logic output timing measurement reference level	1.5	V
Logic input pulse levels	0 or 3.0	V
Input rise/fall time	2	ns
Output load for low and high impedance parameters	See Figure 12	
Output load for all other timing parameters	See Figure 13	

Figure 12 – Output Load for Impedance Parameter Measurements

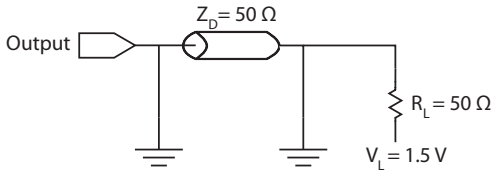
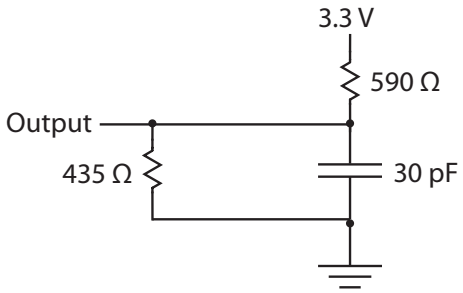


Figure 13 – Output Load for all Other Parameter Measurements



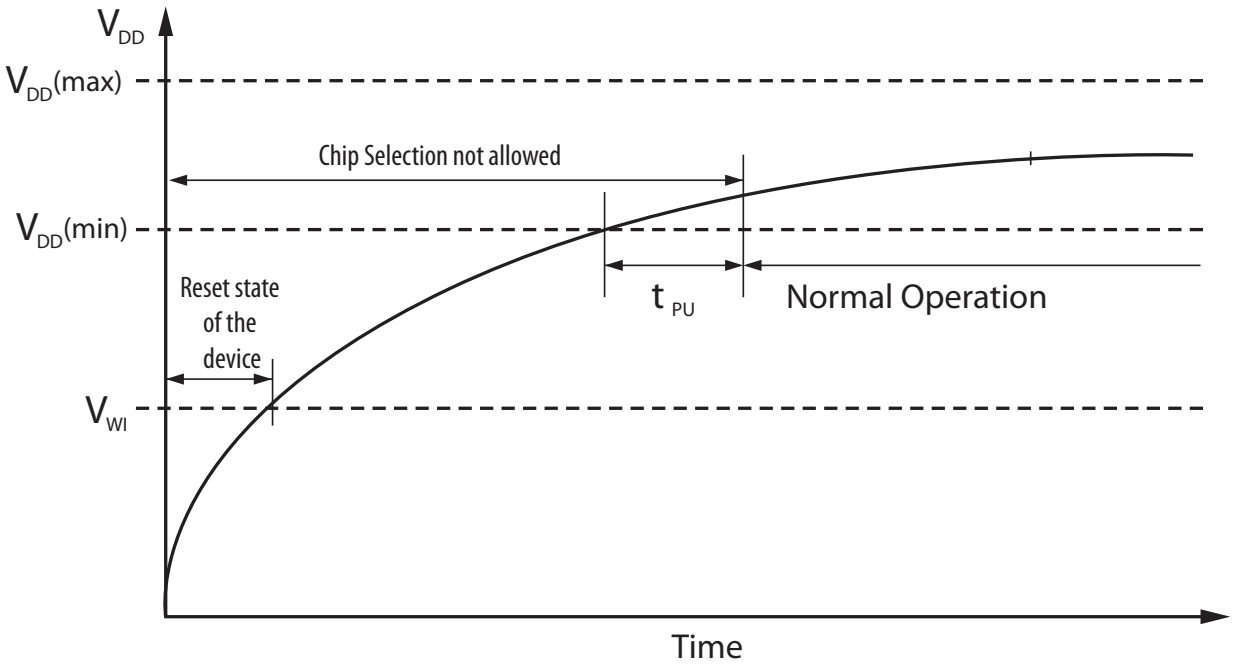
Power Up Timing

The MR2xH40 is not accessible for a start-up time, ^{t}PU= 400 µs after power up. Users must wait this time from the time when V_{DD} (min) is reached until the first $\overline{CS}$ low to allow internal voltage references to become stable. The $\overline{CS}$ signal should be pulled up to V_{DD} so that the signal tracks the power supply during power-up sequence.

Table 12 – Power-Up Timing

Symbol	Parameter	Min	Typical	Max	Unit
V_{WI}	Write Inhibit Voltage	2.2	-	-	V
^{t}PU	Startup Time	400	-	-	µs

Figure 14 – Power-Up Timing



AC Timing Parameters

Table 13 – MR20H40 (^{f}SCK = 50MHz) AC Timing Parameters

Industrial Temperature Range, V_{DD}=3.0 to 3.6 V, C_L= 30 pF for all values.

Symbol	Parameter	Temp Range	Min	Typical	Max	Unit
^{f}SCK	SCK Clock Frequency	Industrial	0	-	50	MHz
^{t}RI	Input Rise Time	Industrial	-	-	50	ns
^{t}RF	Input Fall Time	Industrial	-	-	50	ns
^{t}WH	SCK High Time	Industrial	7	-	-	ns
^{t}WL	SCK Low Time	Industrial	7	-	-	ns
Synchronous Data Timing see Figure 15						
^{t}CS	CS High Time	Industrial	40	-	-	ns
^{t}CSS	CS Setup Time	Industrial	5	-	-	ns
^{t}CSH	CS Hold Time	Industrial	5	-	-	ns
^{t}SU	Data In Setup Time	Industrial	2	-	-	ns
^{t}H	Data In Hold Time	Industrial	5	-	-	ns
^{t}V	Output Valid	Industrial	0	-	9	ns
^{t}HO	Output Hold Time	Industrial	0	-	-	ns
HOLD Timing see Figure 16						
^{t}HD	HOLD Setup Time	Industrial	5	-	-	ns
^{t}CD	HOLD Hold Time	Industrial	5	-	-	ns
^{t}LZ	HOLD to Output Low Impedance	Industrial	-	-	20	ns
^{t}HZ	HOLD to Output High Impedance	Industrial	-	-	20	ns
Other Timing Specifications						
^{t}WPS	WP Setup To CS Low	Industrial	5	-	-	ns
^{t}WPH	WP Hold From CS High	Industrial	5	-	-	ns
^{t}DP	Sleep Mode Entry Time	Industrial	3	-	-	µs
^{t}RDP	Sleep Mode Exit Time	Industrial	400	-	-	µs
^{t}DIS	Output Disable Time	Industrial	12	-	-	ns

Table 14 – MR25H40 (^{f}SCK = 40MHz) AC Timing Parameters

Commercial Industrial, Extended and AEC-Q100 Grade 1 Temperature Ranges, V_{DD}=3.0 to 3.6 V, C_L= 30 pF for all values.

Symbol	Parameter	Temp Grade	Min	Typical	Max	Unit
^{f}SCK	SCK Clock Frequency	All	0	-	40	MHz
^{t}RI	Input Rise Time	All	-	-	50	ns
^{t}RF	Input Fall Time	All	-	-	50	ns
^{t}WH	SCK High Time	All	11	-	-	ns
^{t}WL	SCK Low Time	All	11	-	-	ns
Synchronous Data Timing see Figure 15						
^{t}CS	CS High Time	All	40	-	-	ns
^{t}CSS	CS Setup Time	All	10	-	-	ns
^{t}CSH	CS Hold Time	All	10	-	-	ns
^{t}SU	Data In Setup Time	All	5	-	-	ns
^{t}H	Data In Hold Time	All	5	-	-	ns
^{t}V	Output Valid	Comm./Ind./Ext.	0	-	9	ns
		AEC-Q100 Grade 1	0	-	10	ns
^{t}HO	Output Hold Time	All	0	-	-	ns

Table continues next page.

Table 14 (Cont'd) - MR25H40 (^{f}SCK = 40MHz) AC Timing Parameters

Commercial, Industrial, Extended and AEC-Q100 Grade 1 Temperature Ranges, V_{DD}=3.0 to 3.6 V, C_L= 30 pF for all values.

HOLD Timing see Figure 16						
Symbol	**Parameter**	**Temp Grade**	**Min**	**Typical**	**Max**	**Unit**
^{t}HD	HOLD Setup Time	All	10	-	-	ns
^{t}CD	HOLD Hold Time	All	10	-	-	ns
^{t}LZ	HOLD to Output Low Impedance	All	-	-	20	ns
^{t}HZ	HOLD to Output High Impedance	All	-	-	20	ns
Other Timing Specifications						
^{t}WPS	WP Setup To CS Low	All	5	-	-	ns
^{t}WPH	WP Hold From CS High	All	5	-	-	ns
^{t}DP	Sleep Mode Entry Time	All	3	-	-	µs
^{t}RDP	Sleep Mode Exit Time	All	400	-	-	µs
^{t}DIS	Output Disable Time	All	12	-	-	ns

Table 16 – Ordering Part Numbers

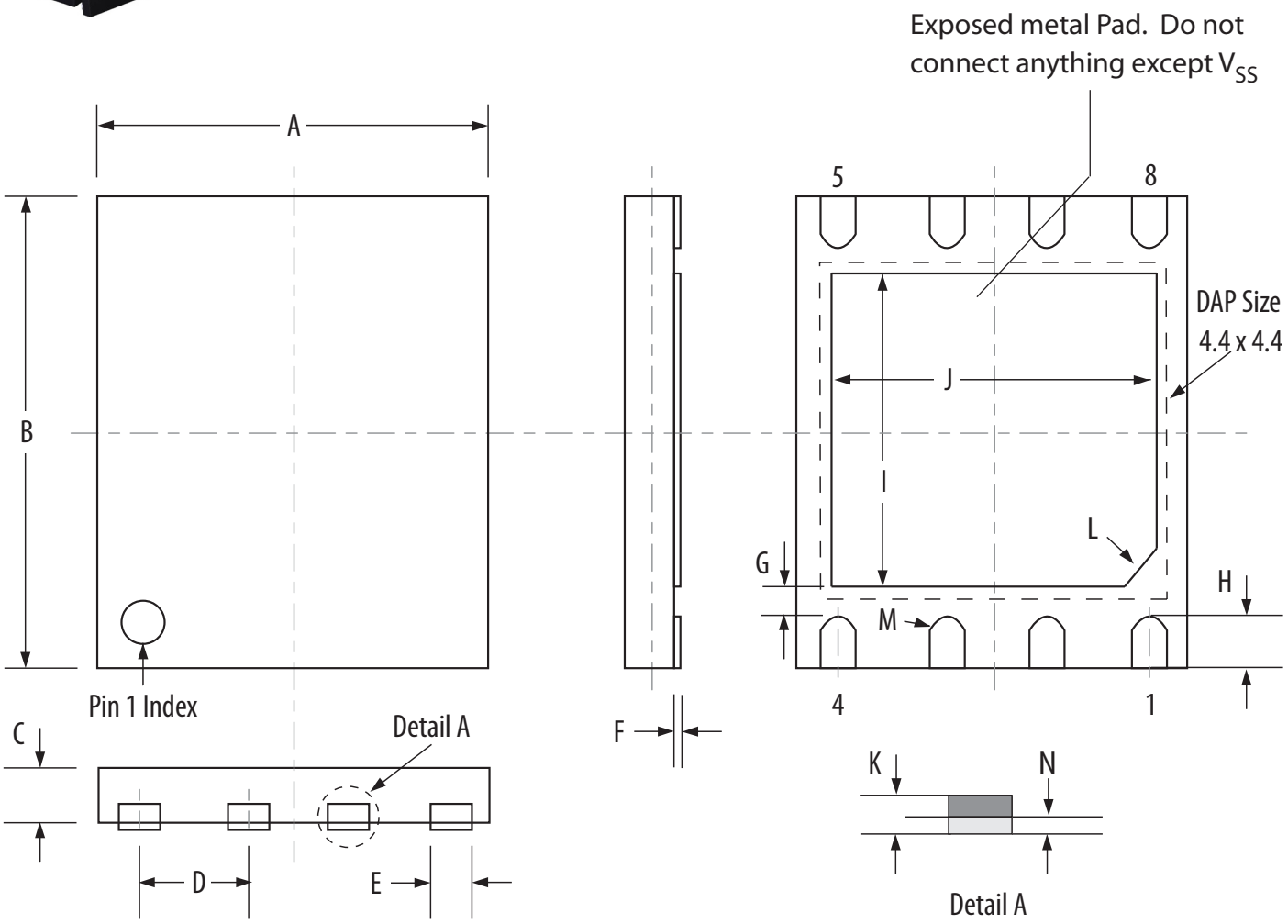
Speed Grade	Temp Grade	Tempera-ture	Package	Shipping Con-tainer	Order Part Number
50MHz	Industrial	-40 to +85 C	8-DFN Small Flag	Trays	MR20H40CDF
				Tape and Reel	MR20H40CDFR
40 MHz	Commercial	0 to +70 C	8-DFN Small Flag	Trays	MR25H40DF
				Tape and Reel	MR25H40DFR
	Industrial	-40 to +85 C	8-DFN [1]	Trays	MR25H40CDC [1]
				Tape and Reel	MR25H40CDCR [1]
			8-DFN Small Flag	Trays	MR25H40CDF
				Tape and Reel	MR25H40CDFR
	Extended	-40 to +105 C	8-DFN Small Flag	Trays	MR25H40VDF
				Tape and Reel	MR25H40VDFR
	AEC-Q100 Grade 1	-40 to +125 C	8-DFN Small Flag	Trays	MR25H40MDF
				Tape and Reel	MR25H40MDFR

Note:

1. The DC pckage option (8-DFN) is not recommended for new designs. Please select the DF (8-DFN small flag) option for new designs.

PACKAGE OUTLINE DRAWINGS

Figure 17 – DFN Package Outline

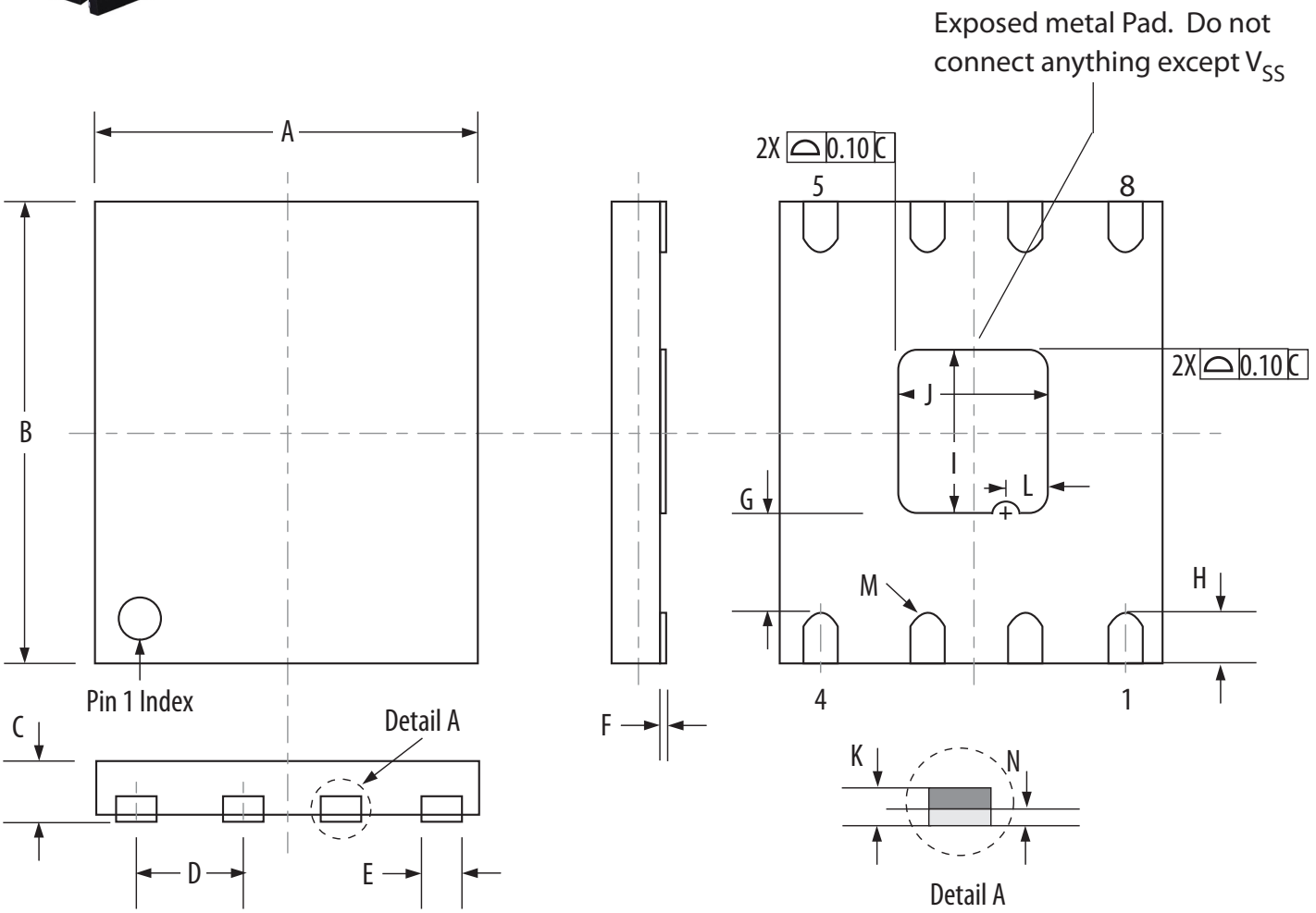


Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M	N
Max.	5.10	6.10	1.00	1.27	0.45	0.05	0.35	0.70	4.20	4.20	0.261	C0.35	R0.20	0.05
Min.	4.90	5.90	0.90	BSC	0.35	0.00	Ref.	0.50	4.00	4.00	0.195			0.00

Notes:

1. Reference JEDEC MO-229.
2. All dimensions are in mm. Angles in degrees.
3. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall be within 0.08 mm.
4. Warpage shall not exceed 0.10 mm.

Figure 18 – DFN Small Flag Package



Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M	N
Max.	5.10	6.10	0.90	1.27 BSC	0.45	0.05	1.60	0.70	2.10	2.10	.210	C0.45	R0.20	0.05
Min.	4.90	5.90	0.80		0.35	0.00	1.20	0.50	1.90	1.90	.196			0.00

Notes:

1. Reference JEDEC MO-229.
2. All dimensions are in mm. Angles in degrees.
3. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall be within 0.08 mm.
4. Warpage shall not exceed 0.10 mm.

CY15B108QN
CY15V108QN

Excelon™ LP 8-Mbit (1024K × 8) Serial (SPI) F-RAM

Features

- 8-Mbit ferroelectric random access memory (F-RAM) logically organized as 1024K × 8
  - Virtually unlimited endurance 1000 trillion (10^{15}) read/writes
  - 151-year data retention (See Data Retention and Endurance on page 20)
  - NoDelay™ writes
  - Advanced high-reliability ferroelectric process
- Fast serial peripheral interface (SPI)
  - Up to 40 MHz frequency
  - Supports SPI mode 0 (0, 0) and mode 3 (1, 1)
- Sophisticated write protection scheme
  - Hardware protection using the Write Protect ($\overline{WP}$) pin
  - Software protection using Write Disable (WRDI) instruction
  - Software block protection for 1/4, 1/2, or entire array
- Device ID and Serial Number
  - Manufacturer ID and Product ID
  - Unique Device ID
  - Serial Number
- Dedicated 256-byte special sector F-RAM
  - Dedicated special sector write and read
  - Stored content can survive up to three standard reflow soldering cycles
- Low-power consumption
  - 2.6 mA (typ) active current at 40 MHz
  - 3.5 µA (typ) standby current
  - 0.90 µA (typ) Deep Power Down mode current
  - 0.1 µA (typ) Hibernate mode current
- Low-voltage operation
  - CY15V108QN: V_{DD} = 1.71 V to 1.89 V
  - CY15B108QN: V_{DD} = 1.8 V to 3.6 V
- Commercial and industrial operating temperature
  - Commercial operating temperature: 0 °C to +70 °C
  - Industrial operating temperature: –40 °C to +85 °C
- Packages
  - 8-pin Small Outline Integrated Circuit (SOIC) package
  - 8-pin Grid-Array Quad Flat No-Lead (GQFN) package
- Restriction of hazardous substances (RoHS) compliant

Functional Description

The Excelon LP CY15X108QN is a low power, 8-Mbit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes similar to a RAM. It provides reliable data retention for 151 years while eliminating the complexities, overhead, and system-level reliability problems caused by serial flash, EEPROM, and other nonvolatile memories.

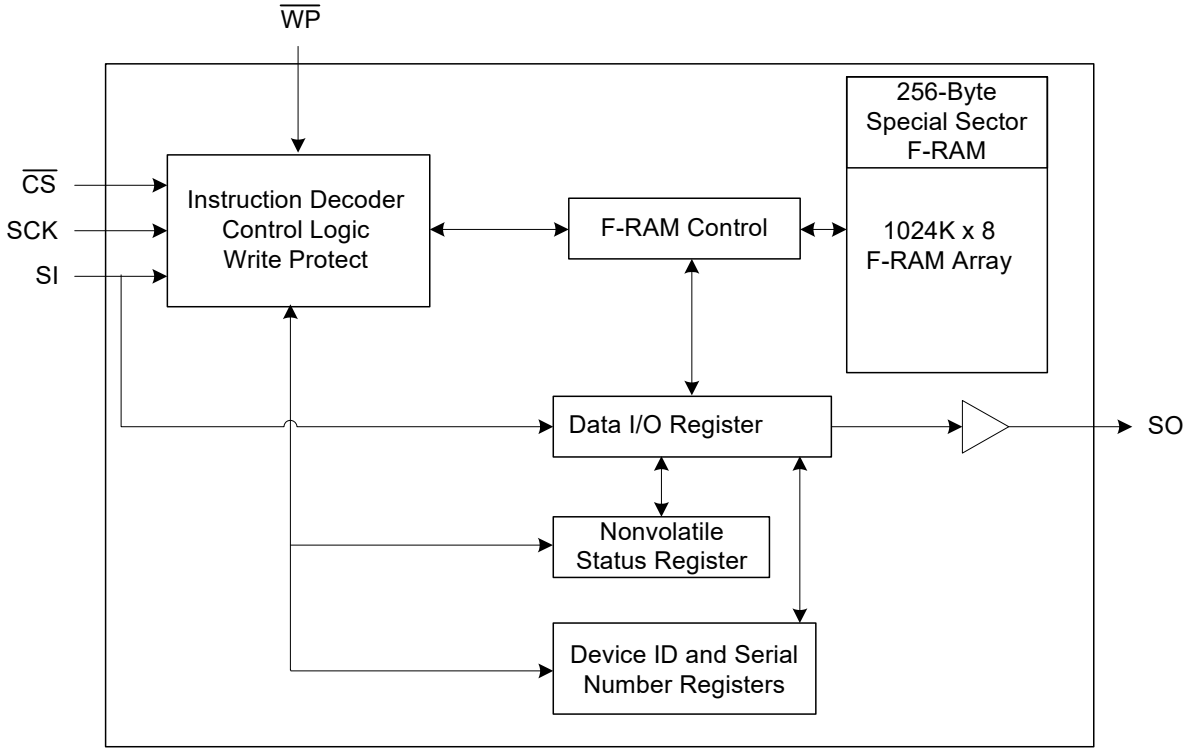
Unlike serial flash and EEPROM, the CY15X108QN performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after each byte is successfully transferred to the device. The next bus cycle can commence without the need for data polling. In addition, the product offers substantial write endurance compared to other nonvolatile memories. The CY15X108QN is capable of supporting 10^{15} read/write cycles, or 1000 million times more write cycles than EEPROM.

These capabilities make the CY15X108QN ideal for nonvolatile memory applications, requiring frequent or rapid writes. Examples range from data collection, where the number of write cycles may be critical, to demanding industrial controls where the long write time of serial flash or EEPROM can cause data loss.

The CY15X108QN provides substantial benefits to users of serial EEPROM or flash as a hardware drop-in replacement. The CY15X108QN uses the high-speed SPI bus, which enhances the high-speed write capability of F-RAM technology. The device incorporates a read-only Device ID and Unique ID features, which allow the host to determine the manufacturer, product density, product revision, and unique ID for each part. The device also provides a writable, 8-byte serial number registers, which can be used to identify a specific board or a system.

For a complete list of related resources, click here.

Logic Block Diagram



Pinout

Figure 1. 8-pin SOIC Pinout

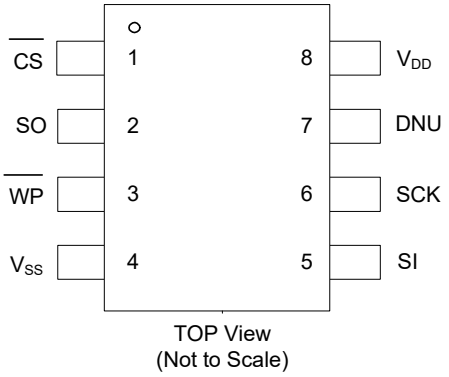
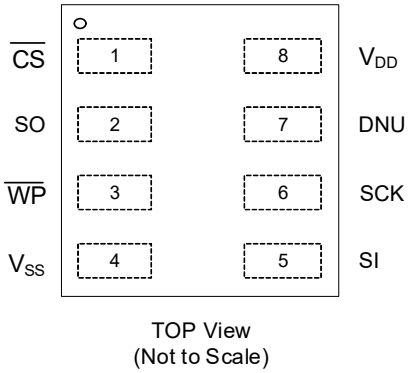


Figure 2. 8-pin GQFN Pinout



Pin Definitions

Pin Name	I/O Type	Description
$\overline{CS}$	Input	**Chip Select**. This active LOW input activates the device. When HIGH, the device enters low-power standby mode, ignores other inputs, and the output is tristated. When LOW, the device internally activates the SCK signal. A falling edge on $\overline{CS}$ must occur before every opcode.
SCK	Input	**Serial Clock**. All I/O activity is synchronized to the serial clock. Inputs are latched on the rising edge and outputs occur on the falling edge of the serial clock. The clock frequency may be any value between 0 and 40 MHz and may be interrupted at any time due to its synchronous behavior.
SI[1]	Input	**Serial Input**. All data is input to the device on this pin. The pin is sampled on the rising edge of SCK and is ignored at other times. It should always be driven to a valid logic level to meet the power (I_{DD}) specifications.
SO[1]	Output	**Serial Output.** This is the data output pin. It is driven during a read and remains tristated at all other times. Data transitions are driven on the falling edge of the serial clock SCK.
$\overline{WP}$	Input	**Write Protect.** This Active LOW pin prevents write operation to the Status Register when WPEN bit in the Status Register is set to '1'. This is critical because other write protection features are controlled through the Status Register. A complete explanation of write protection is provided in Status Register and Write Protection on page 10. This pin has an internal weak pull-up resistor which keeps this pin HIGH if left floating (not connected on the board). This pin can also be tied to V_{DD} if not used.
DNU	Do Not Use	**Do Not Use.** Either leave this pin floating (not connected on the board) or tie to V_{DD}.
V_{SS}	Power supply	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.

Note
1. SI may be connected to SO for a single pin data interface.

Functional Overview

The CY15X108QN is a serial F-RAM memory. The memory array is logically organized as 1,048,576 × 8 bits and is accessed using an industry-standard serial peripheral interface (SPI) bus. The functional operation of the F-RAM is similar to serial flash and serial EEPROMs. The major difference between the CY15X108QN and a serial flash or EEPROM with the same pinout is the F-RAM's superior write performance, high endurance, and low power consumption.

Memory Architecture

When accessing CY15X108QN, the user addresses 1,024K locations of eight data bits each. These eight data bits are shifted in or out serially. The addresses are accessed using the SPI protocol, which includes a chip select (to permit multiple devices on the bus), an opcode, and a three-byte address. The upper four bits of the address range are 'don't care' values. The complete address of 20 bits specifies each byte address uniquely.

Most functions of the CY15X108QN are either controlled by the SPI interface or handled by on-board circuitry. The access time for the memory operation is essentially zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the SPI bus. Unlike a serial flash or EEPROM, it is not necessary to poll the device for a ready condition because writes occur at bus speed. By the time a new bus transaction can be shifted into the device, a write operation is complete. This is explained in more detail in the interface section.

SPI Bus

The CY15X108QN is an SPI slave device and operates at speeds of up to 40 MHz. This high-speed serial bus provides high-performance serial communication to an SPI master. Many common microcontrollers have hardware SPI ports allowing a direct interface. It is simple to emulate the port using ordinary port pins for microcontrollers that do not have this feature. The CY15X108QN operates in SPI Modes 0 and 3.

SPI Overview

The SPI is a four-pin interface with Chip Select ($\overline{CS}$), Serial Input (SI), Serial Output (SO), and Serial Clock (SCK) pins.

The SPI is a synchronous serial interface, which uses clock and data pins for memory access and supports multiple devices on the data bus. A device on the SPI bus is activated using the $\overline{CS}$ pin.

The relationship between chip select, clock, and data is dictated by the SPI mode. This device supports SPI modes 0 and 3. In both of these modes, data is clocked into the F-RAM on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active.

The SPI protocol is controlled by opcodes. These opcodes specify the commands from the bus master to the slave device. After $\overline{CS}$ is activated, the first byte transferred from the bus master is the opcode. Following the opcode, any addresses and data are then transferred. The $\overline{CS}$ must go inactive after an operation is complete and before a new opcode can be issued.

Terms used in SPI Protocol

The commonly used terms in the SPI protocol are as follows.

SPI Master

The SPI master device controls the operations on the SPI bus. An SPI bus may have only one master with one or more slave devices. All the slaves share the same SPI bus lines and the master may select any of the slave devices using the $\overline{CS}$ pin. All of the operations must be initiated by the master activating a slave device by pulling the $\overline{CS}$ pin of the slave LOW. The master also generates the SCK and all the data transmission on SI and SO lines are synchronized with this clock.

SPI Slave

The SPI slave device is activated by the master through the Chip Select line. A slave device gets the SCK as an input from the SPI master and all the communication is synchronized with this clock. An SPI slave never initiates a communication on the SPI bus and acts only on the instruction from the master.

The CY15X108QN operates as an SPI slave and may share the SPI bus with other SPI slave devices.

Chip Select ($\overline{CS}$)

To select any slave device, the master needs to pull down the corresponding $\overline{CS}$ pin. Any instruction can be issued to a slave device only while the $\overline{CS}$ pin is LOW. When the device is not selected, data through the SI pin is ignored and the serial output pin (SO) remains in a high-impedance state.

Note A new instruction must begin with the falling edge of $\overline{CS}$. Therefore, only one opcode can be issued for each active Chip Select cycle.

Serial Clock (SCK)

The serial clock is generated by the SPI master and the communication is synchronized with this clock after $\overline{CS}$ goes LOW.

The CY15X108QN supports SPI modes 0 and 3 for data communication. In both of these modes, the inputs are latched by the slave device on the rising edge of SCK and outputs are issued on the falling edge. Therefore, the first rising edge of SCK signifies the arrival of the first Most Significant Bit (MSb) of an SPI instruction on the SI pin. Further, all data inputs and outputs are synchronized with SCK.

Data Transmission (SI/SO)

The SPI data bus consists of two lines, SI and SO, for serial data communication. SI is also referred to as Master Out Slave In (MOSI) and SO is referred to as Master In Slave Out (MISO). The master issues instructions to the slave through the SI pin, while the slave responds through the SO pin. Multiple slave devices may share the SI and SO lines as described earlier.

The CY15X108QN has two separate pins for SI and SO, which can be connected with the master as shown in Figure 3. For a microcontroller that has no dedicated SPI bus, a general-purpose port may be used. To reduce hardware resources on the controller, it is possible to connect the two data pins (SI, SO) together and tie off (HIGH) the $\overline{WP}$ pin. Figure 4 shows such a configuration, which uses only three pins.

Figure 3. System Configuration with SPI Port

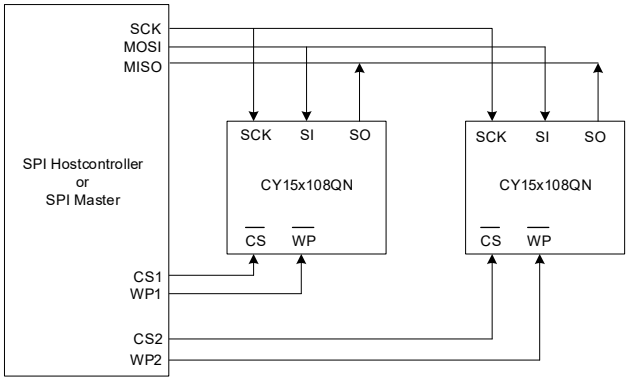
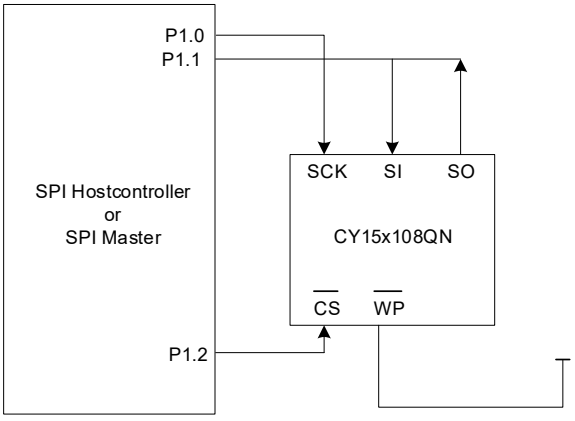


Figure 4. System Configuration without SPI Port



Most Significant Bit (MSb)

The SPI protocol requires that the first bit to be transmitted is the MSb. This is valid for both address and data transmission.

The 8-Mbit serial F-RAM requires a 3-byte address for any read or write operation. Because the address is only 20 bits, the first four bits, which are fed in are ignored by the device. Although these four bits are 'don't care', Cypress recommends that these bits be set to 0s to enable seamless transition to higher memory densities.

Serial Opcode

After the slave device is selected with $\overline{CS}$ going LOW, the first byte received is treated as the opcode for the intended operation. CY15X108QN uses the standard opcodes for memory accesses.

Invalid Opcode

If an invalid opcode is received, the opcode is ignored and the device ignores any additional serial data on the SI pin until the next falling edge of $\overline{CS}$, and the SO pin remains tristated.

Status Register

CY15X108QN has an 8-bit Status Register. The bits in the Status Register are used to configure the device. These bits are described in Table 3 on page 10.

SPI Modes

CY15X108QN may be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

- SPI Mode 0 (CPOL = 0, CPHA = 0)
- SPI Mode 3 (CPOL = 1, CPHA = 1)

For both these modes, the input data is latched in on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active. If the clock starts from a HIGH state (in mode 3), the first rising edge after the clock toggles is considered. The output data is available on the falling edge of SCK. The two SPI modes are shown in Figure 5 and Figure 6. The status of the clock when the bus master is not transferring data is:

- SCK remains at 0 for Mode 0
- SCK remains at 1 for Mode 3

The device detects the SPI mode from the status of the SCK pin when the device is selected by bringing the $\overline{CS}$ pin LOW. If the SCK pin is LOW when the device is selected, SPI Mode 0 is assumed and if the SCK pin is HIGH, it works in SPI Mode 3.

Figure 5. SPI Mode 0

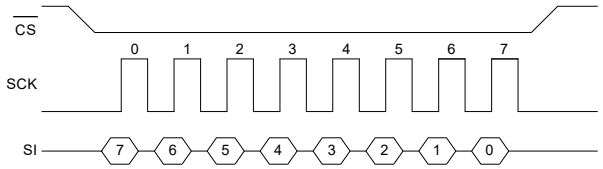
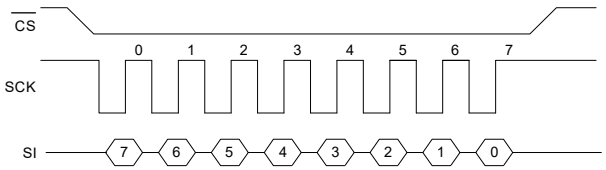


Figure 6. SPI Mode 3



Power-Up to First Access

The CY15X108QN is not accessible for a t_{PU} time after power-up. Users must comply with the timing parameter, t_{PU}, which is the minimum time from V_{DD} (min) to the first $\overline{CS}$ LOW. Refer to Power Cycle Timing on page 23 for details.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +125 °C

Maximum accumulated storage time
At 125 °C ambient temperature ..... 1000 h
At 85 °C ambient temperature ..... 10 Years

Maximum junction temperature ..... 125 °C

Supply voltage on V_{DD} relative to V_{SS}:
CY14V108QI: .....–0.5 V to +2.4 V
CY14B108QI: .....–0.5 V to +4.1 V

Input voltage ..... $V_{IN} \le V_{DD}$ + 0.5 V

DC voltage applied to outputs
in High-Z state ..... –0.5 V to V_{DD} + 0.5 V

Transient voltage (< 20 ns)
on any pin to ground potential ..... –2.0 V to V_{DD} + 2.0 V

Package power dissipation capability
(T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering temperature
(3 seconds) ..... +260 °C

DC output current
(1 output at a time, 1s duration) ..... 15 mA

Electrostatic discharge voltage
Human Body Model (JEDEC Std JESD22-A114-B) ..... 2 kV
Charged Device Model
(JEDEC Std JESD22-C101-A) ..... 500 V

Latch-up current .....>140 mA

Operating Range

Device	Range	Ambient Temperature	V_{DD}
CY15V108QN	Commercial	0 °C to +70 °C	1.71 V to 1.89 V
CY15B108QN			1.8 V to 3.6 V
CY15V108QN	Industrial	–40 °C to +85 °C	1.71 V to 1.89 V
CY15B108QN			1.8 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Temperature	Min	Typ [2, 3]	Max	Unit
V_{DD}	Power supply	CY15V108QN		–	1.71	1.80	1.89	V
		CY15B108QN			1.80	3.30	3.60	
I_{DD}	V_{DD} supply current	V_{DD} = 1.71 V to 1.89 V; SCK toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V. SO = Open; CY15V108QN-20LP part	f_{SCK} = 1 MHz	Commercial	–	0.3	0.38	mA
			f_{SCK} = 20 MHz		–	1.3	1.5	
			f_{SCK} = 1 MHz	Industrial	–	0.3	0.58	
			f_{SCK} = 20 MHz		–	1.3	1.6	
		V_{DD} = 1.8 V to 3.6 V; SCK toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V. SO = Open; CY15B108N-20LP part	f_{SCK} = 1 MHz	Commercial	–	0.35	0.52	
			f_{SCK} = 20 MHz		–	1.4	1.6	
			f_{SCK} = 1 MHz	Industrial	–	0.35	0.7	
			f_{SCK} = 20 MHz		–	1.4	1.75	
		V_{DD} = 1.71 V to 1.89 V; SCK toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V. SO = Open; CY15V108QN-40LP parts	f_{SCK} = 40 MHz	Industrial	–	2.6	3.2	
		V_{DD} = 1.8 V to 3.6 V; SCK toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V. SO = Open; CY15B108QN-40LP parts	f_{SCK} = 40 MHz	Industrial	–	2.6	3.2	

Notes
2. Typical values are at 25 °C, V_{DD} = V_{DD} (typ).
3. This parameter is guaranteed by characterization; not tested in production.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions		Temperature	Min	Typ [2, 3]	Max	Unit
I_{SB}	V_{DD} standby current	V_{DD} = 1.71 V to 1.89 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C	–	–	3.5	–	µA
			T_A = 70 °C		–	–	52	
			T_A = 85°C		–	–	110	
		V_{DD} = 1.8 V to 3.6 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C		–	3.8	–	
			T_A = 70 °C		–	–	55	
			T_A = 85°C		–	–	120	
I_{DPD}	Deep power-down current	V_{DD} = 1.71 V to 1.89 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C	–	–	0.9	–	µA
			T_A = 70 °C		–	–	11	
			T_A = 85°C		–	–	24	
		V_{DD} = 1.8 V to 3.6 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C		–	1	–	
			T_A = 70 °C		–	–	12	
			T_A = 85°C		–	–	26	
I_{HBN}	Hibernate mode current	V_{DD} = 1.71 V to 1.89 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C	–	–	0.1	–	µA
			T_A = 70 °C		–	–	0.4	
			T_A = 85°C		–	–	0.9	
		V_{DD} = 1.8 V to 3.6 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C		–	0.1	–	
			T_A = 70 °C		–	–	0.75	
			T_A = 85°C		–	–	1.6	
I_{LI}	Input leakage current on I/O pins except $\overline{WP}$ pin	V_{SS} < V_{IN} < V_{DD}		–	–1	–	1	µA
	Input leakage current on $\overline{WP}$ pin				–100	–	1	
I_{LO}	Output leakage current	V_{SS} < V_{OUT} < V_{DD}		–	–1	–	1	
V_{IH}	Input HIGH voltage	–		–	0.7 × V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage	–		–	–0.3	–	0.3 × V_{DD}	
V_{OH1}	Output HIGH voltage	I_{OH} = –1 mA, V_{DD} = 2.7 V.		–	2.4	–	–	
V_{OH2}	Output HIGH voltage	I_{OH} = –100 µA		–	V_{DD} – 0.2	–	–	
V_{OL1}	Output LOW voltage	I_{OL} = 2 mA, V_{DD} = 2.7 V		–	–	–	0.4	
V_{OL2}	Output LOW voltage	I_{OL} = 150 µA		–	–	–	0.2	

Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	T_A = 85 °C	10	–	Years
		T_A = 70 °C	141	–	
		T_A = 60 °C	151	–	
		T_A = 50 °C	160	–	
NV_C	Endurance	Over operating temperature	10^{15}	–	Cycles

Capacitance

For all packages.

Parameter [4]	Description	Test Conditions	Max	Unit
C_O	Output pin capacitance (SO)	T_A = 25 °C, f = 1 MHz, V_{DD} = V_{DD} (typ)	8	pF
C_I	Input pin capacitance		6	

Thermal Resistance

Parameter [4]	Description	Test Conditions	8-pin SOIC Package	8-pin GQFN Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	81.5	113.5	°C/W
Θ_{JC}	Thermal resistance (junction to case)		96.5	99	

AC Test Conditions

Input pulse levels ..... 10% and 90% of V_{DD}
Input rise and fall times ..... 3 ns
Input and output timing reference levels ..... 0.5 × V_{DD}
Output load capacitance ..... 30 pF

Note
4. This parameter is guaranteed by characterization; not tested in production.

AC Switching Characteristics

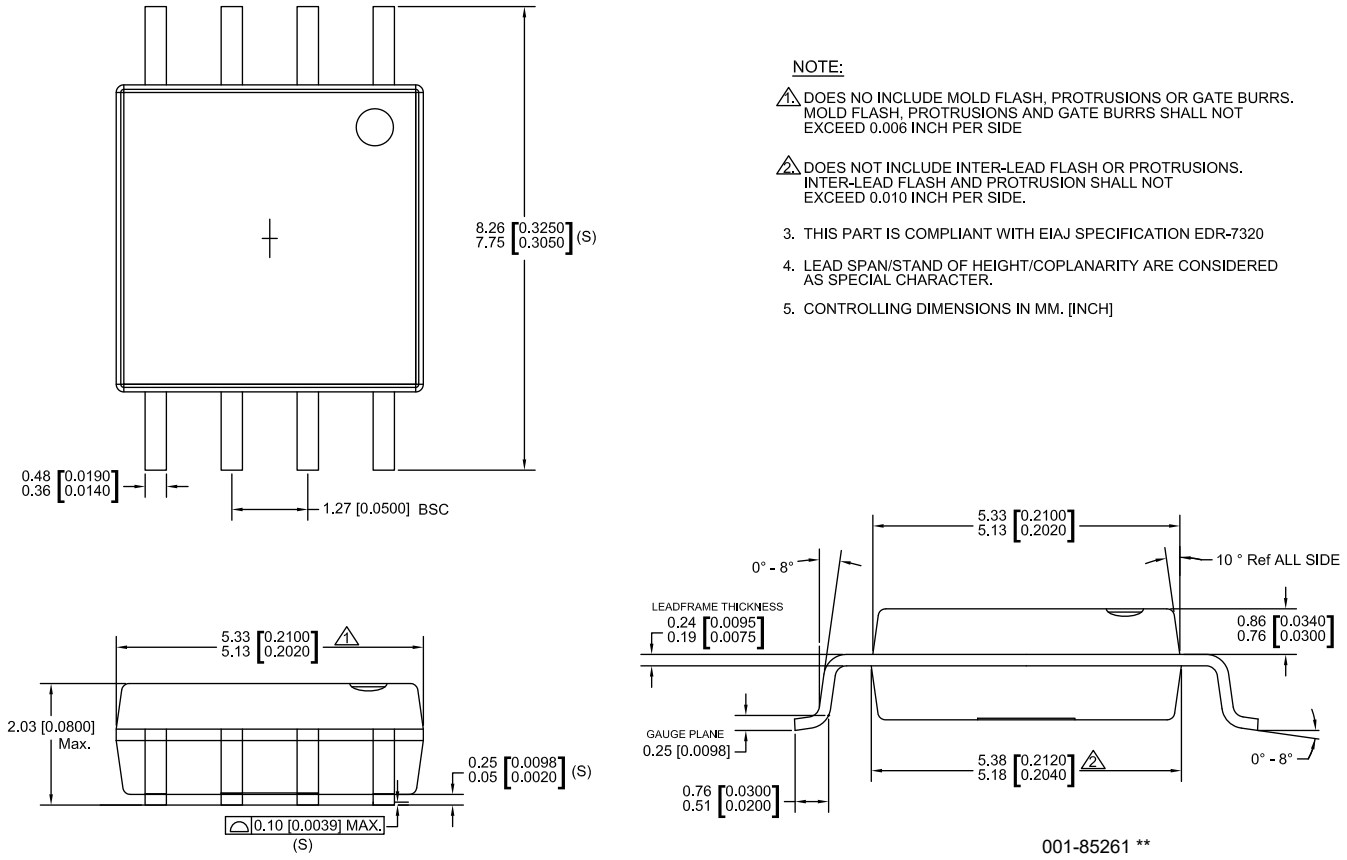
Over the Operating Range

Parameters[5]		Description	20 MHz		40 MHz		Unit
Cypress Parameter	Alt. Parameter		Min	Max	Min	Max	
f_{SCK}	–	SCK clock frequency	0	20	0	40	MHz
t_{CH}	–	Clock HIGH time	22	–	11	–	ns
t_{CL}	–	Clock LOW time	22	–	11	–	
t_{CLZ}[6]	–	Clock LOW to Output low-Z	0	–	0	–	
t_{CSS}	t_{CSU}	Chip select setup	10	–	5	–	
t_{CSH}	t_{CSH}	Chip select hold - SPI mode 0	10	–	5	–	
t_{CSH1}	–	Chip select hold - SPI mode 3	10	–	10	–	
t_{HZCS}[7, 8]	t_{OD}	Output disable time	–	20	–	12	
t_{CO}	t_{ODV}	Output data valid time	–	20	–	9	
t_{OH}	–	Output hold time	1	–	1	–	
t_{CS}	t_{D}	Deselect time	60	–	40	–	
t_{SD}	t_{SU}	Data setup time	5	–	5	–	
t_{HD}	t_{H}	Data hold time	5	–	5	–	
t_{WPS}	t_{WHSL}	$\overline{WP}$ setup time (w.r.t $\overline{CS}$)	20	–	20	–	
t_{WPH}	t_{SHWL}	$\overline{WP}$ hold time (w.r.t $\overline{CS}$)	20	–	20	–	

Notes
5. Test conditions assume a signal transition time of 3 ns or less, timing reference levels of 0.5 × V_{DD}, input pulse levels of 10% to 90% of V_{DD}, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance shown in AC Test Conditions on page 20.
6. Guaranteed by design.
7. t_{HZCS} is specified with a load capacitance of 5 pF. Transition is measured when the output enters a high-impedance state.
8. This parameter is guaranteed by characterization; not tested in production.

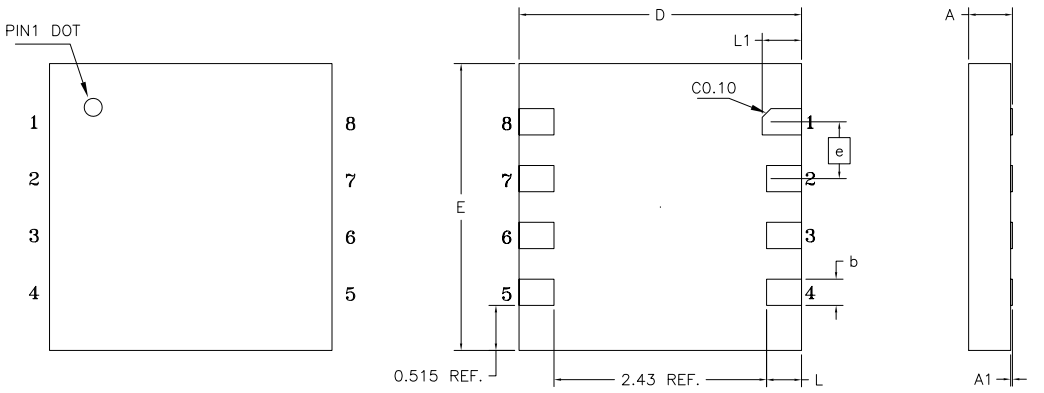
Package Diagram

Figure 26. 8-pin SOIC (208 Mils) Package Outline, 001-85261



Package Diagram (continued)

Figure 27. 8-pin GQFN (3.23 × 3.28 × 0.55 mm) Package Outline, 002-18131



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e	0.65 BSC		
N	8		
L	0.30	0.40	0.50
L1	0.35	0.45	0.55
b	0.25	0.30	0.35
D	3.18	3.23	3.28
E	3.23	3.28	3.33
A	0.45	0.50	0.55
A1	0.00	-	0.05

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

002-18131 *C

Micron Serial NOR Flash Memory

3V, Twin-Quad I/O, 4KB, 32KB, 64KB, Sector Erase

MT25TL01GBBB, MT25TL01GHBB

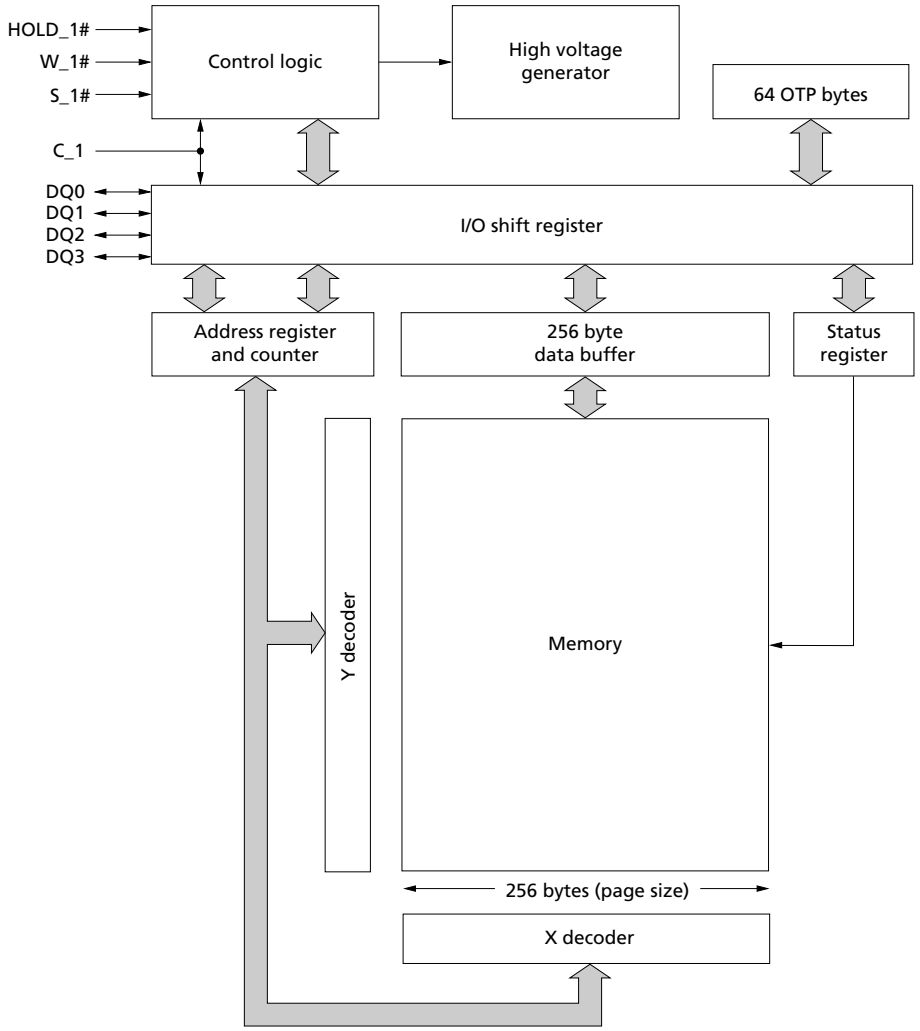
Features

- Stacked device (two 512Mb die)
- SPI-compatible serial bus interface
- Single and double transfer rate (STR/DTR)
- Clock frequency
  - 133 MHz (MAX) for all protocols in STR
  - 90 MHz (MAX) for all protocols in DTR
- Dual/quad I/O instruction provides increased throughput up to 90 MB/s for each die corresponding to 180 MB/s for the twin-quad device
- Supported protocols in both STR and DTR
  - Extended I/O protocol
  - Dual I/O protocol
  - Quad I/O protocol
- Execute-in-place (XIP)
- PROGRAM/ERASE SUSPEND operations
- Volatile and nonvolatile configuration settings
- Software reset
- Additional reset pin for selected part numbers
- 3-byte and 4-byte addressability mode supported
- Dedicated 64-byte OTP area outside main memory
  - Readable and user-lockable
  - Permanent lock with PROGRAM OTP command
- Erase capability
  - Die erase
  - Sector erase 64KB uniform granularity
  - Subsector erase 4KB, 32KB granularity
- Security and write protection
  - Volatile and nonvolatile locking and software write protection for each 64KB sector
  - Nonvolatile configuration locking
  - Password protection
  - Hardware write protection: nonvolatile bits (BP[3:0] and TB) define protected area size
  - Program/erase protection during power-up
  - CRC detects accidental changes to raw data
- Electronic signature
  - JEDEC-standard 3-byte signature (BA20h)
  - Extended device ID: two additional bytes identify device factory options
- JESD47H-compliant
  - Minimum 100,000 ERASE cycles per sector
  - Data retention: 20 years (TYP)

Options	Marking
• Voltage	
– 2.7–3.6V	L
• Density	
– 1Gb	01G
• Device stacking	
– B = 2 die and 1 S# pin	B
– H = 2 die and 2 S# pins	H
• Device generation	B
• Die revision	B
• Pin configuration	
– RESET# and HOLD#	8
• Sector size	
– 64KB	E
• Packages – JEDEC-standard, RoHS-compliant	
– 16-pin SOP2, 300 mils body width (SO16W)	SF
– 24-ball T-PBGA, 05/6mm x 8mm (TBGA24)	12
• Security features	
– Standard	0
• Special options	
– Automotive	A
• Standard security	0
• Operating temperature range	
– From –40°C to +105°C	AT

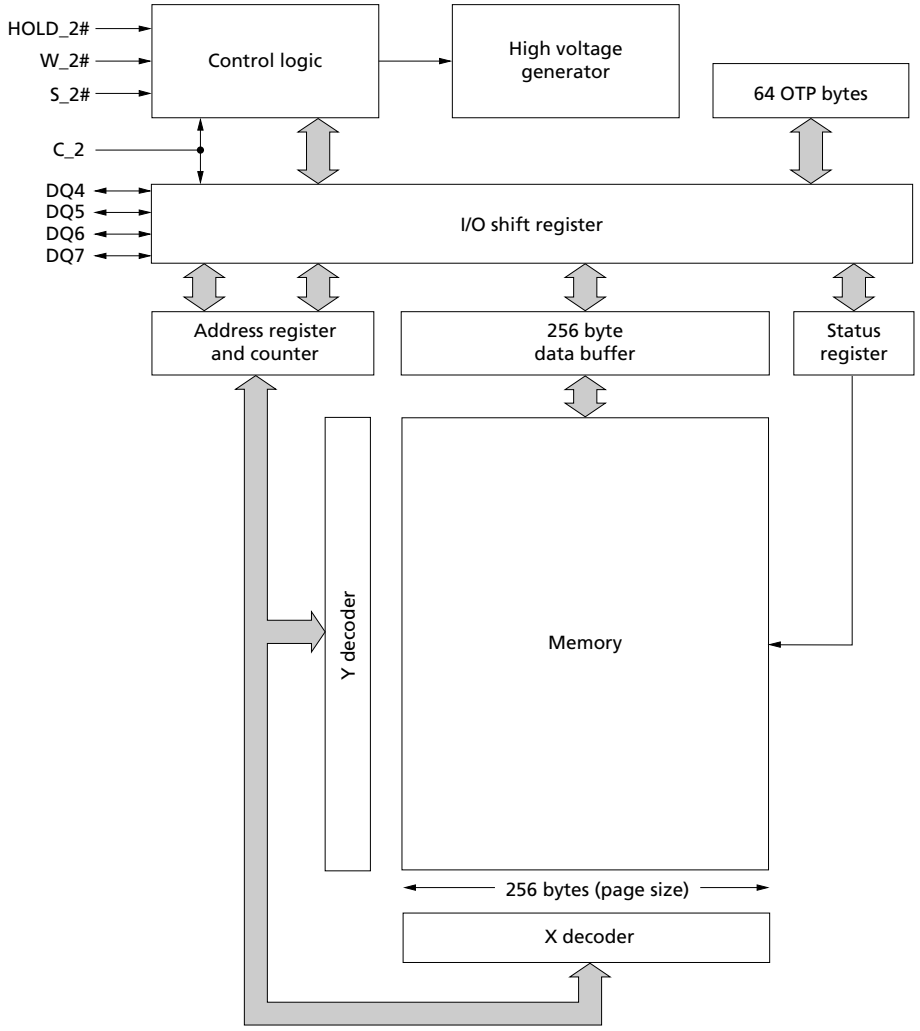
Block Diagram

Figure 2: Block Diagram – Flash Die 1



Note: 1. Each page of memory can be individually programmed, but the device is not page-erasable.

Figure 3: Block Diagram – Flash Die 2



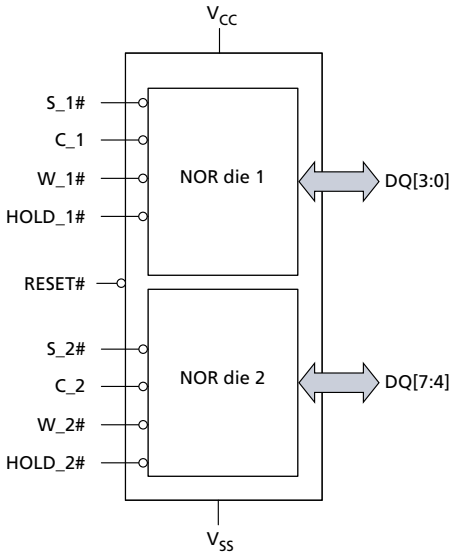
Note: 1. Each page of memory can be individually programmed, but the device is not page-erasable.

Advanced Security Protection

The device offers an advanced security protection scheme where each sector can be independently locked, by either volatile or nonvolatile locking features. The nonvolatile locking configuration can also be locked, as well password-protected. See Block Protection Settings and Sector and Password Protection for more details.

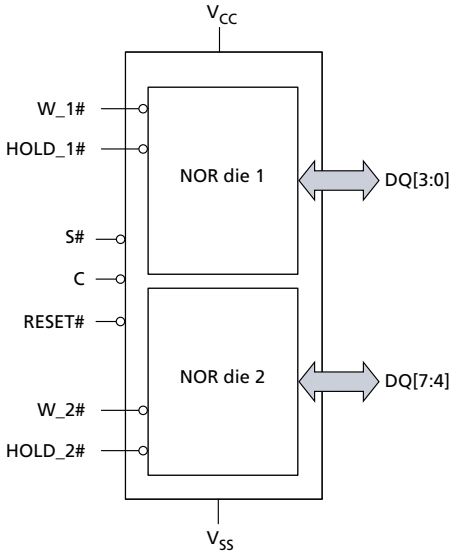
Device Logic Diagram

Figure 4: Logic Diagram – Separate Chip-Select and Clock Signals



Note: 1. The RESET# pin is available on dedicated part numbers. See the Part Numbering Ordering Information section for more details.

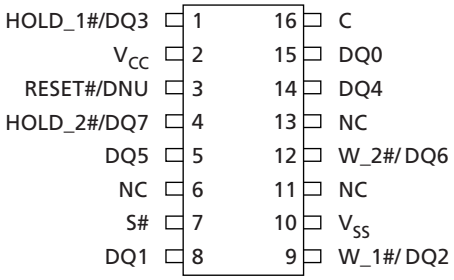
Figure 5: Logic Diagram – Shared Chip-Select and Clock Signals



Note: 1. The RESET# pin is available on dedicated part numbers. See the Part Numbering Ordering section for more details.

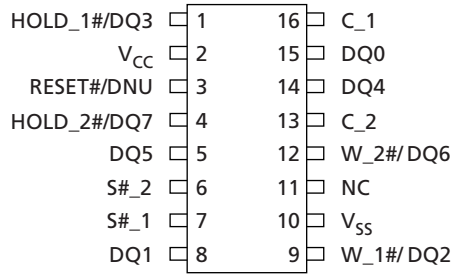
Signal Assignments

Figure 6: 16-Pin, Plastic Small Outline – SO16 (Top View) (Single Chip-Select and Clock)



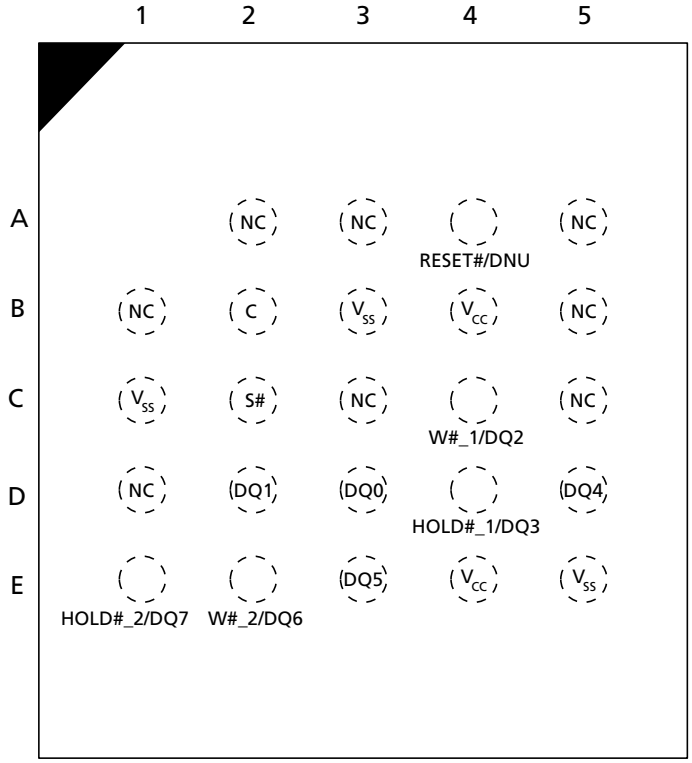
Notes:
1. RESET# or HOLD# signals can share Pin 1 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven HIGH by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
2. Pin 3 = RESET# or DNU, depending on the part number. This signal has an internal pull-up resistor and may be left unconnected if not used.

Figure 7: 16-Pin, Plastic Small Outline – SO16 (Top View) (Dual Chip-Select and Clock)



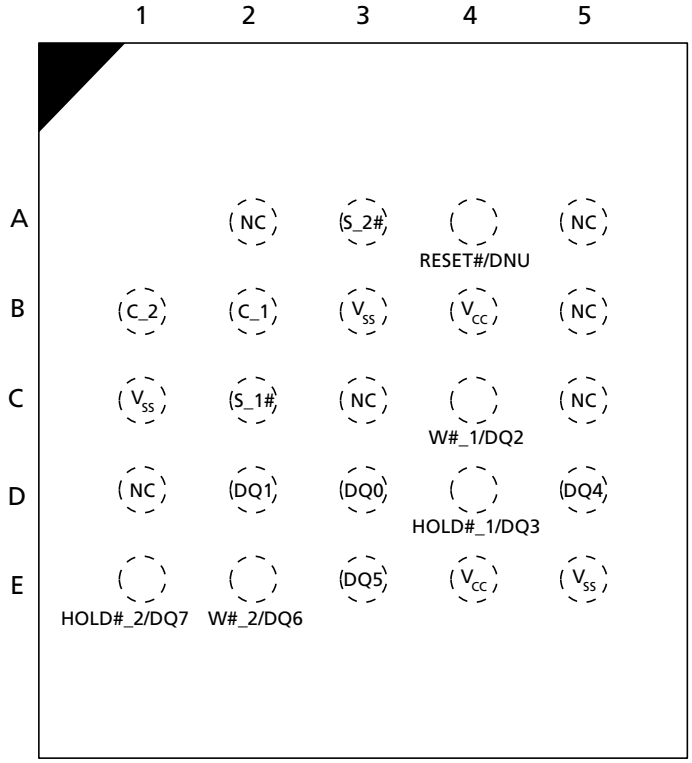
Notes:
1. RESET# or HOLD# signals can share Pin 1 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven HIGH by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
2. Pin 3 = RESET# or DNU, depending on the part number. This signal has an internal pull-up resistor and may be left unconnected if not used.

Figure 8: 24-Ball TBGA – 5 x 5 (Balls Down) (Single Chip-Select and Clock)



Notes:
1. RESET# or HOLD# signals can share Ball D4 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven HIGH by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
2. Ball A4 = RESET# or DNU, depending on the part number. This signal has an internal pull-up resistor and may be left unconnected if not used.

Figure 9: 24-Ball TBGA – 5 x 5 (Balls Down) (Double Chip-Select and Clock)



Notes:
1. RESET# or HOLD# signals can share Ball D4 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven HIGH by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
2. Ball A4 = RESET# or DNU, depending on the part number. This signal has an internal pull-up resistor and may be left unconnected if not used.

Signal Descriptions

The signal description table below is a comprehensive list of signals for the MT25T family devices. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 1: Signal Descriptions

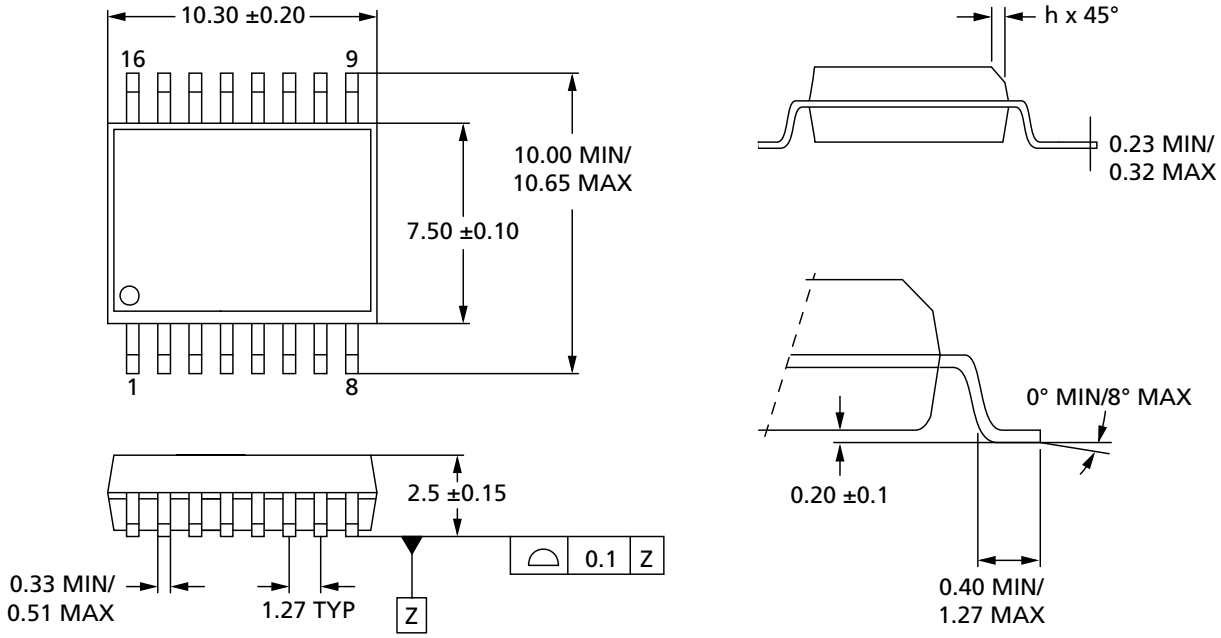
Symbol	Type	Description
C	Input	**Clock:** Provides the timing of the serial interface. Commands are latched on the rising edge of the clock. In STR commands or protocol, address and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock. In DTR commands or protocol, address and data inputs are latched on both edges of the clock, and data is output on both edges of the clock. In single clock C configuration, C_1 and C_2 are connected together internally at package level.
C_1		Associated to die 1.
C_2		Associated to die 2.
S#	Input	**Chip select:** Because each die has its own DQ signals, each die can work independently. When S# is driven HIGH, the device enters standby mode, unless an internal PROGRAM, ERASE, or WRITE STATUS REGISTER cycle is in progress. All other input pins are ignored and the output pins are tri-stated. On parts where the pin configuration offers a dedicated RESET# pin, however, the RESET# input pin remains active when S# is HIGH. Driving S# LOW enables the device, placing it in the active mode. After power-up, a falling edge on S# is required prior to the start of any command. In single S# configuration, S_1# and S_2# are connected together internally at package level.
S_1#		Associated to die 1.
S_2#		Associated to die 2.
DQ[3:0], DQ[7:4]	I/O	**Serial data:** Bidirectional signals that transfer address, data, and command information. When using legacy (x1) SPI commands in extended I/O protocol (XIO-SPI), DQ0/DQ4 is an input and DQ1/DQ5 is an output. DQ[3:2]/DQ[7:6] are not used. When using dual commands in XIO SPI or when using DIO-SPI, DQ[1:0]/DQ[5:4] are I/O. DQ[3:2]/DQ[7:6] are not used. When using quad commands in XIO-SPI or when using QIO-SPI, DQ[3:0]/DQ[7:4] are I/O.
RESET#	Input	**RESET:** Hardware RESET# signal shared by both die. When RESET# is driven LOW, the device is reset and the outputs are tri-stated. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost. The RESET# functionality can be disabled using bit 4 of the nonvolatile configuration register or bit 4 of the enhanced volatile configuration register.The RESET# has an internal pull-up resistor and may be left floating if not used. For pin configurations that share the DQ3/DQ7 pins with RESET#, the RESET# functionality is disabled in QIO-SPI mode.
HOLD_1#, HOLD_2#	Input	**HOLD_1# (die 1), HOLD_2# (die 2):** Pauses any serial communications with the related die without deselecting the device. Outputs are tri-stated and inputs are ignored. To enable HOLD, the related die must be selected by its associated S# being driven LOW. In QIO-SPI, HOLD# acts as an I/O (DQ3/DQ7 functionality), and the HOLD# functionality is disabled when the device is selected. Because each die has its own nonvolatile configuration register, the HOLD# functionality for each die can be disabled using bit 4 of its associated nonvolatile configuration register or bit 4 of its associated enhanced volatile configuration register. HOLD# functionality is disabled in QIO-SPI mode or when DTR operation is enabled.

Table 1: Signal Descriptions (Continued)

Symbol	Type	Description
W_1#, W_2#	Control Input	**Write protect:** W_1# (die 1) and W_2# (die 2) can be used as a protection control input or in QIO-SPI operations. When LOW, the blocks defined by the block protection bits BP[3:0] are protected against PROGRAM or ERASE operations. Status register bit 7 should be set to 1 to enable write protection.
V_{CC}	Supply	**Core and IO power supply:** All V_{CC} pins must be connected to system power supply.
V_{SS}	Supply	**Core and IO ground connection:** All V_{SS} pins must be connected to system ground.
DNU	–	**Do not use:** Do not connect to any other signal, or power supply; must be left floating.
RFU	–	**Reserved for future use:** Reserved by Micron for future device functionality and enhancement. Recommend that these be left floating. May be connected internally, but external connections will not affect operation.
NC	–	**No connect :** No internal connection; can be driven or floated.

Package Dimensions – Package Code: SF

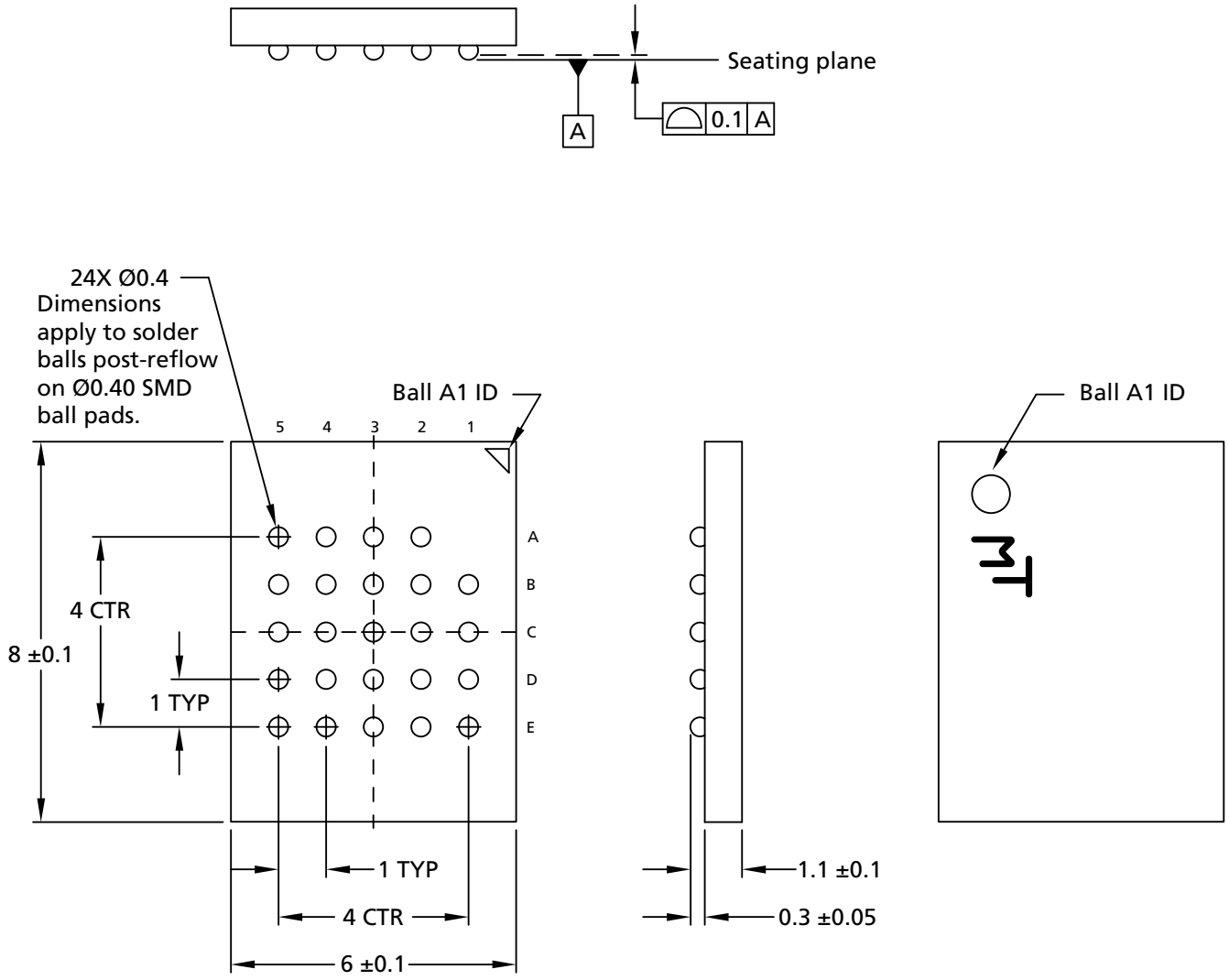
Figure 10: 16-Pin SOP2 – 300 Mils Body Width



Notes:
1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

Package Dimensions – Package Code: 12

Figure 11: 24-Ball T-PBGA (5 x 5 ball grid array) – 6mm x 8mm



Notes:
1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

Absolute Ratings and Operating Conditions

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating for extended periods may adversely affect reliability. Stressing the device beyond the absolute maximum ratings may cause permanent damage.

Table 42: Absolute Ratings

Symbol	Parameter	Min	Max	Units	Notes
T_{STG}	Storage temperature	–65	150	°C	
T_{LEAD}	Lead temperature during soldering	–	See note 1	°C	
V_{CC}	Supply voltage	–0.6	4.0	V	2
V_{IO}	Input/output voltage with respect to ground	–0.6	V_{CC} + 0.6	V	2
V_{ESD}	Electrostatic discharge voltage (human body model)	–2000	2000	V	2, 3

Notes:
1. Compliant with JEDEC Standard J-STD-020C (for small-body, Sn-Pb or Pb assembly), RoHS, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. All specified voltages are with respect to V_{SS}. During infrequent, nonperiodic transitions, the voltage potential between V_{SS} and the V_{CC} may undershoot to –2.0V for periods less than 20ns, or overshoot to $V_{CC,max}$ + 2.0V for periods less than 20ns.
3. JEDEC Standard JESD22-A114A (C1 = 100pF, R1 = 1500Ω, R2 = 500Ω).

Table 43: Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply voltage	2.7	3.6	V
T_A	Ambient operating temperature (AT range)	–40	105	°C

Table 44: Input/Output Capacitance

Note 1 applies to entire table

Symbol	Description	Min	Max	Units
$C_{IN/OUT}$	Input/output capacitance (DQ0/DQ1/DQ2/DQ3) (DQ4/DQ5/DQ6/DQ7)	–	10	pF
C_{IN}	Input capacitance (other pins)	–	6 (2)	pF
$C_{IN/S\#}$	Input/Chip select	–	10 (3)	pF

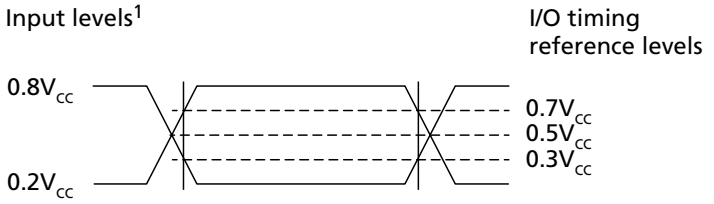
Notes:
1. Verified in device characterization; not 100% tested. These parameters are not subject to a production test. They are verified by design and characterization. The capacitance is measured according to JEP147 ("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA)") with V_{CC} and V_{SS} applied and all other pins floating (except the pin under test), $V_{BIAS} = V_{CC}/2$, T_A = 25°C, Frequency = 54 MHz
2. For 1CS/1CLK configuration, capacitance is double for CLK and it is 12pF.
3. For 1CS/1CLK configuration, capacitance is double for Chip Select pin and it is 20pF.

Table 45: AC Timing Input/Output Conditions

Symbol	Description	Min	Max	Units	Notes
C_L	Load capacitance	10	30	pF	1
–	Input rise and fall times	–	1.5	ns	
	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V	2
	Input timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V	
	Output timing reference voltages	$V_{CC}/2$	$V_{CC}/2$	V	

Notes: 1. Output buffers are configurable by user.
2. For quad/dual operations: 0V to V_{CC}.

Figure 48: AC Timing Input/Output Reference Levels



Note: 1. $0.8V_{CC} = V_{CC}$ for dual/quad operations; $0.2V_{CC} = 0V$ for dual/quad operations.

DC Characteristics and Operating Conditions

The table below applies to each 512Mb Flash device. As each 512Mb device can operate independently from each other, Designer must take into consideration combined total power consumption of Twin-Quad 1Gb device

Table 46: DC Current Characteristics and Operating Conditions

Notes 1–5 apply to entire table

Parameter	Symbol	Test Conditions	Typ	Max	Unit
Input leakage current	I_{LI}		–	±2	µA
Output leakage current	I_{LO}		–	±2	µA
Standby current (AT range)	I_{CC1}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	30	200	µA
Deep power-down current (AT range)	I_{CC2}	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	5	100	µA
Operating current (fast-read extended I/O)	I_{CC3}	C = 0.1V_{CC}/0.9V_{CC} at 133 MHz, DQ1/DQ5 = open	–	16	mA
		C = 0.1V_{CC}/0.9V_{CC} at 54 MHz, DQ1/DQ5 = open	–	10	mA
Operating current (fast-read dual I/O)		C = 0.1V_{CC}/0.9V_{CC} at 133 MHz DQ = open	–	20	mA
Operating current (fast-read quad I/O)		C = 0.1V_{CC}/0.9V_{CC} at 133 MHz, DQ = open	–	24	mA
		C = 0.1V_{CC}/0.9V_{CC} at 80 MHz DTR, DQ = open	–	28	mA
		C = 0.1V_{CC}/0.9V_{CC} at 90 MHz DTR, DQ = open	–	31	mA
Operating current (PROGRAM operations)	I_{CC4}	S# = V_{CC}	–	35	mA
Operating current (WRITE operations)	I_{CC5}	S# = V_{CC}	–	35	mA
Operating current (erase)	I_{CC6}	S# = V_{CC}	–	35	mA

Notes:
1. All currents are RMS unless noted. Typical values at typical V_{CC} (3.0/1.8V); V_{IO} = 0V/V_{CC}; T_C = +25°C.
2. Standby current is the average current measured over any time interval 5µs after S de-assertion (and any internal operations are complete).
3. Deep power-down current is the average current measured 5ms over any 5ms time interval, 100µs after the ENTER DEEP POWER-DOWN operation (and any internal operations are complete).
4. All read currents are the average current measured over any 1KB continuous read. No load, checker-board pattern.
5. All program currents are the average current measured over any 256-byte typical data program.

Table 47: DC Voltage Characteristics and Operating Conditions

Note 1 applies to entire table

Parameter	Symbol	Conditions	Min	Max	Unit
Input low voltage	V_{IL}		–0.5	$0.3V_{CC}$	V
Input high voltage	V_{IH}		$0.7V_{CC}$	V_{CC} + 0.4	V
Output low voltage	V_{OL}	I_{OL} = 1.6mA	–	0.4	V
Output high voltage	V_{OH}	I_{OH} = –100µA	V_{CC} - 0.2	–	V

Note: 1. V_{IL} can undershoot to –1.0V for periods <2ns and V_{IH} may overshoot to $V_{CC,max}$ + 1.0V for periods less than 2ns.

AC Characteristics and Operating Conditions

Table 48: AC Characteristics and Operating Conditions

Parameter	Symbol	Data Transfer Rate	Min	Typ	Max	Unit	Notes
Clock frequency for all commands other than READ (Extended-SPI, DIO-SPI, and QIO-SPI protocol)	^{f}C	STR	DC	–	133	MHz	
		DTR	DC	–	90		
Clock frequency for READ command (03h or 13h)	^{f}R	STR	DC	–	54	MHz	
		DTR	DC	–	27		
Clock HIGH time	^{t}CH	STR	3.375	–	–	ns	2
		DTR	5.0	–	–		
Clock LOW time	^{t}CL	STR	3.375	–	–	ns	2
		DTR	5.0	–	–		
Clock rise time (peak-to-peak)	$^{t}CLCH$	STR/DTR	0.1	–	–	V/ns	3, 4
Clock fall time (peak-to-peak)	$^{t}CHCL$	STR/DTR	0.1	–	–	V/ns	3, 4
S# active setup time (relative to clock)	$^{t}SLCH$	STR/DTR	3.375	–	–	ns	
S# not active hold time (relative to clock)	$^{t}CHSL$	STR/DTR	3.375	–	–	ns	
Data in setup time	$^{t}DVCH$	STR	1.75	–	–	ns	
		DTR	1.5	–	–	ns	
	$^{t}DVCL$	DTR only	1.5	–	–	ns	
Data in hold time	$^{t}CHDX$	STR/DTR	2.3	–	–	ns	
	$^{t}CLDX$	DTR only	2.3	–	–	ns	
S# active hold time (relative to clock)	$^{t}CHSH$	STR	3.375	–	–	ns	
		DTR	5.0	–	–		
S# active hold time (relative to clock LOW) Only for writes in DTR	$^{t}CLSH$	DTR only	3.375	–	–	ns	
S# not active setup time (relative to clock)	$^{t}SHCH$	STR	3.375	–	–	ns	
		DTR	5.0	–	–	ns	
S# deselect time after a READ command	$^{t}SHSL1$	STR/DTR	20	–	–	ns	
S# deselect time after a nonREAD command	$^{t}SHSL2$	STR/DTR	50	–	–	ns	
Output disable time	$^{t}SHQZ$	STR/DTR	–	–	7	ns	3
Clock LOW to output valid under 30pF	$^{t}CLQV$	STR/DTR	–	–	6	ns	
Clock LOW to output valid under 10pF		STR/DTR	–	–	5	ns	
Clock HIGH to output valid under 30pF	$^{t}CHQV$	DTR only	–	–	6	ns	
Clock HIGH to output valid under 10pF		DTR only	–	–	5	ns	
Output hold time	$^{t}CLQX$	STR/DTR	1.5	–	–	ns	
Output hold time	$^{t}CHQX$	DTR only	1.5	–	–	ns	
HOLD setup time (relative to clock)	$^{t}HLCH$	STR/DTR	3.375	–	–	ns	
HOLD hold time (relative to clock)	$^{t}CHHH$	STR/DTR	3.375	–	–	ns	

Table 48: AC Characteristics and Operating Conditions (Continued)

Parameter	Symbol	Data Transfer Rate	Min	Typ	Max	Unit	Notes
HOLD setup time (relative to clock)	^{t}HHCH	STR/DTR	3.375	–	–	ns	
HOLD hold time (relative to clock)	^{t}CHHL	STR/DTR	3.375	–	–	ns	
HOLD to output Low-Z	^{t}HHQX	STR/DTR	–	–	8	ns	3
HOLD to output High-Z	^{t}HLQZ	STR/DTR	–	–	8	ns	3
CRC check time: Main block	^{t}CRC	STR/DTR	–	1.3	–	ms	
CRC check time: Full chip (512Mb)	^{t}CRC	STR/DTR	–	2	–	s	
Write protect setup time	^{t}WHSL	STR/DTR	20	–	–	ns	5
Write protect hold time	^{t}SHWL	STR/DTR	100	–	–	ns	5
S# HIGH to deep power-down	^{t}DP	STR/DTR	3	–	–	us	
S# HIGH to standby mode (DPD exit time)	^{t}RDP	STR/DTR	30	–	–	us	
WRITE STATUS REGISTER cycle time	^{t}W	STR/DTR	–	1.3	8	ms	
WRITE NONVOLATILE CONFIGURATION REGISTER cycle time	^{t}WNVCR	STR/DTR	–	0.2	1	s	
Nonvolatile sector lock time	^{t}PPBP	STR/DTR	–	0.1	2.8	ms	
Program ASP register	^{t}ASPP	STR/DTR	–	0.1	0.5	ms	
Program password	^{t}PASSP	STR/DTR	–	0.2	0.8	ms	
Erase nonvolatile sector lock array	^{t}PPBE	STR/DTR	–	0.2	1	s	
Page program time (256 bytes)	^{t}PP	STR/DTR	–	120	1800	us	7
Page program time (n bytes)			–	18 + 2.5 x int(n/6)	1800	us	8
PROGRAM OTP cycle time (64 bytes)	^{t}POTP	STR/DTR	–	0.12	0.8	ms	
Sector erase time	^{t}SE	STR/DTR	–	0.15	1	s	
4KB subsector erase time	^{t}SSE	STR/DTR	–	0.05	0.4	s	
32KB subsector erase time	^{t}SSE	STR/DTR	–	0.1	1	s	
512Mb bulk erase time	^{t}DE	STR/DTR	–	153	460	s	

Notes:
1. Typical values given for T_A = 25°C.
2. ^{t}CH + ^{t}CL must add up to 1/^{f}C.
3. Value guaranteed by characterization; not 100% tested.
4. Expressed as a slew-rate.
5. Only applicable as a constraint for a WRITE STATUS REGISTER command when STATUS REGISTER WRITE is set to 1.
6. Typical value is applied for pattern: 50% 0 and 50% 1.
7. int(n) correspond to the integer part of n, For example int (12/8) = 1, int (32/8) = 4 int(15.3) = 15.

AC Reset Specifications

Table 49: AC Reset Conditions

Note 1 applies to entire table

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reset pulse width	^{t}RLRH[2]		50	–	–	ns
Reset recovery time	^{t}RHSL	Device deselected (S# HIGH) and is in XIP mode	40	–	–	ns
		Device deselected (S# HIGH) and is in standby mode	40	–	–	ns
		Commands are being decoded, any READ operations are in progress or any WRITE operation to volatile registers are in progress	40	–	–	ns
		Any device array PROGRAM/ERASE/SUSPEND/RESUME, PROGRAM OTP, NONVOLATILE SECTOR LOCK, and ERASE NONVOLATILE SECTOR LOCK ARRAY operations are in progress	30	–	–	µs
		While a WRITE STATUS REGISTER operation is in progress	–	^{t}W	–	ms
		While a WRITE NONVOLATILE CONFIGURATION REGISTER operation is in progress	–	^{t}WNVCR	–	ms
		On completion or suspension of a SUBSECTOR ERASE operation	–	^{t}SSE	–	s
		Device in deep power-down mode	–	^{t}RDP	–	ms
		While ADVANCED SECTOR PROTECTION PROGRAM operation is in progress	–	^{t}ASPP	–	ms
		While PASSWORD PROTECTION PROGRAM operation is in progress	–	^{t}PASSP	–	ms
Software reset recovery time	^{t}SHSL3	Device deselected (S# HIGH) and is in standby mode	40	–	–	ns
		Any Flash array PROGRAM/ERASE/SUSPEND/RESUME, PROGRAM OTP, NONVOLATILE SECTOR LOCK, and ERASE NONVOLATILE SECTOR LOCK ARRAY operations are in progress	30	–	–	µs
		While WRITE STATUS REGISTER operation is in progress	–	^{t}W	–	ms
		While a WRITE NONVOLATILE CONFIGURATION REGISTER operation is in progress	–	^{t}WNVCR	–	ms
		On completion or suspension of a SUBSECTOR ERASE operation	–	^{t}SSE	–	s
		Device in deep power-down mode	–	^{t}RDP	–	ms
		While ADVANCED SECTOR PROTECTION PROGRAM operation is in progress	–	^{t}ASPP	–	ms
		While PASSWORD PROTECTION PROGRAM operation is in progress	–	^{t}PASSP	–	ms

Program/Erase Specifications

Table 50: Program/Erase Specifications

Parameter	Condition	Typ	Max	Units	Notes
Erase to suspend	Sector erase or erase resume to erase suspend	150	–	µs	1
Program to suspend	Program resume to program suspend	5	–	µs	1
Subsector erase to suspend	Subsector erase or subsector erase resume to erase suspend	50	–	µs	1
Suspend latency	Program	7	25	µs	2
Suspend latency	Subsector erase	15	30	µs	2
Suspend latency	Erase	15	30	µs	3

Notes:
1. Timing is not internally controlled.
2. Any READ command accepted.
3. Any command except the following are accepted: SECTOR, SUBSECTOR, or DIE ERASE; WRITE STATUS REGISTER; WRITE NONVOLATILE CONFIGURATION REGISTER; and PROGRAM OTP.

1. GENERAL DESCRIPTIONS

The W25N01GV (1G-bit) Serial SLC NAND Flash Memory provides a storage solution for systems with limited space, pins and power. The W25N SpiFlash family incorporates the popular SPI interface and the traditional large NAND non-volatile memory space. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 25mA active and 10µA for standby. All W25N SpiFlash family devices are offered in space-saving packages which were impossible to use in the past for the typical NAND flash memory.

The W25N01GV 1G-bit memory array is organized into 65,536 programmable pages of 2,048-bytes each. The entire page can be programmed at one time using the data from the 2,048-Byte internal buffer. Pages can be erased in groups of 64 (128KB block erase). The W25N01GV has 1,024 erasable blocks.

The W25N01GV supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 416MHz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions.

The W25N01GV provides a new Continuous Read Mode that allows for efficient access to the entire memory array with a single Read command. This feature is ideal for code shadowing applications.

A Hold pin, Write Protect pin and programmable write protection, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID, one 2,048-Byte Unique ID page, one 2,048-Byte parameter page and ten 2,048-Byte OTP pages. To provide better NAND flash memory manageability, user configurable internal ECC, bad block management are also available in W25N01GV.

2. FEATURES

- **New W25N Family of SpiFlash Memories**
  - W25N01GV: 1G-bit / 128M-byte
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Compatible SPI serial flash commands
- **Highest Performance Serial NAND Flash**
  - 104MHz Standard/Dual/Quad SPI clocks
  - 208/416MHz equivalent Dual/Quad SPI
  - 50MB/S continuous data transfer rate
  - Fast Program/Erase performance
  - More than 100,000 erase/program cycles(4)
  - More than 10-year data retention
- **Efficient "Continuous Read Mode"(1)**
  - Alternative method to the Buffer Read Mode
  - No need to issue "Page Data Read" between Read commands
  - Allows direct read access to the entire array
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 25mA active, 10µA standby current
  - -40°C to +85°C operating range
- **Flexible Architecture with 128KB blocks**
  - Uniform 128K-Byte Block Erase
  - Flexible page data load methods
- **Advanced Features**
  - On chip 1-Bit ECC for memory array
  - ECC status bits indicate ECC results
  - bad block management and LUT(2) access
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - 2KB Unique ID and 2KB parameter pages
  - Ten 2KB OTP pages(3)
- **Space Efficient Packaging**
  - 8-pad WSON 8x6-mm
  - 16-pin SOIC 300-mil
  - 24-ball TFBGA 8x6-mm
  - Contact Winbond for other package options

Notes:

1. Only the Read command structures are different between the "Continuous Read Mode (BUF=0)" and the "Buffer Read Mode (BUF=1)", all other commands are identical. W25N01GVxxIG: Default BUF=1 after power up W25N01GVxxIT: Default BUF=0 after power up
2. LUT stands for Look-Up Table.
3. OTP pages can only be programmed.
4. Endurance specification is based on the on-chip ECC or 1bit/528 byte ECC(Error Correcting Code)

3. PACKAGE TYPES AND PIN CONFIGURATIONS

W25N01GV is offered in an 8-pad WSON 8x6-mm (package code ZE), a 16-pin SOIC 300-mil (package code SF), and two 24-ball 8x6-mm TFBGA (package code TB & TC) packages as shown in Figure 1a-c respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

3.1 Pad Configuration WSON 8x6-mm

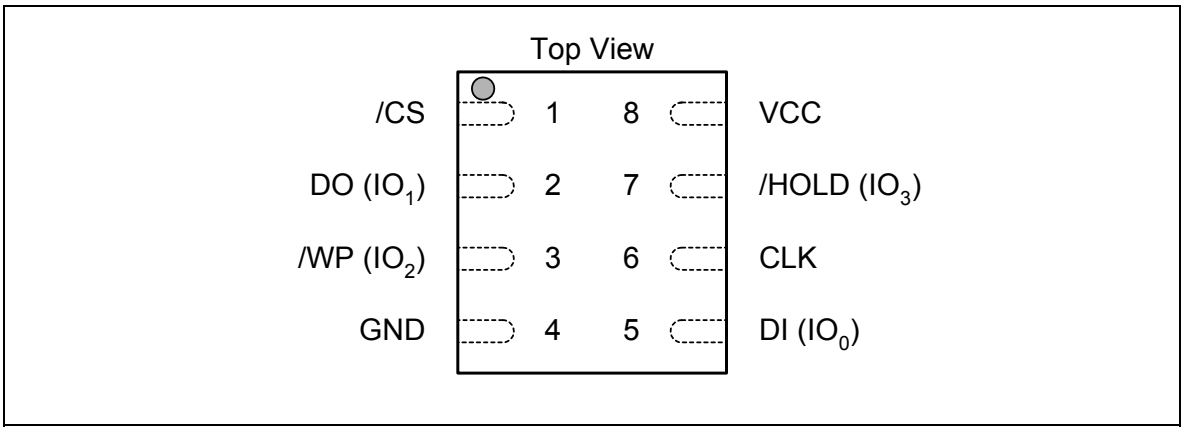


Figure 1a. W25N01GV Pad Assignments, 8-pad WSON 8x6-mm (Package Code ZE)

3.2 Pad Description WSON 8x6-mm

PAD NO.	PAD NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)(2)
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.

3.3 Pin Configuration SOIC 300-mil

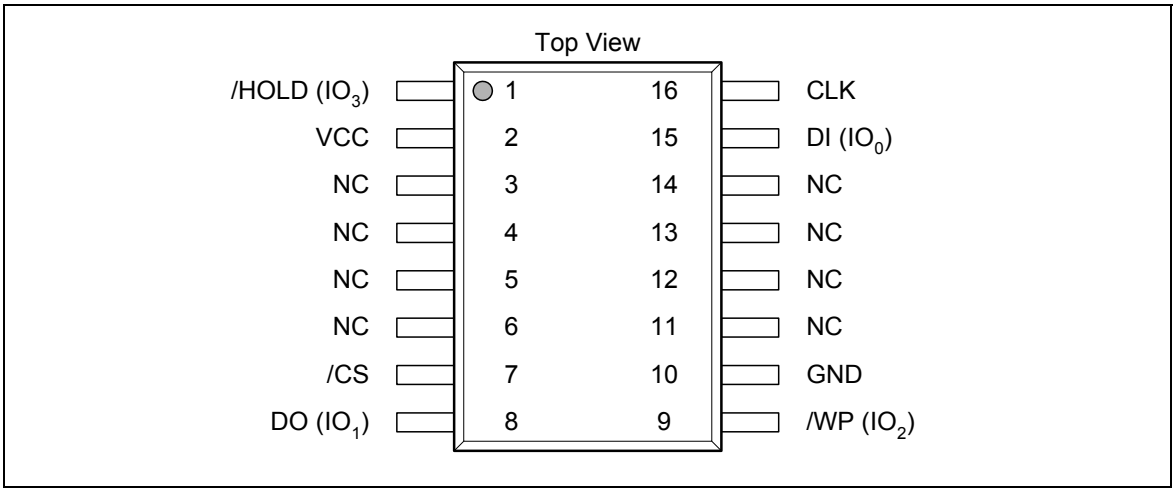


Figure 1b. W25N01GV Pin Assignments, 16-pin SOIC 300-mil (Package Code SF)

3.4 Pin Description SOIC 300-mil

PIN NO.	PIN NAME	I/O	FUNCTION
1	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)(2)
2	VCC		Power Supply
3	N/C		No Connect
4	N/C		No Connect
5	N/C		No Connect
6	N/C		No Connect
7	/CS	I	Chip Select Input
8	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
9	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
10	GND		Ground
11	N/C		No Connect
12	N/C		No Connect
13	N/C		No Connect
14	N/C		No Connect
15	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
16	CLK	I	Serial Clock Input

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.

3.5 Ball Configuration TFBGA 8x6-mm (5x5 or 6x4 Ball Array)

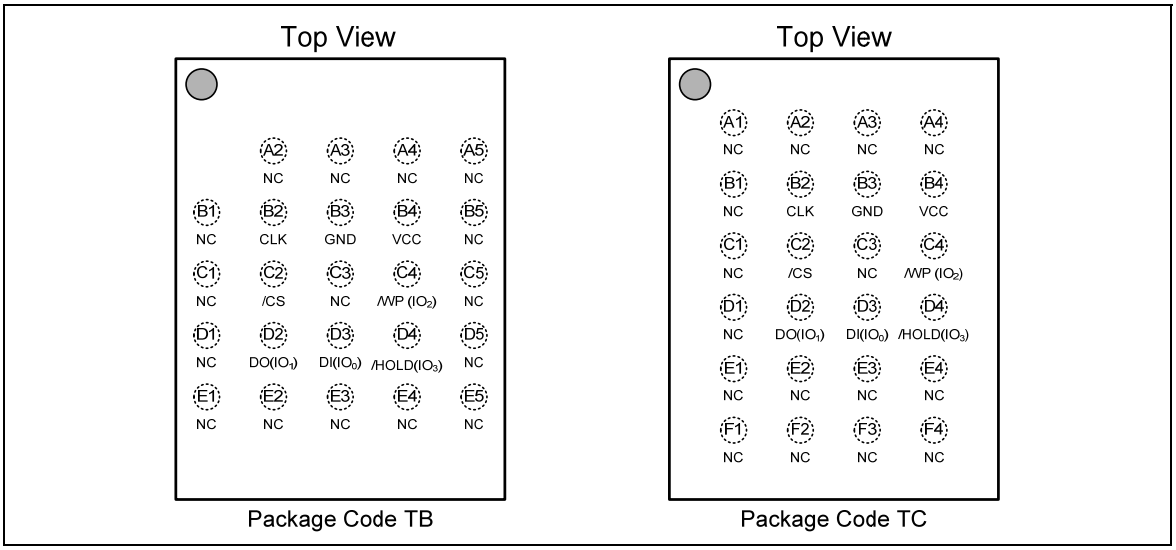


Figure 1c. W25N01GV Ball Assignments, 24-ball TFBGA 8x6-mm (Package Code TB & TC)

3.6 Ball Description TFBGA 8x6-mm

BALL NO.	PIN NAME	I/O	FUNCTION
B2	CLK	I	Serial Clock Input
B3	GND		Ground
B4	VCC		Power Supply
C2	/CS	I	Chip Select Input
C4	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
D2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
D3	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
D4	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)(2)
Multiple	NC		No Connect

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.

4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 30b). If needed, a pull-up resistor on the /CS pin can be used to accomplish this.

4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25N01GV supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

4.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect bits BP[3:0] and Status Register Protect SRP bits SRP[1:0], a portion as small as 256K-Byte (2x128KB blocks) or up to the entire memory array can be hardware protected. The WP-E bit in the Protection Register (SR-1) controls the functions of the /WP pin.

When WP-E=0, the device is in the Software Protection mode that only SR-1 can be protected. The /WP pin functions as a data I/O pin for the Quad SPI operations, as well as an active low input pin for the Write Protection function for SR-1. Refer to section 7.1.3 for detail information.

When WP-E=1, the device is in the Hardware Protection mode that /WP becomes a dedicated active low input pin for the Write Protection of the entire device. If /WP is tied to GND, all “Write/Program/Erase” functions are disabled. The entire device (including all registers, memory array, OTP pages) will become read-only. Quad SPI read operations are also disabled when WP-E is set to 1.

4.4 HOLD (/HOLD)

During Standard and Dual SPI operations, the /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low.

When a Quad SPI Read/Buffer Load command is issued, /HOLD pin will become a data I/O pin for the Quad operations and no HOLD function is available until the current Quad operation finishes. /HOLD (IO3) must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the /HOLD input to float.

4.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings[1]

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to +4.6	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to +4.6	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Short Circuit Output Crrent, IOs			5	mA
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		See Note [2]	°C
Electrostatic Discharge Voltage	VESD	Human Body Model[3]	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Standard JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

9.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC		2.7	3.6	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	°C

9.3 Power-up Power-down Timing Requirements

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	t_{VSL}(1)	1		ms
Time Delay Before Write Instruction	t_{PUW}(1)	5		ms
Write Inhibit Threshold Voltage	V_{WI}(1)	1.0	2.0	V

Note:

1. These parameters are characterized only.

9.3.1 Power-up Timing and Voltage Levels

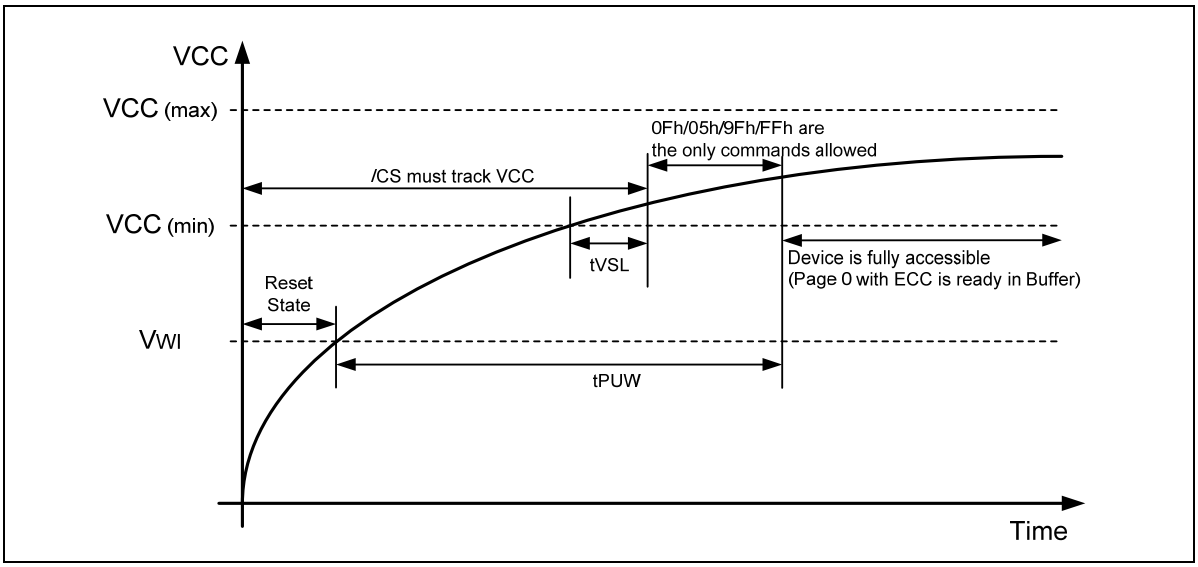


Figure 30a. Power-up Timing and Voltage Levels

9.3.2 Power-up, Power-Down Requirement

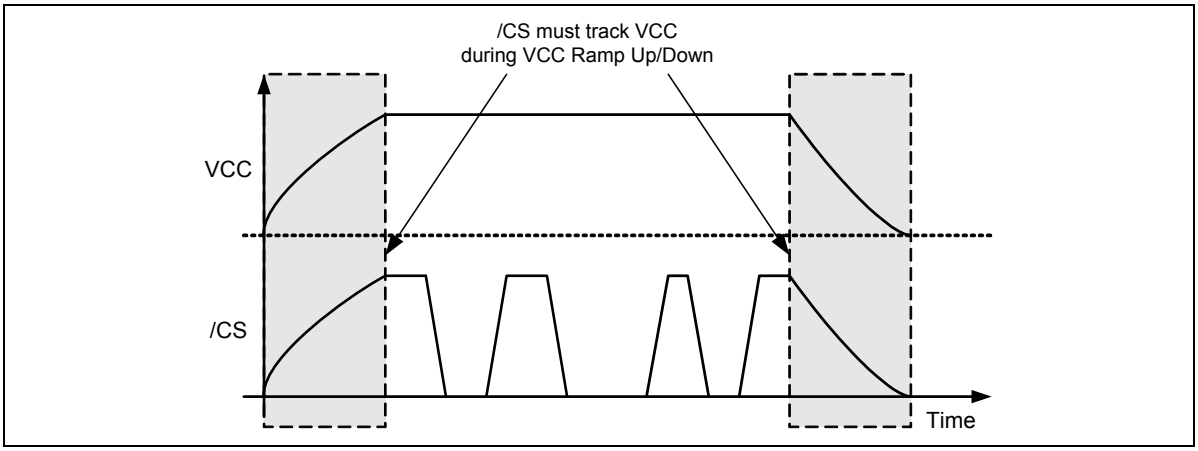


Figure 30b. Power-up, Power-Down Requirement

9.4 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN}[1]	V_{IN} = 0V[1]			6	pF
Output Capacitance	C_{out}[1]	V_{OUT} = 0V[1]			8	pF
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	/CS = VCC, VIN = GND or VCC		10	50	µA
Read Current	I_{CC2}	C = 0.1 VCC / 0.9 VCC DO = Open		25	35	mA
Current Page Program	I_{CC3}	/CS = VCC		25	35	mA
Current Block Erase	I_{CC4}	/CS = VCC		25	35	mA
Input Low Voltage	V_{IL}				VCC x 0.3	V
Input High Voltage	V_{IH}		VCC x 0.7			V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = –400 µA	2.4			V

Notes:

1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.

9.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC		V

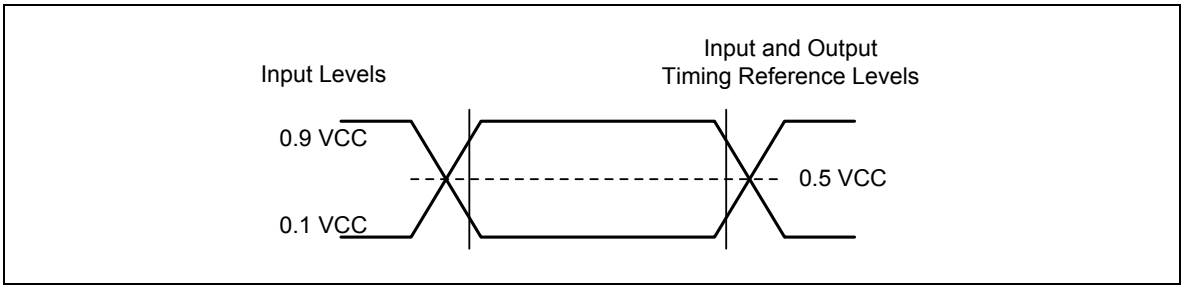


Figure 31. AC Measurement I/O Waveform

9.6 AC Electrical Characteristics(3)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency for all instructions	F_R	f_{C1}	D.C.		104	MHz
Clock High, Low Time for all instructions	t_{CLH}, t_{CLL}(1)		4			ns
Clock Rise Time peak to peak	t_{CLCH}(2)		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL}(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	3			ns
/CS Active Hold Time relative to CLK	t_{CHSH}		3			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		3			ns
/CS Deselect Time (for Array Read → Array Read)	t_{SHSL1}	t_{CSH}	10			ns
/CS Deselect Time (for Erase, Program or Read Status Registers → Read Status Registers)	t_{SHSL2}	t_{CSH}	50			ns
Output Disable Time	t_{SHQZ}(2)	t_{DIS}			7	ns
Clock Low to Output Valid	t_{CLQV}	t_V			7	ns
Output Hold Time	t_{CLQX}	t_{HO}	2			ns
/HOLD Active Setup Time relative to CLK	t_{HLCH}		5			ns
/HOLD Active Hold Time relative to CLK	t_{CHHH}		5			ns

Continued – next page

AC Electrical Characteristics (cont'd)

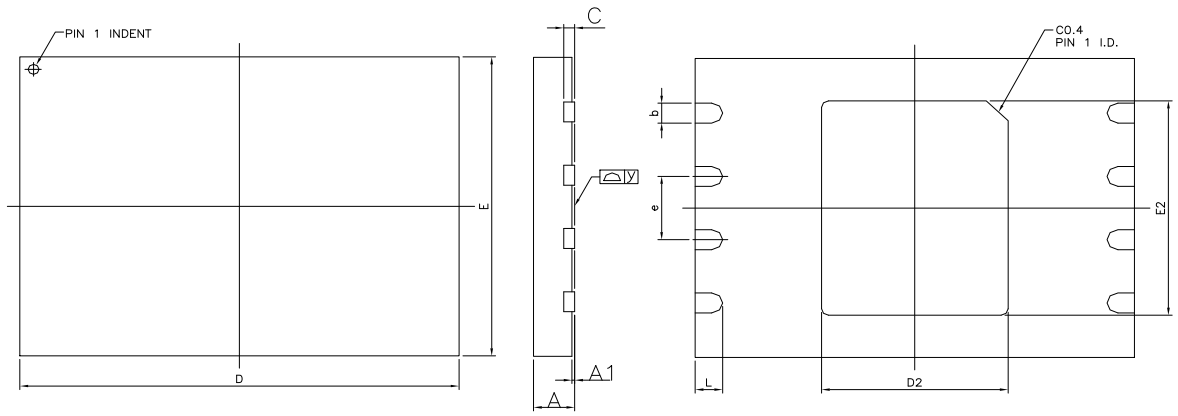
DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD Not Active Setup Time relative to CLK	t_{HHCH}		5			ns
/HOLD Not Active Hold Time relative to CLK	t_{CHHL}		5			ns
/HOLD to Output Low-Z	t_{HHQX}(2)	t_{LZ}			7	ns
/HOLD to Output High-Z	t_{HLQZ}(2)	t_{HZ}			12	ns
Write Protect Setup Time Before /CS Low	t_{WHSL}		20			ns
Write Protect Hold Time After /CS High	t_{SHWL}		100			ns
Status Register Write Time	t_{W}				50	ns
/CS High to next Instruction after Reset during Page Data Read / Program Execute / Block Erase	t_{RST}(2)				5/10/500	µs
Read Page Data Time (ECC disabled)	t_{RD1}				25	µs
Read Page Data Time (ECC enabled)	t_{RD2}				60	µs
Page Program, OTP Lock, BBM Management Time	t_{PP}			250	700	us
Block Erase Time	t_{BE}			2	10	ms
Number of partial page programs	NoP				4	times

Notes:

1. Clock high + Clock low must be less than or equal to 1/fC.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.

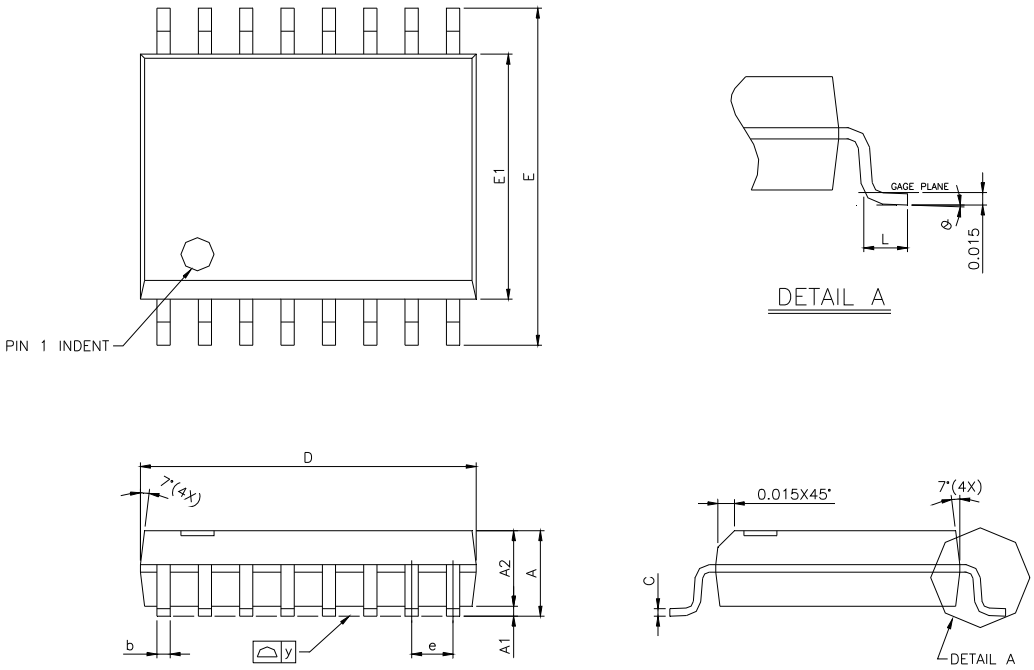
11. PACKAGE SPECIFICATIONS

11.1 8-Pad WSON 8x6-mm (Package Code ZE)



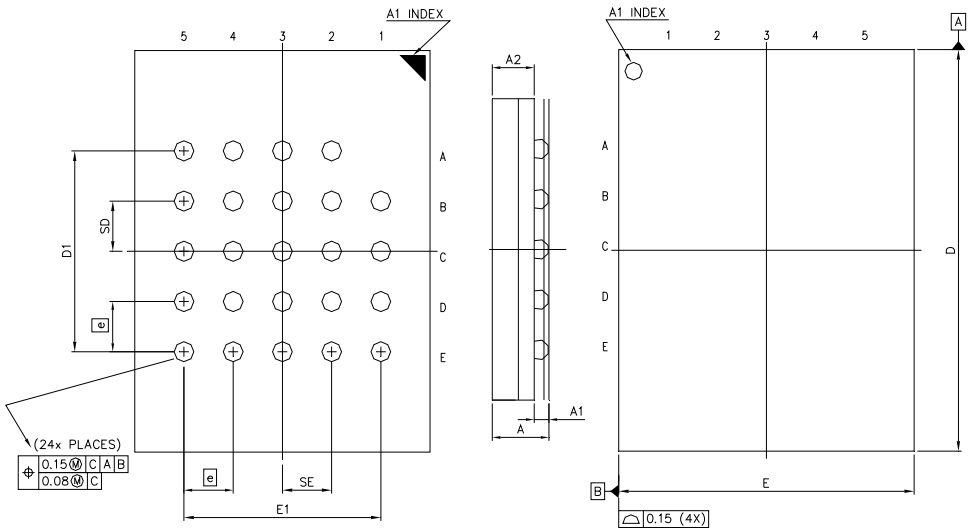
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.48	0.014	0.016	0.019
C	---	0.20 REF	---	---	0.008 REF	---
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	3.35	3.40	3.45	0.132	0.134	0.136
E	5.90	6.00	6.10	0.232	0.236	0.240
E2	4.25	4.30	4.35	0.167	0.169	0.171
e	---	1.27	---	---	0.050	---
L	0.45	0.50	0.55	0.018	0.020	0.022
y	0.00	---	0.050	0.000	---	0.002

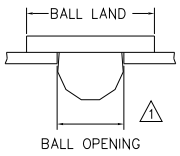
11.2 16-Pin SOIC 300-mil (Package Code SF)



Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	---	0.30	0.004	---	0.012
A2	---	2.31	---	---	0.091	---
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	10.08	10.31	10.49	0.397	0.406	0.413
E	10.01	10.31	10.64	0.394	0.406	0.419
E1	7.39	7.49	7.59	0.291	0.295	0.299
e	1.27 BSC			0.050 BSC		
L	0.38	0.81	1.27	0.015	0.032	0.050
y	---	---	0.076	---	---	0.003
θ	0°	---	8°	0°	---	8°

11.3 24-Ball TFBGA 8x6-mm (Package Code TB, 5x5-1 Ball Array)

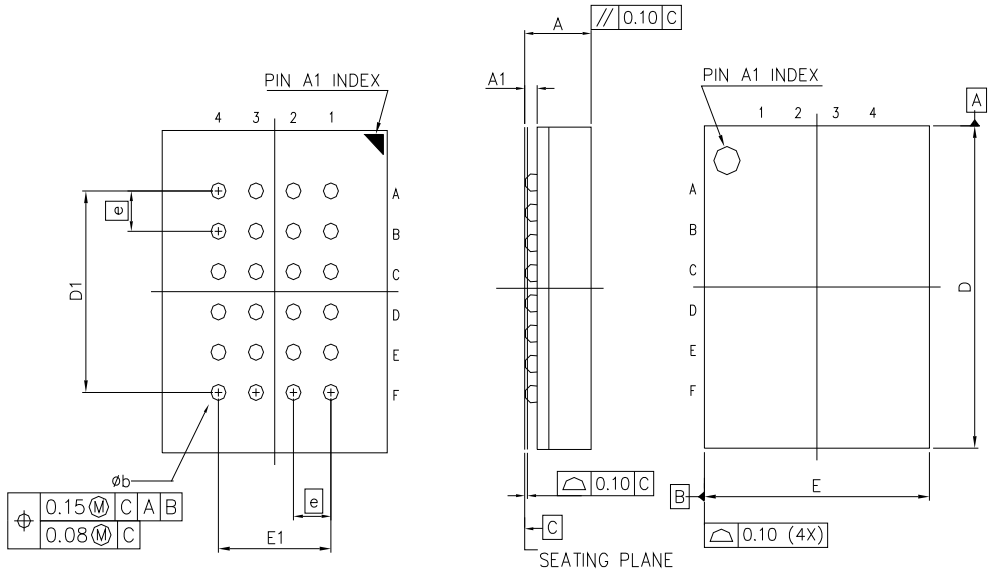


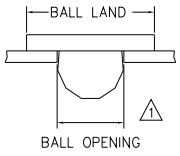


Note:
Ball land: 0.45mm. Ball Opening: 0.35mm
PCB ball land suggested <= 0.35mm

Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.20	---	---	0.047
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	---	0.85	---	---	0.033	---
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.90	8.00	8.10	0.311	0.315	0.319
D1		4.00 BSC			0.157 BSC	
E	5.90	6.00	6.10	0.232	0.236	0.240
E1		4.00 BSC			0.157 BSC	
SE		1.00 TYP			0.039 TYP	
SD		1.00 TYP			0.039 TYP	
e		1.00 BSC			0.039 BSC	

11.4 24-Ball TFBGA 8x6-mm (Package Code TC, 6x4 Ball Array)





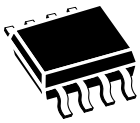
Note:
Ball land: 0.45mm. Ball Opening: 0.35mm
PCB ball land suggested <= 0.35mm

Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.20	---	---	0.047
A1	0.25	0.30	0.35	0.010	0.012	0.014
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.95	8.00	8.05	0.313	0.315	0.317
D1		5.00 BSC			0.197 BSC	
E	5.95	6.00	6.05	0.234	0.236	0.238
E1		3.00 BSC			0.118 BSC	
e		1.00 BSC			0.039 BSC	

M95M02-A125

Automotive 2 Mbit serial SPI bus EEPROM

Datasheet - production data



SO8 (MN)
150 mil width

Features

- Compatible with the Serial Peripheral Interface (SPI) bus
- Memory array
  - 2 Mbit (256 Kbyte) of EEPROM
  - Page size: 256 byte
  - Write protection by block: 1/4, 1/2 or whole memory
  - Additional Write lockable Page (Identification page)
- Extended temperature and voltage ranges
  - Up to 125 °C (V_{CC} from 2.5 V to 5.5 V)
- Clock frequency
  - 10 MHz for $V_{CC} \geq 4.5$ V @ 105°C
  - 5 MHz for $V_{CC} \geq 2.5$ V @ 125°C
- Schmitt trigger inputs for noise filtering
- Short Write cycle time
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Write cycle endurance
  - 4 million Write cycles at 25 °C
  - 1.2 million Write cycles at 85 °C
  - 100 k Write cycles at 125 °C
- Data retention
  - 100 years at 25 °C
- ESD Protection (Human Body Model)
  - 3000 V
- Packages
  - RoHS-compliant and halogen-free (ECOPACK2®)

1 Description

The M95M02-A125 is 2-Mbit serial EEPROM Automotive grade device operating up to 125°C. The M95M02-A125 is compliant with the very high level of reliability defined by the Automotive standard AEC-Q100 grade 0.

The device is accessed by a simple serial SPI compatible interface running up to 10 MHz.

The memory array is based on advanced true EEPROM technology (Electrically Erasable PROgrammable Memory). The M95M02-A125 is byte-alterable memories (262144 × 8 bits) organized as 1024 pages of 256 byte in which the data integrity is significantly improved with an embedded Error Correction Code logic.

The M95M02-A125 offers an additional Identification Page (256 byte) in which the ST device identification can be read. This page can also be used to store sensitive application parameters which can be later permanently locked in read-only mode.

Figure 1. Logic diagram

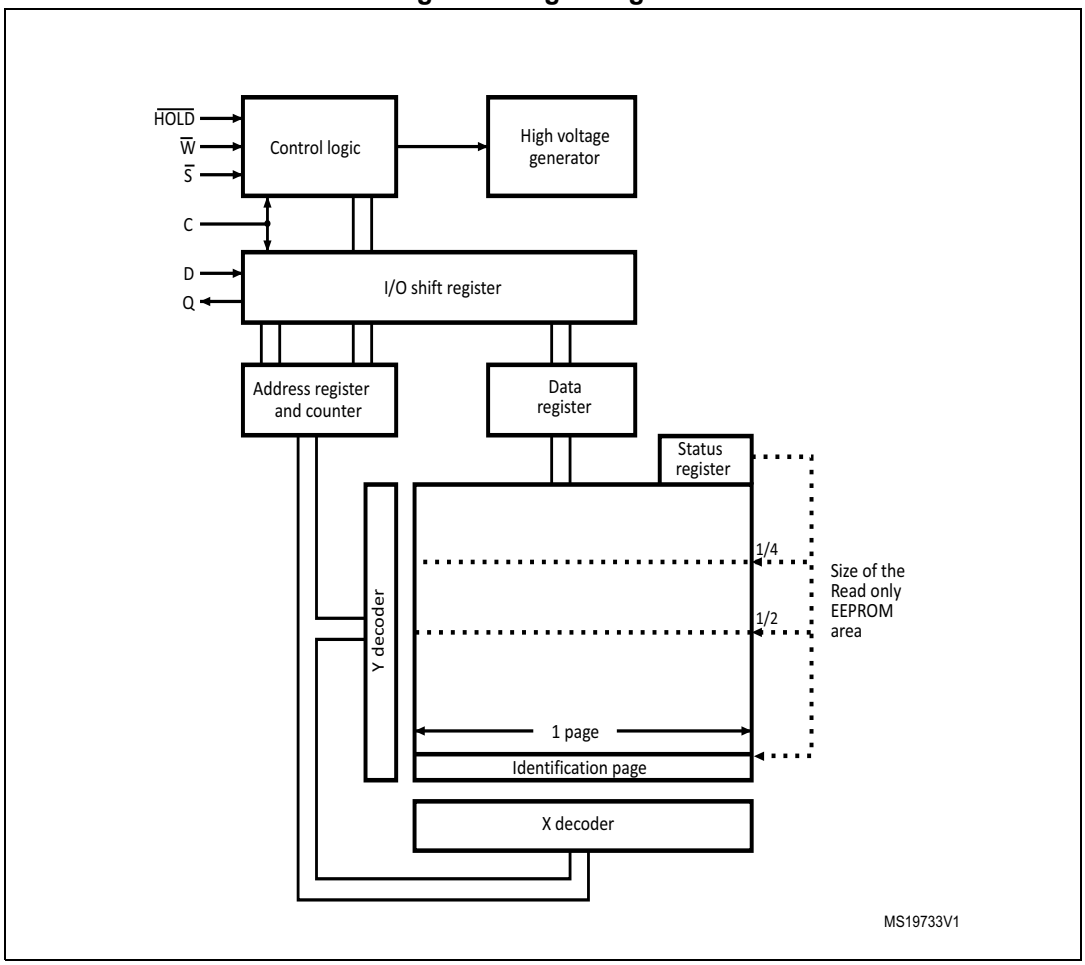
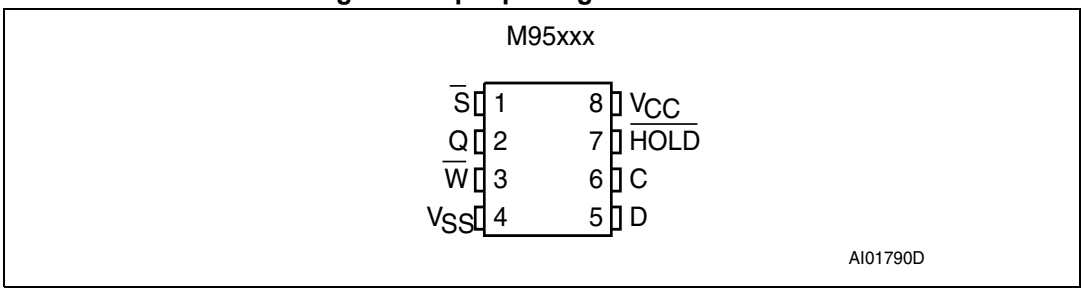


Figure 2. 8-pin package connections



1. See *Package mechanical data* section for package dimensions and how to identify pin-1.

Table 1. Signal names

Signal name	Description
C	Serial Clock
D	Serial data input
Q	Serial data output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply voltage
V_{SS}	Ground

2 Signal description

All input signals must be held high or low (according to voltages of V_{IH} or V_{IL}, as specified in *Table 12*). These signals are described below.

2.1 Serial Data output (Q)

This output signal is used to transfer data serially out of the device during a Read operation. Data is shifted out on the falling edge of Serial Clock (C), most significant bit (MSB) first. In all other cases, the Serial Data output is in high impedance.

2.2 Serial Data input (D)

This input signal is used to transfer data serially into the device. D input receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C), most significant bit (MSB) first.

2.3 Serial Clock (C)

This input signal allows to synchronize the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

Driving Chip Select ($\overline{S}$) low selects the device in order to start communication. Driving Chip Select ($\overline{S}$) high deselects the device and Serial Data output (Q) enters the high impedance state.

2.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

2.6 Write Protect ($\overline{W}$)

This pin is used to write-protect the Status Register.

2.7 V_{SS} ground

V_{SS} is the reference for all signals, including the V_{CC} supply voltage.

2.8 V_{CC} supply voltage

V_{CC} is the supply voltage pin. Refer to *Section 3.1: Active power and Standby power modes* and to *Section 5.1: Supply voltage (V_{CC})*.

6 Delivery state

The device is delivered with:

- the memory array set to all 1s (each byte = FFh),
- Status register: bit SRWD =0, BP1 =0 and BP0 =0,
- Identification page: the first three bytes define the Device identification code (value defined in *Table 5*). The content of the following bytes is Don't Care.

7 Absolute maximum ratings

Stressing the device outside the ratings listed in *Table 8* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage temperature	–65	150	°C
T_{AMR}	Ambient operating temperature	–40	130	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_O	Voltage on Q pin	–0.50	V_{CC}+0.6	V
V_I	Input voltage	–0.50	6.5	V
I_{OL}	DC output current (Q = 0)	-	5	mA
I_{OH}	DC output current (Q = 1)	-	5	mA
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (Human Body Model)(2)	-	3000	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb-free assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions of Hazardous Substances (RoHS directive 2011/65/EU of July 2011).
2. Positive and negative pulses applied on pin pairs, in accordance with AEC-Q100-002 (compliant with ANSI/ESDA/JEDEC JS-001-2012, C1=100 pF, R1=1500 Ω, R2=500 Ω)

8 DC and AC parameters

This section summarizes the operating conditions and the DC/AC characteristics of the device.

Table 9. Cycling performance by groups of 4 byte

Symbol	Parameter	Test condition	Min.	Max.	Unit
Ncycle	Write cycle endurance(1)	TA ≤ 25 °C, V < V_{CC} < 5.5 V	-	4,000,000	Write cycle(2)
		TA = 85 °C, V < V_{CC} < 5.5 V	-	1,200,000	
		TA = 105 °C, 2.5 V < V_{CC} < 5.5 V	-	300,000	
		TA = 125 °C, 2.5 V < V_{CC} < 5.5 V	-	100,000	

1. The Write cycle endurance is defined for groups of four data bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer, or for the status register byte (refer also to *Section 5.3: Cycling with Error Correction Code (ECC)*). The Write cycle endurance is defined by characterization and qualification.
2. A Write cycle is executed when either a Page Write, a Byte Write, a WRSR, a WRID or an LID instruction is decoded. When using the Byte Write, the Page Write or the WRID, refer also to *Section 5.3: Cycling with Error Correction Code (ECC)*

Table 10. Operating conditions (voltage range W, temperature range 3)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage	-	2.5	5.5	V
T_A	Ambient operating temperature	-	–40	125	°C
f_C	Operating clock frequency	V_{CC} ≥ 2.5 V, capacitive load on Q pin ≤100pF	-	5	MHz

Table 11. Operating conditions (voltage range W, temperature range 3) for high-speed communications

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage	-	4.5	5.5	V
T_A	Ambient operating temperature	-	–40	105	°C
f_C	Operating clock frequency	V_{CC} ≥ 4.5 V, capacitive load on Q pin ≤ 100 pF	-	10	MHz

Table 12. DC characteristics (voltage range W, temperature range 3)

Symbol	Parameter	Test conditions (in addition to conditions specified in *Table 10*)	Min.	Max.	Unit
C_{OUT}(3)	Output capacitance (Q)	V_{OUT} = 0 V	-	8	pF
C_{IN}(3)	Input capacitance	V_{IN} = 0 V	-	6	
I_{LI}	Input leakage current	V_{IN} = V_{SS} or V_{CC}	-	2	µA
I_{LO}	Output leakage current	$\overline{S}$ = V_{CC}, V_{OUT} = V_{SS} or V_{CC}	-	3	
I_{CC}	Supply current (Read)	V_{CC} = 2.5 V, C = 0.1V_{CC}/0.9 V_{CC}, Q = open f_C = 5 MHz	-	3	mA
		V_{CC} = 5.5 V, 10 MHz(1) C = 0.1 V_{CC}/0.9 V_{CC}, Q = open	-	5	
I_{CC0}(2)	Supply current (Write)	2.5 V ≤ V_{CC} < 5.5 V during t_W, $\overline{S}$ = V_{CC}	-	2(3)	mA
I_{CC1}	Supply current (Standby mode)	t° = 85 °C, V_{CC} = 2.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}(3)	-	5	µA
		t° = 85 °C, V_{CC} = 5.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}(3)	-	5	
		t° = 105 °C, VCC = 2.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	15	
		t° = 105 °C, VCC = 5.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	15	
		t° = 125 °C, V_{CC} = 2.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	20	
		t° = 125 °C, VCC = 5.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	40	
V_{IL}	Input low voltage	2.5 V ≤ V_{CC} < 5.5 V	–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage	2.5 V ≤ V_{CC} < 5.5 V	0.7 V_{CC}	V_{CC}+ 1	V
V_{OL}	Output low voltage	V_{CC} ≥ 2.5 V, I_{OL} = 2 mA	-	0.4	V
V_{OH}	Output high voltage	V_{CC} ≥ 2.5 V, I_{OH} = -2 mA	0.8 V_{CC}	-	V
V_{RES}(3)	Internal reset threshold voltage	-	0.5	1.5	V

1. When –40 °C < t° < 105 °C.
2. Average value during the Write cycle (t_W)
3. Characterized only, not 100% tested

Table 13. AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Min.	Max.	Unit
			Test conditions specified in *Table 10*		Test conditions specified in *Table 11*		
f_C	f_{SCK}	Clock frequency	-	5	-	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	60	-	30	-	ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	60	-	30	-	
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	90	-	40	-	
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	60	-	30	-	
t_{CHSL}		$\overline{S}$ not active hold time	60	-	30	-	
t_{CH}(1)	t_{CLH}	Clock high time	90	-	40	-	
t_{CL}(1)	t_{CLL}	Clock low time	90	-	40	-	
t_{CLCH}(2)	t_{RC}	Clock rise time	-	2	-	2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time	-	2	-	2	
t_{DVCH}	t_{DSU}	Data in setup time	20	-	10	-	ns
t_{CHDX}	t_{DH}	Data in hold time	20	-	10	-	
t_{HHCH}	-	Clock low hold time after $\overline{HOLD}$ not active	60	-	30	-	
t_{HLCH}	-	Clock low hold time after $\overline{HOLD}$ active	60	-	30	-	
t_{CLHL}	-	Clock low set-up time before $\overline{HOLD}$ active	0	-	0	-	
t_{CLHH}	-	Clock low set-up time before $\overline{HOLD}$ not active	0	-	0	-	
t_{SHQZ}(2)	t_{DIS}	Output disable time	-	80	-	40	
t_{CLQV}(3)	t_V	Clock low to output valid	-	80	-	40	
t_{CLQX}	t_{HO}	Output hold time	0	-	0	-	
t_{QLQH}(2)	t_{RO}	Output rise time	-	80	-	20	
t_{QHQL}(2)	t_{FO}	Output fall time	-	80	-	20	
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid	-	80	-	40	
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z	-	80	-	40	
t_W	t_{WC}	Write time	-	5	-	5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.
3. t_{CLQV} must be compatible with t_{CL} (clock low time): if t_{SU} is the Read setup time of the SPI bus master, t_{CL} must be equal to (or greater than) $t_{CLQV}+t_{SU}$.