UPGRADED METALLURGICAL GRADE SILICON FOR SOLAR CELL FABRICATION

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ABSTRACT: This paper discusses the gettering process during emitter diffusion in upgraded metallurgical grade (UMG) silicon and the effect of a subsequent low temperature annealing (LTA) which is proven to be a suitable method to increase the cell lifetime and efficiency according to recent studies from other authors. Neighboring wafers of the same ingot were selected to be processed and characterized by means of μW-PCD lifetime measurements. An increase in minority carrier lifetime by a factor of 3.8 is obtained after the phosphorus gettering, although no improvement due to the LTA process in these wafers was observed.

Keywords: UMG, Silicon, Gettering, Diffusion, Annealing, Solar cells.

1 INTRODUCTION

During the last years the PV industry has experienced a very strong economic growth accompanied with a very high demand of high quality silicon feedstock. multicrystalline silicon is still the preferred material for PV production among all current technologies with a share of more than 60% of the shipped PV modules world-wide. This high demand is the drive to a predicted shortage of silicon feedstock in the future [1–3] and thus other sources of silicon must be investigated, including low quality silicon obtained by purification of upgraded metallurgical silicon as a low cost solution [4]. Regarding the use of this silicon and its use in solar applications, several groups have developed very promising metallurgical routes to increase production for UMG silicon [5, 6].

Metallic impurities, are mainly responsible of a decreasing in the minority carrier lifetime in multicrystalline silicon as they act as recombination centers. As it is widely described in the literature, gettering processes are able to minimize this effect [7, 8]. Gettering processes remove impurities in silicon from the active areas to regions where their recombining effect is lower. A typical example of these gettering processes is phosphorous diffusion. The phosphorous diffusion generates a high concentration of these elements above the solubility limit. Precipitates of Si-P are formed, and at interfaces between the Si-P layer and the silicon matrix, dislocations are generated, which can constitute the gettering sites [9]. Parallel the atomic radius difference between phosphorous and silicon atoms introduces dislocations that can constitute also gettering sites.

Therefore, a great improvement in the minority carrier lifetime can be obtained with a standard industrial diffusion emitter process.

There are two approximations of this process, one right after the phosphorus diffusion (low temperature tail) [10] and another once the wafer has returned to room temperature conditions (low temperature annealing).

Recent studies demonstrate the effect on the minority carrier lifetime of iron-rich multicrystalline silicon material of a low temperature annealing (LTA) process at about 300 to 700ºC [11-13], after the phosphorus diffusion. This process could be suitable also for UMG silicon grade, where a high concentration of iron is expected.

2 EXPERIMENTAL

P-type 156x156 mm UMG multicrystalline silicon wafers were cut into 100x100 mm squares, saw damage etched and chemically cleaned prior to perform spin-on doping and phosphorous diffusion. The diffusion of the phosphorous solution was carried out in a furnace at 900°C.

After the phosphorous diffusion the phosphorous silicate glass (PSG) formed on the surface was removed and the wafers were divided in five groups to be submitted to different processes in order to study the effects of the phosphorous gettering and the LTA. In fig. 1 the different processes A, B, C, D and E are explained. One of the batches (E) was not phosphorous diffused and set as reference wafers.

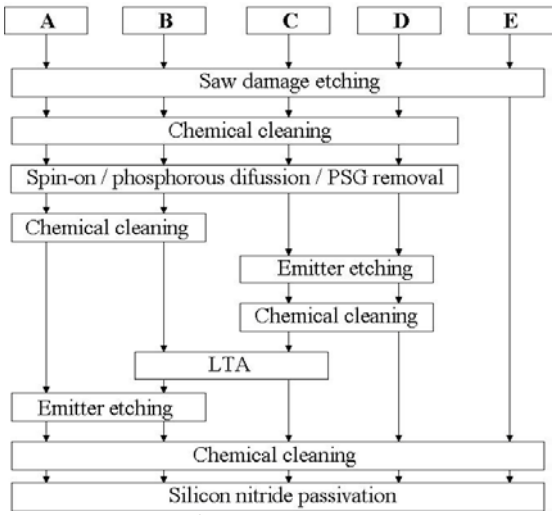

Figure 1: Scheme of the experimental process

The emitter was removed from the wafers in NaOH solution and the LTA was performed at 575ºC during 90 minutes. Chemical cleanings of the wafers were carried out during the process not to introduce further contamination that could modify the minority carrier lifetimes. After the surface passivation by PECVD with silicon nitride, the minority carrier lifetimes were measured and mapped with a Micro-Wave Photoconductance Decay (μW-PCD) from Semilab at

500 µm resolution with $150 \cdot 10^{10}$ photons per pulse laser power, 500 mSun bias ligth and 5 mV sensitivity.

3 RESULTS AND DISCUSSION

3.1 Previous lifetime characterization of the wafers.

Figure 2 shows the reference wafer lifetime map distribution after saw damage etching and passivation (process E). The median lifetime of the lifetime distribution is chosen as the representative lifetime of the samples. For the reference samples the median lifetime obtained was between 4 µs and 5 µs. The lifetime of these wafers is clearly higher than expected regarding to the silicon type (UMG) and according to the datasheet of the material provider. We can attribute this difference to the fact that the provider gives lifetime measures by brick, so according to the position of the wafer in the ingot different lifetime can be expected. We could suspect that these wafers come originally from the center of the ingot where we expect to find the lowest level of impurities, and consequently, better lifetimes.

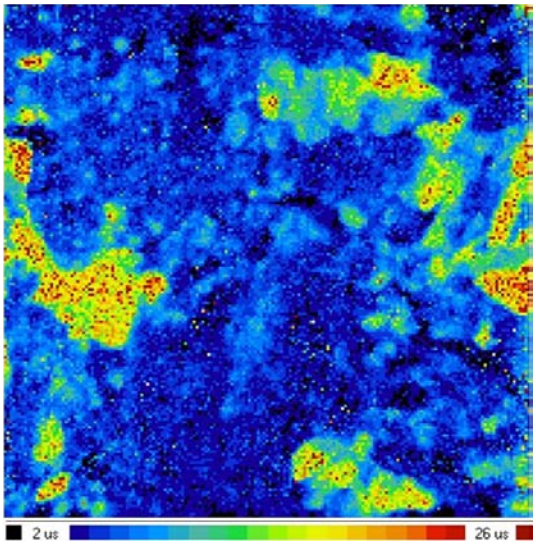

Figure 2: Lifetime map of reference sample

3.2 Influence of the phosphorous gettering on the lifetime.

In figure 3 is showed the lifetime map of a wafer submitted to saw damage etching process with subsequent emitter formation, phosphorous glass removal and silicon nitride passivation (process A). The median lifetime observed was 16.67 µs. Several mono-crystalline zones expose lifetime improvement. The distribution shows a shift to higher minority carrier lifetimes with any value below 3 µs. Some crystals, that before diffusion showed a higher lifetime in their central part while this decreased near of the grain boundaries, appear now with a higher homogeneity within almost their whole area. According to the existing literature we can explain this improvement by the effect of the segregation of the impurities present in the crystals to the rich phosphorous layer due to the phosphorous diffusion [8].

In general, the lifetime near to the grain boundary is increased as well respect to the non diffused sample, showing that no degradation has occurred during the gettering process due to precipitation of impurities at grain boundaries, which would be expected at higher temperature processes, enhancing the recombination activity in grain boundaries [14].

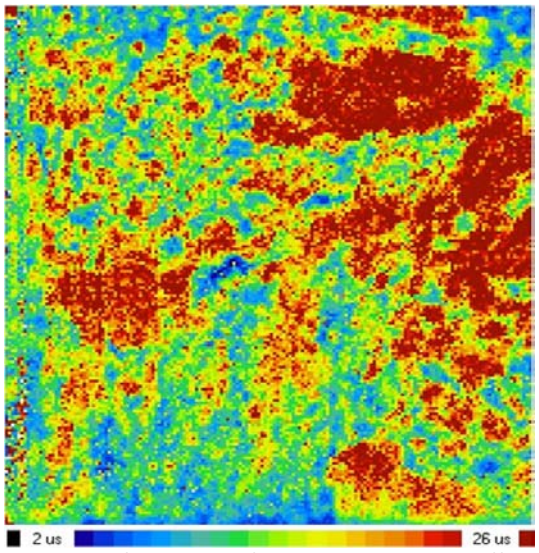

Figure 3: Lifetime map of a sample phosphorus diffused

3.3 Influence of the LTA on the lifetime

To evaluate the influence of the phosphorous gettering followed by LTA process, we have submitted the samples to the thermal process before and after etching the emitter (process B and C). In this way, the effect of internal and external gettering could be differentiated in case a further gettering occurs.

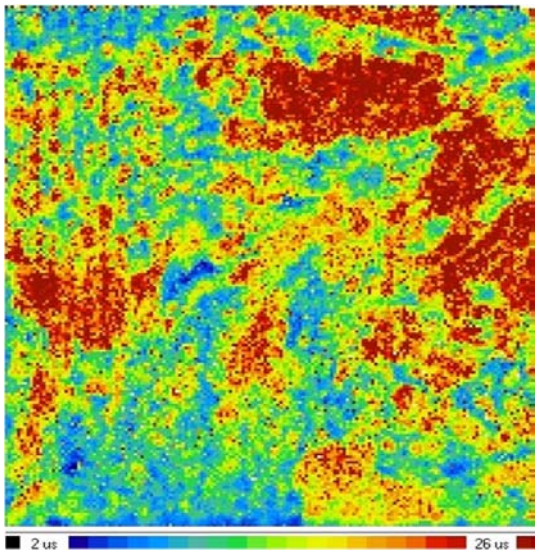

Figure 4: Lifetime map of a sample submitted to LTA before emitter etching

In figure 4 lifetime measurements reveal a minor reduction in minority carrier lifetime in low thermal annealed (16.25µs) with respect to non annealed sample (16.67µs), that shows that LTA does not introduce any effect in this wafer. Most of crystals do not show any modification in their lifetime map. However, some of them have slightly deteriorated lifetimes after the LTA that could be attributed to a contamination during the process or to slight differences in impurity concentration at the crystal in question of this wafer respect to the

neighbors.

In figure 5 it can be observed the result of the neighboring wafer, which was submitted to the LTA process after emitter etching.

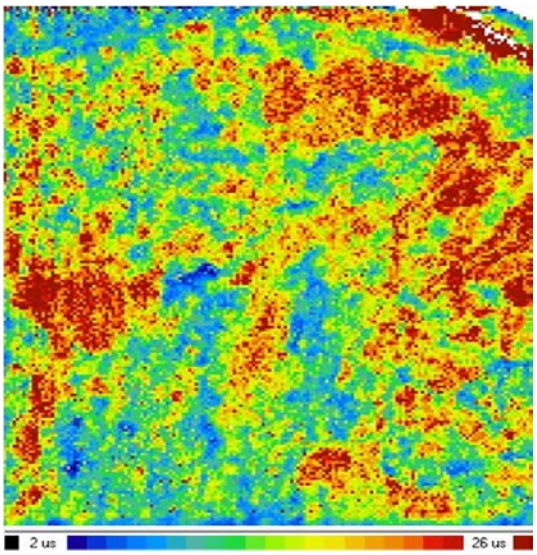

Figure 5: Lifetime map of a sample submitted to LTA after emitter etching

In this case there is a slight increase in minority carrier lifetime from 14.07 µs (wafer with process D) to 15.78µs (process C), that we do not consider as significant, due to the lifetime range. This treatment has been successfully verified in wafers with high level of impurities by Rinio et al. [11, 15] where a clear improvement is observed with the LTA process. According to the assumption that the wafers are from the less contaminated part of the ingot, we can expect a lower effect on them.

4 CONCLUSION

General improvement of minority carrier lifetime has been achieved by external phosphorus gettering process during emitter diffusion in UMG silicon wafers. An increase by a factor 3.8 is obtained. The phosphorous gettering of impurities will decrease the recombination activity and will be the responsible for this improved lifetime observed.

The low thermal annealing did not introduce any further improvement in the lifetimes in the UMG wafers used for the experiments, as they are supposed to come from a low contaminated part of the ingot.

5 ACKNOWLEDGEMENTS

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