ESCUELA SUPERIOR DE INGENIERÍA Y TECNOLOGÍA

SECCIÓN DE INGENIERÍA INDUSTRIAL

TRABAJO DE FIN DE GRADO

SISTEMA DE RIEGO INTELIGENTE DE BAJO COSTE

GRADO EN INGENIERÍA ELECTRÓNICA INDUSTRIAL Y AUTOMÁTICA

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Septiembre, 2019

AGRADECIMIENTOS:

Me gustaría agradecer a todas aquellas personas que me han apoyado y ayudado durante estos intensos cuatro años de universidad, sin las cuáles no hubiera sido capaz de llegar a dónde estoy ahora. Agradecer de manera especial a mi madre, mi padre y mi hermano el apoyo diario y la paciencia que han tenido conmigo durante estos últimos años. A Andrea, por apoyarme y ayudarme siempre de una manera especial.

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RESUMEN

El proyecto desarrollado se centra en la implementación un sistema de comunicaciones alámbrico cuya aplicación principal es servir de sistema de riego inteligente para obtener datos de sensores y actuar sobre electro válvulas. Este proyecto se basará en el proyecto “Sistema de riego inteligente de bajo coste”, realizado por Doña Yaiza Tejera Fumero y presentado en julio de 2018.

Para implementar este sistema de comunicación se desarrollará una placa de circuitos impresos, que se utilizará como módem. El circuito electrónico del módem se basará en el circuito diseñado en el proyecto anterior, modificando y añadiendo algunos componentes que le darán al diseño nuevas capacidades. Entre estas modificaciones destaca la inclusión de una electroválvula que será controlada mediante la placa Arduino UNO utilizada como esclavo y un puente en H para conseguir dos sentidos de giro de manera sencilla.

Por último, se realizará una conclusión en la que se mostrarán los puntos débiles de la implementación del sistema y se destacarán los aspectos positivos que tendría el proyecto y el ahorro que se podría producir si se continúa desarrollando la idea del proyecto.

ABSTRACT

The project developed is to implement a wire communication system to carry out an automatic irrigation system. This project will be based on the previous project "*Sistema de riego inteligente de bajo coste*", done by Miss Yaiza Tejera Fumero and shown in July, 2018.

To carry out this communication system it will be developed a print circuit board (PCB) used as a modem. The modem electronic circuit will be based on the design made in the previous project, changing and adding some components that will give the design new capabilities. Among these changes it can find the addition of an electrovalve that will be controlled with Arduino UNO board, used as slave. Another addition is the H Bridge as controller for the electrovalve. With these component it is easy to control de electrovalve with two directions of rotation.

Finally, the weaknesses of the implementation of the system will be shown and the positive aspects that the project would have and the savings that could be produced if the project idea continues to be developed will be highlighted.

CAPÍTULO 1 . INTRODUCCIÓN GENERAL

ANTECEDENTES

Este proyecto se desarrollará a partir del proyecto realizado por Doña Yaiza Tejera Fumero "Sistema de Riego inteligente de Bajo coste". En este proyecto su autora se centró en desarrollar un sistema de riego inteligente a través de sensores y actuadores de bajo coste, añadiendo algunas funcionalidades a un sistema de riego convencional.

En un sistema de riego convencional se dispone de un circuito de tuberías donde cada cierto número de metros habrá una electroválvula que abastecerá el agua necesaria para el terreno. Normalmente, estas electroválvulas están controladas por una pareja de cables desde el controlador hasta la misma. Este par de cables debe recorrer la distancia que separe cada electroválvula del controlador, que en ocasiones será muy grande. Además, se utilizará un único par de cables por cada electroválvula, lo que supone un gasto muy grande de material.

La innovación que supone este proyecto, en comparación con un sistema de riego convencional, se centra en el ahorro, tanto económico como material. En lugar de utilizar un único par de cables para cada electroválvula se utilizara un único par de cables, al que se conectarán las electroválvulas que se deseen. En cada una de estas electroválvulas se instalará un microcontrolador que se encargará de gestionar la electroválvula. Para realizarlo de esta manera, es necesario implementar un sistema de comunicación.

El proyecto anterior se centró en el sistema de comunicación de bajo nivel, lo que se denomina capa física de transporte. Se encargó de analizar distintas formas de comunicación entre diferentes puntos de riego y la cabecera, tanto de manera alámbrica como inalámbrica.

Se implementó un código simple de un único maestro – esclavo para poner a prueba el funcionamiento del sistema, pero sin contemplar el código que se encarga del funcionamiento de la electroválvula correspondiente al esclavo. Este código se implementará en proyecto actual.

Este trabajo, en conjunto con el proyecto realizado por Doña Yaiza Tejera Fumero, tiene por objetivo final alcanzar un sistema de comunicación entre múltiples esclavos, sensores y actuadores.

ESTADO DE LA TÉCNICA

Los sistemas de riego inteligentes surgen como solución al reto de aumentar la eficiencia hídrica y energética. Estos sistemas consisten en la utilización de las Tecnologías de la Información y la Comunicación (TICs) para realizar una gestión óptima del riego. Con esto se consigue utilizar de forma más eficiente los recursos productivos de las fincas, como lo son el agua, la energía y los fertilizantes. Un sistema de riego inteligente toma decisiones basadas en la monitorización y adquisición de datos, procesamiento de datos y representación de la información.

Netafim, empresa pionera en el sector de los sistemas de riego inteligente por goteo, fue fundada en 1965 en Kibbutz Hatzerim, Israel. Esta compañía se convirtió en el principal proveedor mundial de soluciones de riego inteligente. La situación de escasez de agua en esa zona de Israel les llevó a trabajar y desarrollar nuevas formas de hacer eficiente el uso de los recursos, como el agua. A partir de una necesidad se ha generado una gran compañía que opera hoy en más de 30 países, con 17 fábricas y con ventas a más de 100 países.

En la actualidad existen varias compañías que se dedican a desarrollar y comercializar esta tecnología que cada vez está más avanzada. Existen sistemas que no solo son capaces de regar cuando el cultivo lo necesite, sino que también ofrecen la posibilidad de mostrar en una aplicación en un Smartphone todos los datos referentes a como se encuentra el terreno, además de imagen por video en directo.

El futuro de la agricultura de regadío a nivel mundial depende, en buena parte, de la implantación de sistemas de riego inteligente, que sean capaces de conseguir un uso más eficiente del agua y otros recursos relacionados con el cuidado de los cultivos. Con los sistemas de riego inteligente se incrementa considerablemente la rentabilidad de las explotaciones y se minimiza el impacto ambiental, ya que solo se gastará agua cuando sea estrictamente necesario, en lugar del riego tradicional, en el que no se tenía en cuenta las condiciones que rodean los cultivos. [1]

OBJETIVO

El objetivo principal del presente proyecto es implementar un sistema de comunicaciones alámbrico multidireccional, cuyo fin principal es servir de sistema de riego inteligente. Este sistema de riego recogerá datos de sensores y actuará en electro válvulas.

Para ello, se utilizará el diseño electrónico diseñado en el proyecto anterior pero se añadirán algunas funcionalidades y componentes. Además, se hará uso de la programación de Arduino implementando un sistema Maestro – Esclavo, recogiendo valores de distintos sensores y actuando sobre electro válvulas.

ESTRUCTURA GENERAL DEL PROYECTO

En este apartado se detallará el contenido del proyecto, así como los capítulos en los que se divide el mismo. Se añade una breve descripción del contenido de cada capítulo del proyecto.

CAPÍTULO 1. Introducción general. Se describe el punto del que se parte en este proyecto. Además, se realiza una breve descripción del estado de la técnica y se describe el objetivo del proyecto. Se detalla la estructura general del proyecto.

CAPÍTULO 2. Herramientas de diseño y desarrollo. Se describen las herramientas desarrollo empleadas, tanto hardware como software.

CAPÍTULO 3. Descripción del sistema implementado. Se explican los bloques que componen el sistema, el funcionamiento de los mismos y el código a implementar.

CAPÍTULO 4. Modificaciones realizadas en el esquema. Se detallan las modificaciones realizadas por el alumno sobre el diseño del sistema inicial.

CAPÍTULO 5. Implementación en PCB. Se describen los pasos seguidos para el diseño e impresión de la placa de circuitos impresos utilizada.

CAPÍTULO 6. Pruebas y resultados. Se explica el proceso seguido para verificar el funcionamiento del sistema, incluyendo los problemas que han surgido y como se han solucionado.

CAPÍTULO 7. Conclusiones. Se describen los resultados del proyecto, los aspectos positivos y negativos de la implementación de este sistema.

CAPÍTULO 2 : HERRAMIENTAS DE DISEÑO Y DESARROLLO.

En este apartado se explicará las herramientas empleadas en el diseño de este proyecto, tantos herramientas *hardware* como de *software*.

HERRAMIENTAS DE DESARROLLO *SOFTWARE*

KiCAD

Para el desarrollo del circuito electrónico, tanto para los esquemas electrónicos como para la impresión de la PCB se utilizó el *software* KiCAD (Fig. 1).

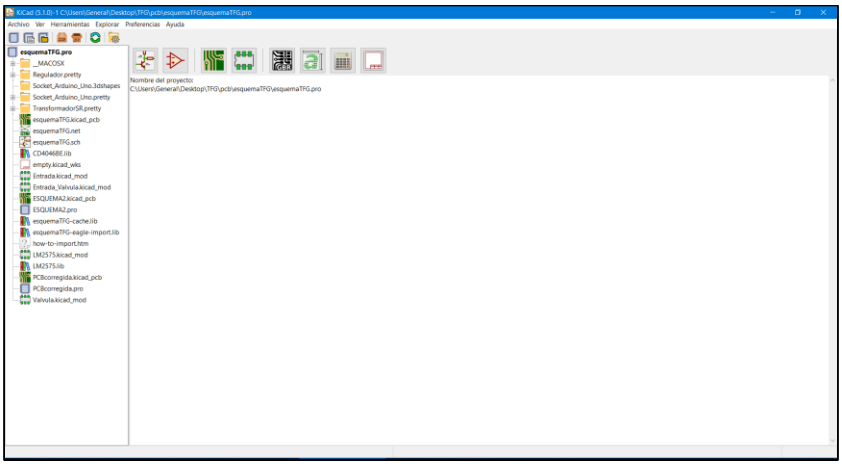


Fig. 1: Entorno de desarrollo de KiCAD.

Se trata de un *software* libre para la automatización del diseño electrónico (*Electronic Design Automation*, ("*EDA*"). Este programa facilita el diseño de esquemáticos de circuitos electrónicos y su conversión a placa de circuito impreso. Permite realizar todas las etapas de diseño, desde el diseño del esquema del circuito, el diseño de PCB, la creación o modificación de símbolos y huellas que se adapten a las necesidades del usuario y generación de archivos de impresión, como GERBER para las fresadores CNC.

Para el desarrollo de las etapas previamente comentadas, este *software* cuenta con cuatro módulos principales:

KiCAD: administrador principal de proyectos. Coordina los demás módulos.

Eeschema: permite el diseño del esquema de las conexiones electrónicas del proyecto

Pcbnew: permite el diseño del circuito impreso, cargando los componentes y las conexiones desde el esquemático. Desde aquí se definen las pistas que unirán estos componentes.

Gerberview: se utiliza para generar el archivo GERBER para la impresión y permite su visualización.

[2]

LTspice IV

Para la simulación de algunos componentes del circuito se utilizó el *software* LTspice IV (Fig. 2). Es un *software* de descarga gratuita muy potente para el diseño electrónico.

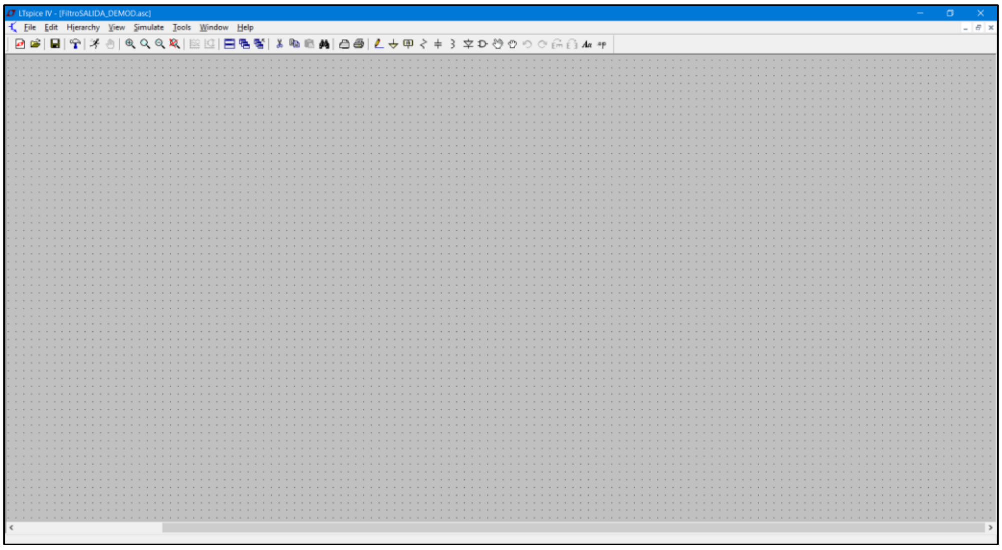


Fig. 2: entorno de desarrollo de LTspice IV.

Este programa es un simulador SPICE III de alto rendimiento en el que se pueden simular multitud de componentes y circuitos electrónicos, como los ejemplos que vienen en el paquete del programa. Con él se pueden diseñar nuevos circuitos, simulándose y obteniendo gráficas. En las simulaciones simula un osciloscopio, pudiendo observar los valores de voltaje, intensidad, etc...en cualquier punto del circuito diseñado.

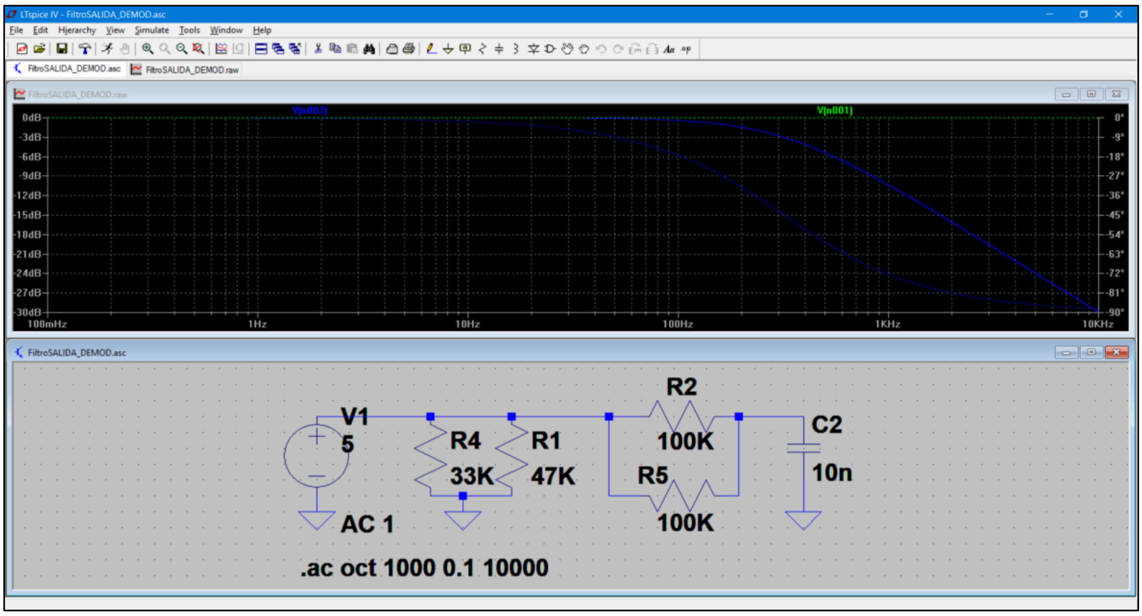


Fig. 3: simulación del filtro de salida del demodulador en LTspice IV.

Se ha utilizado para simular el filtro de salida del demodulador (Fig. 3), dado que aparecieron problemas y hubo que rediseñarlo.

IDE v1.8.9 de Arduino

El entorno de desarrollo integrado "Arduino IDE v1.8.9" (Fig. 4), siglas en inglés de Integrated Development Environment, es un *software* compuesto por un conjunto de herramientas de programación en el que se pueden utilizar varios lenguajes de programación. Este entorno está dotado de un editor de código, un compilador, un depurador y un constructor de interfaz gráfica (GUI). [3]

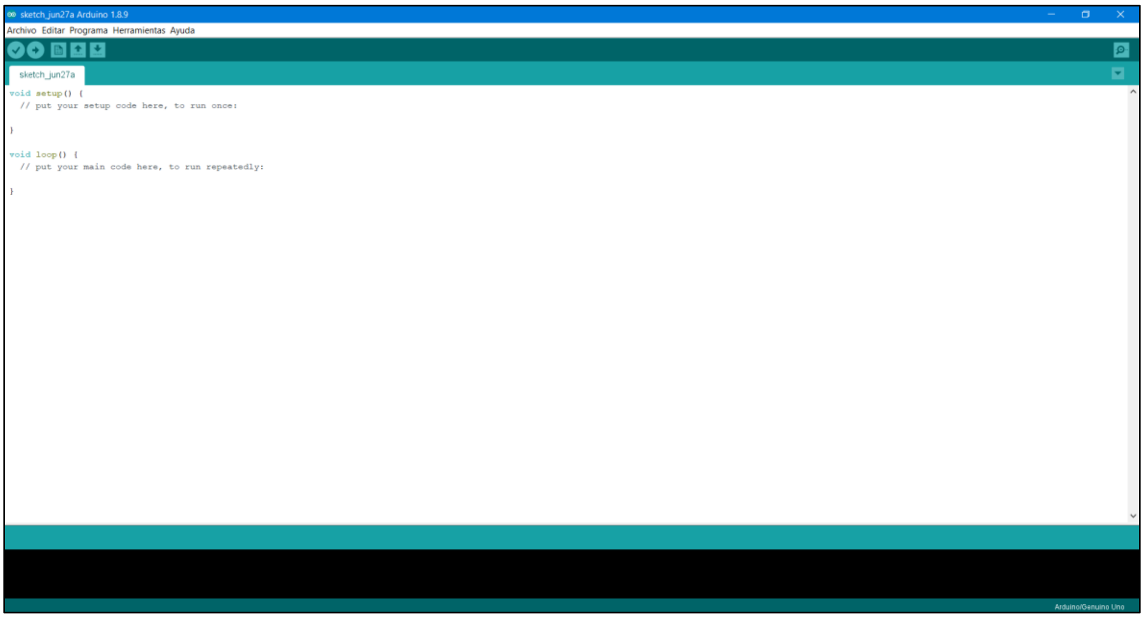


Fig. 4: IDE v1.8.9 de Arduino

Este programa se utilizará la programación del microcontrolador ATmega328P, integrado en la placa Arduino UNO, que se explicará posteriormente. Información sobre Arduino IDE:

HERRAMIENTAS DE DESARROLLO *HARDWARE*

PROTOBOARD

Una *protoboard* es una herramienta que permite implementar circuitos electrónicos fácilmente, sin necesidad de soldarlos o dejarlos fijos. Son placas, normalmente de plástico, con orificios que se encuentran conectados entre sí, de una determinada manera. Está compuesta de plástico, que hace de aislante, y de un material conductor, que hará de unión entre los componentes.

En este proyecto se ha utilizado la protoboard para probar el diseño previo del circuito electrónico además de las modificaciones, como por ejemplo el regulador de tensión. También se utilizó de receptor de la señal a través del par de cables, utilizando el circuito de la PCB como emisor.

OSCILOSCOPIO

El osciloscopio es un instrumento electrónico de medida en el que se visualizan representaciones gráficas de señales. En nuestro caso se utilizó el modelo HAMEG HMO2524 para comprobar el funcionamiento del circuito, tanto del bloque modulador como del demodulador.

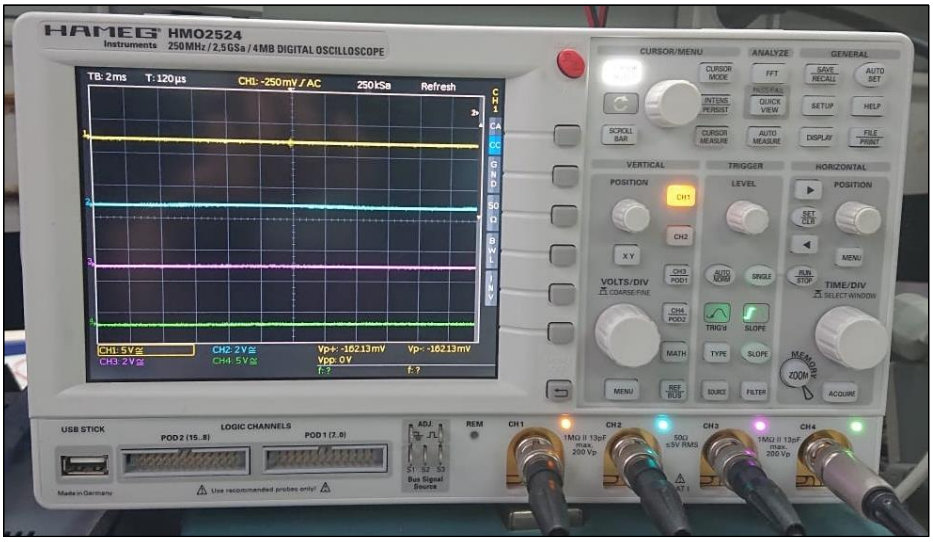


Fig. 5: osciloscopio Hameg HMO2524.

Dispone de cuatro canales para realizar mediciones, cada uno se puede configurar a una escala determinada. También dispone de un amplio menú para tomar valores de medida, como se aprecia en la parte inferior derecha de la pantalla, en la Fig. 5. Estos cuatro canales se utilizaron simultáneamente para comparar las señales de entrada y salida de los circuitos de modulación y demodulación.

FUENTE DE ALIMENTACIÓN

En este proyecto de utilizó una fuente de alimentación para suministrar los 12 voltios a la PCB. Se utilizó el modelo FAC-363B que dispone de tres fuentes de alimentación independiente, aunque solo se usó una de ellas. Esta fuente dispone de un limitador de corriente ajustable entre 0 y 2 Amperios, lo que fue de gran utilidad para proteger el circuito ante una sobre intensidad. [4]

MULTÍMETRO

Un multímetro es un instrumento electrónico de medida, con el que se puede medir voltaje, intensidad, resistencia y dependiendo del modelo utilizado, también se pueden medir algunos parámetros más como continuidad o capacidad.

Fig. 6: multímetro de las marca MASTECH©.

El modelo utilizado es el MS8268 de la marca MASTECH© y se utilizó para comprobar la continuidad de las pistas cuando se soldaron los componentes en la PCB. También se utilizó para comprobar que la alimentación de 5 voltios llegaba correctamente a toda la placa. Aunque existe la posibilidad de medir la capacidad de los condensadores, como se ve en la Fig. 6Fig. 6: multímetro de las marca MASTECH©., no se utilizó para esto puesto que se comprobó que realiza unas medidas bastante inexactas, sobre todo con los condensadores de capacidad muy pequeña (nanofaradios, microfaradios, etc...).

GENERADOR DE FUNCIONES

El generador de funciones utilizado es el modelo HM8030-3 de la marca HAMEG. Este dispositivo genera ondas cuadrada, triangular o senoidal. Además dispone de una salida en la que genera una señal TTL. De esta señal se puede seleccionar la frecuencia mediante el selector ubicado debajo del indicador digital, en el que indica el valor de la frecuencia, como se ve en la Fig. 7.

Fig. 7: generador de funciones HAMEG HM 8030-3

Para simular la señal de comunicación que emite el Arduino, se utilizó la salida TTL de este dispositivo a una frecuencia de 220 Hz. Se generan unos pulsos de 5 voltios de amplitud, simulando así la señal digital que genera la placa Arduino Uno.

PLACA ARDUINO UNO

Arduino Uno es una placa que contiene el microcontrolador ATmega328P. Tiene catorce pines digitales entrada/salida, de los cuáles seis se pueden usar como salidas de *PWM*. Además tiene seis salidas analógicas, un cristal de cuarzo de 16 MHz, un conector USB, un conector de alimentación, un conector ICSP y un botón de reset, como se puede ver en Fig. 8. Solo es necesario conectar la placa a un ordenador mediante el cable USB para comenzar a utilizarla. [5]

Fig. 8: placa Arduino UNO.

Este dispositivo se programa en lenguaje Arduino, que está basado en el lenguaje de programación C++, aunque también acepta C.

CAPÍTULO 3 : DESCRIPCIÓN DEL SISTEMA IMPLEMENTADO.

Se decidió partir del diseño anterior, realizado por doña Yaiza Tejera Fumero en el proyecto “Sistema de riego inteligente de bajo coste”. Se utilizó como base el diseño de comunicación alámbrica entre placas, con un maestro y uno o varios esclavos. Sobre este diseño se realizarán modificaciones y se añadirán algunos componentes, que serán detallados en el Capítulo 4.

A continuación se realizará una descripción de la estructura de comunicación, parte que se aprovechó del proyecto anterior, y del funcionamiento de los bloques que componen el circuito a implementar en este proyecto, con las nuevas modificaciones realizadas.

ESTRUCTURA DE COMUNICACIÓN ENTRE MAESTRO Y ESCLAVO

Para este proyecto, interesa que la comunicación sea de tipo *half-duplex*. Esto quiere decir que sea bidireccional pero el envío y recepción de datos no sea simultánea.

Esta comunicación se realizará a través de los cables de alimentación a los que estarán conectados cada uno de las electroválvulas y los esclavos. A continuación se explica el proceso de comunicación entre un maestro y un esclavo, mostrando dos diagramas de flujo para facilitar la comprensión del maestro (Fig. 9) y del esclavo.

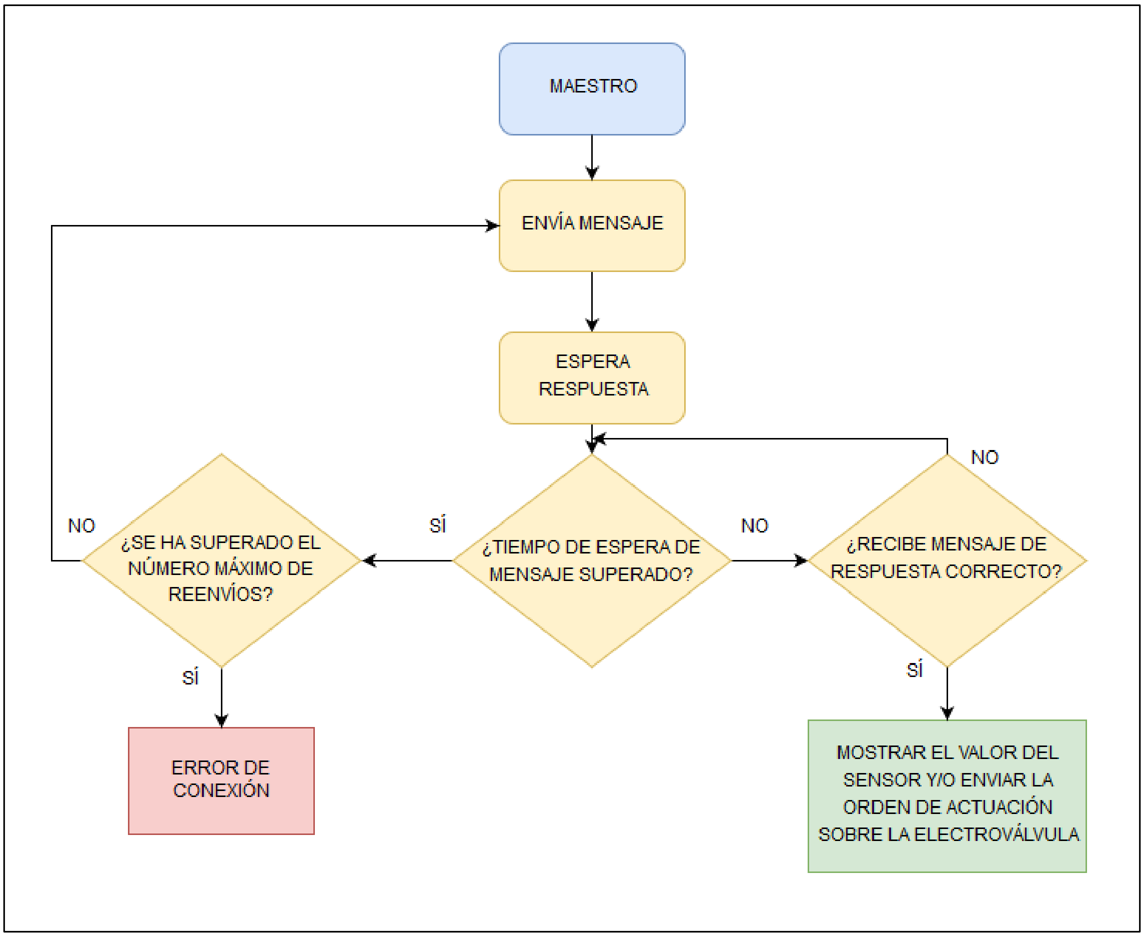


Fig. 9: diagrama de flujo del maestro.

En primer lugar, el maestro es el encargado de pedir información al esclavo. Para ello envía una “T”, suponiendo que se quiera pedir el valor de temperatura. Una vez enviado el mensaje, espera la respuesta y se pueden dar dos casos: que el tiempo de espera de respuesta sea mayor que el establecido o que sea menor. Si el tiempo de espera es mayor, se comprueba que no se ha superado el número máximos de reenvíos. Si se ha superado el sistema da un mensaje de error. Por el contrario, si no se ha superado el número máximo de reenvíos se envía de nuevo el mensaje, se espera la respuesta y se vuelve a comprobar si el tiempo de espera es mayor que el establecido.

Se puede apreciar en la Fig. 10 el fragmento del código en el que se realiza lo mencionado en este párrafo. Mediante el segundo “*while*” se comprueba si el tiempo de envío del mensaje es menor que el tiempo máximo establecido. Este bucle se encuentra dentro de otro “*while*” en el que se comprueba el número de reenvíos.

```
Serial.println("Iniciando comunicacion");

while ((Mensaje_Correcto == 0) && (reenvio_actual < Numero_reenvios)) {

digitalWrite(CD4046, LOW);
delay(320);

Serial.print("He enviado: ");
vw_send((uint8_t *)msg1, strlen(msg1));
vw_wait_tx();
Serial.println(msg1);
digitalWrite(CD4046, HIGH);

reenvio_actual = reenvio_actual +1;
Serial.print("Reenvio numero: ");
Serial.println(reenvio_actual);
long Tiempo_Maximo = 1000;
long Tiempo_Envio = millis();

while ((Mensaje_Correcto == 0) && (millis() - Tiempo_Envio < Tiempo_Maximo)) {

  if (vw_get_message((uint8_t *)buf, &buflen)) {
    Serial.print("He recibido ");
    Serial.print(buflen);
    Serial.print(" ");
    for( int i = 0; i < buflen; i++)
      Serial.print(buf[i], HEX);
      Serial.println();
    if (buflen == 2) {
        Mensaje_Correcto = 1;
    }
  }
  delay(50);
}
}
```

Fig. 10: fragmento de código del maestro. Envío.

Por otro lado, si no se ha superado el tiempo espera establecido se comprueba si se ha recibido. Se repite esta acción hasta que el mensaje sea recibido. Por último se comprueba que el mensaje recibido es correcto y en caso afirmativo, se realizan las acciones correspondientes con la electroválvula o se muestra el valor del sensor o de los sensores correspondientes. En este caso solo está implementado para el valor de temperatura. Si se desea implementar algún otro sensor simplemente se añadiría siguiendo la misma lógica.

```
if (Mensaje_Correcto == 1) {
  Serial.println("Mensaje correcto");
  int ValorSensor;
      ValorSensor = buf[0] << 8 | buf[1];
      Serial.print("Valor sensor recibido: ");
      Serial.println(ValorSensor);
  float Temperatura;
      Temperatura = (ValorSensor * 5.0)/(1024.0 * 0.01);
      Serial.print("Valor temperatura: ");
      Serial.println(Temperatura);

   if (Temperatura >= 28.0) {
      digitalWrite(CD4046, LOW);
      delay(320);
      Serial.println("Se debe regar");
      Serial.println("He enviado");
      vw_send((uint8_t *)regar, strlen(regar));
      vw_wait_tx();
      Serial.println(regar);
      digitalWrite(CD4046, HIGH);
    }
    if (Temperatura < 28.0) {
      digitalWrite(CD4046, LOW);
      delay(320);
      Serial.println("NO se debe regar");
      Serial.println("He enviado");
      vw_send((uint8_t *)no_regar, strlen(no_regar));
      vw_wait_tx();
      Serial.println(no_regar);
      digitalWrite(CD4046, HIGH);
    }

  }else
    Serial.println("Error de Conexion");
 delay(3000);
```

Fig. 11: fragmento de código del maestro. Comprobación y órdenes.

A continuación se explica el funcionamiento del esclavo:

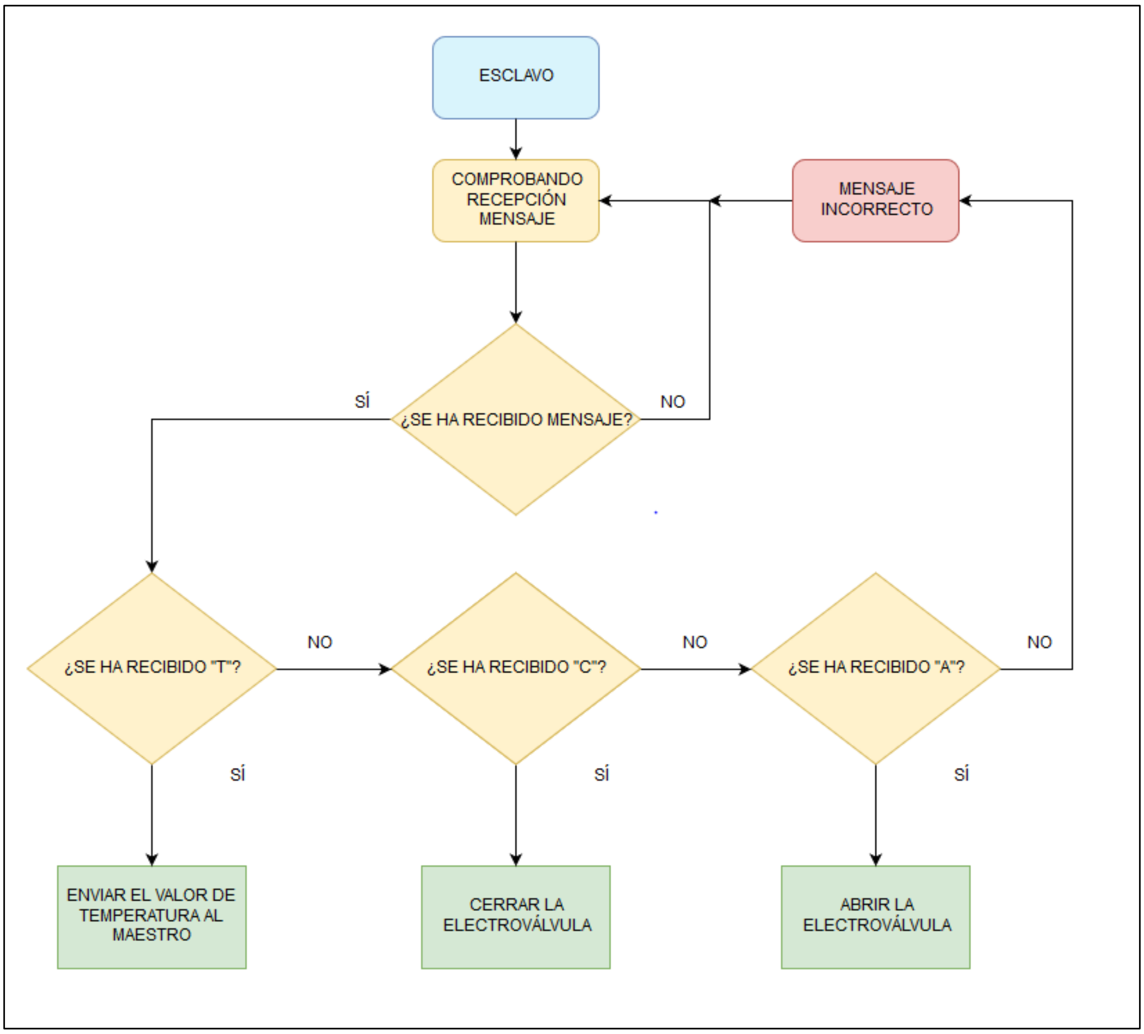


Fig. 12: diagrama de flujo del esclavo.

El esclavo comienza su comunicación comprobando si recibe el mensaje. Se hace uso de un primer "*if*" que comprueba si hay mensaje para recibir y de un segundo "*if*" que muestra el mensaje recibido, como se puede ver en la Fig. 13.

```
void loop() {

  uint8_t buf[VW_MAX_MESSAGE_LEN];
  uint8_t buflen = VW_MAX_MESSAGE_LEN;
  uint8_t Mensaje_Correcto = 0;
  int i;

    if (millis() - Tiempo_mensaje >= 200){
        Serial.println("Comprobando existencia mensaje");
        Tiempo_mensaje = millis();
    }

       if (vw_get_message(buf, &buflen)){
           Serial.println("Recibiendo mensaje");
           Serial.print("He recibido: ");
           for(i = 0; i < buflen; i++)
               Serial.print((char)buf[i]);
              Serial.println();
```

Fig. 13: fragmento de código del esclavo. Recepción del mensaje.

Si se ha recibido, se comprueba si el maestro ha solicitado información del valor del sensor de temperatura (“T”), si ha enviado la orden de “Se debe regar” (“A”) o si ha enviado la orden de “No se debe regar” (“C”). Si no es ninguna de estas tres opciones, se considera que el mensaje no es correcto y el sistema muestra que el mensaje recibido es incorrecto y se vuelve a comprobar si se recibe mensaje. Cuando la orden es “Se debe regar”, se abre la electroválvula, se deja abierta durante un tiempo determinado y luego se cierra, como se ve en el código mostrado en la Fig. 14. Aunque este código funciona correctamente, se podría optimizar para abrir la electroválvula durante un tiempo proporcional a la cantidad de agua que se estime que necesite la planta en un momento dado, pero no se ha realizado porque se considera fuera de los objetivos de este proyecto.

```
if((char)buf[0] == 'A') {
 Serial.println("Se debe regar");
 digitalWrite(ENABLEelectrovalvula, true);
 digitalWrite(Giro1, HIGH); // Se abre la electroválvula.
 digitalWrite(Giro2, LOW);
 delay(20);
 digitalWrite(ENABLEelectrovalvula, true);
 digitalWrite(Giro2, HIGH); // Se cierra la electroválvula.
 digitalWrite(Giro1, LOW);
 delay(20);
 digitalWrite(Giro1, LOW);
 digitalWrite(Giro2, LOW);
 digitalWrite(ENABLEelectrovalvula, false);
 delay(2000);
}
```

Fig. 14: fragmento del código del esclavo. Funcionamiento de la electroválvula.

Esta estructura de comunicación es implementable para varios esclavos, puesto que solo es necesario añadirle un identificador a cada uno para conocer los valores de los parámetros de cada zona donde esté colocada la electroválvula con su esclavo correspondiente.

(*Sistema de riego de bajo coste, Yaiza Tejera Fumero, julio 2018*).

MODULACIÓN DE LA SEÑAL

Para un sistema de riego inteligente, las distancias entre el controlador y las electroválvulas se suponen bastantes grandes, en grandes terrenos hasta de cientos de metros. Además de esto, el diseño del sistema contempla que los datos viajan por el mismo cable que la alimentación, por lo que estas son las dos razones por las que es necesario realizar la modulación de la señal. Con esto se evitan interferencias, se protege la información del mensaje de las degradaciones por ruido y se aumenta la calidad de la información transmitida, consiguiendo así una mayor probabilidad de que el mensaje llegue correcto a su destino.

Para este proyecto se ha decidido utilizar la técnica de modulación FSK (*Frequency Shift Keying*). Se ha elegido una modulación digital frente a las analógicas debido a que las modulaciones digitales tienen una menor sensibilidad al ruido que las analógicas. Dentro de las digitales, se ha optado por la modulación FSK dado que al conectar elementos pasivos al circuito se producen variaciones de voltaje. Con una modulación ASK, estas variaciones podrían causar errores en los mensajes transmitidos. Las variaciones de frecuencia también se pueden producir, pero son mucho más estables, por lo que la probabilidad de cometer un error en la comunicación es mucho menor.

FUNCIONAMIENTO DE LOS BLOQUES DEL CIRCUITO

Para el correcto funcionamiento de la comunicación, es necesario poder transmitir las señales de una placa a otra. Para ello, se debe modular y demodular estas señales, ya que se va a utilizar un único cable y se prevé que la distancia entre las placas sea grande. Además se han implementado componentes con el fin de controlar las electroválvulas y proteger el circuito.

Para ello se han implementado los siguientes bloques: bobina de aislamiento, regulador de tensión, puente en H, transformador, modulador y demodulador. A continuación se explicará el funcionamiento de los bloques del esquema electrónico.

BOBINA DE AISLAMIENTO Y CONDENSADOR DE DERIVACIÓN

Esta bobina se encuentra en el esquema del circuito (Fig. 15, en el cuadro rojo) justo después del conector y antes del regulador de tensión. Dado que este componente necesita que la corriente continua le llegue con el menos ruido posible, se coloca esta bobina que hace la función de filtro paso bajo, es decir, aísla los datos de alta frecuencia, separando la corriente alterna de la corriente continua de potencia hacia el lado que se encuentra el regulador. Debido a problemas con la señal de salida de la fuente fue necesario añadir el condensador (“C7” en Fig. 15). Este se encarga de derivar la señal de alterna, es decir, el ruido que pueda tener la señal de la fuente de alimentación, para conseguir una señal de continua aún más limpia.

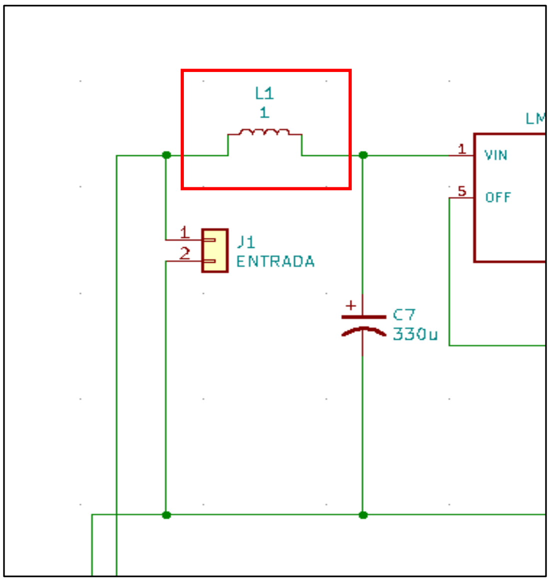


Fig. 15: bobina de aislamiento y condensador de derivación entre la entrada y el regulador.

TRANSFORMADOR

El transformador se utiliza para acoplar la señal modulada de alta frecuencia de corriente alterna a la señal de corriente continua que circula por el par de cables proporcionada por el regulador de tensión. Con esto se consigue que por el par de cables viajen los datos y la alimentación simultáneamente.

REGULADOR DE TENSIÓN

El objetivo de este bloque (Fig. 16), es obtener la alimentación del circuito a 5 voltios. La entrada podrá ser de entre 7 a 40 voltios que el regulador siempre sacar 5 voltios de continua. Para un funcionamiento correcto, este componente necesita una señal de corriente continua estable, que viene filtrada y aislada gracias a la bobina y el condensador de la etapa anterior.

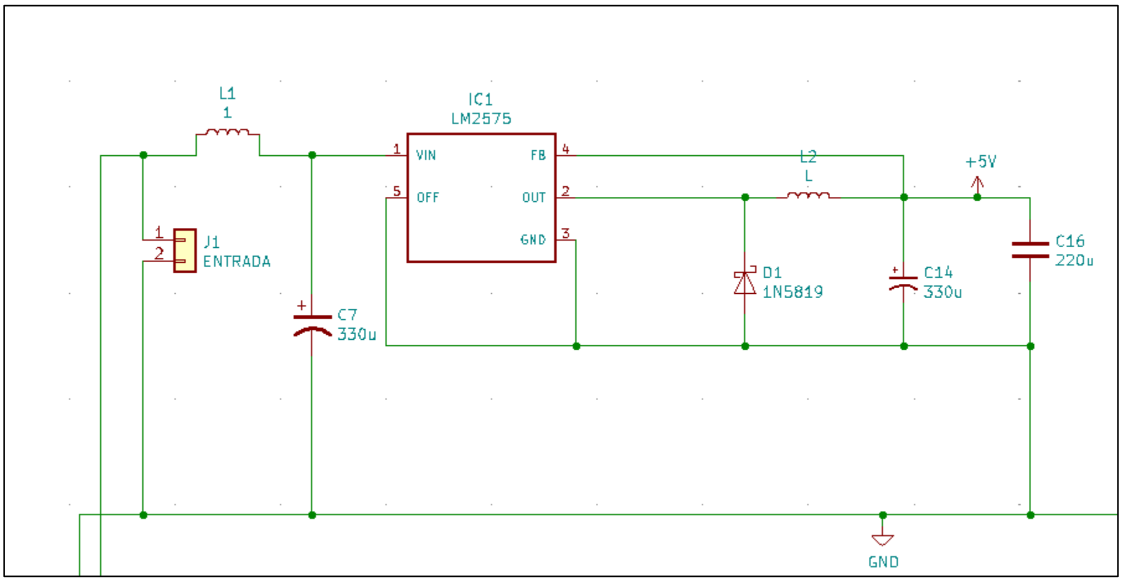


Fig. 16: esquema del regulador LM2575 - 5.0 P+.

A la salida del regulador se encuentra un diodo "*1N5819*"de tipo *schottky*, en conjunto con una bobina y un par de condensadores, uno cerámico y otro electrolítico, con el fin de obtener un mejor filtrado. El "*LM2575T*" toma una realimentación de la salida donde se obtienen los 5 voltios regulados.

Estos 5 voltios se utilizarán para alimentar todos los componentes de la PCB, además de la placa Arduino correspondiente, por lo que es de vital importancia para el buen funcionamiento del sistema que se obtengan esos 5 voltios con calidad.

PUENTE EN H

Para el control de la electroválvula (Fig. 17) se utilizó un circuito integrado "L293D". Este componente incluye cuatro circuitos para manejar cargas de potencia media, como pequeños motores y cargas inductivas, como es nuestro caso. Tiene una capacidad de controlar corriente hasta 600 mA por circuito y una tensión entre 4,5 y 36 voltios. Estos cuatro circuitos se pueden utilizar de manera independiente. [6]

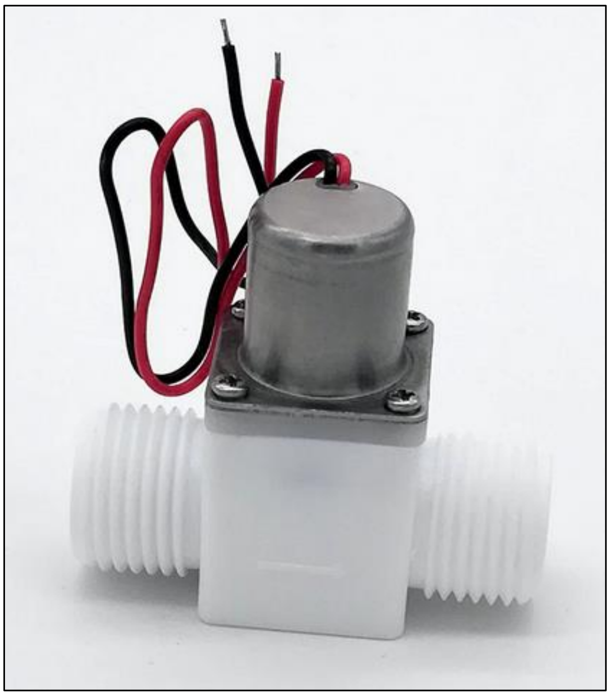


Fig. 17: electroválvula G1/2 pulgadas de solenoide.

En el caso de controlar la electroválvula se utilizará solo la mitad del puente en H, en concreto los pines 3 y 6, que se ven en el esquema de la Fig. 18. En este esquema aparece un motor en lugar de la electroválvula, pero el principio de funcionamiento sería el mismo, utilizando los dos sentidos de giro.

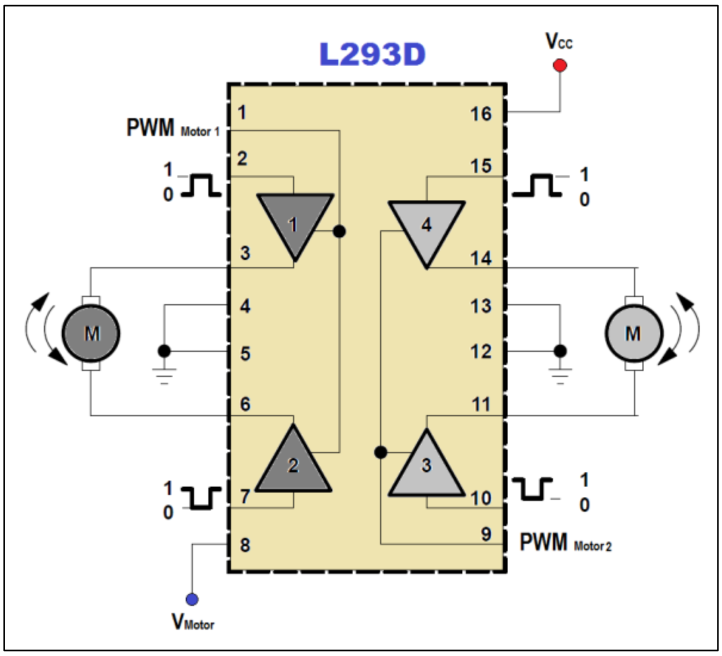


Fig. 18: esquema del L293 con motores.

Este circuito está formado por cuatro transistores, dos PNP y dos NPN. Con esto se consigue que en función de si la señal está a '1' lógico o a '0' lógico se puedan obtener dos sentidos de giro, en nuestro caso para la electroválvula estos dos sentidos serán abrir y cerrar. Cuando el Arduino envíe un pulso positivo, se abrirá la electroválvula mientras que cuando envíe un pulso negativo, se cerrará. Para que esto funcione debe estar activada la señal PWM (pin 11 del Arduino), que se activa mediante el "ENABLE". Mientras esta señal esté desactivada la electroválvula se mantendrá en la última posición ordenada. Esto ha sido explicado más atrás y se ha mostrado el código en la Fig. 14. [7]

MODULADOR

Este bloque está formado por un circuito integrado "CD4046BE" en configuración de modulador y un "TS924IN", como se observa en Fig. 19. La señal entra directamente de la placa Arduino, del pin 10 y sale directamente hacia uno de los cuatro operacionales que tiene el "TS924IN", que opera en configuración de seguidor de tensión para que se mantenga con su nivel de voltaje mientras pasa a la red por el transformador.

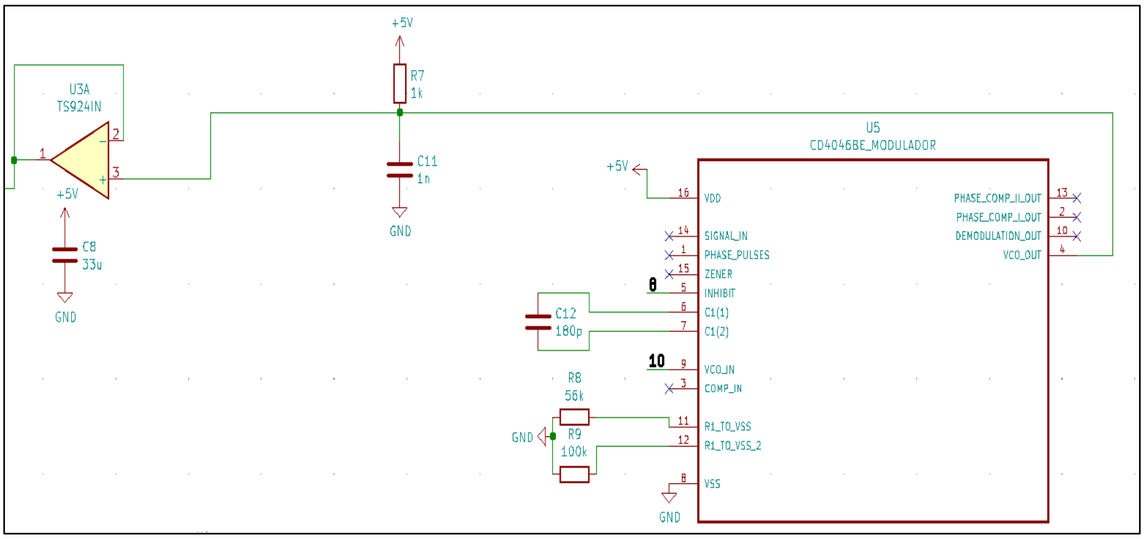


Fig. 19: esquema del bloque modulador.

El componente "CD4046BE" es un *PLL* (*Phase-locked loop*). Para el modulador se utilizará únicamente como VCO (Fig. 20). Un VCO (*Voltage-Controlled oscillator* u Oscilador controlado por tensión) es un dispositivo electrónico que se usa para amplificación, realimentación y circuitos resonantes que da a su salida una señal eléctrica de frecuencia proporcional a la tensión de entrada. A continuación se describe su funcionamiento.

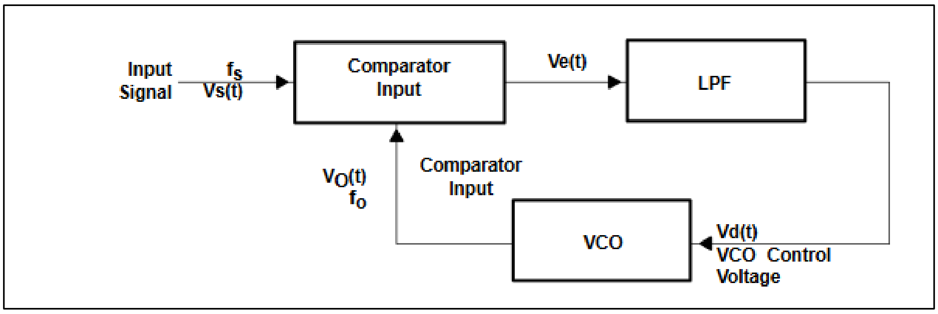


Fig. 20: Phase locked loop.

Mientras no se conecte ninguna señal de entrada, el error del voltaje de salida del comparador de fase es cero al igual que el voltaje de salida del filtro paso bajo (*LPF*). La frecuencia del VCO será f_0 en este momento. En torno a esta frecuencia oscilará la señal.

Cuando se conecte una señal de entrada, el comparador de fase compara la fase y la frecuencia de la señal de entrada con el VCO y genera un voltaje de error proporcional a la diferencia de fase y frecuencia entre la señal de entrada y el VCO. Este voltaje de error generado se filtra para eliminar el ruido y se introduce en el VCO. Se suman las dos señales afectando a la diferencia de frecuencia entre la señal de entrada y el VCO. Cuando la frecuencia de la señal de entrada sea lo suficientemente cercana a la frecuencia del VCO, este circuito forzará al VCO a seguir en frecuencia a la señal de entrada. [8]

Se utilizó ese componente para conseguir una modulación y demodulación FSK (*Frequency Shift Keying*). Su función es aumentar la frecuencia de la señal portadora en función de la señal moduladora. Esto quiere decir que cuando la señal cambie de nivel lógico (1 ó 0), la frecuencia cambiará. Con esto se consigue una señal de alta frecuencia que será más fácil de transmitir sin pérdida de información a una distancia mayor. En este caso, se ha utilizado solamente como VCO a una frecuencia de 100 kHz.

DEMODULADOR

El bloque demodulador (Fig. 21) está formado por dos "*LM311N*", ambos en configuración de comparador, y un "*CD4046BE*" en configuración de demodulador. A la salida del demodulador encontramos un filtro cuya función es obtener una señal reducida pero más estable de la señal demodulada.

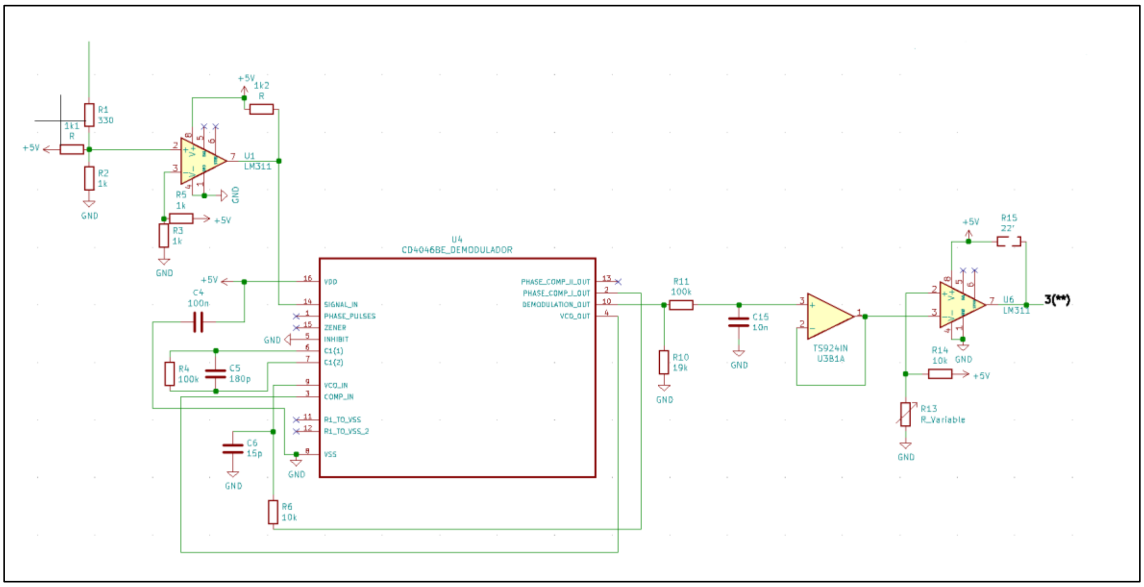


Fig. 21: esquema electrónico del bloque "Demodulador"

En este caso, el “CD4046BE”, explicado en más atrás, utiliza el comparador de fase que contiene el circuito integrado que compara la fase de la señal modulada con la fase de la señal periódica de entrada. El demodulador extrae la señal moduladora a partir de los pulsos que le llegan.

Previo al demodulador, encontramos un comparador que asegura que llegue una señal estable para su demodulación. Compara el nivel de la señal obteniendo una señal limpia y sin ruido idealmente.

A la salida del demodulador encontramos un filtro pasa baja con una resistencia a tierra (Fig. 22: filtro pasa bajas previo al comparador.Fig. 22), que se encarga de modificar la amplitud de la señal. Este filtro elimina el ruido de alta frecuencia y consiguiendo una señal más pequeña y estable que la que nos encontramos en la salida del demodulador. Este filtro permite que la señal pase en su nivel de continua. En cambio, si se utilizase un filtro pasa banda, la señal perdería su nivel de continua y retrasaría el voltaje, por lo que la señal se puede perder.

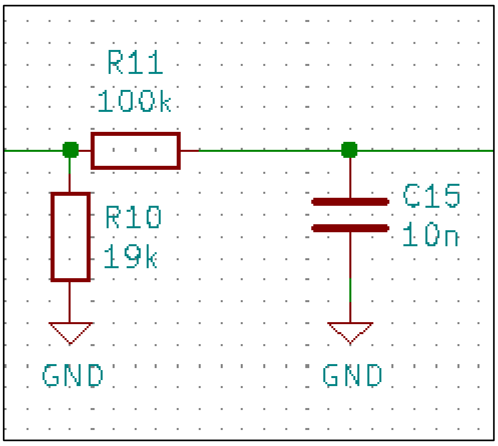


Fig. 22: filtro pasa bajas previo al comparador.

A la salida del filtro se obtiene una señal fácilmente comparable con un nivel de continua que se ajusta mediante un potenciómetro. Esta señal se compara con un nivel de voltaje que permita sacar una señal estable y sin ruido pero ahora a 5 voltios.

CAPÍTULO 4 : MODIFICACIONES REALIZADAS EN EL ESQUEMA.

A partir del esquema del proyecto realizado por Doña Yaiza Tejera Fumero, se realizaron algunas modificaciones para corregir algunos errores y se incluyeron algunos componentes nuevos con el fin de añadir funcionalidades al sistema.

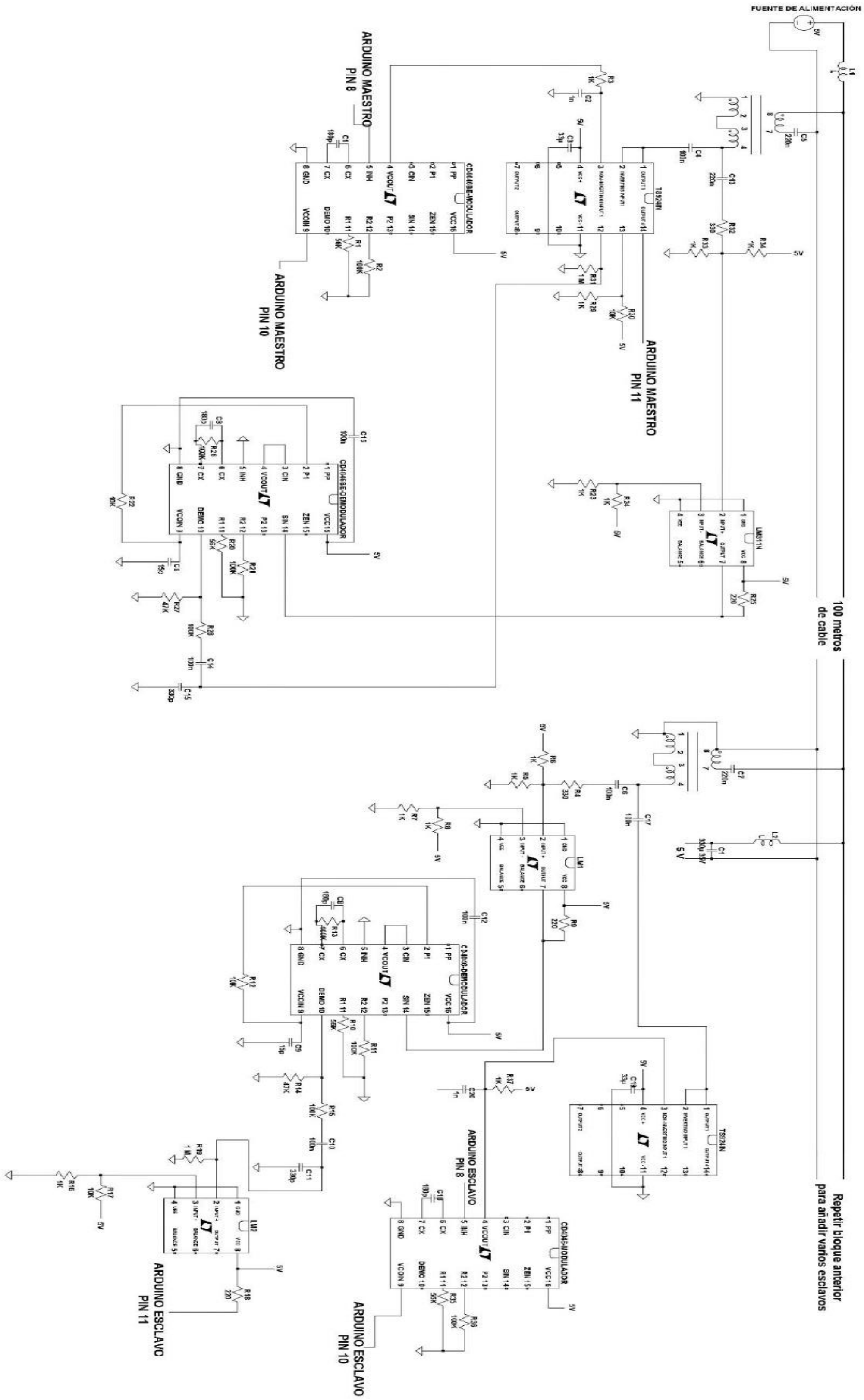


Fig. 23: Esquema electrónico inicial

A continuación, se procede a detallar todas las modificaciones realizadas y los componentes que se han añadido:

BLOQUE REGULADOR

En el esquema previo aparece una fuente de alimentación al comienzo del circuito. Esta se sustituye por un conector de dos entradas con el fin de que se pueda conectar a cualquier fuente siempre que su voltaje esté entre 7 y 40 voltios. Se incluye un regulador "*LM2576T*" que se encarga de obtener una tensión de 5 voltios para la alimentación de todo el circuito. La placa Arduino utilizada también se alimentará con ese voltaje, lo que significa que puede operar sin necesidad de estar conectada a un ordenador o una fuente independiente. El esquemático de este bloque se ve en la Fig. 24.

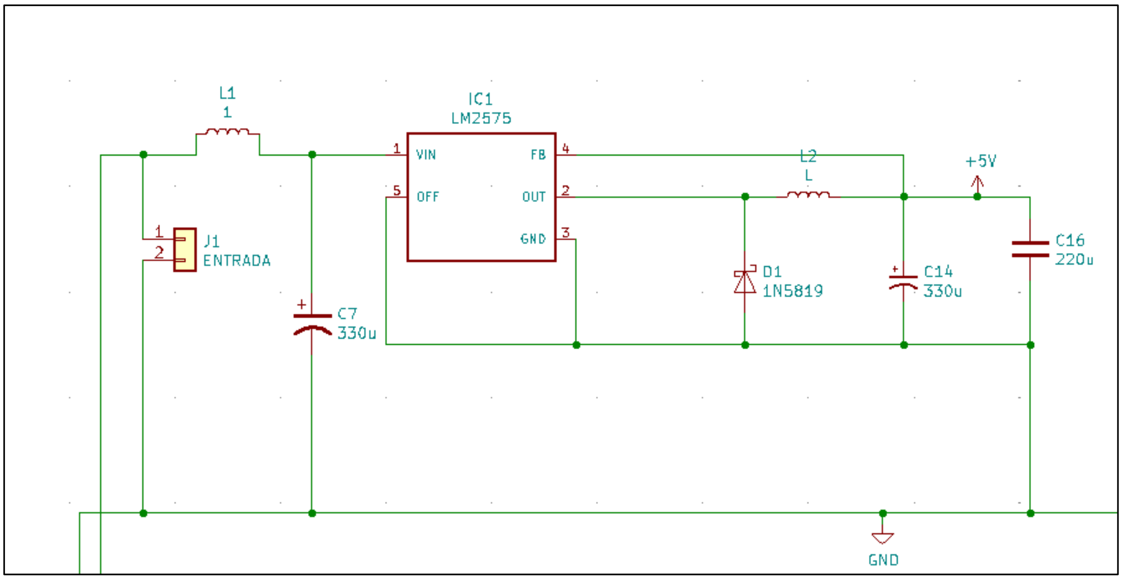


Fig. 24: Conector de entrada y regulador de tensión.

PUENTE EN H

Se incluye en el esquema un puente en H para controlar la electroválvula en cada esclavo. Se ha elegido un "*L293D*", con la conexión que se puede ver en la Fig. 25. Este integrado incluye cuatro circuitos para manejar cargas de potencia media, como pequeños motores y cargas inductivas. Tiene una capacidad de controlar corriente hasta 600 mA por circuito y una tensión entre 4,5 y 36 voltios. Estos cuatro circuitos se pueden utilizar de manera independiente. En el caso de controlar la electroválvula se utilizará solo la mitad de un puente en H.

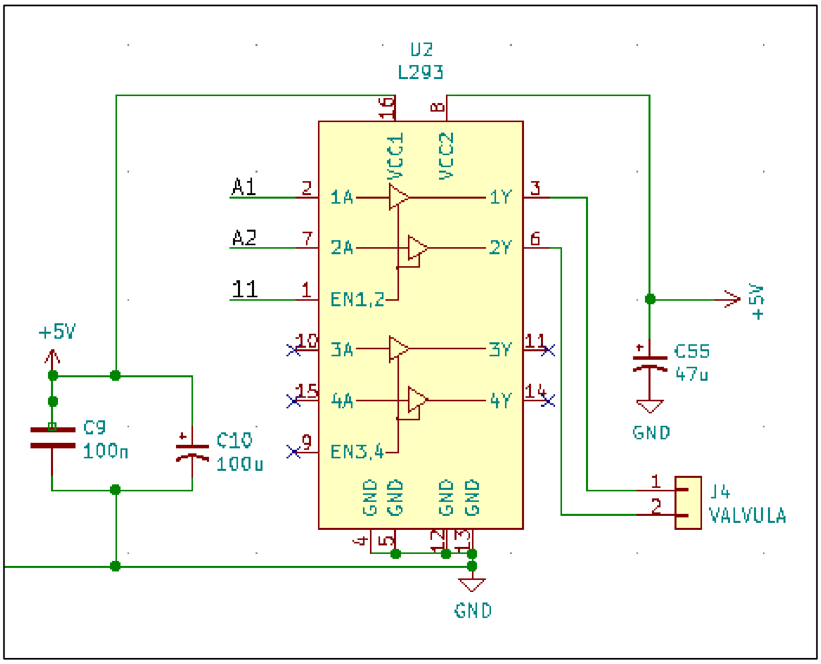


Fig. 25: Puente en H "L293D".

FILTRO EN LA ETAPA DE SALIDA

En el esquema previo, del trabajo de fin de grado anterior, se había diseñado un filtro pasa banda (Fig. 26) que se encargase de reducir y filtrar la señal de salida del demodulador. La salida de este filtro es la entrada del comparador de salida del circuito, el que se obtiene la señal cuadrada, de 0 – 5 voltios, demodulada. La frecuencia de corte inferior de este filtro es de 33.86 Hz mientras que la superior es de 4.82 kHz, por lo que debería funcionar en nuestro sistema, aunque cuando se implementó, no se consiguió obtener una señal correcta por lo que se optó por modificar este filtro.

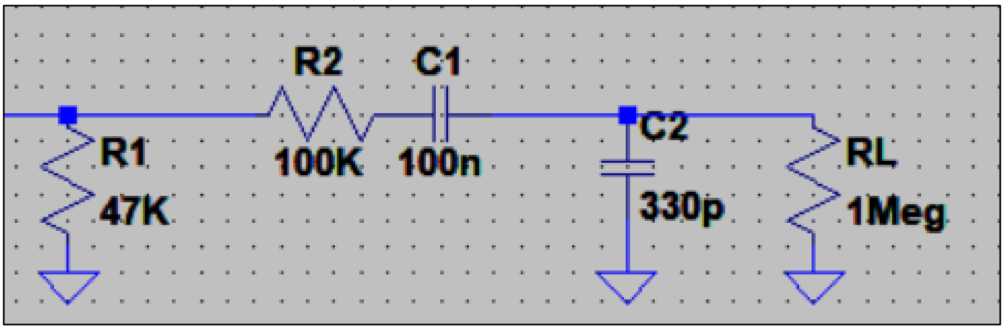


Fig. 26: filtro pasa banda.

En primer lugar, se decidió realizar una simulación del filtro para comprobar si había sido bien diseñado. Para realizar la simulación de utilizó el *software LTspice IV*. Se observó que en la banda de paso se produce una pérdida de casi 2 dB en la señal, como se ve en Fig. 27, por lo que la señal podría perderse debido a esto. Además, este filtro elimina la componente de continua sobre la que se transmite la señal. Por tanto, se decide modificar este filtro.

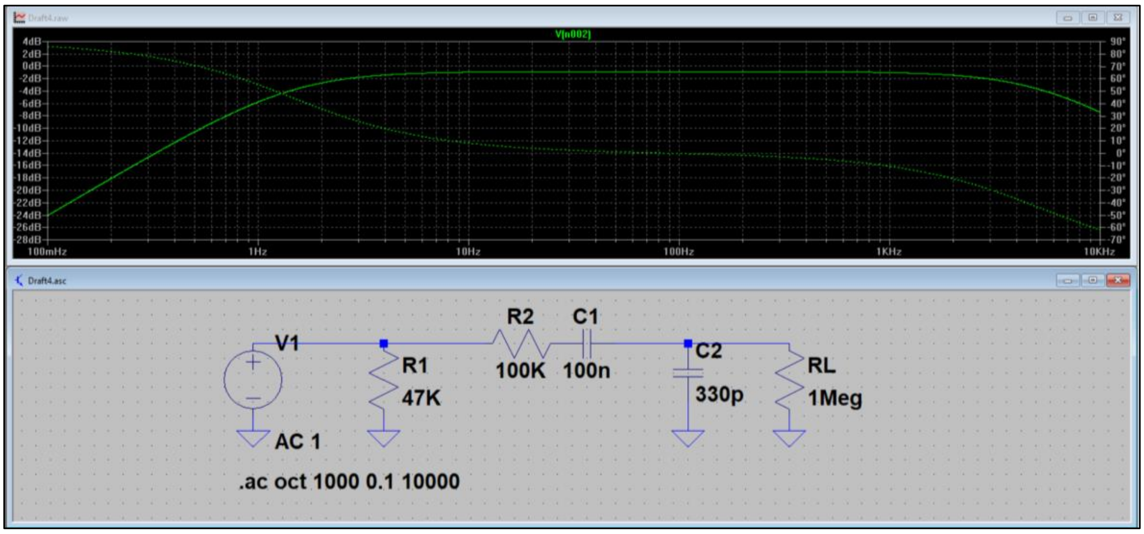


Fig. 27: simulación del filtro pasa banda en LTspice IV.

Una vez se comprobó que este filtro no era el correcto, se decidió implementar un filtro pasa bajas (Fig. 28) que filtraría los ruidos de alta frecuencia sin eliminar la componente de continua sobre la que se transmite la señal. Aprovechando parte del filtro anterior, se añadió una resistencia en paralelo a la resistencia de 47K con el fin de aumentar la amplitud de salida y una de 100K en paralelo con la de 100K para modificar el ancho de banda. Además, se cambió el condensador de 330p por uno de 10n y se quitó el de 100n. También se eliminó la resistencia de 1 MΩ ya que no es necesaria. Se optó por colocar las resistencias en paralelo ya que los componentes estaban soldados en la PCB y así no dañar las pistas.

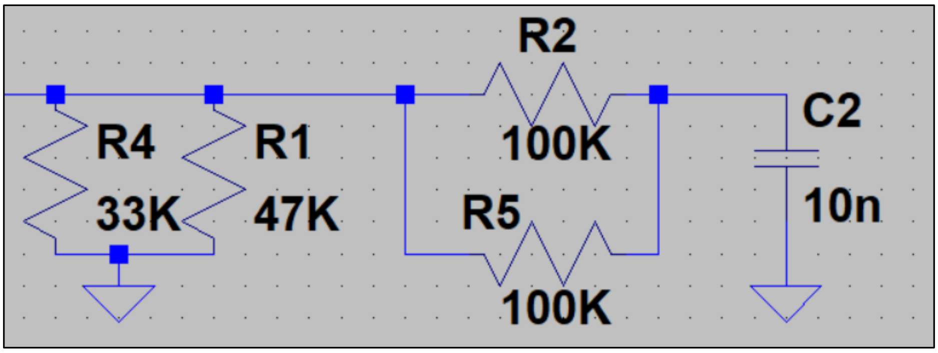


Fig. 28: filtro pasa bajas.

Posteriormente se realizó la simulación del nuevo filtro pasa bajas en la que se puede observar como no se produce pérdida de dB. Este filtro tiene una frecuencia de corte de unos 338 Hz y nuestra señal es de unos 220 Hz, por lo que debería filtrar correctamente la señal.

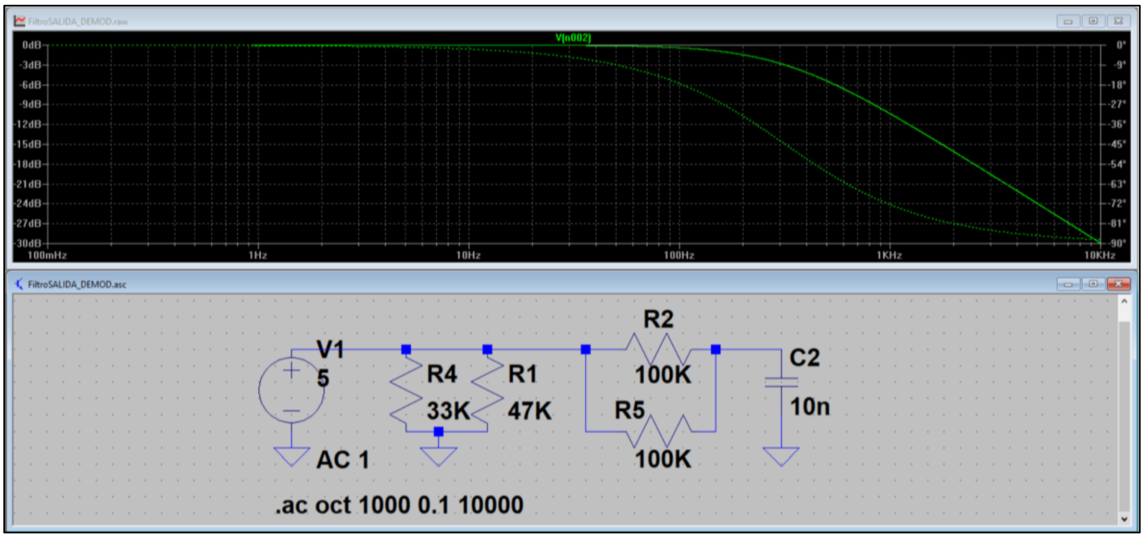


Fig. 29: simulación del filtro pasa bajas en LTspice IV.

Finalmente, se colocaron los nuevos componentes en la PCB y se comprobó su funcionamiento en la PCB. A la salida del filtro obtuvo una señal prácticamente cuadrada de unos milivoltios, sobre su nivel de continua, con mucho menos ruido que la señal de salida del demodulador. En la Fig. 30 se aprecia en amarillo la señal que emite Arduino (antes de modular), en azul la señal de salida del filtro pasa bajas (demodulada), en rosa el nivel de comparación y en verde la señal de salida del circuito, demodulada y comparada, preparada para ser recibida por el Arduino.

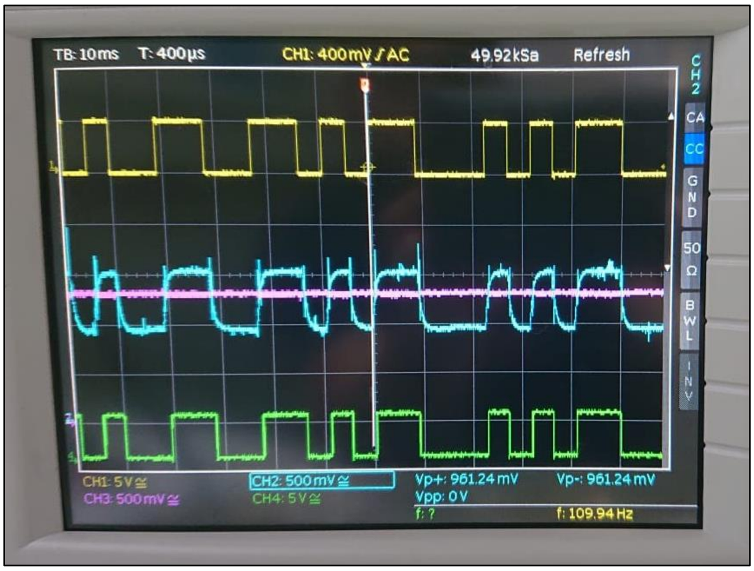


Fig. 30: señales en el comparador de salida.

CAPÍTULO 5 : IMPLEMENTACIÓN EN PCB.

Para realizar la PCB se utilizó el *software* KiCAD. Con este programa se desarrolló todo el proceso necesario para la realización de este proyecto.

En primer lugar, se realizó el esquema, con "*Eeschema*" (Fig. 31), del circuito con todos los componentes para la impresión de la PCB, puesto que el circuito fue probado en la protoboard previamente. Se añadieron los componentes al esquema y se crearon los que no existían en la librería del KiCAD. Además, se añadió el conexionado de la placa Arduino UNO para incluirla en la placa de circuitos impresos.

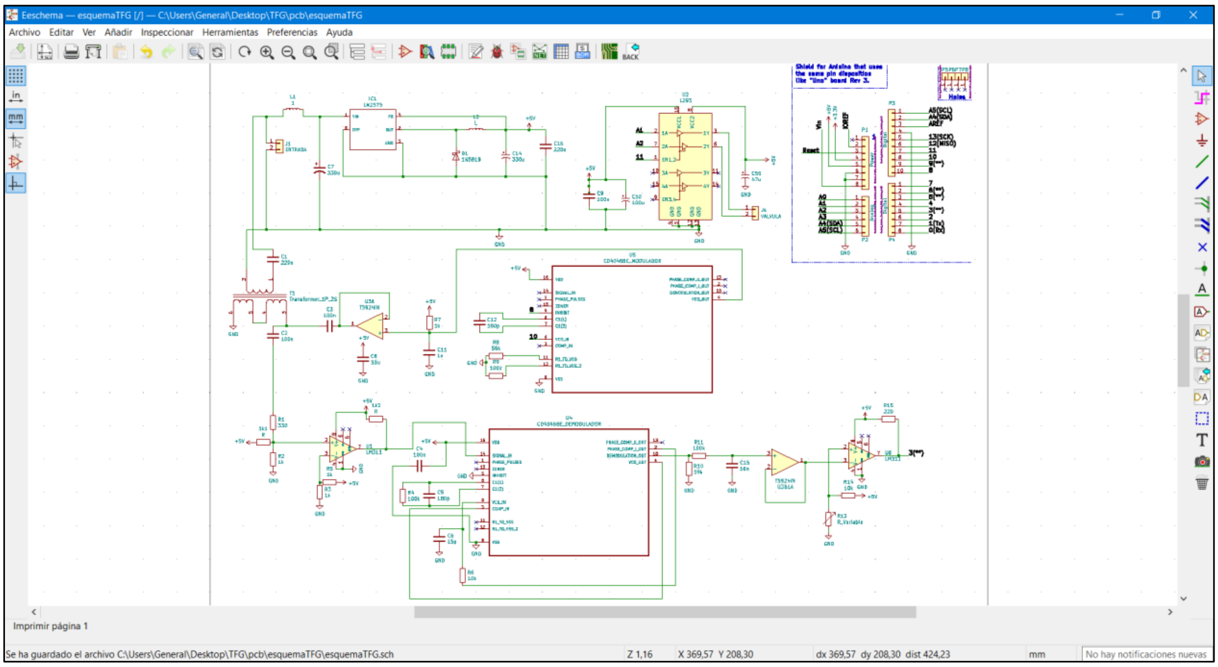


Fig. 31: Vista de "Eeschema" con el esquema creado.

Una vez creado el esquema, el siguiente paso fue asignar a los componentes los "*footprints*" en los que se colocarán en la placa impresa. Debido a que algunos componentes no aparecían en la librería, hubo que crear dichas huellas o modificar algunas de las ya existentes, para conseguir que los componentes encajen correctamente en la PCB. Por ejemplo, hubo que crear la huella del regulador "LM2575" (Fig. 32).

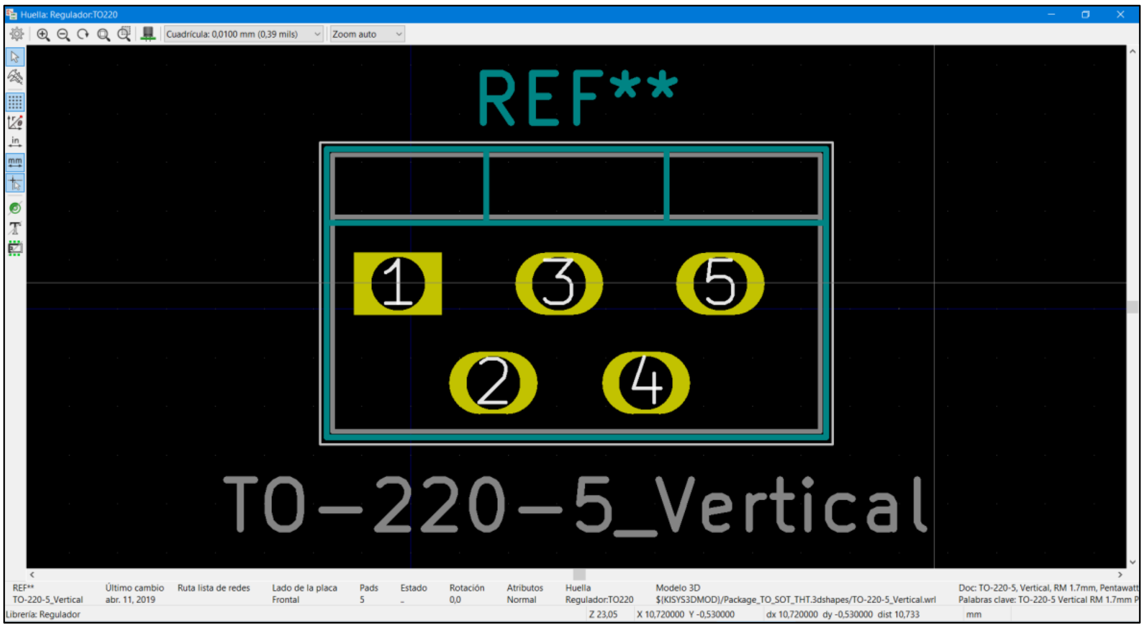


Fig. 32: huella del regulador "LM2575" en el editor de huellas de KiCAD.

Una vez asignados todos los "*footprints*" de los componentes del esquema, se genera el listado de redes. Esta acción genera las conexiones entre los componentes para pasar los datos a "*Pcbnew*", es decir, establece como se van a conectar los componentes en la placa. Una vez finalizada esta acción se pasa al "*Pcbnew*".

A continuación se procede a ordenar los componentes de manera que se crucen el menor número de conexiones, para facilitar el posterior trazado de las pistas. La placa estará formada por los componentes en su parte superior y la placa Arduino UNO, unida a ella mediante pines de conexión, por la parte posterior de la placa. Dado que la placa será a doble cara, se pueden aprovechar las dos caras para el trazado de las pistas, aunque se debe tener en cuenta el lado por el que se soldarán componentes como los integrados, que deben soldarse por la cara "*bottom*", o como los pines que unirán la placa Arduino, que deben soldarse por la cara "*top*". Esto es debido a la dificultad que supone soldar los componentes si se traza la pista por el lado en el que se van a colocar. Con el "Visor3D" (Fig. 33) se puede apreciar cómo quedará la PCB.

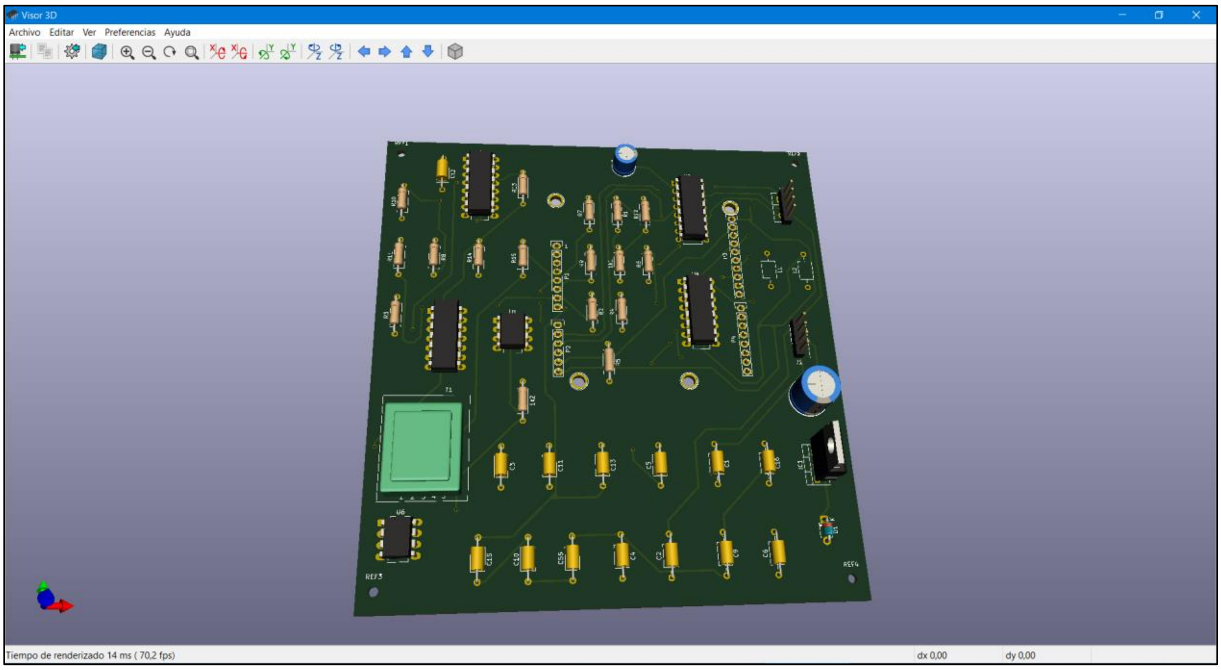


Fig. 33: visualización de la PCB con "Visor3D".

Una vez decidida la disposición de los componentes se procede a realizar el trazado de las pistas, teniendo en cuenta las reglas de diseño. Se añaden vías para facilitar el trazado, puesto que existen una gran cantidad de conexiones entre componentes. Se puede observar en la Fig. 33 los componentes conectados entre sí mediante las pistas. Se puede observar también la huella de la placa Arduino UNO. Las pistas tienen un ancho de 0.5 milímetros. Para las resistencias se escogió una huella estándar, ya que las utilizadas en este proyecto son todas de las mismas dimensiones. Para los condensadores se asignaron huellas en función de que fueran cerámicos o electrolíticos. Se asignaron huellas para los integrados en función de su tamaño. Estos se colocarán sobre zócalos para una mayor comodidad a la hora de tener que sustituirlos. Para el transformador y para el regulador se le asignaron las huellas creadas.

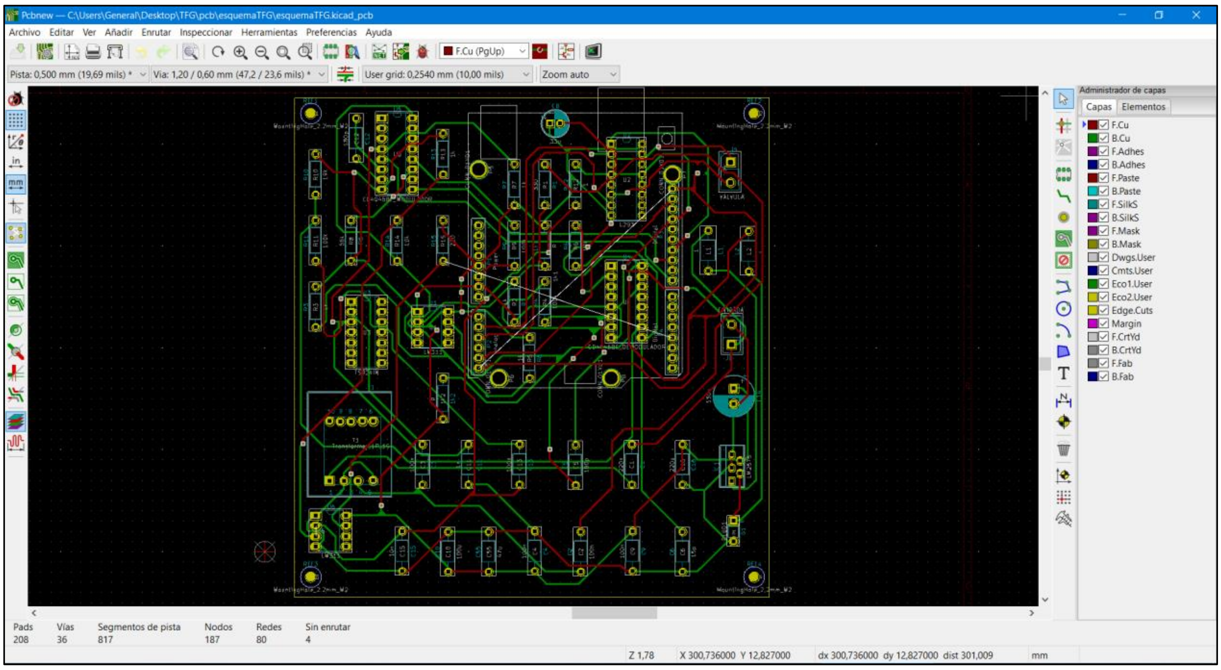


Fig. 34: trazado de las pistas con "Pcbnew".

Una vez finalizado el proceso trazar las pistas, se revisaron las reglas de diseño y las reglas eléctrica.

El proceso de impresión de la PCB lo realizará el Servicio de Electrónica de la Universidad de La Laguna. La primera opción era generar los archivos GERBER para su impresión con una fresadora CNC, pero por decisiones internas del servicio, este proceso ya no se realiza con dicha fresadora, sino con las transparencias (Fig. 35 y Fig. 36), mediante el proceso clásico. Finalmente se generaron las transparencias de la cara *top* y la cara *bottom* y se enviaron para la impresión de la PCB.

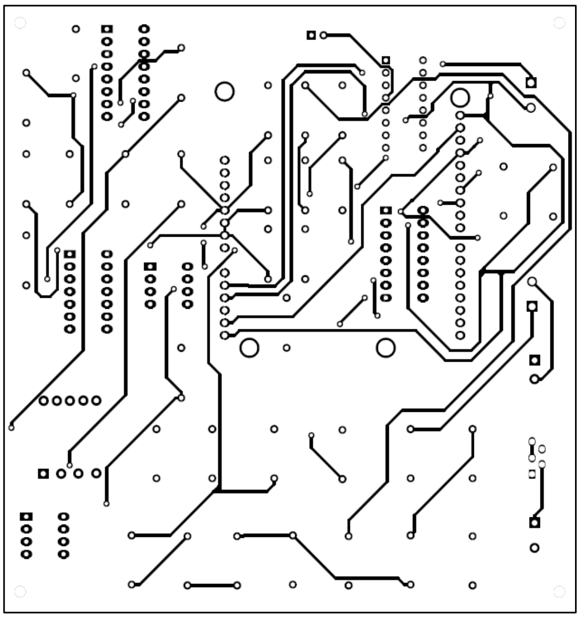


Fig. 35: transparencias de la cara top.

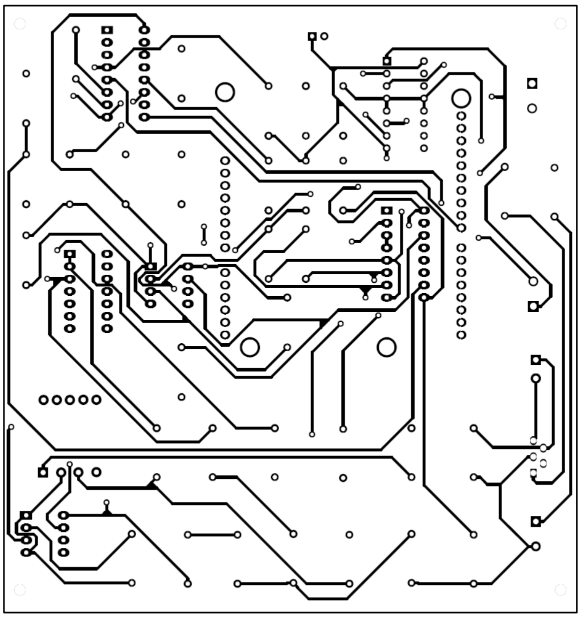


Fig. 36: Transparencias de la cara bottom.

Una vez impresa la placa por el servicio de electrónica, se realizó el taladrado de los agujeros y el soldado de los componentes. Se comprobó la continuidad en cada soldadura, comprobando que todos los componentes estuviesen debidamente conectados y se pasó a probar el funcionamiento de la placa.

CAPÍTULO 6 : PRUEBAS Y RESULTADOS.

En este apartado se explicará el procedimiento para evaluar el funcionamiento del sistema implementado. Se comentarán los pasos seguidos para simular el funcionamiento de los distintos bloques del circuito como si se estuvieran transmitiendo las señales de Arduino y, posteriormente, se comprobará el funcionamiento real conectando las placas Arduino. Además, se destacarán los problemas que han surgido durante las pruebas realizadas y se comentarán las soluciones aportadas para corregir estos problemas.

En primer lugar, se comenzó por comprobar el funcionamiento del bloque “REGULADOR”, puesto que es necesario para comprobar el funcionamiento del resto del circuito porque es el encargado de la alimentación de todos los componentes del circuito. Se comenzó comprobando que llegaba el voltaje correcto desde la fuente, es decir, los 12 voltios de continua que marca la fuente deben mantenerse hasta la entrada del regulador, pasando por la primera bobina y el condensador electrolítico (recuadro rojo de la Fig. 37). Una vez se comprueba este aspecto, se procede a comprobar el componente “LM2575T”. Se comprueba que las pines a tierra del regulador marcan cero voltios y que no hay ningún cortocircuito haciendo uso del MULTÍMETRO, ya que nos ofrece esta posibilidad.

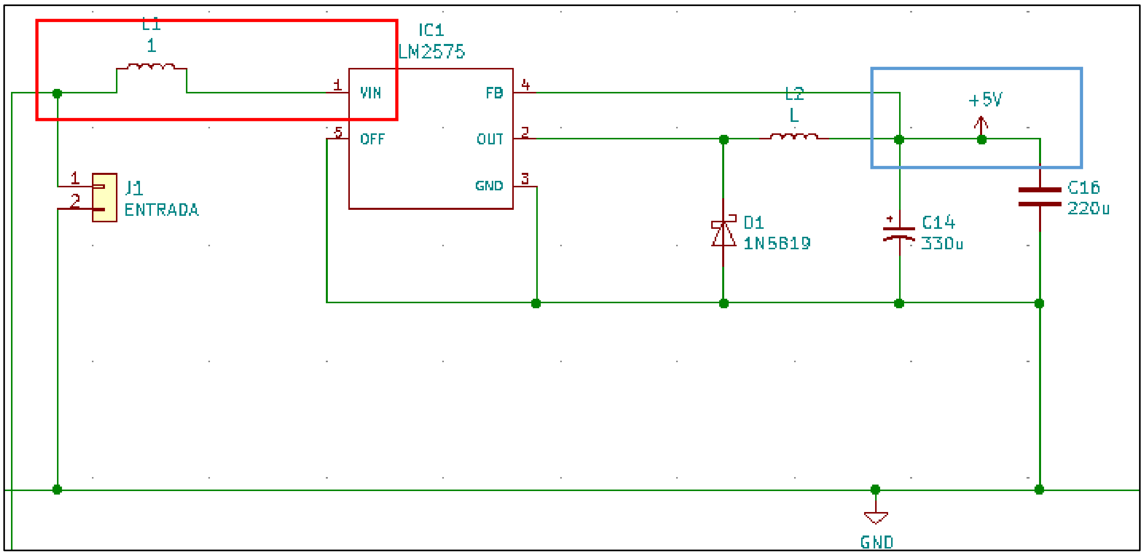


Fig. 37: bloque regulador.

Durante esta primera parte de la comprobación de este bloque no surgió ningún problema mientras se medía con el multímetro. Una vez se toma el valor de voltaje en la salida (recuadro azul de la Fig. 37) del dispositivo se aprecia que no es correcto. A pesar de que los componentes que conforman el regulador son correctos, el valor de salida, que debe ser de 5 voltios estables, varía entre 2 y 4 voltios. Tras pruebas y cambios de componentes y viendo que nada cambió, se probó a medir con el osciloscopio la señal de salida de la fuente (12 Vdc) y se puedo apreciar que esta señal tenía un nivel correcto pero también tenía mucho ruido, lo que provocaba esas variaciones irregulares en el voltaje de salida. Por tanto, se colocó un condensador electrolítico, como se ve en la Fig. 38 (recuadro rojo), para filtrar este ruido y obtener una señal de entrada al regulador “LM2575T” más limpia.

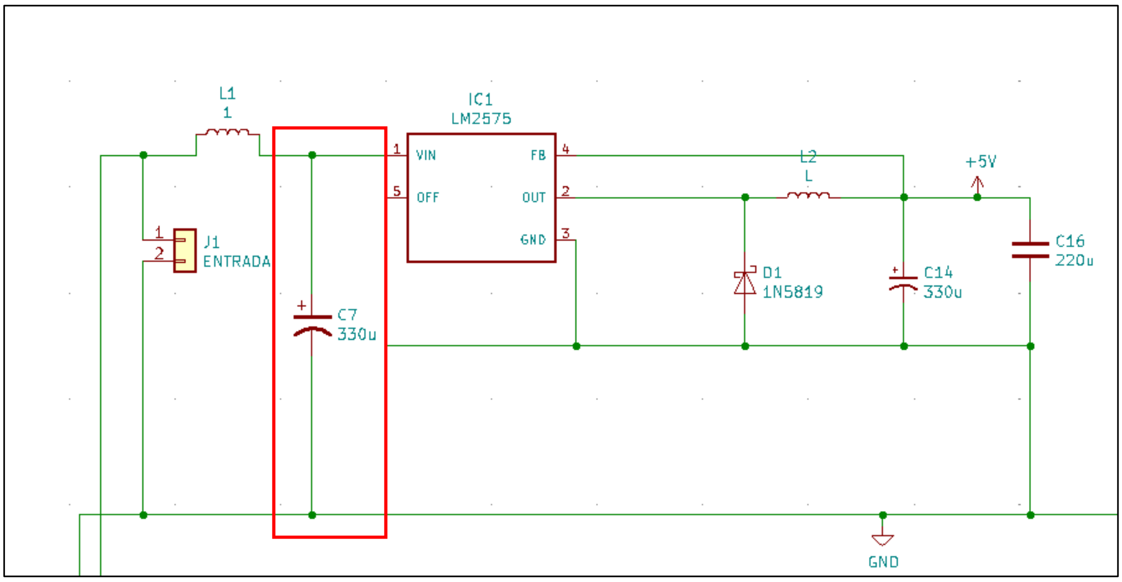


Fig. 38: bloque regulador modificado.

Paralelamente, mientras se trabajó en solucionar el problema con el regulador, se continuó comprobando el funcionamiento del bloque “MODULADOR”. Para ello, se utilizó directamente la fuente de voltaje para conseguir la alimentación de 5 voltios a la que funciona el circuito. En este bloque se comprobó el funcionamiento del componente “CD4046BE” en configuración de modulador. Para ello se utilizó el GENERADOR DE FUNCIONES como simulador de la señal de la placa Arduino UNO. Se generó una señal TTL de unos 220 Hz aproximadamente y se conectó al pin de entrada VCO de este *PLL*. El pin de salida de este componente (VCO out) se conectó al osciloscopio y se visualizó junto con la señal de emitida por el generador de funciones. Para la correcta visualización fue necesario corregir el nivel de disparo puesto que la señal modulada sale con dos frecuencias diferenciadas (Fig. 39).

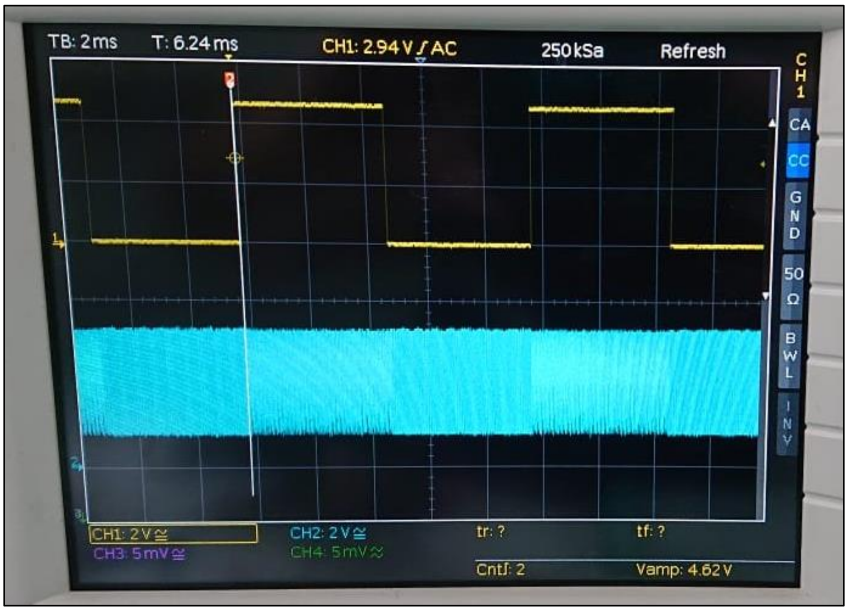


Fig. 39: señal TTL y señal modulada FSK.

Se pudo comprobar así como se realizaba una correcta modulación *FSK*, es decir, en los ‘1’ lógicos la señal tiene una frecuencia superior que en los ‘0’ lógicos.

Esta señal de salida del modulador, tras pasar por un filtro sencillo es conectada al “TS924IN”. Este componente está en configuración de amplificador de potencia, es decir, mantiene la misma señal pero amplifica la corriente para evitar que se debilite la señal en su paso por el transformador y el cable hasta su receptor.

Ya que el dispositivo implementado hace tanto de modulador como demodulador, para comprobar el funcionamiento de los componentes de la PCB realizada se puede utilizar la señal modulada por el bloque “MODULADOR” de esta misma placa para comprobar el funcionamiento del bloque “DEMODULADOR”. Por tanto, se comenzó verificando que la señal modulada de salida del amplificador de potencia llegaba correctamente al comparador “LM311N” situado antes del “CD4046BE” en configuración de demodulador. Esta señal se ve en el osciloscopio prácticamente igual que la señal de salida del modulador, como debe ocurrir.

Una vez se ha comprobado esto se verificó que el nivel de comparación es el deseado haciendo uso del osciloscopio y se compara la señal con el nivel de comparación visualmente en el osciloscopio. Se aprecia que la señal de entrada de este componente es correcta, presenta las variaciones de frecuencia en función de los niveles lógicos, pero muestra también una reducción de la amplitud y algunos picos de ruido significativos. En cambio, la señal de salida de este comparador es una señal estable de 5 voltios en la que se diferencia también las dos frecuencias de la modulación, como se aprecia en la Fig. 40. Esto se realiza puesto que esta señal es la señal de entrada del demodulador, por lo que es necesario que entre lo más limpia y estable posible para evitar un mensaje erróneo.

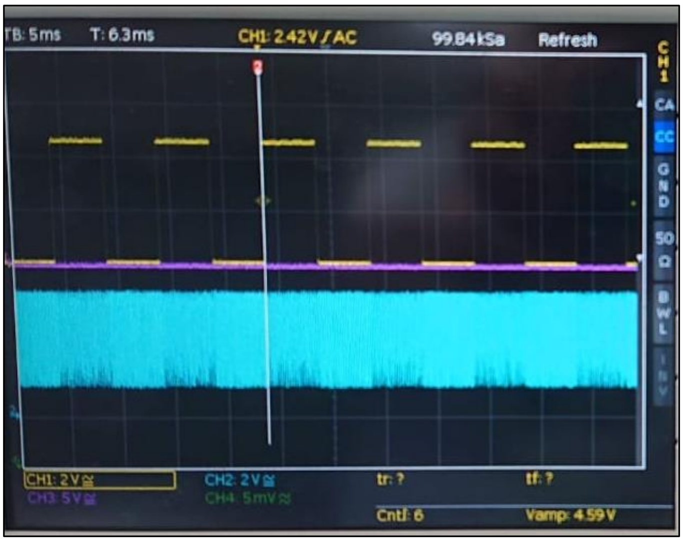


Fig. 40: señal modulada en la salida del comparador.

A continuación se verifica con el osciloscopio que la señal de salida del comparador se transmite por la pista correspondiente de la PCB hasta el pin de entrada del componente demodulador. Luego, se conecta la señal de salida de este componente al osciloscopio para comprobar que sale una señal con dos niveles de tensión diferenciados, que deberían ser 0 y 5 voltios. En la práctica se obtuvo una señal de salida en la que se podía diferenciar dos niveles (Fig. 41), pero con mucho ruido e invertida.

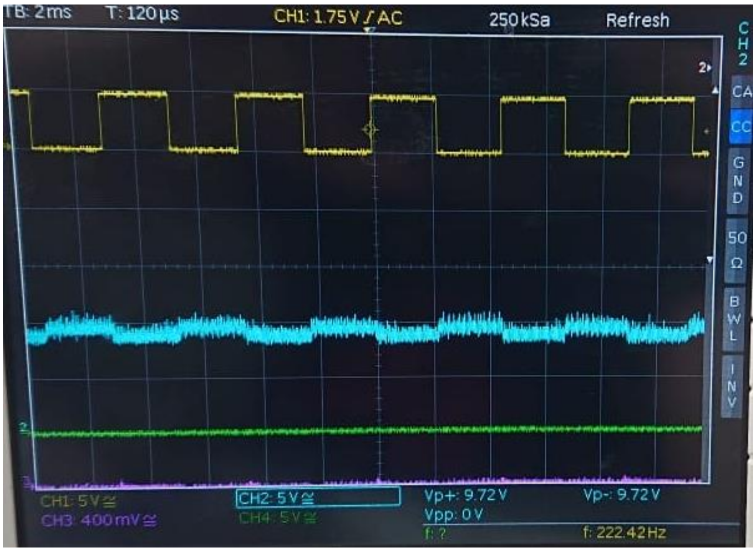


Fig. 41: señal de salida del demodulador sin corregir.

El primer problema era esperado puesto que en el diseño se implementa un filtro, cuya función es limpiar la señal de ruido, lo cual puede hacer que se reduzca la señal. No se esperaba que surgiera el segundo problema. Pese a esto, la solución tomada fue sencilla puesto que se cambiaría el pin de entrada inversor por el no inversor en el comparador de salida de esta etapa y se solucionaría el problema.

Para la solución del primer problema se diseñó un filtro pasa banda que reduce la amplitud de la señal, eliminando los ruidos de muy baja y alta frecuencia. En cambio en la práctica, lo que ocurre es que la señal se pierde, por tanto se optó por convertir este filtro en un filtro pasa bajas (Fig. 42). Además se cambió la resistencia que modifica la amplitud de la señal (R4 y R1 en la Fig. 42), consiguiendo que no se reduzca tanto.

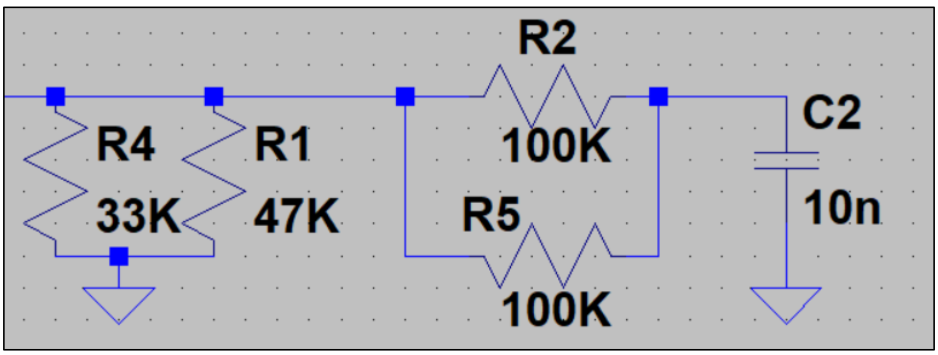


Fig. 42: nuevo filtro pasa bajas.

En el osciloscopio se comprobó el funcionamiento de este filtro y se observó que el nivel de continua no coincida con el nivel medio de la señal, ya que al modificar el filtro se vio modificada la componente de continua de esta señal. Para solventar este problema se decidió sustituir una de las resistencias del partidor de tensión que está conectado a la pata positiva, por un potenciómetro que permita ajustar este nivel de continua. Este nivel (en azul) se ve ajustado a la mitad de la señal de salida del filtro (en rosa) en la Fig. 43. También se podría haber resuelto quitando las dos resistencias, dejando únicamente el potenciómetro, pero había que hacer algunos cambios en la PCB que se prefirió no realizar.

Por último, se comprobó la salida del comparador de la etapa de salida. En este punto se debe obtener una señal estable de 0 – 5 voltios que debe copiar la señal de entrada, en este caso la señal TTL del generador de señales. Se puede apreciar que la señal de salida, en color verde en la Fig. 43, copia la entrada, en color amarillo en la misma figura.

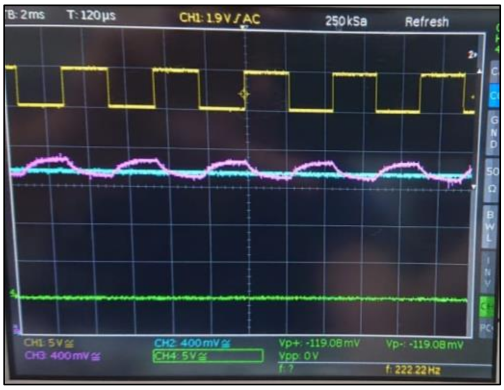


Fig. 43: señales en el comparador de salida I.

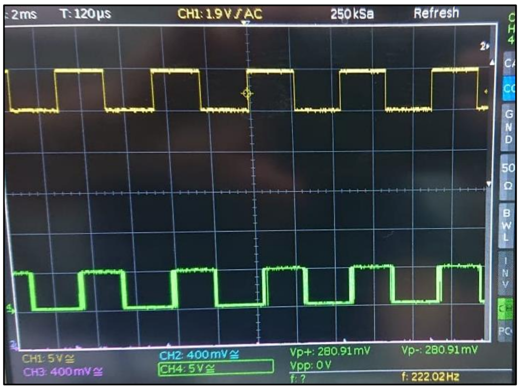


Fig. 44: señales en el comparador de salida II.

El problema que apareció ahora fue que mientras se mide las dos patas de entrada del operacional, inversora y no inversora, y la salida, se ve la señal en la pantalla del osciloscopio, mientras que si solo se mide la salida, no se observa señal alguna.

Tras realizar algunas pruebas y cambiar el componente "LM311N", se llegó a la conclusión que era posible que se tratase de una impedancia de salida demasiado alta, por lo que se aprovechó el circuito integrado "TS924IN" para utilizar uno de sus tres operacionales libres como amplificador de potencia (como se ve en el esquemático de la Fig. 45), consiguiendo así incrementar la intensidad en la etapa de salida. Una vez realizado este ajuste, se comprobó y se midió la señal de salida y se observó cómo seguía a la perfección a la señal de entrada.

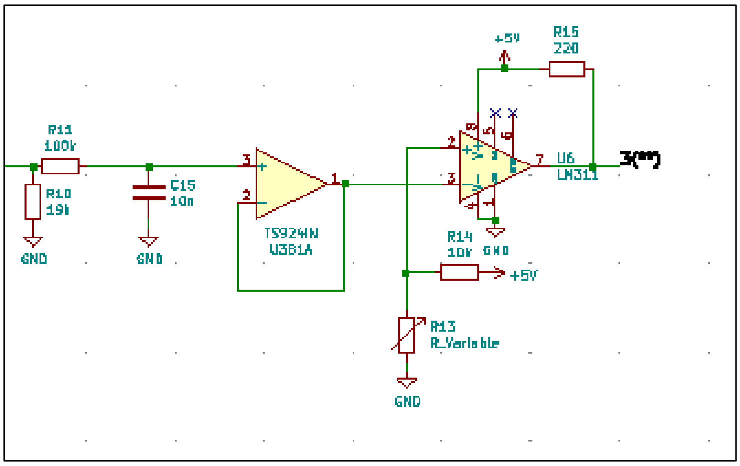
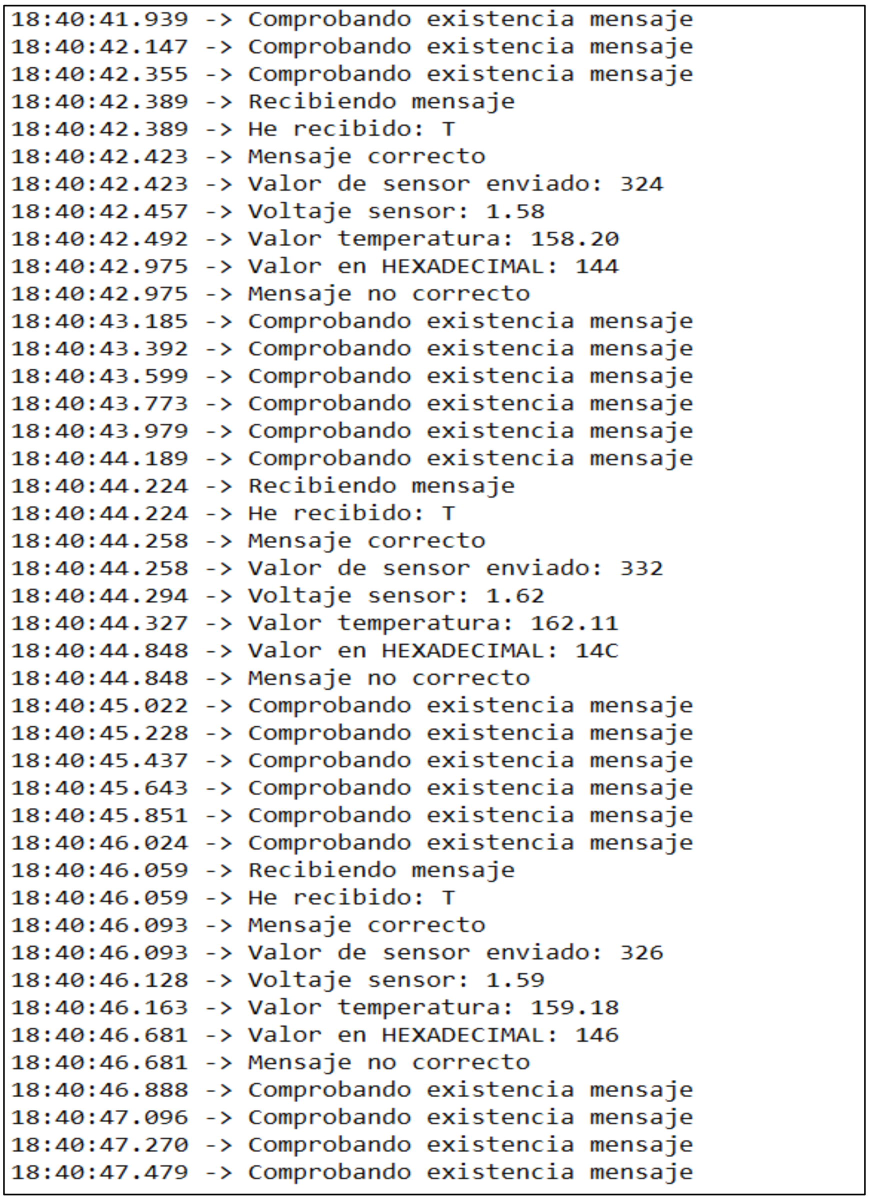


Fig. 45: esquemático de la etapa de salida modificada.

Una vez se consiguió que funcionasen correctamente todos los bloques que contiene la PCB, se implementó un módulo receptor para probar la comunicación entre la PCB y este receptor, es decir, entre maestro y esclavo. Se conectó un cable de unos cuantos metros por el que se transmiten los datos modulados en frecuencia. Durante este proceso surgieron problemas similares a los que iban surgiendo mientras se probó el funcionamiento de la PCB, por lo que se solventaron con mayor agilidad.

Se comprobó, en primer lugar, simulando la señal de Arduino con la señal TTL del generador de funciones, la comunicación entre el maestro y el esclavo y luego se conectaron las placas Arduino, cada uno con su código correspondiente, manteniendo la placa conectada al ordenador para poder comprobar los mensajes en el monitor serie. A continuación se muestra un fragmento de la comunicación del maestro (Fig. 46), conectado al puerto serie. Se observa cómo funciona correctamente aunque muestra que el mensaje no es correcto, debido a que no se conectó ningún sensor de temperatura.



```
18:40:41.939 -> Comprobando existencia mensaje
18:40:42.147 -> Comprobando existencia mensaje
18:40:42.355 -> Comprobando existencia mensaje
18:40:42.389 -> Recibiendo mensaje
18:40:42.389 -> He recibido: T
18:40:42.423 -> Mensaje correcto
18:40:42.423 -> Valor de sensor enviado: 324
18:40:42.457 -> Voltaje sensor: 1.58
18:40:42.492 -> Valor temperatura: 158.20
18:40:42.975 -> Valor en HEXADECIMAL: 144
18:40:42.975 -> Mensaje no correcto
18:40:43.185 -> Comprobando existencia mensaje
18:40:43.392 -> Comprobando existencia mensaje
18:40:43.599 -> Comprobando existencia mensaje
18:40:43.773 -> Comprobando existencia mensaje
18:40:43.979 -> Comprobando existencia mensaje
18:40:44.189 -> Comprobando existencia mensaje
18:40:44.224 -> Recibiendo mensaje
18:40:44.224 -> He recibido: T
18:40:44.258 -> Mensaje correcto
18:40:44.258 -> Valor de sensor enviado: 332
18:40:44.294 -> Voltaje sensor: 1.62
18:40:44.327 -> Valor temperatura: 162.11
18:40:44.848 -> Valor en HEXADECIMAL: 14C
18:40:44.848 -> Mensaje no correcto
18:40:45.022 -> Comprobando existencia mensaje
18:40:45.228 -> Comprobando existencia mensaje
18:40:45.437 -> Comprobando existencia mensaje
18:40:45.643 -> Comprobando existencia mensaje
18:40:45.851 -> Comprobando existencia mensaje
18:40:46.024 -> Comprobando existencia mensaje
18:40:46.059 -> Recibiendo mensaje
18:40:46.059 -> He recibido: T
18:40:46.093 -> Mensaje correcto
18:40:46.093 -> Valor de sensor enviado: 326
18:40:46.128 -> Voltaje sensor: 1.59
18:40:46.163 -> Valor temperatura: 159.18
18:40:46.681 -> Valor en HEXADECIMAL: 146
18:40:46.681 -> Mensaje no correcto
18:40:46.888 -> Comprobando existencia mensaje
18:40:47.096 -> Comprobando existencia mensaje
18:40:47.270 -> Comprobando existencia mensaje
18:40:47.479 -> Comprobando existencia mensaje
```

Fig. 46: fragmento de la comunicación vista desde el maestro.

CAPÍTULO 7 : CONCLUSIONES

En este proyecto se ha desarrollado la comunicación alámbrica bidireccional maestro-esclavo, que sirve de base para un sistema de riego inteligente. Para ello se rediseñaron algunas partes del circuito realizado en el proyecto “Sistema de riego inteligente de bajo coste”, por Yaiza Tejera Fumero, y se añadieron algunas funcionalidades.

Teniendo en cuenta las pruebas realizadas, se considera que el sistema funciona correctamente y cumple con el objetivo especificado en el primer capítulo de este proyecto, a pesar de todos los problemas que surgieron durante el desarrollo del mismo. Haber utilizado de base el circuito electrónico diseñado en el proyecto previo supuso un ahorro de tiempo para el alumno ya que este funcionaba montado en protoboard. A pesar de esto, al diseñar la PCB se tuvieron que realizar algunos cambios debido a que el diseño realizado anteriormente no tenía en cuenta algunos aspectos de las PCB, como las posibles altas impedancias de algunas pistas que queden mal formadas.

La implementación de este sistema de comunicación podría ser útil en terrenos muy extensos o en los que existan elementos que produzcan interferencias. En estos casos, las antenas de los módulos de radiofrecuencia que se podrían instalar ya no serían útiles, no solo porque el rango de alcance de los módulos de bajo coste puede no ser suficiente para cubrir el área de riego, sino también porque estos módulos necesitan un cable de alimentación que recorrería demasiados metros en el terreno. Este diseño de la comunicación soluciona ese problema sin realizar una inversión excesiva, ya que con solo un par de cables podemos abastecer toda la extensión de terreno, desde la caseta donde se ubica el dispositivo maestro hasta la electroválvula más alejada.

CONCLUSSIONS

In this Project it has been developed the bidirectional communication between the master and the slave, that which serves as the basis for an intelligent irrigation system. For this, it has been redesign some parts of the electronic circuit carried out by Miss Yaiza Tejera Fumero in the project "*Sistema de riego inteligente de bajo coste*". Other functionalities were added to the system.

Taking into account the tests carried out, it is considered that the system works correctly and meets the objective specified in the first chapter of this project, despite all the problems that happened during its development. Having used the electronic circuit designed in the previous project as a base meant a saving of time for the student because it worked on the protoboard. Despite this, when designing the PCB some changes had to be made because the design made previously did not take into account some aspects of the PCBs, such as the possible high impedances of some tracks that are poorly formed.

The implementation of this communication system could be useful in very large areas or where there are elements that produce interferences. In these cases, the antennas of the radiofrequency modules that could be installed would no longer be useful, not only because the range of low-cost modules may not be sufficient to cover the irrigation area, but also because these modules need a power cord that would travel too many meters in the irrigation field. This communication design solves this problem without making an excessive investment. Using only a pair of wires it can be supplied the entire area of land, from the master booth to the most remote electrovalve.

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ESCUELA SUPERIOR DE INGENIERÍA Y TECNOLOGÍA

SECCIÓN DE INGENIERÍA INDUSTRIAL

ANEXOS

TRABAJO DE FIN DE GRADO:

Titulación: Grado en Ingeniería Electrónica Industrial y Automática

TÍTULO:

SISTEMA DE RIEGO INTELIGENTE DE BAJO COSTE

AUTOR**:**

Carlo Hernández Rodríguez

Septiembre, 2019

ÍNDICE DE LOS ANEXOS

ANEXO 1: Datasheets

Anexo 1.1: LM2575

LM2575, NCV2575

1.0 A, Adjustable Output Voltage, Step-Down Switching Regulator

The LM2575 series of regulators are monolithic integrated circuits ideally suited for easy and convenient design of a step−down switching regulator (buck converter). All circuits of this series are capable of driving a 1.0 A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3 V, 5.0 V, 12 V, 15 V, and an adjustable output version.

These regulators were designed to minimize the number of external components to simplify the power supply design. Standard series of inductors optimized for use with the LM2575 are offered by several different inductor manufacturers.

Since the LM2575 converter is a switch−mode power supply, its efficiency is significantly higher in comparison with popular three−terminal linear regulators, especially with higher input voltages. In many cases, the power dissipated by the LM2575 regulator is so low, that no heatsink is required or its size could be reduced dramatically.

The LM2575 features include a guaranteed ±4% tolerance on output voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency (±2% over 0°C to 125°C). External shutdown is included, featuring 80 μA typical standby current. The output switch includes cycle−by−cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

Features

- 3.3 V, 5.0 V, 12 V, 15 V, and Adjustable Output Versions
- Adjustable Version Output Voltage Range of 1.23 V to 37 V ±4% Maximum Over Line and Load Conditions
- Guaranteed 1.0 A Output Current
- Wide Input Voltage Range: 4.75 V to 40 V
- Requires Only 4 External Components
- 52 kHz Fixed Frequency Internal Oscillator
- TTL Shutdown Capability, Low Power Standby Mode
- High Efficiency
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current Limit Protection
- Moisture Sensitivity Level (MSL) Equals 1
- Pb−Free Packages are Available*

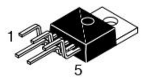
Applications

- Simple and High−Efficiency Step−Down (Buck) Regulators
- Efficient Pre−Regulator for Linear Regulators
- On−Card Switching Regulators
- Positive to Negative Converters (Buck−Boost)
- Negative Step−Up Converters
- Power Supply for Battery Chargers

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

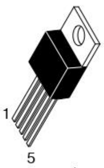
ON Semiconductor®

http://onsemi.com



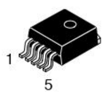
TO−220
TV SUFFIX
CASE 314B

Heatsink surface connected to Pin 3



TO−220
T SUFFIX
CASE 314D

Pin 1. V_{in}
2. Output
3. Ground
4. Feedback
5. $\overline{ON}$/OFF



D^2PAK
D2T SUFFIX
CASE 936A

Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3

ORDERING INFORMATION

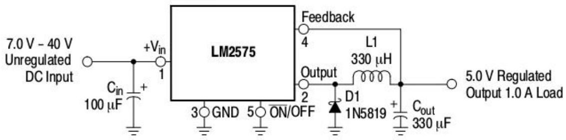
See detailed ordering and shipping information in the package dimensions section on page 25 of this data sheet.

DEVICE MARKING INFORMATION

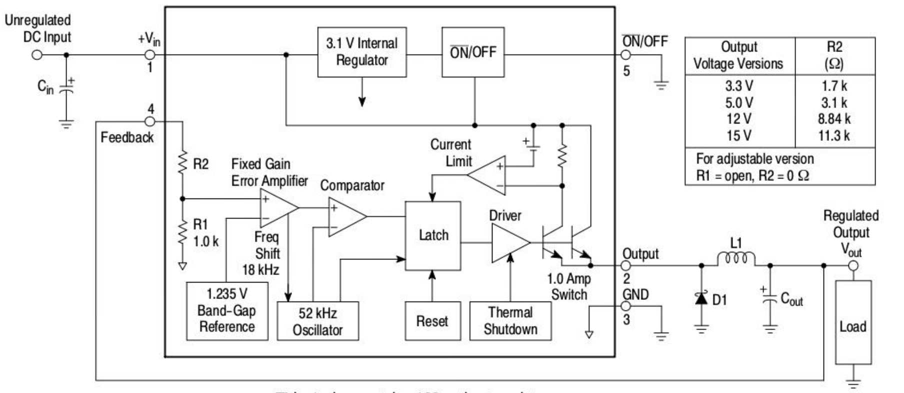
See general marking information in the device marking section on page 26 of this data sheet.

LM2575, NCV2575

Typical Application (Fixed Output Voltage Versions)



Representative Block Diagram and Typical Application



This device contains 162 active transistors.

Figure 1. Block Diagram and Typical Application

ABSOLUTE MAXIMUM RATINGS (Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.)

Rating	Symbol	Value	Unit
Maximum Supply Voltage	V_{in}	45	V
$\overline{ON}$/OFF Pin Input Voltage	–	$-0.3\ V \le V \le +V_{in}$	V
Output Voltage to Ground (Steady−State)	–	−1.0	V
Power Dissipation			
Case 314B and 314D (TO−220, 5−Lead)	P_D	Internally Limited	W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	65	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	5.0	°C/W
Case 936A (D^2PAK)	P_D	Internally Limited	W
Thermal Resistance, Junction−to−Ambient (Figure 34)	$R_{\theta JA}$	70	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	5.0	°C/W
Storage Temperature Range	T_{stg}	−65 to +150	°C
Minimum ESD Rating (Human Body Model: C = 100 pF, R = 1.5 kΩ)	–	2.0	kV
Lead Temperature (Soldering, 10 s)	–	260	°C
Maximum Junction Temperature	T_J	150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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OPERATING RATINGS (Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	–40 to +125	°C
Supply Voltage	V_{in}	40	V

SYSTEM PARAMETERS ([Note 1] Test Circuit Figure 14)

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{in} = 12 V for the 3.3 V, 5.0 V, and Adjustable version, V_{in} = 25 V for the 12 V version, and V_{in} = 30 V for the 15 V version. I_{Load} = 200 mA. For typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies [Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
LM2575–3.3 (Note 1 Test Circuit Figure 14)					
Output Voltage (V_{in} = 12 V, I_{Load} = 0.2 A, T_J = 25°C)	V_{out}	3.234	3.3	3.366	V
Output Voltage (4.75 V ≤ V_{in} ≤ 40 V, 0.2 A ≤ I_{Load} ≤ 1.0 A) T_J = 25°C T_J = –40 to +125°C	V_{out}	 3.168 3.135	 3.3 –	 3.432 3.465	V
Efficiency (V_{in} = 12 V, I_{Load} = 1.0 A)	η	–	75	–	%
LM2575–5 ([Note 1] Test Circuit Figure 14)					
Output Voltage (V_{in} = 12 V, I_{Load} = 0.2 A, T_J = 25°C)	V_{out}	4.9	5.0	5.1	V
Output Voltage (8.0 V ≤ V_{in} ≤ 40 V, 0.2 A ≤ I_{Load} ≤ 1.0 A) T_J = 25°C T_J = –40 to +125°C	V_{out}	 4.8 4.75	 5.0 –	 5.2 5.25	V
Efficiency (V_{in} = 12 V, I_{Load} = 1.0 A)	η	–	77	–	%
LM2575–12 (Note 1 Test Circuit Figure 14)					
Output Voltage (V_{in} = 25 V, I_{Load} = 0.2 A, T_J = 25°C)	V_{out}	11.76	12	12.24	V
Output Voltage (15 V ≤ V_{in} ≤ 40 V, 0.2 A ≤ I_{Load} ≤ 1.0 A) T_J = 25°C T_J = –40 to +125°C	V_{out}	 11.52 11.4	 12 –	 12.48 12.6	V
Efficiency (V_{in} = 15V, I_{Load} = 1.0 A)	η	–	88	–	%
LM2575–15 (Note 1 Test Circuit Figure 14)					
Output Voltage (V_{in} = 30 V, I_{Load} = 0.2 A, T_J = 25°C)	V_{out}	14.7	15	15.3	V
Output Voltage (18 V ≤ V_{in} ≤ 40 V, 0.2 A ≤ I_{Load} ≤ 1.0 A) T_J = 25°C T_J = –40 to +125°C	V_{out}	 14.4 14.25	 15 –	 15.6 15.75	V
Efficiency (V_{in} = 18 V, I_{Load} = 1.0 A)	η	–	88	–	%
LM2575 ADJUSTABLE VERSION (Note 1 Test Circuit Figure 14)					
Feedback Voltage (V_{in} = 12 V, I_{Load} = 0.2 A, V_{out} = 5.0 V, T_J = 25°C)	V_{FB}	1.217	1.23	1.243	V
Feedback Voltage (8.0 V ≤ V_{in} ≤ 40 V, 0.2 A ≤ I_{Load} ≤ 1.0 A, V_{out} = 5.0 V) T_J = 25°C T_J = –40 to +125°C	V_{FB}	 1.193 1.18	 1.23 –	 1.267 1.28	V
Efficiency (V_{in} = 12 V, I_{Load} = 1.0 A, V_{out} = 5.0 V)	η	–	77	–	%

1. External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2575 is used as shown in the Figure 14 test circuit, system performance will be as shown in system parameters section.
2. Tested junction temperature range for the LM2575 and the NCV2575: T_{low} = –40°C T_{high} = +125°C

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DEVICE PARAMETERS

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{in} = 12 V for the 3.3 V, 5.0 V, and Adjustable version, V_{in} = 25 V for the 12 V version, and V_{in} = 30 V for the 15 V version. I_{Load} = 200 mA. For typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies [Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
ALL OUTPUT VOLTAGE VERSIONS					
Feedback Bias Current (V_{out} = 5.0 V Adjustable Version Only)	I_b				nA
T_J = 25°C		–	25	100	
T_J = −40 to +125°C		–	–	200	
Oscillator Frequency Note 3	f_{osc}				kHz
T_J = 25°C		–	52	–	
T_J = 0 to +125°C		47	–	58	
T_J = −40 to +125°C		42	–	63	
Saturation Voltage (I_{out} = 1.0 A Note 4)	V_{sat}				V
T_J = 25°C		–	1.0	1.2	
T_J = −40 to +125°C		–	–	1.3	
Max Duty Cycle (“on”) Note 5	DC	94	98	–	%
Current Limit (Peak Current Notes 4 and 3)	I_{CL}				A
T_J = 25°C		1.7	2.3	3.0	
T_J = −40 to +125°C		1.4	–	3.2	
Output Leakage Current Notes 6 and 7, T_J = 25°C	I_L				mA
Output = 0 V		–	0.8	2.0	
Output = −1.0 V		–	6.0	20	
Quiescent Current Note 6	I_Q				mA
T_J = 25°C		–	5.0	9.0	
T_J = −40 to +125°C		–	–	11	
Standby Quiescent Current ($\overline{ON}$/OFF Pin = 5.0 V (“off”))	I_{stby}				μA
T_J = 25°C		15	80	200	
T_J = −40 to +125°C		–	–	400	
$\overline{ON}$/OFF Pin Logic Input Level (Test Circuit Figure 14)					V
V_{out} = 0 V	V_{IH}				
T_J = 25°C		2.2	1.4	–	
T_J = −40 to +125°C		2.4	–	–	
V_{out} = Nominal Output Voltage	V_{IL}				
T_J = 25°C		–	1.2	1.0	
T_J = −40 to +125°C		–	–	0.8	
$\overline{ON}$/OFF Pin Input Current (Test Circuit Figure 14)					μA
$\overline{ON}$/OFF Pin = 5.0 V (“off”), T_J = 25°C	I_{IH}	–	15	30	
$\overline{ON}$/OFF Pin = 0 V (“on”), T_J = 25°C	I_{IL}	–	0	5.0	

3. The oscillator frequency reduces to approximately 18 kHz in the event of an output short or an overload which causes the regulated output voltage to drop approximately 40% from the nominal output voltage. This self protection feature lowers the average dissipation of the IC by lowering the minimum duty cycle from 5% down to approximately 2%.
4. Output (Pin 2) sourcing current. No diode, inductor or capacitor connected to output pin.
5. Feedback (Pin 4) removed from output and connected to 0 V.
6. Feedback (Pin 4) removed from output and connected to +12 V for the Adjustable, 3.3 V, and 5.0 V versions, and +25 V for the 12 V and 15 V versions, to force the output transistor “off”.
7. V_{in} = 40 V.

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TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 14)

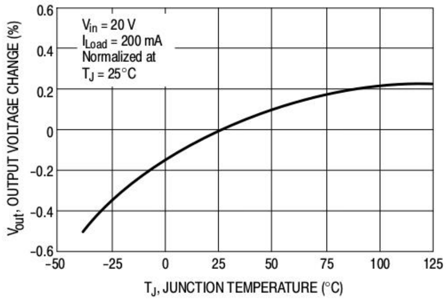

Figure 2. Normalized Output Voltage

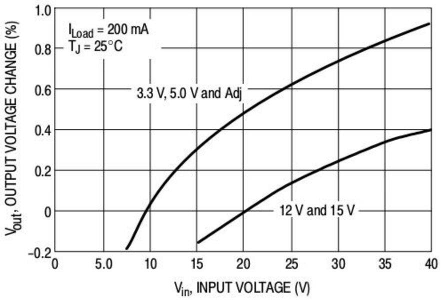

Figure 3. Line Regulation

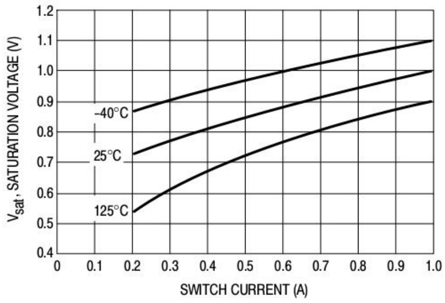

Figure 4. Switch Saturation Voltage

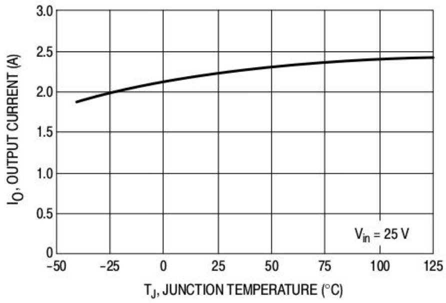

Figure 5. Current Limit

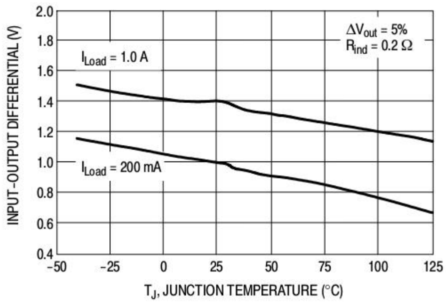

Figure 6. Dropout Voltage

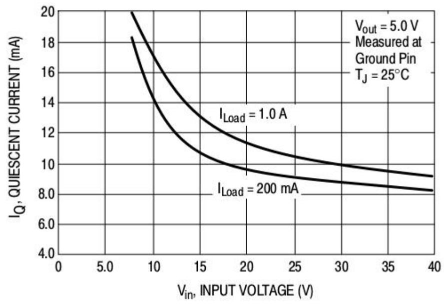

Figure 7. Quiescent Current

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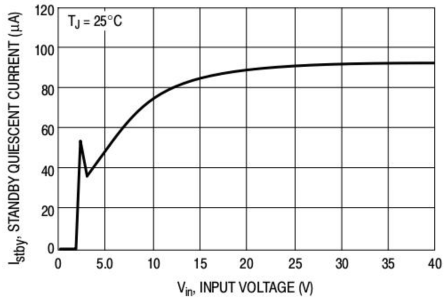

Figure 8. Standby Quiescent Current

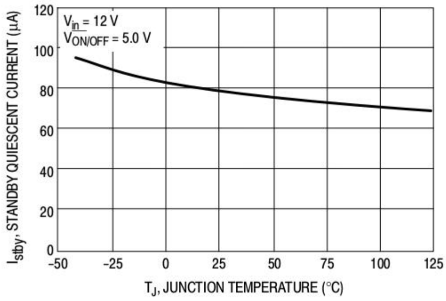

Figure 9. Standby Quiescent Current

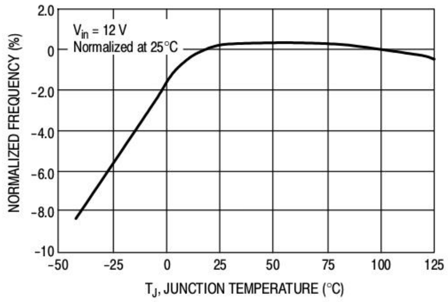

Figure 10. Oscillator Frequency

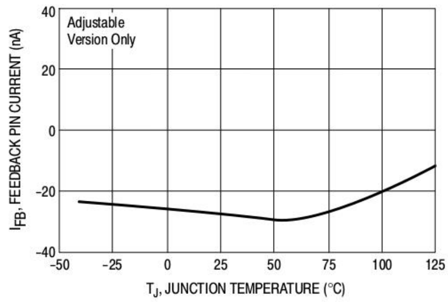

Figure 11. Feedback Pin Current

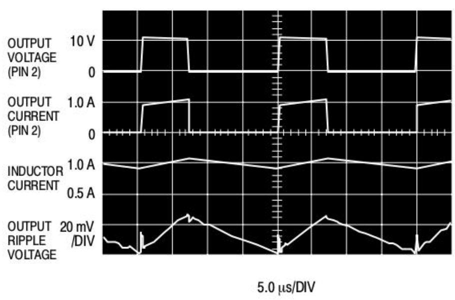

Figure 12. Switching Waveforms

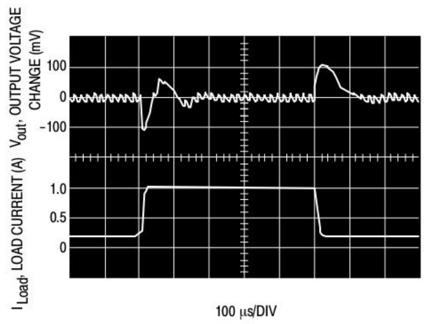

Figure 13. Load Transient Response

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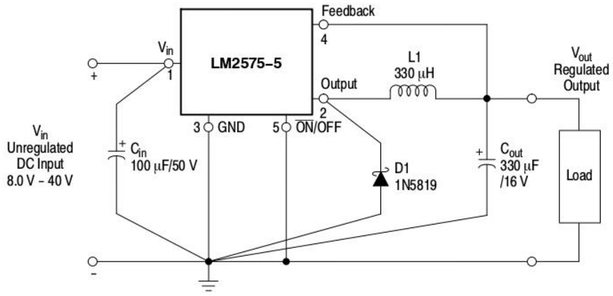
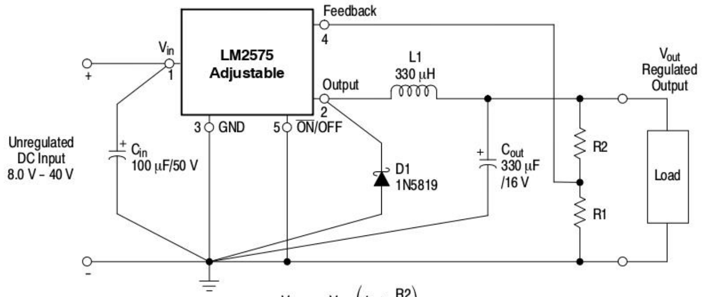
5.0 Output Voltage Versions



Adjustable Output Voltage Versions



$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right)$$

$$R2 = R1\left(\frac{V_{out}}{V_{ref}} - 1\right)$$

Where V_{ref} = 1.23 V, R1 between 1.0 kΩ and 5.0 kΩ

Figure 14. Typical Test Circuit

PCB LAYOUT GUIDELINES

As in any switching regulator, the layout of the printed circuit board is very important. Rapidly switching currents associated with wiring inductance, stray capacitance and parasitic inductance of the printed circuit board traces can generate voltage transients which can generate electromagnetic interferences (EMI) and affect the desired operation. As indicated in the Figure 14, to minimize inductance and ground loops, the length of the leads indicated by heavy lines should be kept as short as possible. For best results, single−point grounding (as indicated) or ground plane construction should be used.

On the other hand, the PCB area connected to the Pin 2 (emitter of the internal switch) of the LM2575 should be kept to a minimum in order to minimize coupling to sensitive circuitry.

Another sensitive part of the circuit is the feedback. It is important to keep the sensitive feedback wiring short. To assure this, physically locate the programming resistors near to the regulator, when using the adjustable version of the LM2575 regulator.

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PIN FUNCTION DESCRIPTION

Pin	Symbol	Description (Refer to Figure 1)
1	V_{in}	This pin is the positive input supply for the LM2575 step−down switching regulator. In order to minimize voltage transients and to supply the switching currents needed by the regulator, a suitable input bypass capacitor must be present (C_{in} in Figure 1).
2	Output	This is the emitter of the internal switch. The saturation voltage V_{sat} of this output switch is typically 1.0 V. It should be kept in mind that the PCB area connected to this pin should be kept to a minimum in order to minimize coupling to sensitive circuitry.
3	GND	Circuit ground pin. See the information about the printed circuit board layout.
4	Feedback	This pin senses regulated output voltage to complete the feedback loop. The signal is divided by the internal resistor divider network R2, R1 and applied to the non−inverting input of the internal error amplifier. In the Adjustable version of the LM2575 switching regulator this pin is the direct input of the error amplifier and the resistor network R2, R1 is connected externally to allow programming of the output voltage.
5	$\overline{\text{ON}}$/OFF	It allows the switching regulator circuit to be shut down using logic level signals, thus dropping the total input supply current to approximately 80 μA. The input threshold voltage is typically 1.4 V. Applying a voltage above this value (up to $+V_{in}$) shuts the regulator off. If the voltage applied to this pin is lower than 1.4 V or if this pin is connected to ground, the regulator will be in the "on" condition.

DESIGN PROCEDURE

Buck Converter Basics

The LM2575 is a "Buck" or Step−Down Converter which is the most elementary forward−mode converter. Its basic schematic can be seen in Figure 15.

The operation of this regulator topology has two distinct time periods. The first one occurs when the series switch is on, the input voltage is connected to the input of the inductor.

The output of the inductor is the output voltage, and the rectifier (or catch diode) is reverse biased. During this period, since there is a constant voltage source connected across the inductor, the inductor current begins to linearly ramp upwards, as described by the following equation:

$$I_{L(on)} = \frac{\left(V_{in} - V_{out}\right) t_{on}}{L}$$

During this "on" period, energy is stored within the core material in the form of magnetic flux. If the inductor is properly designed, there is sufficient energy stored to carry the requirements of the load during the "off" period.

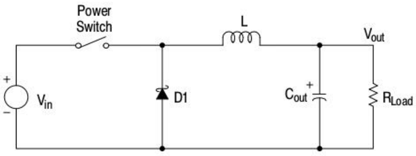

Figure 15. Basic Buck Converter

The next period is the "off" period of the power switch. When the power switch turns off, the voltage across the inductor reverses its polarity and is clamped at one diode voltage drop below ground by catch dioded. Current now flows through the catch diode thus maintaining the load current loop. This removes the stored energy from the inductor.

The inductor current during this time is:

$$I_{L(off)} = \frac{\left(V_{out} - V_{D}\right) t_{off}}{L}$$

This period ends when the power switch is once again turned on. Regulation of the converter is accomplished by varying the duty cycle of the power switch. It is possible to describe the duty cycle as follows:

$d = \frac{t_{on}}{T}$, where T is the period of switching.

For the buck converter with ideal components, the duty cycle can also be described as:

$$d = \frac{V_{out}}{V_{in}}$$

Figure 16 shows the buck converter idealized waveforms of the catch diode voltage and the inductor current.

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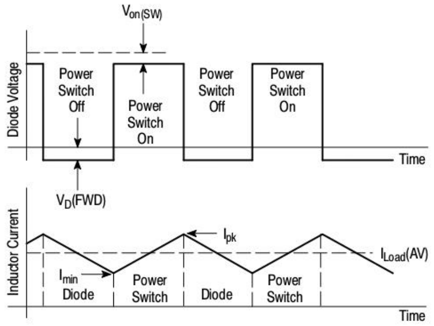

Figure 16. Buck Converter Idealized Waveforms

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Procedure (Fixed Output Voltage Version) In order to simplify the switching regulator design, a step−by−step design procedure and example is provided.

Procedure	Example
Given Parameters: V_{out} = Regulated Output Voltage (3.3 V, 5.0 V, 12 V or 15 V) $V_{in(max)}$ = Maximum DC Input Voltage $I_{Load(max)}$ = Maximum Load Current	**Given Parameters:** V_{out} = 5.0 V $V_{in(max)}$ = 20 V $I_{Load(max)}$ = 0.8 A
1. Controller IC Selection According to the required input voltage, output voltage and current, select the appropriate type of the controller IC output voltage version.	**1. Controller IC Selection** According to the required input voltage, output voltage, current polarity and current value, use the LM2575−5 controller IC
2. Input Capacitor Selection (C_{in}) To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin $+V_{in}$ and ground pin GND. This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value.	**2. Input Capacitor Selection (C_{in})** A 47 μF, 25 V aluminium electrolytic capacitor located near to the input and ground pins provides sufficient bypassing.
3. Catch Diode Selection (D1) **A.** Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design the diode should have a current rating equal to the maximum current limit of the LM2575 to be able to withstand a continuous output short **B.** The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	**3. Catch Diode Selection (D1)** **A.** For this example the current rating of the diode is 1.0 A. **B.** Use a 30 V 1N5818 Schottky diode, or any of the suggested fast recovery diodes shown in the Table 4.
4. Inductor Selection (L1) **A.** According to the required working conditions, select the correct inductor value using the selection guide from Figures 17 to 21. **B.** From the appropriate inductor selection guide, identify the inductance region intersected by the Maximum Input Voltage line and the Maximum Load Current line. Each region is identified by an inductance value and an inductor code. **C.** Select an appropriate inductor from the several different manufacturers part numbers listed in Table 1 or Table 2. When using Table 2 for selecting the right inductor the designer must realize that the inductor current rating must be higher than the maximum peak current flowing through the inductor. This maximum peak current can be calculated as follows: $I_{p(max)} = I_{Load(max)} + \frac{(V_{in} - V_{out})\, t_{on}}{2L}$ where t_{on} is the "on" time of the power switch and $t_{on} = \frac{V_{out}}{V_{in}} \times \frac{1}{f_{osc}}$ For additional information about the inductor, see the inductor section in the "External Components" section of this data sheet.	**4. Inductor Selection (L1)** **A.** Use the inductor selection guide shown in Figures 17 to 21. **B.** From the selection guide, the inductance area intersected by the 20 V line and 0.8 A line is L330. **C.** Inductor value required is 330 μH. From the Table 1 or Table 2, choose an inductor from any of the listed manufacturers.

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Procedure (Fixed Output Voltage Version) (continued) In order to simplify the switching regulator design, a step−by−step design procedure and example is provided.

Procedure	Example
5. Output Capacitor Selection (C_{out}) **A.** Since the LM2575 is a forward−mode switching regulator with voltage mode control, its open loop 2−pole−2−zero frequency characteristic has the dominant pole−pair determined by the output capacitor and inductor values. For stable operation and an acceptable ripple voltage, (approximately 1% of the output voltage) a value between 100 μF and 470 μF is recommended. **B.** Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating at least 8V is appropriate, and a 10 V or 16 V rating is recommended.	**5. Output Capacitor Selection (C_{out})** **A.** C_{out} = 100 μF to 470 μF standard aluminium electrolytic. **B.** Capacitor voltage rating = 16 V.

Procedure (Adjustable Output Version: LM2575−Adj)

Procedure	Example
Given Parameters: V_{out} = Regulated Output Voltage $V_{in(max)}$ = Maximum DC Input Voltage $I_{Load(max)}$ = Maximum Load Current	**Given Parameters:** V_{out} = 8.0 V $V_{in(max)}$ = 12 V $I_{Load(max)}$ = 1.0 A
1. Programming Output Voltage To select the right programming resistor R1 and R2 value (see Figure 14) use the following formula: $V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right)$ where V_{ref} = 1.23 V Resistor R1 can be between 1.0 k and 5.0 kΩ. (For best temperature coefficient and stability with time, use 1% metal film resistors). $R2 = R1\left(\frac{V_{out}}{V_{ref}} \square\right)$	**1. Programming Output Voltage** (selecting R1 and R2) Select R1 and R2: $V_{out} = 1.23\left(1 + \frac{R2}{R1}\right)$ Select R1 = 1.8 kΩ $R2 = R1\left(\frac{V_{out}}{V_{ref}} - 1\right) = 1.8\,k\left(\frac{8.0\ V}{1.23\ V} - 1\right)$ R2 = 9.91 kΩ, choose a 9.88 k metal film resistor.
2. Input Capacitor Selection (C_{in}) To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin $+V_{in}$ and ground pin GND This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value. For additional information see input capacitor section in the "External Components" section of this data sheet.	**2. Input Capacitor Selection (C_{in})** A 100 μF aluminium electrolytic capacitor located near the input and ground pin provides sufficient bypassing.
3. Catch Diode Selection (D1) **A.** Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design, the diode should have a current rating equal to the maximum current limit of the LM2575 to be able to withstand a continuous output short. **B.** The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	**3. Catch Diode Selection (D1)** **A.** For this example, a 3.0 A current rating is adequate. **B.** Use a 20 V 1N5820 or MBR320 Schottky diode or any suggested fast recovery diode in the Table 4.

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Procedure (Adjustable Output Version: LM2575–Adj) (continued)

Procedure	Example
4. Inductor Selection (L1) **A.** Use the following formula to calculate the inductor Volt x microsecond [V x μs] constant: $E \times T = \left(V_{in} - V_{out}\right) \frac{V_{out}}{V_{on}} \times \frac{10^6}{F[Hz]}$ [V x μs] **B.** Match the calculated E x T value with the corresponding number on the vertical axis of the Inductor Value Selection Guide shown in Figure 21. This E x T constant is a measure of the energy handling capability of an inductor and is dependent upon the type of core, the core area, the number of turns, and the duty cycle. **C.** Next step is to identify the inductance region intersected by the E x T value and the maximum load current value on the horizontal axis shown in Figure 21. **D.** From the inductor code, identify the inductor value. Then select an appropriate inductor from the Table 1 or Table 2. The inductor chosen must be rated for a switching frequency of 52 kHz and for a current rating of 1.15 x I_{load}. The inductor current rating can also be determined by calculating the inductor peak current: $I_{p(max)} = I_{Load(max)} + \frac{\left(V_{in} - V_{out}\right) t_{on}}{2L}$ where t_{on} is the "on" time of the power switch and $t_{on} = \frac{V_{out}}{V_{in}} \times \frac{1}{f_{osc}}$ For additional information about the inductor, see the inductor section in the "External Components" section of this data sheet.	**4. Inductor Selection (L1)** **A.** Calculate E x T [V x μs] constant: $E \times T = (12 - 8.0) \times \frac{8.0}{12} \times \frac{1000}{52} = 51$ [V x μs] **B.** E x T = 51 [V x μs] **C.** $I_{Load(max)}$ = 1.0 A Inductance Region = L220 **D.** Proper inductor value = 220 μH Choose the inductor from the Table 1 or Table 2.
5. Output Capacitor Selection (C_{out}) **A.** Since the LM2575 is a forward–mode switching regulator with voltage mode control, its open loop 2–pole–2–zero frequency characteristic has the dominant pole–pair determined by the output capacitor and inductor values. For stable operation, the capacitor must satisfy the following requirement: $C_{out} \geq 7.785 \frac{V_{in(max)}}{V_{out} \times L\,[\mu H]}$ [μF] **B.** Capacitor values between 10 μF and 2000 μF will satisfy the loop requirements for stable operation. To achieve an acceptable output ripple voltage and transient response, the output capacitor may need to be several times larger than the above formula yields. **C.** Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating of at least 8V is appropriate, and a 10 V or 16 V rating is recommended.	**5. Output Capacitor Selection (C_{out})** **A.** $C_{out} \geq 7.785 \frac{12}{8.220} = 53\ \mu F$ To achieve an acceptable ripple voltage, select C_{out} = 100 μF electrolytic capacitor.

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INDUCTOR VALUE SELECTION GUIDE

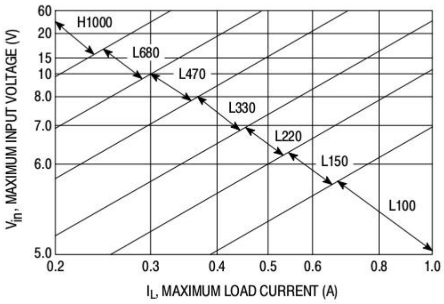

Figure 17. LM2575−3.3

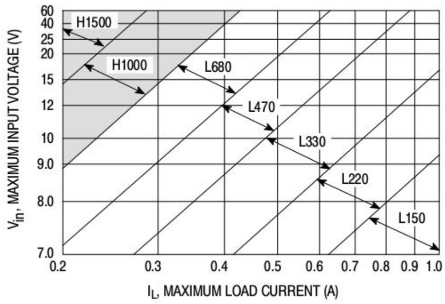

Figure 18. LM2575−5.0

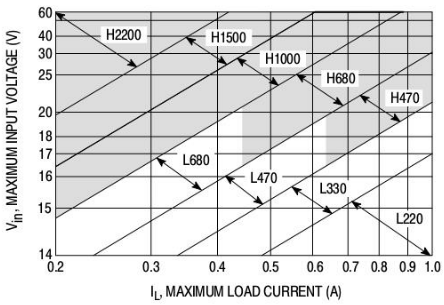

Figure 19. LM2575−12

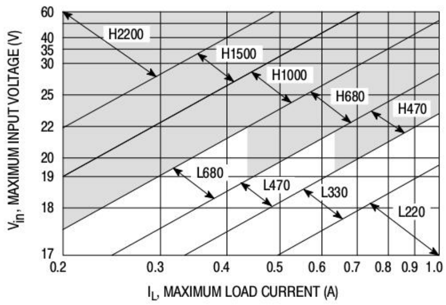

Figure 20. LM2575−15

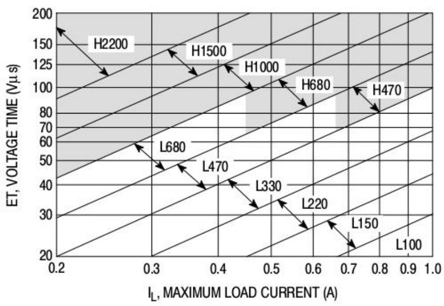

Figure 21. LM2575−Adj

NOTE: This Inductor Value Selection Guide is applicable for continuous mode only.

Table 1. Inductor Selection Guide

Inductor Code	Inductor Value	Pulse Eng	Renco	AIE	Tech 39
L100	100 μH	PE–92108	RL2444	415–0930	77 308 BV
L150	150 μH	PE–53113	RL1954	415–0953	77 358 BV
L220	220 μH	PE–52626	RL1953	415–0922	77 408 BV
L330	330 μH	PE–52627	RL1952	415–0926	77 458 BV
L470	470 μH	PE–53114	RL1951	415–0927	–
L680	680 μH	PE–52629	RL1950	415–0928	77 508 BV
H150	150 μH	PE–53115	RL2445	415–0936	77 368 BV
H220	220 μH	PE–53116	RL2446	430–0636	77 410 BV
H330	330 μH	PE–53117	RL2447	430–0635	77 460 BV
H470	470 μH	PE–53118	RL1961	430–0634	–
H680	680 μH	PE–53119	RL1960	415–0935	77 510 BV
H1000	1000 μH	PE–53120	RL1959	415–0934	77 558 BV
H1500	1500 μH	PE–53121	RL1958	415–0933	–
H2200	2200 μH	PE–53122	RL2448	415–0945	77 610 BV

Table 2. Inductor Selection Guide

Inductance	Current	Schott		Renco		Pulse Engineering		Coilcraft
(μH)	(A)	THT	SMT	THT	SMT	THT	SMT	SMT
68	0.32	67143940	67144310	RL–1284–68–43	RL1500–68	PE–53804	PE–53804–S	DO1608–68
	0.58	67143990	67144360	RL–5470–6	RL1500–68	PE–53812	PE–53812–S	DO3308–683
	0.99	67144070	67144450	RL–5471–5	RL1500–68	PE–53821	PE–53821–S	DO3316–683
	1.78	67144140	67144520	RL–5471–5	–	PE–53830	PE–53830–S	DO5022P–683
100	0.48	67143980	67144350	RL–5470–5	RL1500–100	PE–53811	PE–53811–S	DO3308–104
	0.82	67144060	67144440	RL–5471–4	RL1500–100	PE–53820	PE–53820–S	DO3316–104
	1.47	67144130	67144510	RL–5471–4	–	PE–53829	PE–53829–S	DO5022P–104
150	0.39	–	67144340	RL–5470–4	RL1500–150	PE–53810	PE–53810–S	DO3308–154
	0.66	67144050	67144430	RL–5471–3	RL1500–150	PE–53819	PE–53819–S	DO3316–154
	1.20	67144120	67144500	RL–5471–3	–	PE–53828	PE–53828–S	DO5022P–154
220	0.32	67143960	67144330	RL–5470–3	RL1500–220	PE–53809	PE–53809–S	DO3308–224
	0.55	67144040	67144420	RL–5471–2	RL1500–220	PE–53818	PE–53818–S	DO3316–224
	1.00	67144110	67144490	RL–5471–2	–	PE–53827	PE–53827–S	DO5022P–224
330	0.42	67144030	67144410	RL–5471–1	RL1500–330	PE–53817	PE–53817–S	DO3316–334
	0.80	67144100	67144480	RL–5471–1	–	PE–53826	PE–53826–S	DO5022P–334

NOTE: Table 1 and Table 2 of this Indicator Selection Guide shows some examples of different manufacturer products suitable for design with the LM2575.

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Table 3. Example of Several Inductor Manufacturers Phone/Fax Numbers

Pulse Engineering Inc.	Phone Fax	+ 1–619–674–8100 + 1–619–674–8262
Pulse Engineering Inc. Europe	Phone Fax	+ 353 93 24 107 + 353 93 24 459
Renco Electronics Inc.	Phone Fax	+ 1–516–645–5828 + 1–516–586–5562
AIE Magnetics	Phone Fax	+ 1–813–347–2181
Coilcraft Inc.	Phone Fax	+ 1–708–322–2645 + 1–708–639–1469
Coilcraft Inc., Europe	Phone Fax	+ 44 1236 730 595 + 44 1236 730 627
Tech 39	Phone Fax	+ 33 8425 2626 + 33 8425 2610
Schott Corp.	Phone Fax	+ 1–612–475–1173 + 1–612–475–1786

Table 4. Diode Selection Guide gives an overview about both surface–mount and through–hole diodes for an effective design. Device listed in bold are available from ON Semiconductor.

	Schottky				**Ultra–Fast Recovery**			
	1.0 A		**3.0 A**		**1.0 A**		**3.0 A**	
V_R	**SMT**	**THT**	**SMT**	**THT**	**SMT**	**THT**	**SMT**	**THT**
20 V	SK12	**1N5817** SR102	SK32 **MBRD320**	**1N5820** **MBR320** SR302				
30 V	**MBRS130LT3** SK13	**1N5818** SR103 11DQ03	SK33 **MBRD330**	**1N5821** **MBR330** SR303 31DQ03	**MURS120T3**	**MUR120** 11DF1 HER102	**MURS320T3**	
40 V	**MBRS140T3** SK14 10BQ040 10MQ040	**1N5819** SR104 11DQ04	**MBRS340T3** **MBRD340** 30WQ04 SK34	**1N5822** **MBR340** SR304 31DQ04	10BF10		**MURD320**	**MUR320** 30WF10 **MUR420**
50 V	**MBRS150** 10BQ050	**MBR150** SR105 11DQ05	**MBRD350** SK35 30WQ05	**MBR350** SR305 11DQ05			31DF1 HER302	

EXTERNAL COMPONENTS

Input Capacitor (C_{in})

The Input Capacitor Should Have a Low ESR

For stable operation of the switch mode converter a low ESR (Equivalent Series Resistance) aluminium or solid tantalum bypass capacitor is needed between the input pin and the ground pin to prevent large voltage transients from appearing at the input. It must be located near the regulator and use short leads. With most electrolytic capacitors, the capacitance value decreases and the ESR increases with lower temperatures. For reliable operation in temperatures below −25°C larger values of the input capacitor may be needed. Also paralleling a ceramic or solid tantalum capacitor will increase the regulator stability at cold temperatures.

RMS Current Rating of C_{in}

The important parameter of the input capacitor is the RMS current rating. Capacitors that are physically large and have large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating. The consequence of operating an electrolytic capacitor above the RMS current rating is a shortened operating life. In order to assure maximum capacitor operating lifetime, the capacitor's RMS ripple current rating should be:

$$I_{rms} > 1.2 \times d \times I_{Load}$$

where d is the duty cycle, for a buck regulator

$$d = \frac{t_{on}}{T} = \frac{V_{out}}{V_{in}}$$

and $d = \frac{t_{on}}{T} = \frac{|V_{out}|}{|V_{out}| + V_{in}}$ for a buck–boost regulator.

Output Capacitor (C_{out})

For low output ripple voltage and good stability, low ESR output capacitors are recommended. An output capacitor has two main functions: it filters the output and provides regulator loop stability. The ESR of the output capacitor and the peak−to−peak value of the inductor ripple current are the main factors contributing to the output ripple voltage value. Standard aluminium electrolytics could be adequate for some applications but for quality design low ESR types are recommended.

An aluminium electrolytic capacitor's ESR value is related to many factors such as the capacitance value, the voltage rating, the physical size and the type of construction. In most cases, the higher voltage electrolytic capacitors have lower ESR value. Often capacitors with much higher voltage ratings may be needed to provide low ESR values that are required for low output ripple voltage.

The Output Capacitor Requires an ESR Value That Has an Upper and Lower Limit

As mentioned above, a low ESR value is needed for low output ripple voltage, typically 1% to 2% of the output voltage. But if the selected capacitor's ESR is extremely low (below 0.05 Ω), there is a possibility of an unstable feedback loop, resulting in oscillation at the output. This situation can occur when a tantalum capacitor, that can have a very low ESR, is used as the only output capacitor.

At Low Temperatures, Put in Parallel Aluminium Electrolytic Capacitors with Tantalum Capacitors

Electrolytic capacitors are not recommended for temperatures below −25°C. The ESR rises dramatically at cold temperatures and typically rises 3 times at −25°C and as much as 10 times at −40°C. Solid tantalum capacitors have much better ESR spec at cold temperatures and are recommended for temperatures below −25°C. They can be also used in parallel with aluminium electrolytics. The value of the tantalum capacitor should be about 10% or 20% of the total capacitance. The output capacitor should have at least 50% higher RMS ripple current rating at 52 kHz than the peak−to−peak inductor ripple current.

Catch Diode

Locate the Catch Diode Close to the LM2575

The LM2575 is a step−down buck converter; it requires a fast diode to provide a return path for the inductor current when the switch turns off. This diode must be located close to the LM2575 using short leads and short printed circuit traces to avoid EMI problems.

Use a Schottky or a Soft Switching Ultra−Fast Recovery Diode

Since the rectifier diodes are very significant source of losses within switching power supplies, choosing the rectifier that best fits into the converter design is an important process. Schottky diodes provide the best performance because of their fast switching speed and low forward voltage drop.

They provide the best efficiency especially in low output voltage applications (5.0 V and lower). Another choice could be Fast−Recovery, or Ultra−Fast Recovery diodes. It has to be noted, that some types of these diodes with an abrupt turnoff characteristic may cause instability or EMI troubles.

A fast−recovery diode with soft recovery characteristics can better fulfill a quality, low noise design requirements. Table 4 provides a list of suitable diodes for the LM2575 regulator. Standard 50/60 Hz rectifier diodes such as the 1N4001 series or 1N5400 series are **NOT** suitable.

Inductor

The magnetic components are the cornerstone of all switching power supply designs. The style of the core and the winding technique used in the magnetic component's design has a great influence on the reliability of the overall power supply.

Using an improper or poorly designed inductor can cause high voltage spikes generated by the rate of transitions in current within the switching power supply, and the possibility of core saturation can arise during an abnormal operational mode. Voltage spikes can cause the semiconductors to enter avalanche breakdown and the part can instantly fail if enough energy is applied. It can also cause significant RFI (Radio Frequency Interference) and EMI (Electro−Magnetic Interference) problems.

Continuous and Discontinuous Mode of Operation

The LM2575 step−down converter can operate in both the continuous and the discontinuous modes of operation. The regulator works in the continuous mode when loads are relatively heavy, the current flows through the inductor continuously and never falls to zero. Under light load conditions, the circuit will be forced to the discontinuous mode when inductor current falls to zero for certain period of time (see Figure 22 and Figure 23). Each mode has distinctively different operating characteristics, which can affect the regulator performance and requirements. In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak currents in the switch, inductor and diode, and can have a lower output ripple voltage. On the other hand it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.

To simplify the inductor selection process, an inductor selection guide for the LM2575 regulator was added to this data sheet (Figures 17 through 21). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak−to−peak inductor ripple current to be a certain percentage of the maximum design load current. This percentage is allowed to change as different design load currents are selected. For light loads (less than approximately 200 mA) it may be desirable to operate the regulator in the discontinuous mode, because the inductor value and size can be kept relatively low. Consequently, the percentage of inductor peak−to−peak current increases. This discontinuous mode of operation is perfectly acceptable for this type of switching converter. Any buck regulator will be forced to enter discontinuous mode if the load current is light enough.

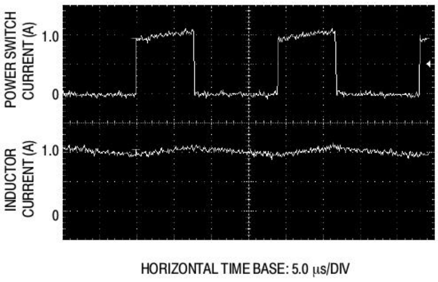

Figure 22. Continuous Mode Switching Current Waveforms

Selecting the Right Inductor Style

Some important considerations when selecting a core type are core material, cost, the output power of the power supply, the physical volume the inductor must fit within, and the amount of EMI (Electro−Magnetic Interference) shielding that the core must provide. The inductor selection guide covers different styles of inductors, such as pot core, E−core, toroid and bobbin core, as well as different core materials such as ferrites and powdered iron from different manufacturers.

For high quality design regulators the toroid core seems to be the best choice. Since the magnetic flux is completely contained within the core, it generates less EMI, reducing noise problems in sensitive circuits. The least expensive is the bobbin core type, which consists of wire wound on a ferrite rod core. This type of inductor generates more EMI due to the fact that its core is open, and the magnetic flux is not completely contained within the core.

When multiple switching regulators are located on the same printed circuit board, open core magnetics can cause interference between two or more of the regulator circuits, especially at high currents due to mutual coupling. A toroid, pot core or E−core (closed magnetic structure) should be used in such applications.

Do Not Operate an Inductor Beyond its Maximum Rated Current

Exceeding an inductor’s maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. Core saturation occurs when the flux density is too high and consequently the cross sectional area of the core can no longer support additional lines of magnetic flux.

This causes the permeability of the core to drop, the inductance value decreases rapidly and the inductor begins to look mainly resistive. It has only the dc resistance of the winding. This can cause the switch current to rise very rapidly and force the LM2575 internal switch into cycle−by−cycle current limit, thus reducing the dc output load current. This can also result in overheating of the inductor and/or the LM2575. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.

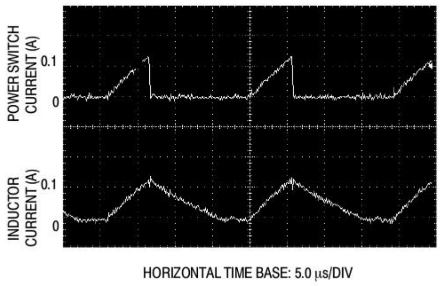

Figure 23. Discontinuous Mode Switching Current Waveforms

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GENERAL RECOMMENDATIONS

Output Voltage Ripple and Transients

Source of the Output Ripple

Since the LM2575 is a switch mode power supply regulator, its output voltage, if left unfiltered, will contain a sawtooth ripple voltage at the switching frequency. The output ripple voltage value ranges from 0.5% to 3% of the output voltage. It is caused mainly by the inductor sawtooth ripple current multiplied by the ESR of the output capacitor.

Short Voltage Spikes and How to Reduce Them

The regulator output voltage may also contain short voltage spikes at the peaks of the sawtooth waveform (see Figure 24). These voltage spikes are present because of the fast switching action of the output switch, and the parasitic inductance of the output filter capacitor. There are some other important factors such as wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all these contribute to the amplitude of these spikes. To minimize these voltage spikes, low inductance capacitors should be used, and their lead lengths must be kept short. The importance of quality printed circuit board layout design should also be highlighted.

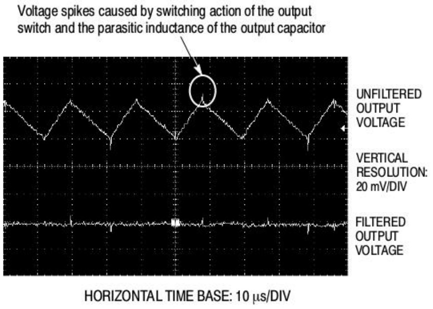


Figure 24. Output Ripple Voltage Waveforms

Minimizing the Output Ripple

In order to minimize the output ripple voltage it is possible to enlarge the inductance value of the inductor L1 and/or to use a larger value output capacitor. There is also another way to smooth the output by means of an additional LC filter (20 μH, 100 μF), that can be added to the output (see Figure 33) to further reduce the amount of output ripple and transients. With such a filter it is possible to reduce the output ripple voltage transients 10 times or more. Figure 24 shows the difference between filtered and unfiltered output waveforms of the regulator shown in Figure 33.

The upper waveform is from the normal unfiltered output of the converter, while the lower waveform shows the output ripple voltage filtered by an additional LC filter.

Heatsinking and Thermal Considerations

The Through−Hole Package TO−220

The LM2575 is available in two packages, a 5−pin TO−220(T, TV) and a 5−pin surface mount D^2PAK(D2T). There are many applications that require no heatsink to keep the LM2575 junction temperature within the allowed operating range. The TO−220 package can be used without a heatsink for ambient temperatures up to approximately 50°C (depending on the output voltage and load current). Higher ambient temperatures require some heatsinking, either to the printed circuit (PC) board or an external heatsink.

The Surface Mount Package D^2PAK and its Heatsinking

The other type of package, the surface mount D^2PAK, is designed to be soldered to the copper on the PC board. The copper and the board are the heatsink for this package and the other heat producing components, such as the catch diode and inductor. The PC board copper area that the package is soldered to should be at least 0.4 in^2 (or 100 mm^2) and ideally should have 2 or more square inches (1300 mm^2) of 0.0028 inch copper. Additional increasing of copper area beyond approximately 3.0 in^2 (2000 mm^2) will not improve heat dissipation significantly. If further thermal improvements are needed, double sided or multilayer PC boards with large copper areas should be considered.

Thermal Analysis and Design

The following procedure must be performed to determine whether or not a heatsink will be required. First determine:

1. $P_{D(max)}$ maximum regulator power dissipation in the application.
2. $T_{A(max)}$ maximum ambient temperature in the application.
3. $T_{J(max)}$ maximum allowed junction temperature (125°C for the LM2575). For a conservative design, the maximum junction temperature should not exceed 110°C to assure safe operation. For every additional 10°C temperature rise that the junction must withstand, the estimated operating lifetime of the component is halved.
4. $R_{\theta JC}$ package thermal resistance junction−case.
5. $R_{\theta JA}$ package thermal resistance junction−ambient.

(Refer to Absolute Maximum Ratings in this data sheet or $R_{\theta JC}$ and $R_{\theta JA}$ values).

The following formula is to calculate the total power dissipated by the LM2575:

$$P_D = (V_{in} \times I_Q) + d \times I_{Load} \times V_{sat}$$

where d is the duty cycle and for buck converter

$$d = \frac{t_{on}}{T} = \frac{V_O}{V_{in}},$$

I_Q (quiescent current) and V_{sat} can be found in the LM2575 data sheet,
V_{in} is minimum input voltage applied,
V_O is the regulator output voltage,
I_{Load} is the load current.

The dynamic switching losses during turn−on and turn−off can be neglected if proper type catch diode is used.

Packages Not on a Heatsink (Free−Standing)

For a free−standing application when no heatsink is used, the junction temperature can be determined by the following expression:

$$T_J = (R_{\theta JA})\,(P_D) + T_A$$

where $(R_{\theta JA})(P_D)$ represents the junction temperature rise caused by the dissipated power and T_A is the maximum ambient temperature.

Packages on a Heatsink

If the actual operating junction temperature is greater than the selected safe operating junction temperature determined in step 3, than a heatsink is required. The junction temperature will be calculated as follows:

$$T_J = P_D\,(R_{\theta JA} + R_{\theta CS} + R_{\theta SA}) + T_A$$

where $R_{\theta JC}$ is the thermal resistance junction−case,
$R_{\theta CS}$ is the thermal resistance case−heatsink,
$R_{\theta SA}$ is the thermal resistance heatsink−ambient.

If the actual operating temperature is greater than the selected safe operating junction temperature, then a larger heatsink is required.

Some Aspects That can Influence Thermal Design

It should be noted that the package thermal resistance and the junction temperature rise numbers are all approximate, and there are many factors that will affect these numbers, such as PC board size, shape, thickness, physical position, location, board temperature, as well as whether the surrounding air is moving or still.

Other factors are trace width, total printed circuit copper area, copper thickness, single− or double−sided, multilayer board, the amount of solder on the board or even color of the traces.

The size, quantity and spacing of other components on the board can also influence its effectiveness to dissipate the heat.

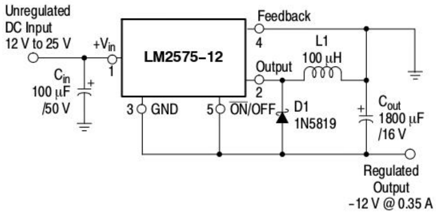


Figure 25. Inverting Buck−Boost Regulator Using the LM2575−12 Develops −12 V @ 0.35 A

ADDITIONAL APPLICATIONS

Inverting Regulator

An inverting buck−boost regulator using the LM2575−12 is shown in Figure 25. This circuit converts a positive input voltage to a negative output voltage with a common ground by bootstrapping the regulators ground to the negative output voltage. By grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.

In this example the LM2575−12 is used to generate a −12 V output. The maximum input voltage in this case cannot exceed +28 V because the maximum voltage appearing across the regulator is the absolute sum of the input and output voltages and this must be limited to a maximum of 40 V.

This circuit configuration is able to deliver approximately 0.35 A to the output when the input voltage is 12 V or higher. At lighter loads the minimum input voltage required drops to approximately 4.7 V, because the buck−boost regulator topology can produce an output voltage that, in its absolute value, is either greater or less than the input voltage.

Since the switch currents in this buck−boost configuration are higher than in the standard buck converter topology, the available output current is lower.

This type of buck−boost inverting regulator can also require a larger amount of startup input current, even for light loads. This may overload an input power source with a current limit less than 1.5 A.

Such an amount of input startup current is needed for at least 2.0 ms or more. The actual time depends on the output voltage and size of the output capacitor.

Because of the relatively high startup currents required by this inverting regulator topology, the use of a delayed startup or an undervoltage lockout circuit is recommended.

Using a delayed startup arrangement, the input capacitor can charge up to a higher voltage before the switch−mode regulator begins to operate.

The high input current needed for startup is now partially supplied by the input capacitor C_{in}.

Design Recommendations:

The inverting regulator operates in a different manner than the buck converter and so a different design procedure has to be used to select the inductor L1 or the output capacitor C_{out}.

The output capacitor values must be larger than is normally required for buck converter designs. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of μF).

The recommended range of inductor values for the inverting converter design is between 68 μH and 220 μH. To select an inductor with an appropriate current rating, the inductor peak current has to be calculated.

The following formula is used to obtain the peak inductor current:

$$I_{peak} \approx \frac{I_{Load}(V_{in} + |V_O|)}{V_{in}} + \frac{V_{in} \times t_{on}}{2L_1}$$

$$\text{where } t_{on} = \frac{|V_O|}{V_{in} + |V_O|} \times \frac{1}{f_{osc}}, \text{ and } f_{osc} = 52\text{ kHz.}$$

Under normal continuous inductor current operating conditions, the worst case occurs when V_{in} is minimal.

Note that the voltage appearing across the regulator is the absolute sum of the input and output voltage, and must not exceed 40 V.

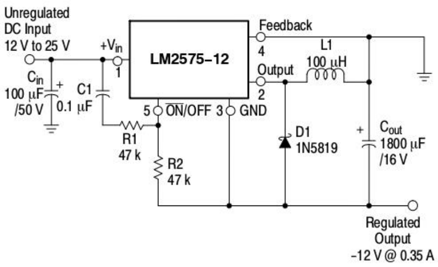
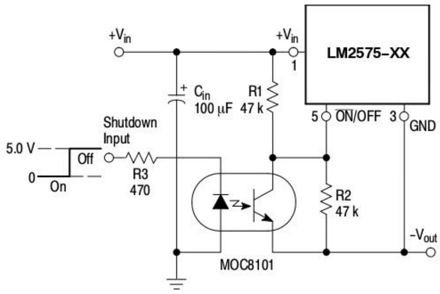


Figure 26. Inverting Buck−Boost Regulator with Delayed Startup

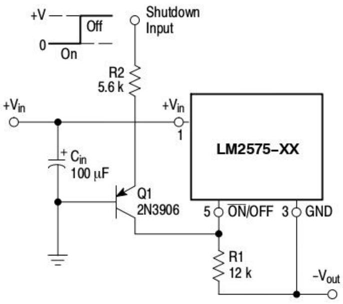
It has been already mentioned above, that in some situations, the delayed startup or the undervoltage lockout features could be very useful. A delayed startup circuit applied to a buck−boost converter is shown in Figure 26. Figure 32 in the “Undervoltage Lockout” section describes an undervoltage lockout feature for the same converter topology.



NOTE: This picture does not show the complete circuit.

Figure 27. Inverting Buck−Boost Regulator Shut Down Circuit Using an Optocoupler

With the inverting configuration, the use of the $\overline{\text{ON}}$/OFF pin requires some level shifting techniques. This is caused by the fact, that the ground pin of the converter IC is no longer at ground. Now, the $\overline{\text{ON}}$/OFF pin threshold voltage (1.4 V approximately) has to be related to the negative output voltage level. There are many different possible shut down methods, two of them are shown in Figures 27 and 28.



NOTE: This picture does not show the complete circuit.

Figure 28. Inverting Buck−Boost Regulator Shut Down Circuit Using a PNP Transistor

Negative Boost Regulator

This example is a variation of the buck−boost topology and is called a negative boost regulator. This regulator experiences relatively high switch current, especially at low input voltages. The internal switch current limiting results in lower output load current capability.

The circuit in Figure 29 shows the negative boost configuration. The input voltage in this application ranges from −5.0 V to −12 V and provides a regulated −12 V output.

LM2575, NCV2575

If the input voltage is greater than −12 V, the output will rise above −12 V accordingly, but will not damage the regulator.

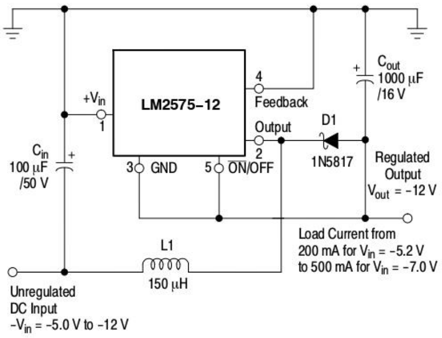


Figure 29. Negative Boost Regulator

Design Recommendations:

The same design rules as for the previous inverting buck−boost converter can be applied. The output capacitor C_{out} must be chosen larger than would be required for a standard buck converter. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of μF). The recommended range of inductor values for the negative boost regulator is the same as for inverting converter design.

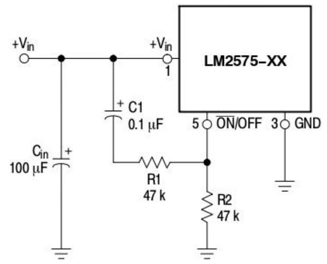
Another important point is that these negative boost converters cannot provide current limiting load protection in the event of a short in the output so some other means, such as a fuse, may be necessary to provide the load protection.

Delayed Startup

There are some applications, like the inverting regulator already mentioned above, which require a higher amount of startup current. In such cases, if the input power source is limited, this delayed startup feature becomes very useful.

To provide a time delay between the time the input voltage is applied and the time when the output voltage comes up, the circuit in Figure 30 can be used. As the input voltage is applied, the capacitor C1 charges up, and the voltage across the resistor R2 falls down. When the voltage on the $\overline{\text{ON}}$/OFF pin falls below the threshold value 1.4 V, the regulator starts up. Resistor R1 is included to limit the maximum voltage applied to the $\overline{\text{ON}}$/OFF pin, reduces the power supply noise sensitivity, and also limits the capacitor C1 discharge current, but its use is not mandatory.

When a high 50 Hz or 60 Hz (100 Hz or 120 Hz respectively) ripple voltage exists, a long delay time can cause some problems by coupling the ripple into the $\overline{\text{ON}}$/OFF pin, the regulator could be switched periodically on and off with the line (or double) frequency.



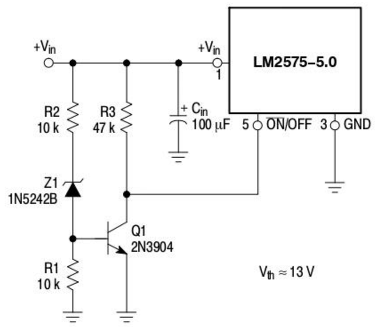
NOTE: This picture does not show the complete circuit.

Figure 30. Delayed Startup Circuitry

Undervoltage Lockout

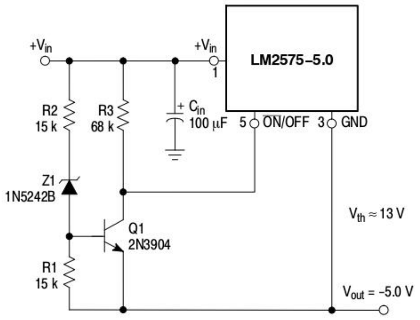
Some applications require the regulator to remain off until the input voltage reaches a certain threshold level. Figure 31 shows an undervoltage lockout circuit applied to a buck regulator. A version of this circuit for buck−boost converter is shown in Figure 32. Resistor R3 pulls the $\overline{\text{ON}}$/OFF pin high and keeps the regulator off until the input voltage reaches a predetermined threshold level, which is determined by the following expression:

$$V_{th} \approx V_{Z1} + \left(1 + \frac{R2}{R1}\right) V_{BE}\ (Q1)$$



NOTE: This picture does not show the complete circuit.

Figure 31. Undervoltage Lockout Circuit for Buck Converter



NOTE: This picture does not show the complete circuit.

Figure 32. Undervoltage Lockout Circuit for Buck−Boost Converter

Adjustable Output, Low−Ripple Power Supply

A 1.0 A output current capability power supply that features an adjustable output voltage is shown in Figure 33.

This regulator delivers 1.0 A into 1.2 V to 35 V output. The input voltage ranges from roughly 8.0 V to 40 V. In order to achieve a 10 or more times reduction of output ripple, an additional L−C filter is included in this circuit.

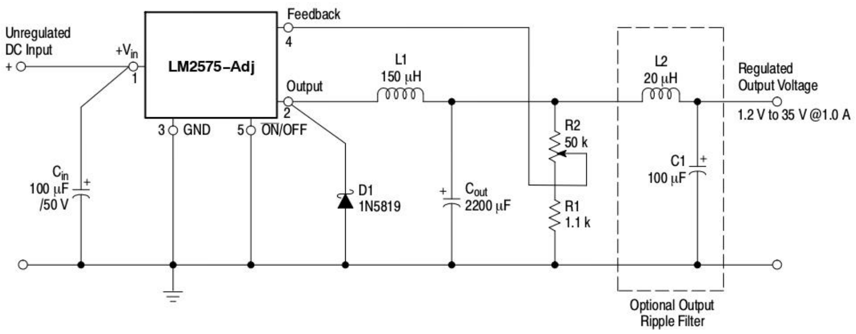


Figure 33. Adjustable Power Supply with Low Ripple Voltage

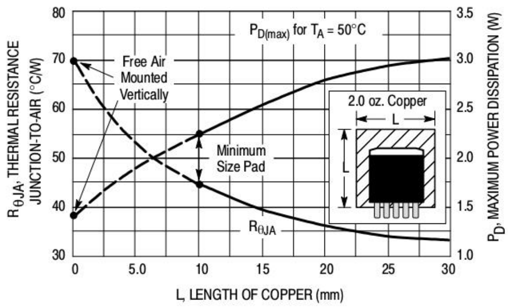
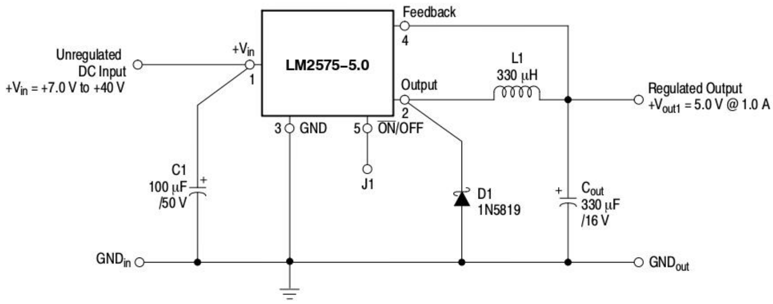


Figure 34. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

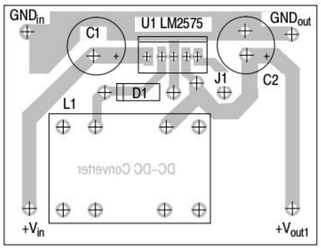
LM2575, NCV2575

THE LM2575−5.0 STEP−DOWN VOLTAGE REGULATOR WITH 5.0 V @ 1.0 A OUTPUT POWER CAPABILITY. TYPICAL APPLICATION WITH THROUGH−HOLE PC BOARD LAYOUT



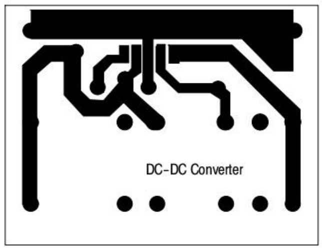
C1 – 100 μF, 50 V, Aluminium Electrolytic
C2 – 330 μF, 16 V, Aluminium Electrolytic
D1 – 1.0 A, 40 V, Schottky Rectifier, 1N5819
L1 – 330 μH, Tech 39: 77 458 BV, Toroid Core, Through−Hole, Pin 3 = Start, Pin 7 = Finish

Figure 35. Schematic Diagram of the LM2575−5.0 Step−Down Converter



NOTE: Not to scale.

Figure 36. Printed Circuit Board Component Side



NOTE: Not to scale.

Figure 37. Printed Circuit Board Copper Side

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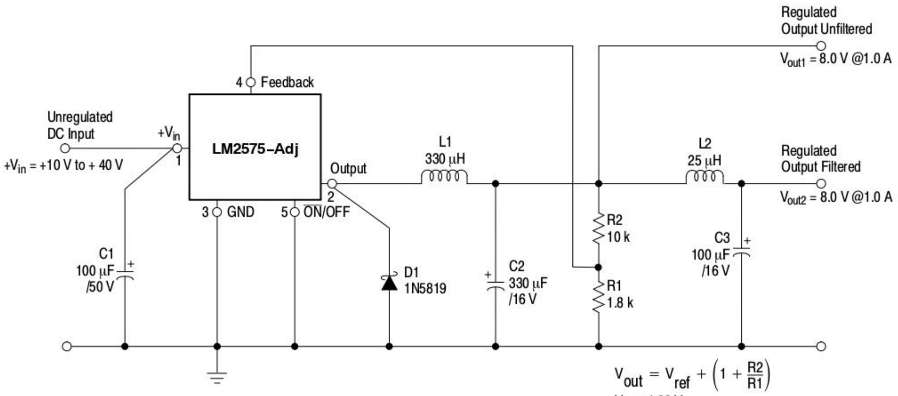
LM2575, NCV2575

THE LM2575–ADJ STEP–DOWN VOLTAGE REGULATOR WITH 8.0 V @ 1.0 A OUTPUT POWER CAPABILITY. TYPICAL APPLICATION WITH THROUGH–HOLE PC BOARD LAYOUT

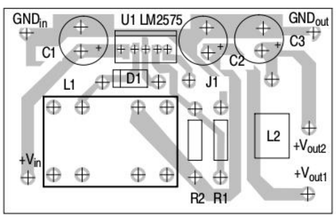


$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right)$$

V_{ref} = 1.23 V
R1 is between 1.0 k and 5.0 k

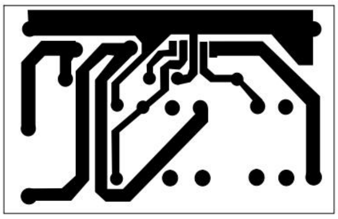
C1 – 100 µF, 50 V, Aluminium Electrolytic
C2 – 330 µF, 16 V, Aluminium Electrolytic
C3 – 100 µF, 16 V, Aluminium Electrolytic
D1 – 1.0 A, 40 V, Schottky Rectifier, 1N5819
L1 – 330 µH, Tech 39: 77 458 BV, Toroid Core, Through–Hole, Pin 3 = Start, Pin 7 = Finish
L2 – 25 µH, TDK: SFT52501, Toroid Core, Through–Hole
R1 – 1.8 k
R2 – 10 k

Figure 38. Schematic Diagram of the 8.0 V @ 1.0 V Step–Down Converter Using the LM2575–Adj
(An additional LC filter is included to achieve low output ripple voltage)



NOTE: Not to scale.

Figure 39. PC Board Component Side



NOTE: Not to scale.

Figure 40. PC Board Copper Side

References

- National Semiconductor LM2575 Data Sheet and Application Note
- National Semiconductor LM2595 Data Sheet and Application Note
- Marty Brown “Practical Switching Power Supply Design”, Academic Press, Inc., San Diego 1990
- Ray Ridley “High Frequency Magnetics Design”, Ridley Engineering, Inc. 1995

LM2575, NCV2575

ORDERING INFORMATION

Device	Nominal Output Voltage	Operating Temperature Range	Package	Shipping†
LM2575TV−ADJG	1.23 V to 37 V	T_J = −40° to +125°C	TO−220 (Vertical Mount) (Pb−Free)	50 Units/Rail
LM2575T−ADJG			TO−220 (Straight Lead) (Pb−Free)	
LM2575D2T−ADJG			D^2PAK (Surface Mount) (Pb−Free)	
LM2575D2T−ADJR4G			D^2PAK (Surface Mount) (Pb−Free)	800 Tape & Reel
NCV2575D2T−ADJG			D^2PAK (Surface Mount) (Pb−Free)	50 Units/Rail
NCV2575D2T−ADJR4G			D^2PAK (Surface Mount) (Pb−Free)	800 Tape & Reel
LM2575TV−3.3G	3.3 V	T_J = −40° to +125°C	TO−220 (Vertical Mount) (Pb−Free)	50 Units/Rail
LM2575T−3.3G			TO−220 (Straight Lead) (Pb−Free)	
LM2575D2T−3.3G			D^2PAK (Surface Mount) (Pb−Free)	
LM2575D2T−3.3R4G			D^2PAK (Surface Mount) (Pb−Free)	800 Tape & Reel
LM2575TV−5G	5.0 V	T_J = −40° to +125°C	TO−220 (Vertical Mount) (Pb−Free)	50 Units/Rail
LM2575T−5G			TO−220 (Straight Lead) (Pb−Free)	
LM2575D2T−5G			D^2PAK (Surface Mount) (Pb−Free)	
LM2575D2T−5R4G			D^2PAK (Surface Mount) (Pb−Free)	800 Tape & Reel
NCV2575D2T−5G			D^2PAK (Surface Mount) (Pb−Free)	50 Units/Rail
NCV2575D2T−5R4G			D^2PAK (Surface Mount) (Pb−Free)	800 Tape & Reel
LM2575TV−012G	12 V	T_J = −40° to +125°C	TO−220 (Vertical Mount) (Pb−Free)	50 Units/Rail
LM2575T−012G			TO−220 (Straight Lead) (Pb−Free)	
LM2575D2T−012G			D^2PAK (Surface Mount) (Pb−Free)	
LM2575D2T−12R4G			D^2PAK (Surface Mount) (Pb−Free)	800 Tape & Reel
NCV2575D2T−12G			D^2PAK (Surface Mount) (Pb−Free)	50 Units/Rail
NCV2575D2T−12R4G			D^2PAK (Surface Mount) (Pb−Free)	800 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

LM2575, NCV2575

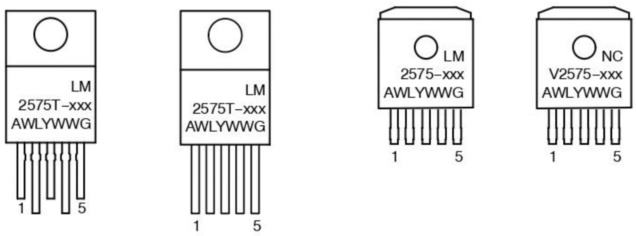
ORDERING INFORMATION

Device	Nominal Output Voltage	Operating Temperature Range	Package	Shipping†
LM2575TV−015G	15 V	T_J = −40° to +125°C	TO−220 (Vertical Mount) (Pb−Free)	50 Units/Rail
LM2575T−015G			TO−220 (Straight Lead) (Pb−Free)	
LM2575D2T−015G			D^2PAK (Surface Mount) (Pb−Free)	
LM2575D2T−15R4G			D^2PAK (Surface Mount) (Pb−Free)	800 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

TO−220 TV SUFFIX CASE 314B | TO−220 T SUFFIX CASE 314D | D^2PAK D2T SUFFIX CASE 936A | D^2PAK D2T SUFFIX CASE 936A

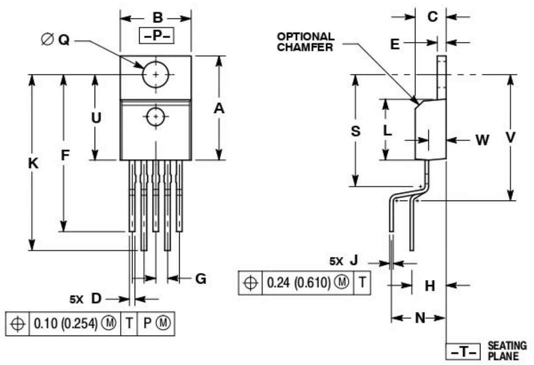


xxx = 3.3, 5.0, 12, 15, or ADJ
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

LM2575, NCV2575

PACKAGE DIMENSIONS

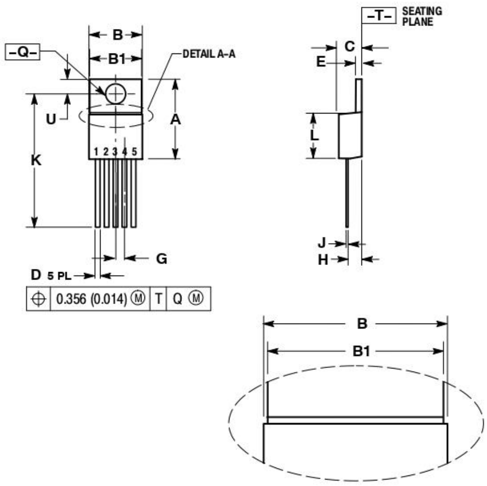
TO−220
TV SUFFIX
CASE 314B−05
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
F	0.850	0.935	21.590	23.749
G	0.067 BSC		1.702 BSC	
H	0.166 BSC		4.216 BSC	
J	0.015	0.025	0.381	0.635
K	0.900	1.100	22.860	27.940
L	0.320	0.365	8.128	9.271
N	0.320 BSC		8.128 BSC	
Q	0.140	0.153	3.556	3.886
S	---	0.620	---	15.748
U	0.468	0.505	11.888	12.827
V	---	0.735	---	18.669
W	0.090	0.110	2.286	2.794

TO−220
T SUFFIX
CASE 314D−04
ISSUE F



DETAIL A−A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
B1	0.375	0.415	9.525	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
G	0.067 BSC		1.702 BSC	
H	0.087	0.112	2.210	2.845
J	0.015	0.025	0.381	0.635
K	0.977	1.045	24.810	26.543
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
U	0.105	0.117	2.667	2.972

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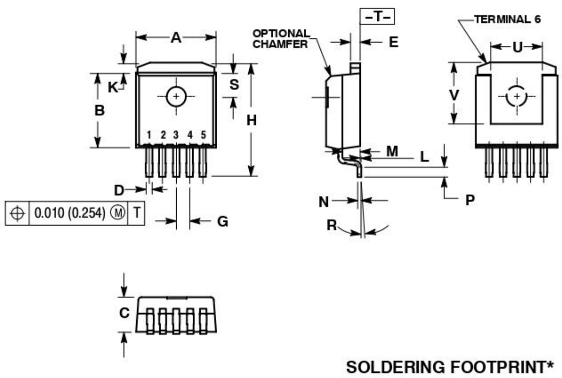
LM2575, NCV2575

PACKAGE DIMENSIONS

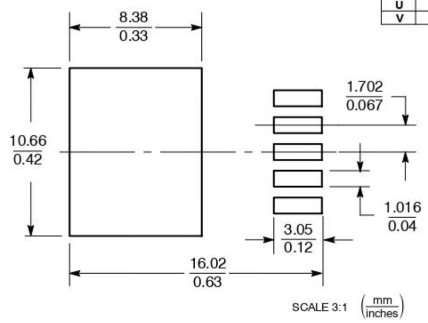
D²PAK
D2T SUFFIX
CASE 936A−02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

LM2575/D

Anexo 1.2: TS924IN

TS924, TS924A

life.augmented

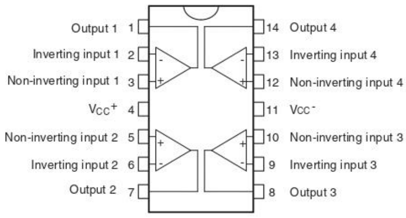
Rail-to-rail output current quad operational amplifier

Datasheet - production data

D
SO14
(plastic micropackage)

P
TSSOP14
(thin shrink small outline package)

Pin connections (top view)



Features

- Rail-to-rail input and output
- Low noise: 9 nV/√Hz
- Low distortion
- High output current: 80 mA (able to drive 32 Ω loads)
- High-speed: 4 MHz, 1.3 V/μs
- Operating range from 2.7 V to 12 V
- Low input offset voltage: 900 μV max. (TS924A)
- ESD internal protection: 3 kV
- Latch-up immunity
- Macromodel included in this specification

Related products

- See the TS921 device for the single version and the TS922 device for the dual version
- See the TSX56x series for smaller packages

Applications

- Headphone amplifiers
- Piezoelectric speaker drivers
- Sound cards
- MPEG boards, multimedia systems
- Line drivers, buffers
- Cordless telephones and portable communication equipment
- Instrumentation with low noise as key factor

Description

The TS924 and TS924A devices are rail-to-rail quad BiCMOS operational amplifiers optimized and fully specified for 3 V and 5 V operation.

High output current allows low load impedances to be driven.

The TS924 and TS924A devices exhibit a very low noise, low distortion, low offset, and high output current capability, making these devices an excellent choice for high-quality, low-voltage, and battery-operated audio systems.

The devices are stable for capacitive loads up to 500 pF.

Contents

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	14	V
V_{id}	Differential input voltage(2)	±1	
V_{in}	Input voltage(3)	V_{CC-} -0.3 to V_{CC+} +0.3	
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	
R_{thja}	Thermal resistance junction-to-ambient(4) SO14 TSSOP14	 66 100	°C/W
ESD	HBM: human body model(5)	3	kV
	MM: machine model(6)	100	V
	CDM: charged device model(7) SO14 TSSOP14	 1.5 1	kV
	Output short-circuit duration	See footnote(8)	
	Latch-up immunity	200	mA
	Soldering temperature (10 sec.), leaded version	250	°C
	Soldering temperature (10 sec.), unleaded version	260	

1. All voltage values, except the differential voltage, are with respect to network ground terminal.
2. The differential voltage is the non-inverting input terminal with respect to the inverting input terminal. If V_{id} > ±1 V, the maximum input current must not exceed ±1 mA. In this case (V_{id} > ±1 V), an input series resistor must be added to limit input current.
3. Do not exceed 14 V.
4. Short-circuits can cause excessive heating and destructive dissipation. R_{th} are typical values.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to ground through only one pin. This is done for all pins.
8. There is no short-circuit protection inside the device: short-circuits from the output to V_{CC} can cause excessive heating. The maximum output current is approximately 80 mA, independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 12	V
V_{icm}	Common mode input voltage range	V_{CC-} -0.2 to V_{CC+} +0.2	
T_{oper}	Operating free air temperature range	-40 to +125	°C

2 Electrical characteristics

Table 3. Electrical characteristics at V_{CC+} = +3 V with V_{CC-} = 0 V, $V_{icm} = V_{CC+}/2$, T_{amb} = 25 °C, and R_L connected to $V_{CC+}/2$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
DC performance					
V_{io}	Input offset voltage TS924 TS924A $T_{min} \le T_{amb} \le T_{max}$ TS924 TS924A			 3 0.9 5 1.8	mV
DV_{io}	Input offset voltage drift		2		µV/°C
I_{io}	Input offset current - $T_{min} \le T_{amb} \le T_{max}$		1	30	nA
I_{ib}	Input bias current - $T_{min} \le T_{amb} \le T_{max}$		15	100	nA
CMR	V_{icm} from 0 to 3 V $T_{min} \le T_{amb} \le T_{max}$	60 56	80		dB
SVR	Supply voltage rejection ratio - V_{CC+} = 2.7 to 3.3 V $T_{min} \le T_{amb} \le T_{max}$	60 60	85		dB
A_{vd}	Large signal voltage gain (V_{out} = 2 V_{pk-pk}) R_L = 10 kΩ, $T_{min} \le T_{amb} \le T_{max}$ R_L = 600 Ω, $T_{min} \le T_{amb} \le T_{max}$ R_L = 32 Ω	 70 15	 200 35 16		V/mV
V_{OH}	High level output voltage R_L = 10 kΩ, $T_{min} \le T_{amb} \le T_{max}$ R_L = 600 Ω, $T_{min} \le T_{amb} \le T_{max}$ R_L = 32 Ω	 2.90 2.87	 2.63		V
V_{OL}	Low level output voltage R_L = 10 kΩ, $T_{min} \le T_{amb} \le T_{max}$ R_L = 600 Ω, $T_{min} \le T_{amb} \le T_{max}$ R_L = 32 Ω		 180	 50 100	mV
I_o	Output short-circuit current	50	80		mA
I_{CC}	Supply current /operator - no load, $V_{out} = V_{CC+}/2$ $T_{min} \le T_{amb} \le T_{max}$		1	1.5 1.6	mA
AC performance					
GBP	Gain bandwidth product - R_L = 600 Ω		4		MHz
ϕm	Phase margin at unit gain - R_L = 600 Ω, C_L =100 pF		68		Degrees
G_m	Gain margin - R_L = 600 Ω, C_L =100 pF		12		dB
SR	Slew rate	0.7	1.3		V/µs
e_n	Equivalent input noise voltage - f = 1 kHz		9		$\frac{nV}{\sqrt{Hz}}$

Table 3. Electrical characteristics at V_{CC+} = +3 V with V_{CC-} = 0 V, V_{icm} = $V_{CC+}/2$, T_{amb} = 25 °C, and R_L connected to $V_{CC+}/2$ (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
THD	Total harmonic distortion V_{out} = 2 V_{pk-pk}, F = 1 kHz, A_v = 1, R_L = 600 Ω		0.005		%
C_s	Channel separation		120		dB

Table 4. V_{CC+} = +5 V, V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T_{amb} = 25 °C, R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
DC performance					
V_{io}	Input offset voltage TS924 TS924A $T_{min} \leq T_{amb} \leq T_{max}$ TS924 TS924A			 3 0.9 5 1.8	mV
DV_{io}	Input offset voltage drift		2		µV/°C
I_{io}	Input offset current - $T_{min} \leq T_{amb} \leq T_{max}$		1	30	nA
I_{ib}	Input bias current - $T_{min} \leq T_{amb} \leq T_{max}$		15	100	
CMR	V_{icm} from 0 to 5 V $T_{min} \leq T_{amb} \leq T_{max}$	60 56	80		dB
SVR	Supply voltage rejection ratio - V_{CC+} = 3 V to 5 V $T_{min} \leq T_{amb} \leq T_{max}$	60 60	85		
A_{vd}	Large signal voltage gain (V_{out} = $2V_{pk-pk}$) R_L= 10 kΩ, $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 600 Ω, $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 32 Ω	 70 20	 200 40 17		V/mV
V_{OH}	High level output voltage R_L= 10 kΩ, $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 600 Ω, $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 32 Ω	 4.90 4.85	 4.4		V
V_{OL}	Low level output voltage R_L= 10 kΩ, $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 600 Ω, $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 32 Ω		 300	 50 120	mV
I_o	Output short-circuit current	50	80		mA
I_{CC}	Supply current / operator - no load, V_{out} = $V_{CC+}/2$ $T_{min} \leq T_{amb} \leq T_{max}$		1	1.5 1.6	
AC performance					
GBP	Gain bandwidth product - R_L = 600 Ω		4		MHz
φm	Phase margin at unit gain - R_L = 600 Ω, C_L =100 pF		68		Degrees
G_m	Gain margin -R_L = 600 Ω, C_L =100 pF		12		dB
SR	Slew rate	0.7	1.3		V/µs
e_n	Equivalent input noise voltage - f = 1 kHz		9		$\frac{nV}{\sqrt{Hz}}$
THD	Total harmonic distortion V_{out} = 2 V_{pk-pk}, F = 1 kHz, A_v = 1, R_L = 600 Ω		0.005		%
C_s	Channel separation		120		dB

Figure 1. Output short-circuit current vs. output voltage (V_{CC} = 0/12 V)

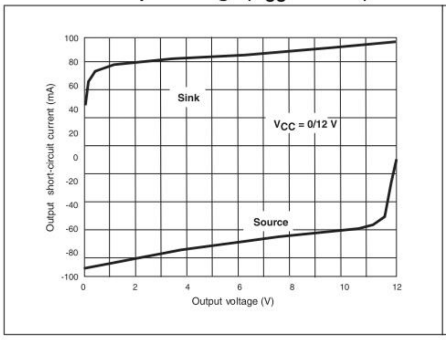


Figure 2. Output short-circuit current vs. output voltage (V_{CC} = 0/3 V)

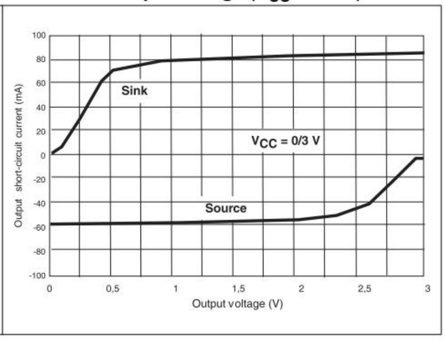


Figure 3. Voltage gain and phase vs. frequency (C_L = 500 pF, V_{CC} = ±1.5 V)

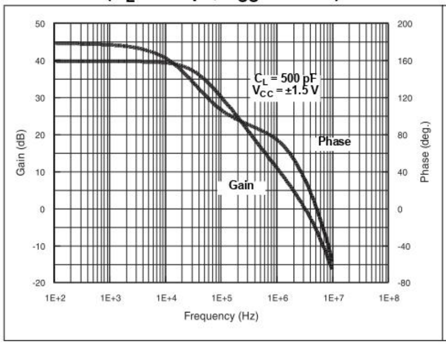


Figure 4. Output short-circuit current vs. output voltage (V_{CC} = 0/5 V)

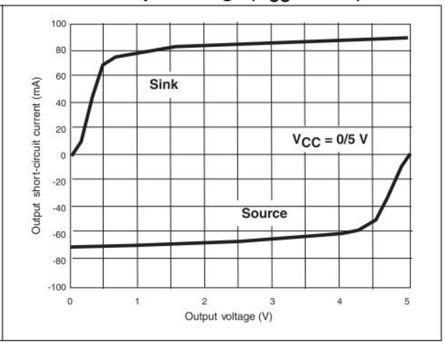


Figure 5. Voltage gain and phase vs. frequency (R_L = 10 kΩ, C_L = 100 pF, V_{CC} = ±1.5 V)

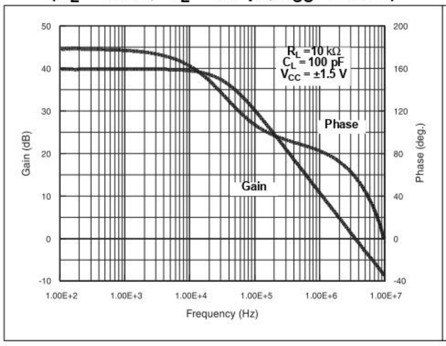


Figure 6. THD + noise vs. frequency (R_L = 2 kΩ, V_O = 10 Vpp, V_{CC} = ±6 V, A_v = -1)

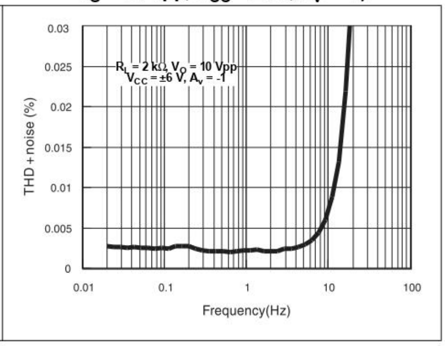


Figure 7. THD + noise vs. frequency (R_L = 2 kΩ, V_O = 10 Vpp, V_{CC} = ±6 V, A_v = 1)

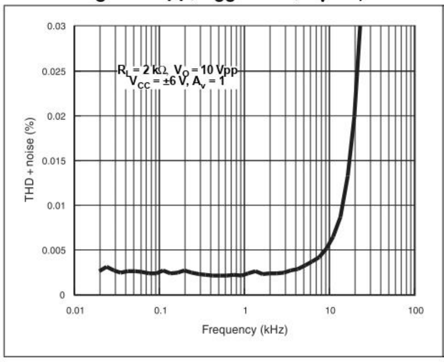


Figure 8. THD + noise vs. frequency (R_L = 32 Ω, V_O = 2 Vpp, V_{CC} = ±1.5 V, A_v = 10)

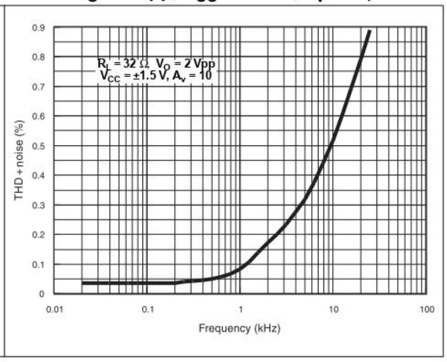


Figure 9. THD + noise vs. V_{out} (R_L = 32 Ω, f = 1 kHz, V_{CC} = ±1.5 V, A_v = -1)

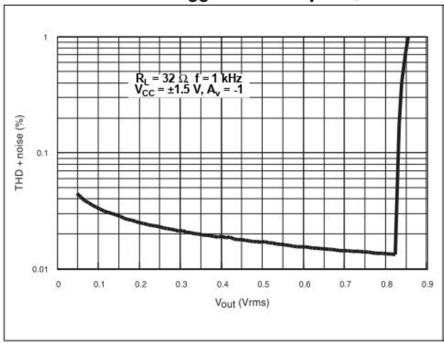


Figure 10. THD + noise vs. frequency (R_L = 32 Ω, V_O = 4 Vpp, V_{CC} = ±2.5 V, A_v = 1)

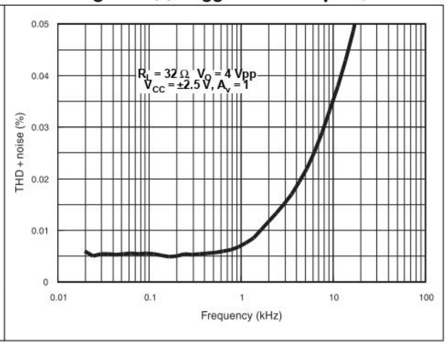


Figure 11. THD + noise vs. V_{out} (R_L = 600 Ω, f = 1 kHz, V_{CC} = ±1.5 V , A_v = -1)

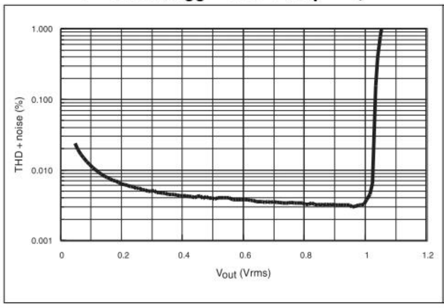


Figure 12. THD + noise vs. V_{out} (R_L = 2 kΩ, f = 1 kHz, V_{CC} = ±1.5 V, A_v = -1)

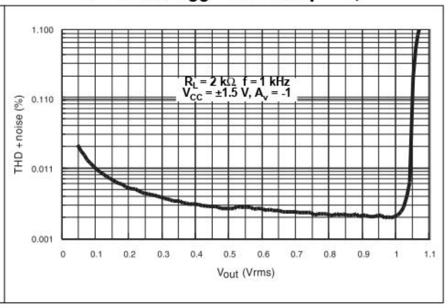
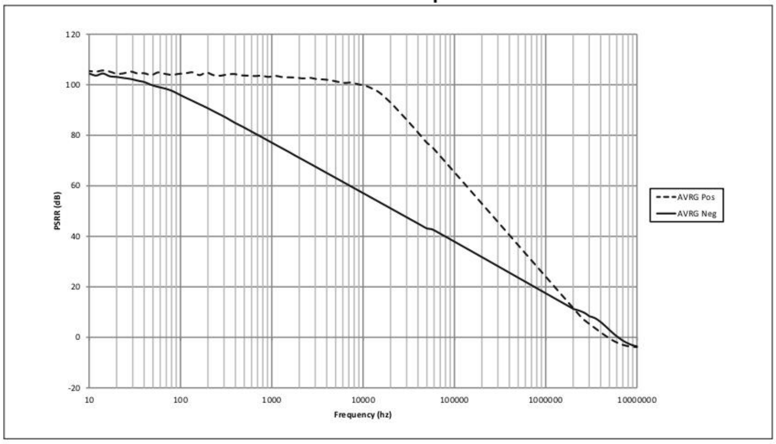


Figure 13. PSRR for TS924/TS924A at V_{CC} = 5 V, V_{icm} = 2.5 V, T = 25 °C, Rl = 100 kΩ, and Cl = 100pF



3 Macromodel

3.1 Important note concerning this macromodel

Note the following remarks before using this macromodel:

- All models are a trade-off between accuracy and complexity (that is, simulation time).
- Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.
- A macromodel emulates the **nominal** performance of a **typical** device within **specified operating conditions** (for example, temperature, supply voltage). Thus, the macromodel is often not as exhaustive as the datasheet, its purpose is to illustrate the main parameters of the product.

Data derived from macromodels used outside of the specified conditions (such as V_{CC} and temperature) or worse, outside of the device operating conditions (such as V_{CC} and V_{icm}), are not reliable in any way.

Section 3.2 presents the electrical characteristics resulting from the use of these macromodels.

3.2 Electrical characteristics from macromodelization

Table 5. Macromodel simulation at V_{CC+} = 3 V, V_{CC-} = 0 V, R_L, C_L connected to V_{CC}/2, and T_{amb} = 25 °C (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	R_L = 10 kΩ	200	V/mV
I_{CC}	No load, per operator	1.2	mA
V_{icm}		-0.2 to 3.2	V
V_{OH}	R_L = 10 kΩ	2.95	
V_{OL}	R_L = 10 kΩ	25	mV
I_{sink}	V_O = 3 V	80	mA
I_{source}	V_O = 0 V	80	
GBP	R_L = 600 kΩ	4	MHz
SR	R_L = 10 kΩ, C_L = 100 pF	1	V/μs
ϕm	R_L = 600 kΩ	68	Degrees

3.3 Macromodel code

```
** Standard Linear Ics Macromodels, 1996.
** CONNECTIONS:
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY

.SUBCKT TS92X 1 2 3 4 5
*
.MODEL MDTH D IS=1E-8 KF=2.664234E-16 CJO=10F
*
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 8.125000E+00
RIN 15 16 8.125000E+00
RIS 11 15 2.238465E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 153.5u
VOFN 13 14 DC 0
IPOL 13 5 3.200000E-05
CPS 11 15 1e-9
DINN 17 13 MDTH 400E-12
VIN 17 5 -0.100000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 0.400000E+00
FCP 4 5 VOFP 1.865000E+02
FCN 5 4 VOFN 1.865000E+02
FIBP 2 5 VOFP 6.250000E-03
FIBN 5 1 VOFN 6.250000E-03
* GM1 STAGE ***************
FGM1P 119 5 VOFP 1.1
FGM1N 119 5 VOFN 1.1
RAP 119 4 2.6E+06
RAN 119 5 2.6E+06
* GM2 STAGE ***************
G2P 19 5 119 5 1.92E-02
G2N 19 5 119 4 1.92E-02
R2P 19 4 1E+07
```

```
R2N 19 5 1E+07
**************************
VINT1 500 0 5
GCONVP 500 501 119 4 19.38
VP 501 0 0
GCONVN 500 502 119 5 19.38
VN 502 0 0
********* orientation isink isource *******
VINT2 503 0 5
FCOPY 503 504 VOUT 1
DCOPYP 504 505 MDTH 400E-9
VCOPYP 505 0 0
DCOPYN 506 504 MDTH 400E-9
VCOPYN 0 506 0
***************************
F2PP 19 5 poly(2) VCOPYP VP 0 0 0 0 0.5
F2PN 19 5 poly(2) VCOPYP VN 0 0 0 0 0.5
F2NP 19 5 poly(2) VCOPYN VP 0 0 0 0 1.75
F2NN 19 5 poly(2) VCOPYN VN 0 0 0 0 1.75
* COMPENSATION ************
CC 19 119 25p
* OUTPUT ***********
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 6.250000E+02
VIPM 28 4 5.000000E+01
HONM 21 27 VOUT 6.250000E+02
VINM 5 27 5.000000E+01
VOUT 3 23 0
ROUT 23 19 6
COUT 3 5 1.300000E-10
DOP 19 25 MDTH 400E-12
VOP 4 25 1.052
DON 24 19 MDTH 400E-12
VON 24 5 1.052
.ENDS ;TS92X
```

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

4.1 SO14 package information

Figure 14. SO14 package outline

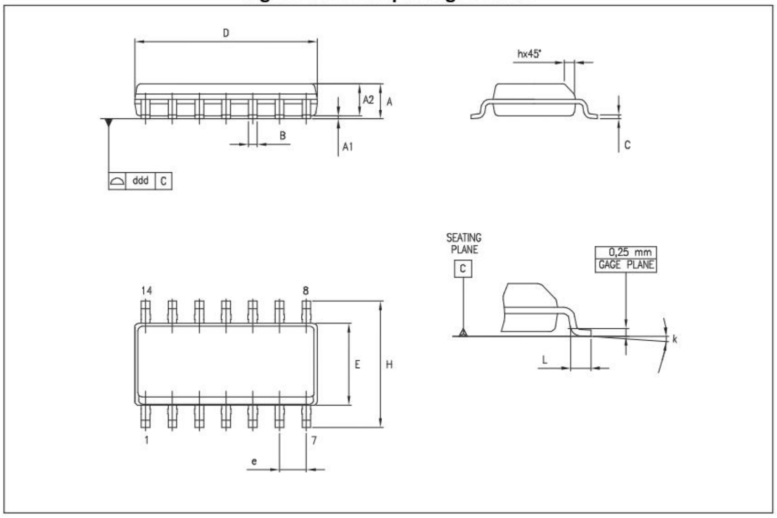


Table 6. SO14 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.05		0.068
A1	0.10		0.25	0.004		0.009
A2	1.10		1.65	0.04		0.06
B	0.33		0.51	0.01		0.02
C	0.19		0.25	0.007		0.009
D	8.55		8.75	0.33		0.34
E	3.80		4.0	0.15		0.15
e		1.27			0.05	
H	5.80		6.20	0.22		0.24
h	0.25		0.50	0.009		0.02
L	0.40		1.27	0.015		0.05
k	8° (max.)					
ddd			0.10			0.004

4.2 TSSOP14 package information

Figure 15. TSSOP14 package outline

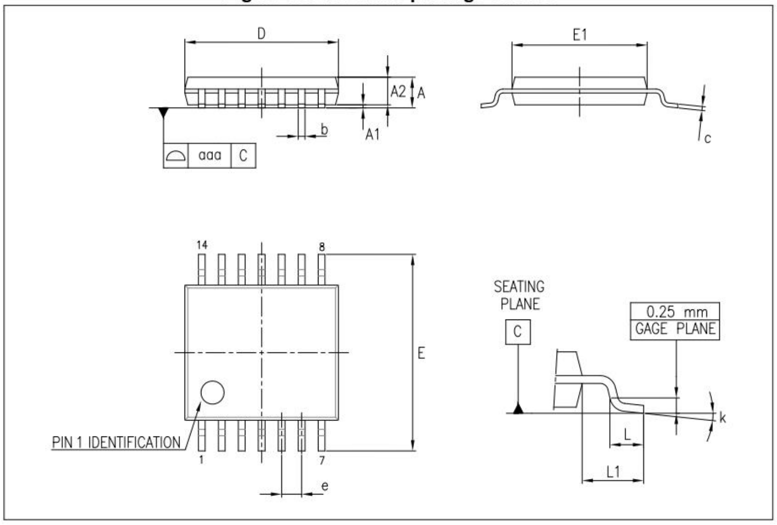


Table 7. TSSOP14 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.176
e		0.65			0.0256	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°		8°	0°		8°
aaa			0.10			0.004

5 Ordering information

Table 8. Order codes

Order code	Temperature range	Package	Packaging	Marking
TS924ID TS924IDT	-40 °C, 125 °C	SO14	Tube or tape and reel	924I
TS924AID TS924AIDT				924AI
TS924IYDT(1)		SO14 (automotive grade)	Tape and reel	924IY
TS924AIYDT(1)				924AIY
TS924IPT		TSSOP14		924I
TS924AIPT				924AI
TS924IYPT(1)		TSSOP14 (automotive grade)		924IY
TS924AIYPT(1)				924AIY

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent.

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
28-May-2001	1	First release.
12-May-2005	2	Modifications on AMR *Table on page 3* (explanation of V_{id} and V_{in} limits, ESD MM and CDM values added, R_{thja} added).
31-Jul-2005	3	PPAP references inserted in the datasheet, see order codes table.
30-Nov-2005	4	Package mechanical data modified. TS924IYPT/TS924AYIPT PPAP reference inserted in order code table. Macromodel modified.
11-Mar-2008	5	Added footnotes for automotive grade order codes in *Table 8: Order codes*. Updated document format.
19-Dec-2008	6	ESD tolerance improved for machine model in *Table 1: Absolute maximum ratings*. Removed TS914AIN order code and corrected footnotes in *Table 8: Order codes*.
08-Oct-2009	7	Added part number TS924A on cover page. Added limits on full temperature range in *Table 3* and *Table 4*. Removed order codes TS924IYD and TS924AIYD from *Table 8*.
15-Apr-2011	8	Modified CMR parameter values in *Table 3* and *Table 4*.
19-May-2011	9	Added A version in title and header.
04-Dec-2012	10	Added DIP14 package to Figure on page 1. Added *Related products* to *Features*. Added DIP14 with value for R_{thja} in *Table 1*. Added conditions to titles of *Figure 1* to *Figure 12*. Replaced V_{CC} by V_{CC+} and V_{DD} by V_{CC-} in title of *Table 5*. Qualified status of TS924IYPT and TS924AIYPT order codes in *Table 8*. Minor corrections throughout document.
05-Jun-2014	11	Removed DIP14 package and order code pertaining to it Added *Figure 13*

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

STMicroelectronics:
TS924ID TS924AID TS924IDT TS924AIPT TS924IPT TS924IN TS924AIDT TS924AIYPT TS924IYPT
TS924AIYDT TS924IYDT

Anexo 1.3: LM311N

Order this document by LM311/D

MOTOROLA

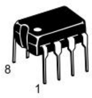
LM311
LM211

Highly Flexible Voltage Comparators

The ability to operate from a single power supply of 5.0 V to 30 V or ±15 V split supplies, as commonly used with operational amplifiers, makes the LM211/LM311 a truly versatile comparator. Moreover, the inputs of the device can be isolated from system ground while the output can drive loads referenced either to ground, the V_{CC} or the V_{EE} supply. This flexibility makes it possible to drive DTL, RTL, TTL, or MOS logic. The output can also switch voltages to 50 V at currents to 50 mA. Thus the LM211/LM311 can be used to drive relays, lamps or solenoids.

HIGH PERFORMANCE VOLTAGE COMPARATORS

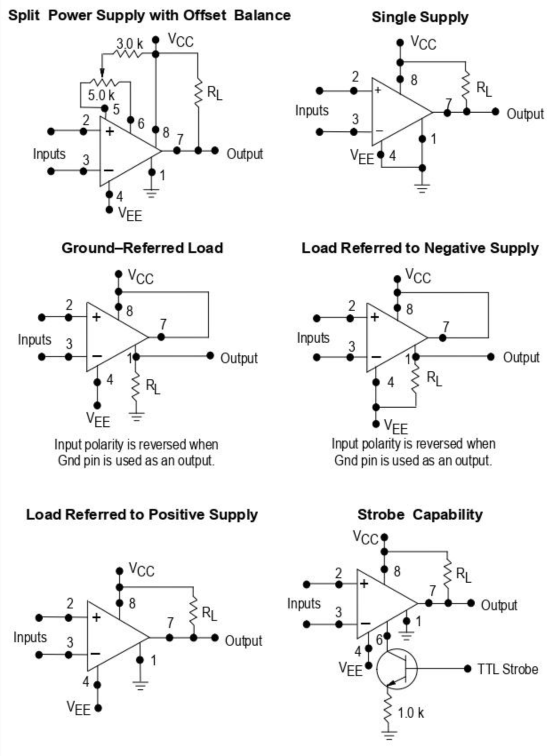
SEMICONDUCTOR TECHNICAL DATA



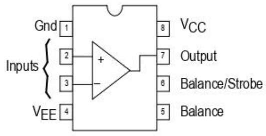
N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Typical Comparator Design Configurations



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM211D	T_A = 25° to +85°C	SO–8
LM311D LM311N	T_A = 0° to +70°C	SO–8 Plastic DIP

[redacted]

LM311 LM211

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	LM211	LM311	Unit
Total Supply Voltage	$V_{CC} + \lvert V_{EE} \rvert$	36	36	Vdc
Output to Negative Supply Voltage	$V_O - V_{EE}$	50	40	Vdc
Ground to Negative Supply Voltage	V_{EE}	30	30	Vdc
Input Differential Voltage	V_{ID}	±30	±30	Vdc
Input Voltage (Note 2)	V_{in}	±15	±15	Vdc
Voltage at Strobe Pin	–	V_{CC} to V_{CC}–5	V_{CC} to V_{CC}–5	Vdc
Power Dissipation and Thermal Characteristics Plastic DIP Derate Above T_A = +25°C	 P_D $1/\theta_{JA}$	 625 5.0		 mW mW/°C
Operating Ambient Temperature Range	T_A	–25 to +85	0 to +70	°C
Operating Junction Temperature	$T_{J(max)}$	+150	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted [Note 1].)

Characteristic	Symbol	LM211 Min	LM211 Typ	LM211 Max	LM311 Min	LM311 Typ	LM311 Max	Unit
Input Offset Voltage (Note 3) $R_S \leq$ 50 kΩ, T_A = +25°C $R_S \leq$ 50 kΩ, $T_{low} \leq T_A \leq T_{high}$*	V_{IO}	 – –	 0.7 –	 3.0 4.0	 – –	 2.0 –	 7.5 10	mV
Input Offset Current (Note 3) T_A = +25°C $T_{low} \leq T_A \leq T_{high}$*	I_{IO}	– –	1.7 –	10 20	– –	1.7 –	50 70	nA
Input Bias Current T_A = +25°C $T_{low} \leq T_A \leq T_{high}$*	I_{IB}	– –	45 –	100 150	– –	45 –	250 300	nA
Voltage Gain	A_V	40	200	–	40	200	–	V/mV
Response Time (Note 4)		–	200	–	–	200	–	ns
Saturation Voltage $V_{ID} \leq$ –5.0 mV, I_O = 50 mA, T_A = 25°C $V_{ID} \leq$ –10 mV, I_O = 50 mA, T_A = 25°C $V_{CC} \geq$ 4.5 V, V_{EE} = 0, $T_{low} \leq T_A \leq T_{high}$* $V_{ID} \angle \leq$ 6.0 mV, $I_{sink} \leq$ 8.0 mA $V_{ID} \angle \leq$ 10 mV, $I_{sink} \leq$ 8.0 mA	V_{OL}	 – – – –	 0.75 – 0.23 –	 1.5 – 0.4 –	 – – – –	 – 0.75 – 0.23	 – 1.5 – 0.4	V
Strobe "On" Current (Note 5)	I_S	–	3.0	–	–	3.0	–	mA
Output Leakage Current $V_{ID} \geq$ 5.0 mV, V_O= 35 V, T_A = 25°C, I_{strobe}= 3.0 mA $V_{ID} \geq$ 10 mV, V_O= 35 V, T_A = 25°C, I_{strobe}= 3.0 mA $V_{ID} \geq$ 5.0 mV, V_O= 35 V, $T_{low} \leq T_A \leq T_{high}$*		 – – –	 0.2 – 0.1	 10 – 0.5	 – – –	 – 0.2 –	 – 50 –	 nA nA µA
Input Voltage Range ($T_{low} \leq T_A \leq T_{high}$*)	V_{ICR}	–14.5	–14.7 to 13.8	+13.0	–14.5	–14.7 to 13.8	+13.0	V
Positive Supply Current	I_{CC}	–	+2.4	+6.0	–	+2.4	+7.5	mA
Negative Supply Current	I_{EE}	–	–1.3	–5.0	–	–1.3	–5.0	mA

* T_{low} = –25°C for LM211 T_{high} = +85°C for LM211
= 0°C for LM311 = +70°C for LM311

NOTES: 1. Offset voltage, offset current and bias current specifications apply for a supply voltage range from a single 5.0 V supply up to ±15 V supplies.
2. This rating applies for ±15 V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
3. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the "worst case" effects of voltage gain and input impedance.
4. The response time specified is for a 100 mV input step with 5.0 mV overdrive.
5. Do not short the strobe pin to ground; it should be current driven at 3.0 mA to 5.0 mA.

LM311 LM211

Figure 1. Circuit Schematic

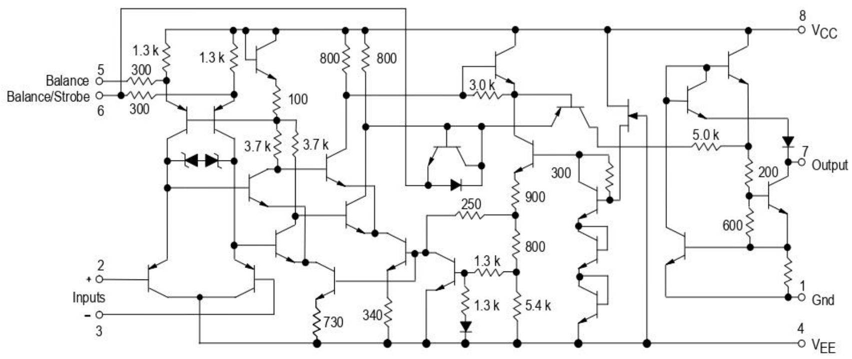


Figure 2. Input Bias Current versus Temperature

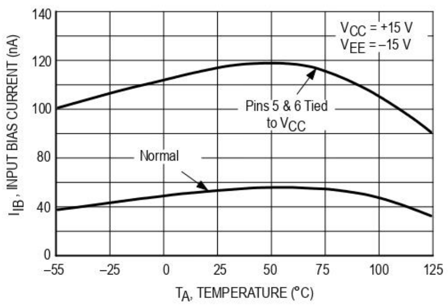


Figure 3. Input Offset Current versus Temperature

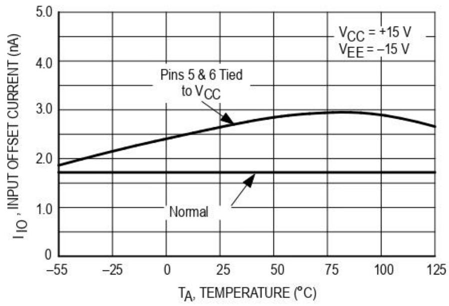


Figure 4. Input Bias Current versus Differential Input Voltage

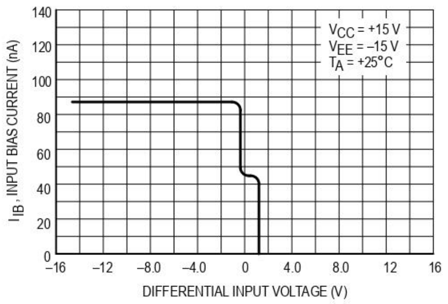


Figure 5. Common Mode Limits versus Temperature

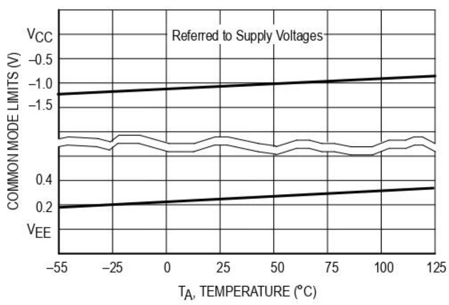


Figure 6. Response Time for Various Input Overdrives

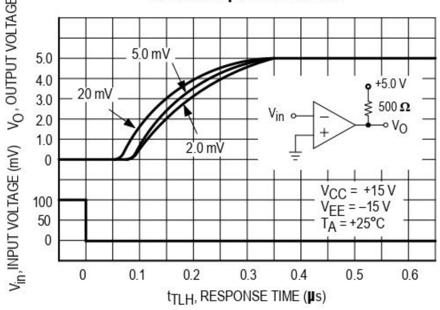


Figure 7. Response Time for Various Input Overdrives

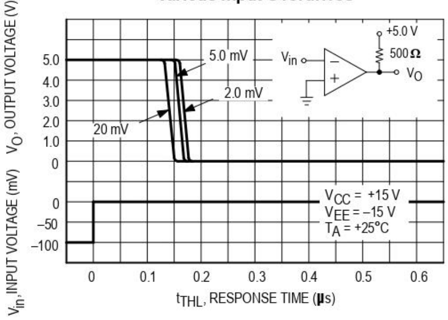


Figure 8. Response Time for Various Input Overdrives

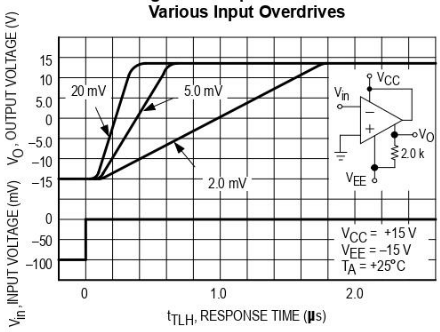


Figure 9. Response Time for Various Input Overdrives

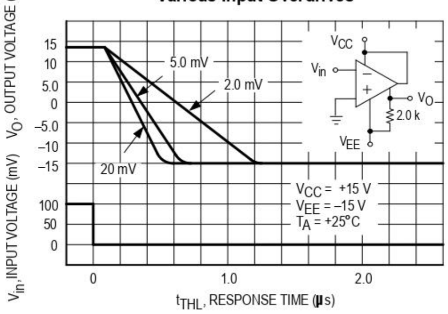


Figure 10. Output Short Circuit Current Characteristics and Power Dissipation

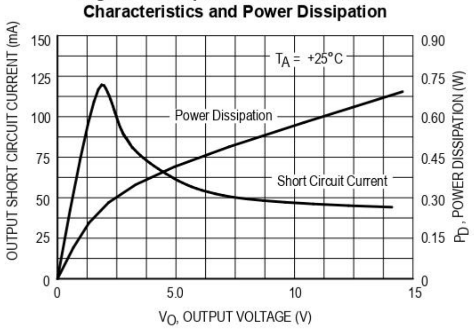
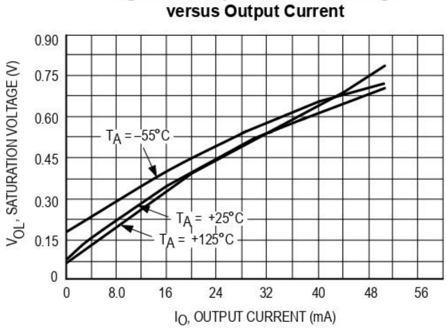


Figure 11. Output Saturation Voltage versus Output Current



LM311 LM211

Figure 12. Output Leakage Current versus Temperature

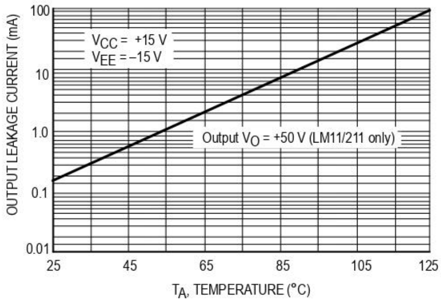


Figure 13. Power Supply Current versus Supply Voltage

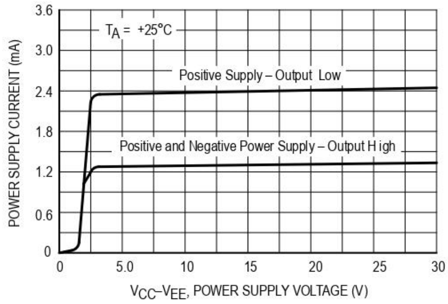
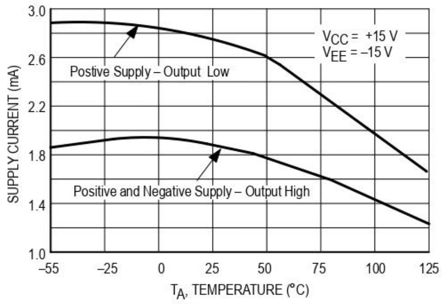


Figure 14. Power Supply Current versus Temperature



APPLICATIONS INFORMATION

Figure 15. Improved Method of Adding Hysteresis Without Applying Positive Feedback to the Inputs

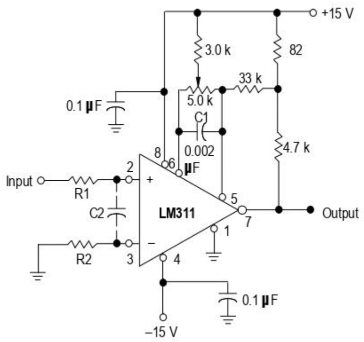
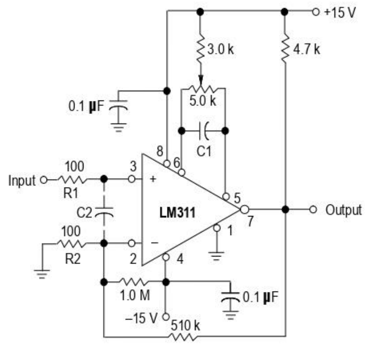


Figure 16. Conventional Technique for Adding Hysteresis



TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high speed comparator such as the LM211 is used with high speed input signals and low source impedances, the output response will normally be fast and stable, providing the power supplies have been bypassed (with 0.1 µF disc capacitors), and that the output signal is routed well away from the inputs (Pins 2 and 3) and also away from Pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1.0 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing–point. This is due to the high gain and wide bandwidth of comparators like the LM211 series. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 15.

The trim pins (Pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim–pot, they should be shorted together. If they are connected to a trim–pot, a 0.01 µF capacitor (C1) between Pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if Pin 5 is used for positive feedback as in Figure 15. For the fastest response time, tie both balance pins to V_{CC}.

Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor (C2) is connected directly across the input pins. When the signal source is applied through a resistive network, R1, it is usually advantageous to choose R2 of the same value, both for DC and for dynamic (AC) considerations. Carbon, tin–oxide, and metal–film resistors have all been used with good results in comparator input circuitry, but inductive wirewound resistors should be avoided.

When comparator circuits use input resistors (e.g., summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words, there should be a very short lead length or printed–circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R1 = 10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to dampen. Twisting these input leads tightly is the best alternative to placing resistors close to the comparator.

Since feedback to almost any pin of a comparator can result in oscillation, the printed–circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM211 circuitry (e.g., one side of a double layer printed circuit board). Ground, positive supply or negative supply foil should extend between the output and the inputs to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides to guard against capacitive coupling from any fast high–level signals (such as the output). If Pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim–pot, the trim–pot should be located no more than a few inches away from the LM211, and a 0.01 µF capacitor should be installed across Pins 5 and 6. If this capacitor cannot be used, a shielding printed–circuit foil may be advisable between Pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM211.

A standard procedure is to add hysteresis to a comparator to prevent oscillation, and to avoid excessive noise on the output. In the circuit of Figure 16, the feedback resistor of 510 kΩ from the output to the positive input will cause about 3.0 mV of hysteresis. However, if R2 is larger than 100 Ω, such as 50 kΩ, it would not be practical to simply increase the value of the positive feedback resistor proportionally above 510 kΩ to maintain the same amount of hysteresis.

When both inputs of the LM211 are connected to active signals, or if a high–impedance signal is driving the positive input of the LM211 so that positive feedback would be disruptive, the circuit of Figure 15 is ideal. The positive feedback is applied to Pin 5 (one of the offset adjustment pins). This will be sufficient to cause 1.0 mV to 2.0 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive–feedback signal across the 82 Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at Pin 5, so this feedback does not add to the offset voltage of the comparator. As much as 8.0 mV of offset voltage can be trimmed out, using the 5.0 kΩ pot and 3.0 kΩ resistor as shown.

Figure 17. Zero–Crossing Detector Driving CMOS Logic

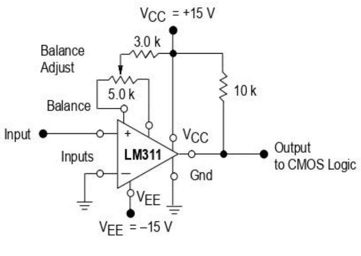
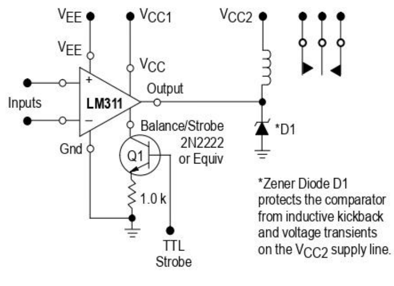


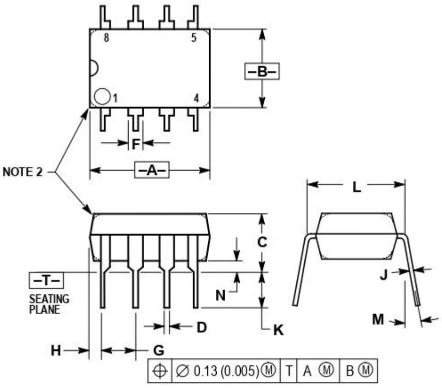
Figure 18. Relay Driver with Strobe Capability



LM311 LM211

OUTLINE DIMENSIONS

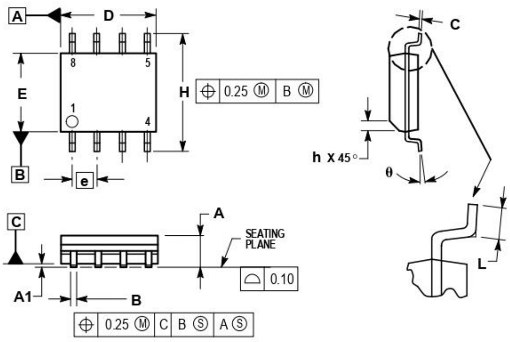
N SUFFIX
PLASTIC PACKAGE
CASE 626–05
ISSUE K



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

D SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SO–8)
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

MOTOROLA ANALOG IC DEVICE DATA 7

LM311 LM211

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MOTOROLA

◊

LM311/D

Anexo 1.4: CD4046B

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS043B – Revised July 2003

CD4046B Types

CMOS Micropower Phase-Locked Loop

■ **CD4046B CMOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-V zener diode is provided for supply regulation if necessary.**

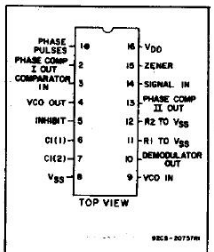
The CD4046B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 kΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CMOS frequency dividers such as the RCA-CD4024, CD4018, CD4020, CD4022, CD4029, and CD4059. One or more CD4018 (Presettable Divide-by-N Counter) or CD4029 (Presettable Up/Down Counter), or CD4059A (Programmable Divide-by-"N" Counter), together with the CD4046B (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Features:

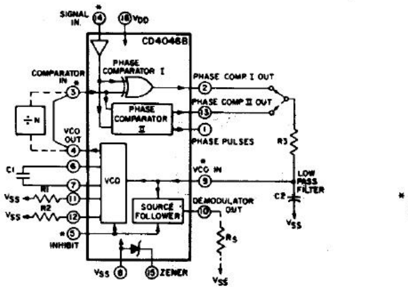
- **Very low power consumption: 70 µW (typ.) at VCO f_o = 10 kHz, V_{DD} = 5 V**
- **Operating frequency range up to 1.4 MHz (typ.) at V_{DD} = 10 V, RI = 5 kΩ**
- **Low frequency drift: 0.04%/°C (typ.) at V_{DD} = 10 V**
- **Choice of two phase comparators:**
  Exclusive-OR network (I)
  Edge-controlled memory network with phase-pulse output for lock indication (II)
- **High VCO linearity: <1% (typ.) at V_{DD} = 10 V**
- **VCO inhibit control for ON-OFF keying and ultra-low standby power consumption**
- **Source-follower output of VCO control input (Demod. output)**
- **Zener diode to assist supply regulation**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

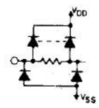


TERMINAL ASSIGNMENT

Applications:

- **FM demodulator and modulator**
- **Frequency synthesis and multiplication**
- **Frequency discriminator**
- **Data synchronization**
- **Voltage-to-frequency conversion**
- **Tone decoding**
- **FSK – Modems**
- **Signal conditioning**
- **(See ICAN-6101) "RCA COS/MOS Phase-Locked Loop – A Versatile Building Block for Micropower Digital and Analog Applications"**





* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

Fig.1 – CMOS phase-locked loop block diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
Voltages referenced to V_{SS} Terminal)	−0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −55°C to +100°C	500mW
For T_A = +100°C to +125°C	Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T_A)	−55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels [logic "0" ≤30% (V_{DD}−V_{SS}), logic "1" ≥ 70% (V_{DD}−V_{SS})]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package-Temperature Range
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

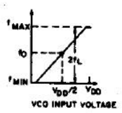
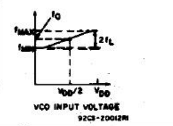
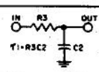
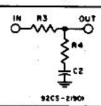
CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range VCO Section:			
As Fixed Oscillator	3	18	V
Phased-Lock-Loop Operation	5	18	V
Supply-Voltage Range Phase Comparator Section:			
Comparators	3	18	V
VCO Operation	5	18	V

DESIGN INFORMATION

This information is a guide for approximating the values of external components for the CD4046B in a Phase-Locked-Loop system.

The selected external components must be within the following ranges:

$5\ k\Omega \leqslant R1, R2, R_S \leqslant 1\ M\Omega$
$C1 \geqslant 100\ pF$ at $V_{DD} \geqslant 5\ V$;
$C1 \geqslant 50\ pF$ at $V_{DD} \geqslant 10\ V$

Characteristics	Phase Comparator Used	Design Information	
		VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET
VCO Frequency	1		
	2	Same as for No.1	
For No.Signal Input	1	VCO will adjust to center frequency, f_o	
	2	VCO will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2\ f_L$	1	$2\ f_L$ = full VCO frequency range	
		$2\ f_L = f_{max} - f_{min}$	
	2	Same as for No.1	
Frequency Capture Range, $2\ f_C$ / Loop Filter Component Selection	1		(1), (2) $2\ f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$
			For $2\ f_C$, see Ref. (2)
	2	$f_C = f_L$	
Phase Angle Between Signal and Comparator	1	90^o at center frequency (f_o) approximating 0^o and 180^o at ends of lock range ($2\ f_L$)	
	2	Always 0^o in lock	
Locks On Harmonic of Center Frequency	1	Yes	
	2	No	
Signal Input Noise Rejection	1	High	
	2	Low	

For further information, see

(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966
(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o).

The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_c$).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is ⩽ the lock range.

With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0^o and 180^o, and is 90^o at the center frequency. Fig. 2 shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms **for a CMOS phase-locked-loop employing** phase comparator I in locked condition of f_o is shown in Fig. 3.

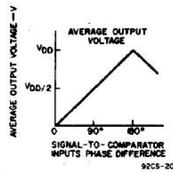


Fig.2 – Phase-comparator I characteristics at low-pass filter output.

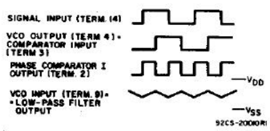


Fig. 3—Typical waveforms for CMOS phase-locked loop employing phase comparator in locked condition of f_o.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions

CD4046B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
VCO Section											
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0.15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	Term. 4 driving CMOS	0,5	5	0.05				–	0	0.05	V
		0,10	10	0.05				–	0	0.05	
		0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	e.g. Term.3	0,5	5	4.95				4.95	5	–	
		0,10	10	9.95				9.95	10	–	
		0,15	15	14.95				14.95	15	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	µA
Phase Comparator Section											
Total Device Current, I_{DD} Max. Term. 14 open, Term. 5 = V_{DD}	–	0,5	5	0.2				–	0.1	0.2	mA
	–	0,10	10	1				–	0.5	1	
	–	0,15	15	1.5				–	0.75	1.5	
	–	0,20	20	4				–	2	4	
Term. 14 = V_{SS} or V_{DD}, Term. 5 = V_{DD}	–	0,5	5	20				–	10	20	µA
	–	0,10	10	40				–	20	40	
	–	0,15	15	80				–	40	80	
	–	0,20	20	160				–	80	160	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
DC-Coupled Signal Input and Comparator Input Voltage Sensitivity Low Level V_{IL} Max.	0.5,4.5	–	5			1.5		–	–	1.5	V
	1,9	–	10			3		–	–	3	
	1.5,13.5	–	15			4		–	–	4	
High Level V_{IH} Min.	0.5,4.5	–	5			3.5		3.5	–	–	
	1,9	–	10			7		7	–	–	
	1.5,13.5	–	15			11		11	–	–	

control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Phase Comparator Section (cont'd)											
Input Current I_{IN} Max. (except Term. 14)	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
3-State Leakage Current, I_{OUT} Max.	0,18	0,18	18	±0.1	±0.1	±0.2	±0.2	–	$\pm10^{-5}$	±0.1*	μA

*Limit determined by minimum feasible leakage current measurement for automatic testing.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS		V_{DD} (V)	LIMITS ALL TYPES Min.	Typ.	Max.	UNITS
VCO Section							
Operating Power Dissipation, P_D	f_o = 10 kHz, $R_2 = \infty$	R_1 = 1 MΩ, $VCO_{IN} = \frac{V_{DD}}{2}$	5 10 15	– – –	70 800 3000	140 1600 6000	μW
Maximum Operating Frequency f_{max}	C_1=50 pF, $R_2 = \infty$, $VCO_{IN}=V_{DD}$	R_1 = 10 kΩ	5 10 15	0.3 0.6 0.8	0.6 1.2 1.6	– – –	MHz
	C_1 = 50 pF, $R_2 = \infty$, $VCO_{IN}=V_{DD}$	R_1 = 5 kΩ	5 10 15	0.5 1 1.4	0.8 1.4 2.4	– – –	
Center Frequency (f_o) and Frequency Range ($f_{max}-f_{min}$)	Programmable with external components R1, R2, and C1 *See Design Information*						
Linearity	VCO_{IN} = 2.5 V ± 0.3V,	R_1=10 kΩ	5	–	1.7	–	%
	=5 V ± 1 V,	= 100 kΩ	10	–	0.5	–	
	=5 V ± 2.5 V,	=400 kΩ	10	–	4	–	
	=7.5 V ± 1.5 V,	= 100 kΩ	15	–	0.5	–	
	= 7.5 V ± 5 V,	= 1 MΩ	15	–	7	–	
Temperature - Frequency Stability: No Frequency Offset f_{MIN} = 0			5 10 15	– – –	±0.12 ±0.04 ±0.015	– – –	%/°C
Frequency Offset $f_{MIN} \neq 0$			5 10 15	– – –	±0.09 ±0.07 ±0.03	– – –	
Output Duty Cycle			5,10,15	–	50	–	%
Output Transition Times, t_{THL}, t_{TLH}			5 10 15	– – –	100 50 40	200 100 80	ns

the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. 10 shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

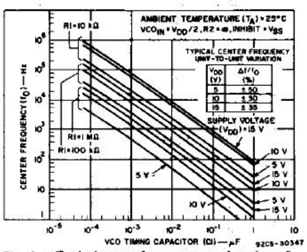

Fig. 4 – Typical center frequency as a function of C1 and R1 at V_{DD} = 5 V, 10 V, and 15 V.

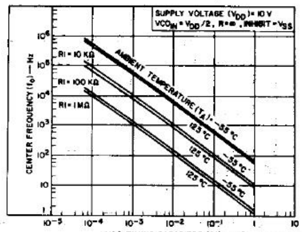

Fig. 5 – Center frequency as a function of C1 and R1 for ambient temperatures of −55°C to 125°C.

CD4046B Types

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTIC	TEST CONDITIONS		V_{DD} (V)	LIMITS ALL TYPES Min.	Typ.	Max.	UNITS
VCO Section (cont'd)							
Source-Follower Output (Demodulated Output): Offset Voltage $\|VCO_{IN}-V_{DEM}\|$	RS > 10 kΩ		5 10 15	– – –	1.8 1.8 1.8	2.5 2.5 2.5	V
Linearity	R_S=100 kΩ = 300 kΩ =500 kΩ	VCO_{IN} = 2.5±0.3 V = 5±2.5 V = 7.5± 5 V	5 10 15	– – –	0.3 0.7 0.9	– – –	%
Zener Diode Voltage (V_z)	I_Z = 50 µA			4.45	5.5	6.15	V
Zener Dynamic Resistance, R_z	I_Z = 1 mA			–	40	–	Ω
Phase Comparator Section							
Term. 14 (SIGNAL IN) Input Resistance R_{14}			5 10 15	1 0.2 0.1	2 0.4 0.2	– – –	MΩ
AC Coupled Signal Input Voltage Sensitivity* (peak-to-peak)	f_{IN} = 100 kHz, sine wave		5 10 15	– – –	180 330 900	360 660 1800	mV
Propagation Delay Times, Terms. 14 to 1: High to Low Level, t_{PHL}			5 10 15	– – –	225 100 65	450 200 130	ns
Low to High Level, t_{PLH}			5 10 15	– – –	350 150 100	700 300 200	ns
3-State Propagation Delay Times, Terms. 3 to 13: High Level to High Impedance, t_{PHZ}			5 10 15	– – –	225 100 95	450 200 190	ns
Terms. 14 to 13: Low Level to High Impedance, t_{PLZ}			5 10 15	– – –	285 130 95	570 260 190	ns
Input Rise or Fall Times, t_r, t_f Comparator Input, Term. 3	See Fig. 5 for Phase Comp. II output loading		5 10 15	– – –	– – –	50 1 0.3	µs
Signal Input, Term. 14			5 10 15	– – –	– – –	500 20 2.5	µs
Output Transition Times, t_{THL}, t_{TLH}			5 10 15	– – –	100 50 40	200 100 80	ns

* For sine wave, the frequency must be greater than 10 kHz for Phase Comparator II.

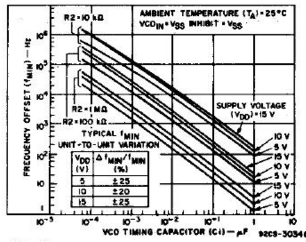

Fig. 6 — Typical frequency offset as a function of C1 and R2 for V_{DD} = 5 V, 10 V, and 15 V.

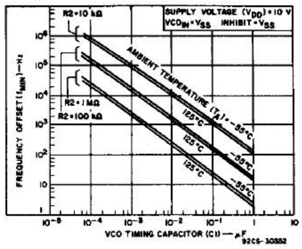

Fig. 7 — Frequency offset as a function of C1 and R2 for ambient temperatures of −55°C to 125°C.

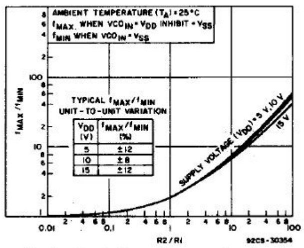

Fig. 8 — Typical f_{MAX}/f_{MIN} as a function of R2/R1.

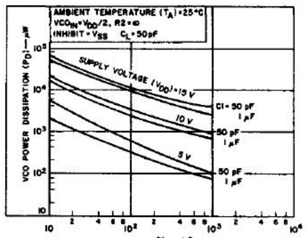

Fig. 9 — Typical VCO power dissipation at center frequency as a function of R1.

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CD4046B Types

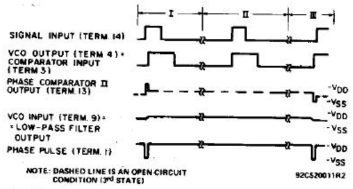


Fig. 10 - Typical waveforms for COS/MOS phase-locked loop employing phase comparator II in locked condition.

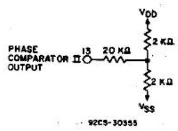


Fig. 11 – Phase comparator II output loading circuit.

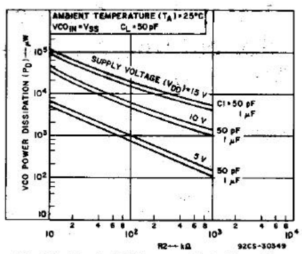


Fig. 12 – Typical VCO power dissipation at f_{MIN} as a function of R2.

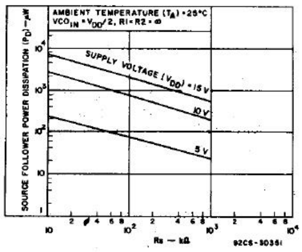


Fig. 13 – Typical source follower power dissipation as a function of Rs.

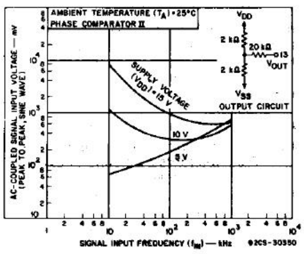


Fig. 14 – AC-coupled signal input voltage as a function of signal input frequency.

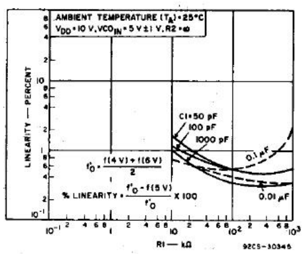
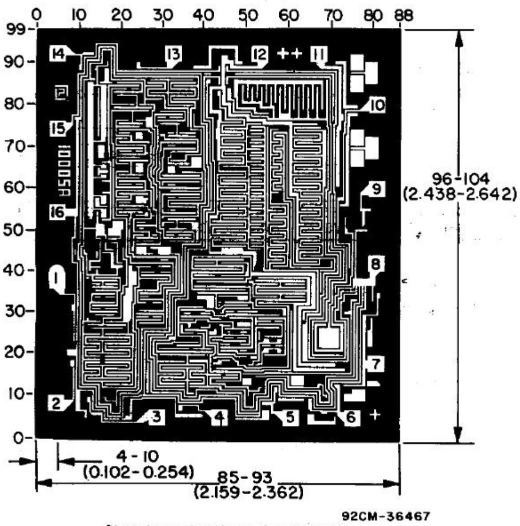


Fig. 15 – Typical VCO linearity as a function of R1 and C1 at V_{DD} = 10 V.

3

COMMERCIAL CMOS HIGH VOLTAGE ICs



Dimensions and pad layout for CD4046BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

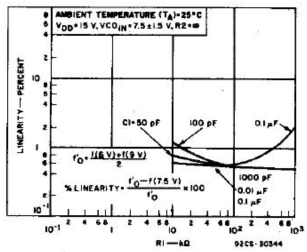


Fig. 16 – Typical VCO linearity as a function of R1 and C1 at V_{DD} = 15 V.

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TEXAS INSTRUMENTS
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PACKAGE OPTION ADDENDUM

28-Feb-2005

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-9466401MEA	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4046BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4046BF	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4046BF3A	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4046BNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4046BPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4046BPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

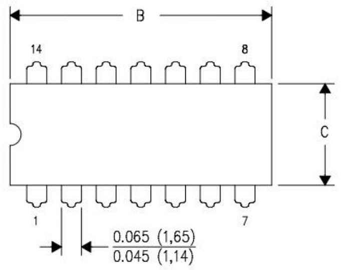
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

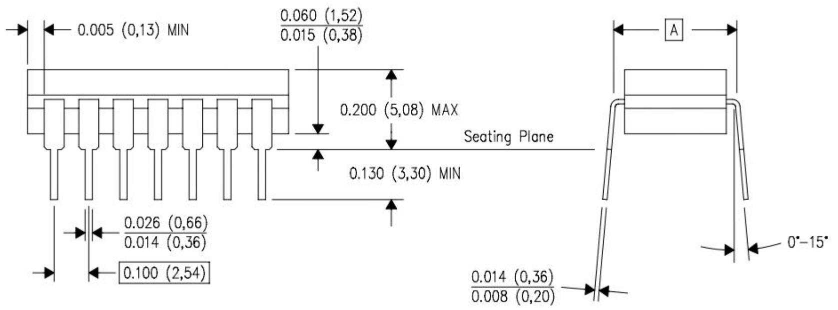
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

J (R-GDIP-T**) CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



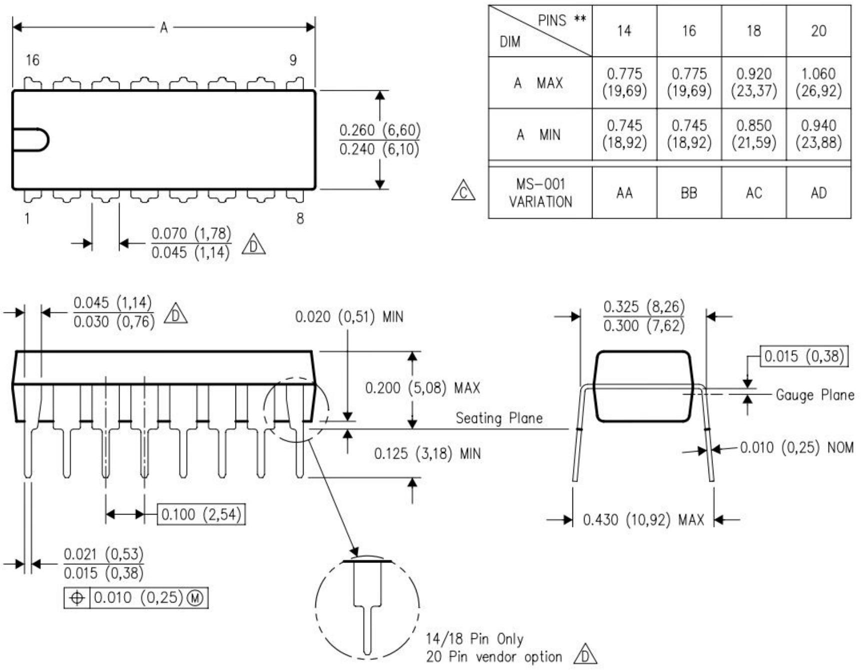
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

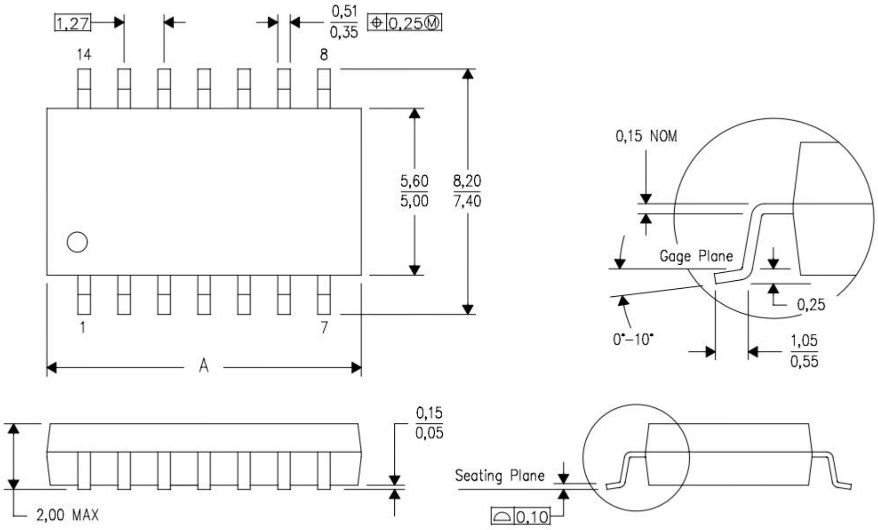


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

NS (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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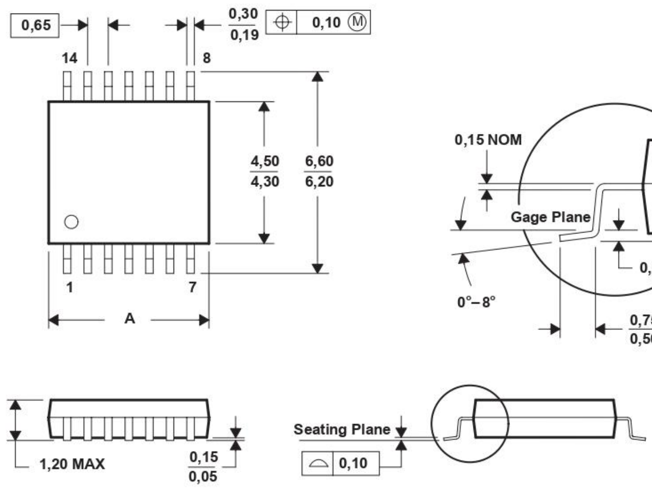
MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
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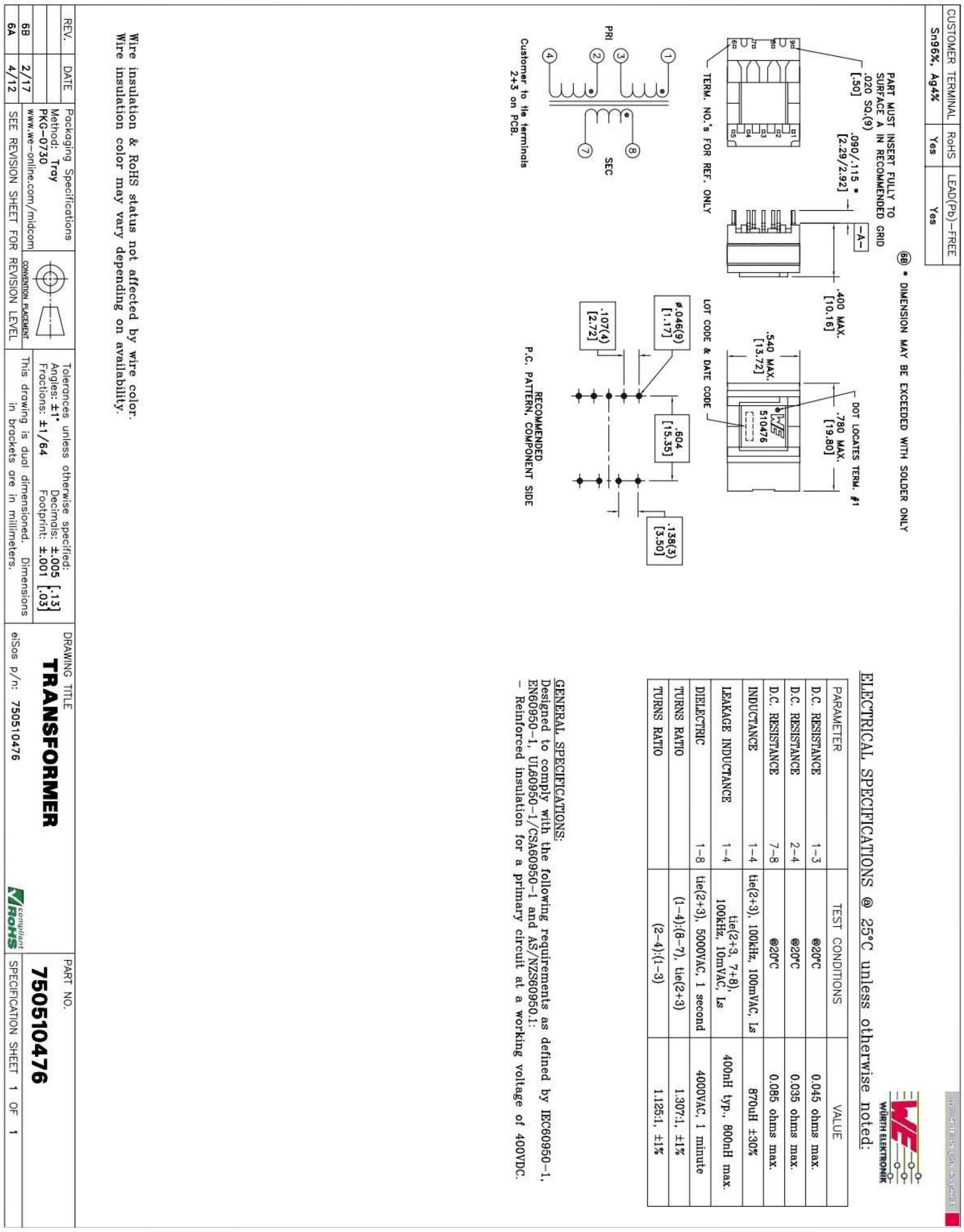
Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Anexo 1.5: Transformador



CUSTOMER TERMINAL	RoHS	LEAD(Pb)–FREE
Sn96%, Ag4%	Yes	Yes

(6B) * DIMENSION MAY BE EXCEEDED WITH SOLDER ONLY

ELECTRICAL SPECIFICATIONS @ 25°C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	1–3	@20°C	0.045 ohms max.
D.C. RESISTANCE	2–4	@20°C	0.035 ohms max.
D.C. RESISTANCE	7–8	@20°C	0.085 ohms max.
INDUCTANCE	1–4	tie(2+3), 100kHz, 100mVAC, Ls	870uH ±30%
LEAKAGE INDUCTANCE	1–4	tie(2+3, 7+8), 100kHz, 10mVAC, Ls	400nH typ., 800nH max.
DIELECTRIC	1–8	tie(2+3), 5000VAC, 1 second	4000VAC, 1 minute
TURNS RATIO		(1–4):(8–7), tie(2+3)	1.307:1, ±1%
TURNS RATIO		(2–4):(1–3)	1.125:1, ±1%

GENERAL SPECIFICATIONS:
Designed to comply with the following requirements as defined by IEC60950–1, EN60950–1, UL60950–1/CSA60950–1 and AS/NZS60950.1:
– Reinforced insulation for a primary circuit at a working voltage of 400VDC.

Wire insulation & RoHS status not affected by wire color.
Wire insulation color may vary depending on availability.

REV.	DATE	Packaging Specifications	Tolerances unless otherwise specified	DRAWING TITLE	PART NO.
6B	2/17	Method: Tray PKG–0730 www.we–online.com/midcom	Angles: ±1° Fractions: ±1/64 Decimals: ±.005 [.13] Footprint: ±.001 [.03]	TRANSFORMER	750510476
6A	4/12	SEE REVISION SHEET FOR REVISION LEVEL	This drawing is dual dimensioned. Dimensions in brackets are in millimeters.	eiSos p/n: 750510476	SPECIFICATION SHEET 1 OF 1

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Wurth Electronics:
750510476

Anexo 1.6: L293D (Puente en H)

Product Folder | Sample & Buy | Technical Documents | Tools & Software | Support & Community

TEXAS INSTRUMENTS

L293, L293D

SLRS008D – SEPTEMBER 1986 – REVISED JANUARY 2016

L293x Quadruple Half-H Drivers

1 Features

- Wide Supply-Voltage Range: 4.5 V to 36 V
- Separate Input-Logic Supply
- Internal ESD Protection
- High-Noise-Immunity Inputs
- Output Current 1 A Per Channel (600 mA for L293D)
- Peak Output Current 2 A Per Channel (1.2 A for L293D)
- Output Clamp Diodes for Inductive Transient Suppression (L293D)

2 Applications

- Stepper Motor Drivers
- DC Motor Drivers
- Latching Relay Drivers

3 Description

The L293 and L293D devices are quadruple high-current half-H drivers. The L293 is designed to provide bidirectional drive currents of up to 1 A at voltages from 4.5 V to 36 V. The L293D is designed to provide bidirectional drive currents of up to 600-mA at voltages from 4.5 V to 36 V. Both devices are designed to drive inductive loads such as relays, solenoids, DC and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

Each output is a complete totem-pole drive circuit, with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs, with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN.

The L293 and L293D are characterized for operation from 0°C to 70°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
L293NE	PDIP (16)	19.80 mm × 6.35 mm
L293DNE	PDIP (16)	19.80 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram

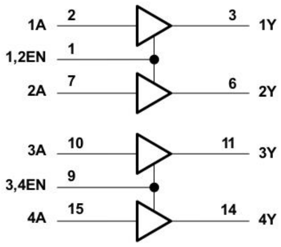


Table of Contents

4 Revision History

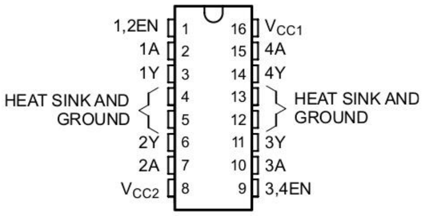
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2004) to Revision D — **Page**

- Removed *Ordering Information* table 1
- Added *ESD Ratings* and *Thermal Information* tables, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1

5 Pin Configuration and Functions

NE Package
16-Pin PDIP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1,2EN	1	I	Enable driver channels 1 and 2 (active high input)
<1:4>A	2, 7, 10, 15	I	Driver inputs, noninverting
<1:4>Y	3, 6, 11, 14	O	Driver outputs
3,4EN	9	I	Enable driver channels 3 and 4 (active high input)
GROUND	4, 5, 12, 13	—	Device ground and heat sink pin. Connect to printed-circuit-board ground plane with multiple solid vias
V_{CC1}	16	—	5-V supply for internal logic translation
V_{CC2}	8	—	Power VCC for drivers 4.5 V to 36 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{CC1} (2)		36	V
Output supply voltage, V_{CC2}		36	V
Input voltage, V_I		7	V
Output voltage, V_O	–3	V_{CC2} + 3	V
Peak output current, I_O (nonrepetitive, t ≤ 5 ms): L293	–2	2	A
Peak output current, I_O (nonrepetitive, t ≤ 100 µs): L293D	–1.2	1.2	A
Continuous output current, I_O: L293	–1	1	A
Continuous output current, I_O: L293D	–600	600	mA
Maximum junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Supply voltage	V_{CC1}	4.5		7	V
		V_{CC2}	V_{CC1}		36	
V_{IH}	High-level input voltage	V_{CC1} ≤ 7 V	2.3		V_{CC1}	V
		V_{CC1} ≥ 7 V	2.3		7	V
V_{IL}	Low-level output voltage		–0.3(1)		1.5	V
T_A	Operating free-air temperature		0		70	°C

(1) The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for logic voltage levels.

6.4 Thermal Information

THERMAL METRIC(1)		L293, L293D NE (PDIP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	36.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		L293: I_{OH} = −1 A		V_{CC2} – 1.8	V_{CC2} – 1.4		V
			L293D: I_{OH} = − 0.6 A					
V_{OL}	Low-level output voltage		L293: I_{OL} = 1 A			1.2	1.8	V
			L293D: I_{OL} = 0.6 A					
V_{OKH}	High-level output clamp voltage		L293D: I_{OK} = –0.6 A			V_{CC2} + 1.3		V
V_{OKL}	Low-level output clamp voltage		L293D: I_{OK} = 0.6 A			1.3		V
I_{IH}	High-level input current	A	V_I = 7 V			0.2	100	μA
		EN				0.2	10	
I_{IL}	Low-level input current	A	V_I = 0			–3	–10	μA
		EN				–2	–100	
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level		13	22	mA
				All outputs at low level		35	60	
				All outputs at high impedance		8	24	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level		14	24	mA
				All outputs at low level		2	6	
				All outputs at high impedance		2	4	

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from A input	L293NE, L293DNE	C_L = 30 pF, See Figure 2		800		ns
		L293DWP, L293N L293DN			750		
t_{PHL}	Propagation delay time, high-to-low-level output from A input	L293NE, L293DNE			400		ns
		L293DWP, L293N L293DN			200		
t_{TLH}	Transition time, low-to-high-level output	L293NE, L293DNE			300		ns
		L293DWP, L293N L293DN			100		
t_{THL}	Transition time, high-to-low-level output	L293NE, L293DNE			300		ns
		L293DWP, L293N L293DN			350		

6.7 Typical Characteristics

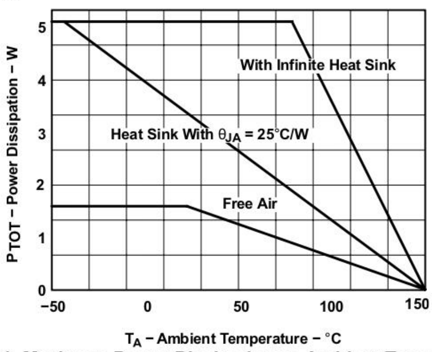
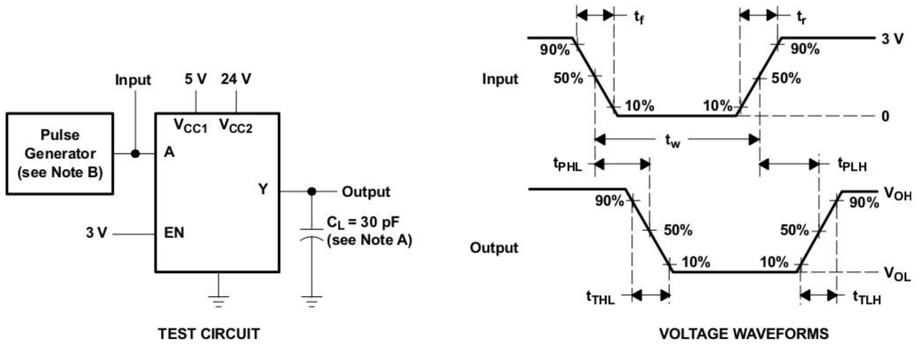


Figure 1. Maximum Power Dissipation vs Ambient Temperature

7 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10$ µs, PRR = 5 kHz, $Z_O = 50\ \Omega$.

Figure 2. Test Circuit and Voltage Waveforms

8 Detailed Description

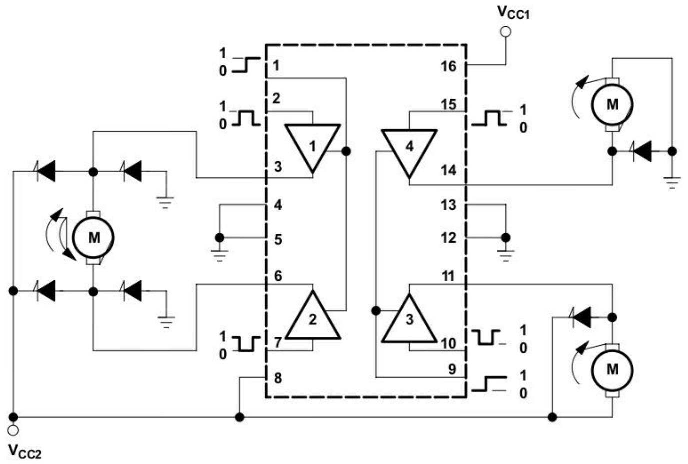
8.1 Overview

The L293 and L293D are quadruple high-current half-H drivers. These devices are designed to drive a wide array of inductive loads such as relays, solenoids, DC and bipolar stepping motors, as well as other high-current and high-voltage loads. All inputs are TTL compatible and tolerant up to 7 V.

Each output is a complete totem-pole drive circuit, with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs, with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled, and their outputs are active and in phase with their inputs. When the enable input is low, those drivers are disabled, and their outputs are off and in the high-impedance state. With the proper data inputs, each pair of drivers forms a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

On the L293, external high-speed output clamp diodes should be used for inductive transient suppression. On the L293D, these diodes are integrated to reduce system complexity and overall system size. A V_{CC1} terminal, separate from V_{CC2}, is provided for the logic inputs to minimize device power dissipation. The L293 and L293D are characterized for operation from 0°C to 70°C.

8.2 Functional Block Diagram



Output diodes are internal in L293D.

8.3 Feature Description

The L293x has TTL-compatible inputs and high voltage outputs for inductive load driving. Current outputs can get up to 2 A using the L293.

8.4 Device Functional Modes

Table 1 lists the fuctional modes of the L293x.

Table 1. Function Table (Each Driver)(1)

INPUTS (2)		OUTPUT (Y)
A	EN	
H	H	H
L	H	L
X	L	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)
(2) In the thermal shutdown mode, the output is in the high-impedance state, regardless of the input levels.

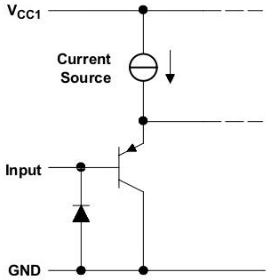


Figure 3. Schematic of Inputs for the L293x

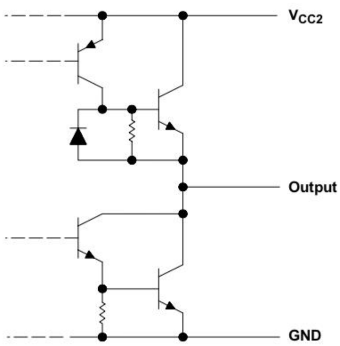


Figure 4. Schematic of Outputs for the L293

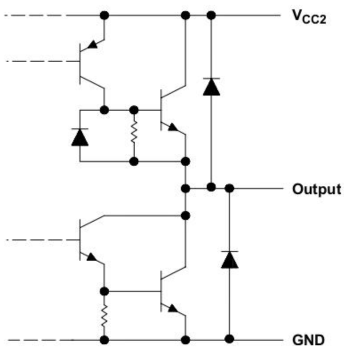


Figure 5. Schematic of Outputs for the L293D

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A typical application for the L293 device is driving a two-phase motor. Below is an example schematic displaying how to properly connect a two-phase motor to the L293 device.

Provide a 5-V supply to V_{CC1} and valid logic input levels to data and enable inputs. V_{CC2} must be connected to a power supply capable of supplying the needed current and voltage demand for the loads connected to the outputs.

9.2 Typical Application

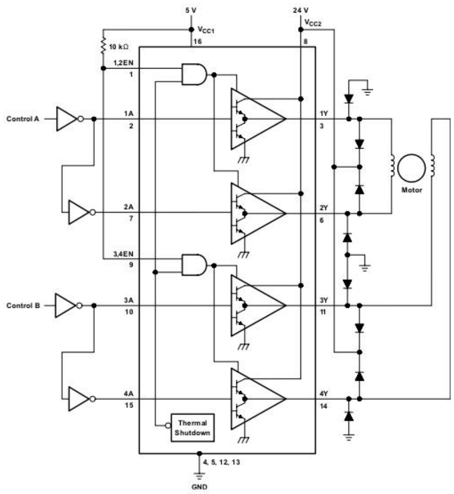


Figure 6. Two-Phase Motor Driver (L293)

9.2.1 Design Requirements

The design techniques in the application above as well as the applications below should fall within the following design requirements.

1. V_{CC1} should fall within the limits described in the *Recommended Operating Conditions*.
2. V_{CC2} should fall within the limits described in the *Recommended Operating Conditions*.
3. The current per channel should not exceed 1 A for the L293 (600mA for the L293D).

9.2.2 Detailed Design Procedure

When designing with the L293 or L293D, careful consideration should be made to ensure the device does not exceed the operating temperature of the device. Proper heatsinking will allow for operation over a larger range of current per channel. Refer to the *Power Supply Recommendations* as well as the *Layout Example*.

Typical Application (continued)

9.2.3 Application Curve

Refer to *Power Supply Recommendations* for additional information with regards to appropriate power dissipation. Figure 7 describes thermal dissipation based on Figure 14.

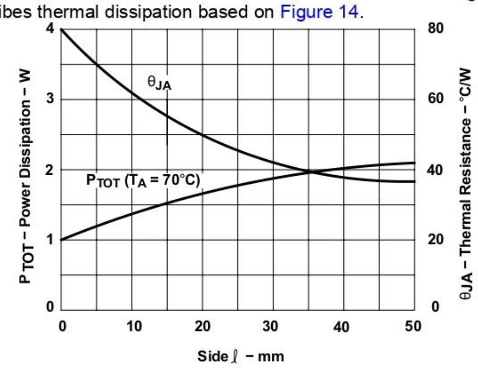


Figure 7. Maximum Power and Junction vs Thermal Resistance

9.3 System Examples

9.3.1 L293D as a Two-Phase Motor Driver

Figure 8 below depicts a typical setup for using the L293D as a two-phase motor driver. Refer to the *Recommended Operating Conditions* when considering the appropriate input high and input low voltage levels to enable each channel of the device.

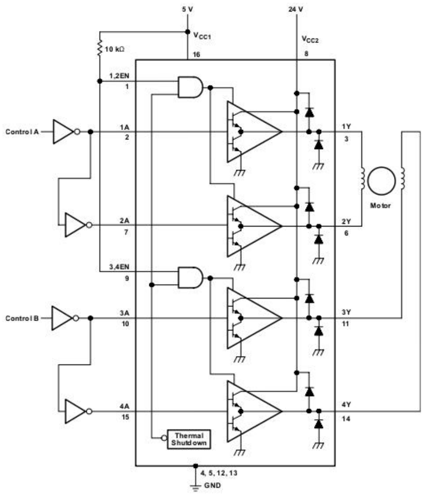
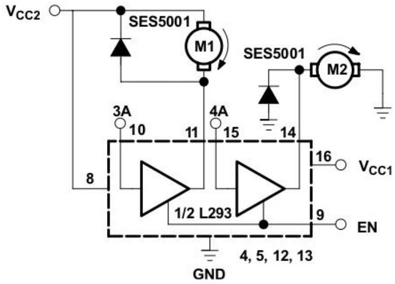


Figure 8. Two-Phase Motor Driver (L293D)

System Examples (continued)

9.3.2 DC Motor Controls

Figure 9 and Figure 10 below depict a typical setup for using the L293 device as a controller for DC motors. Note that the L293 device can be used as a simple driver for a motor to turn on and off in one direction, and can also be used to drive a motor in both directions. Refer to the function tables below to understand unidirectional vs bidirectional motor control. Refer to the *Recommended Operating Conditions* when considering the appropriate input high and input low voltage levels to enable each channel of the device.



Connections to ground and to supply voltage

Figure 9. DC Motor Controls

Table 2. Unidirectional DC Motor Control

EN	3A	M1 (1)	4A	M2
H	H	Fast motor stop	H	Run
H	L	run	L	Fast motor stop
L	X	Free-running motor stop	X	Free-running motor stop

(1) L = low, H = high, X = don't care

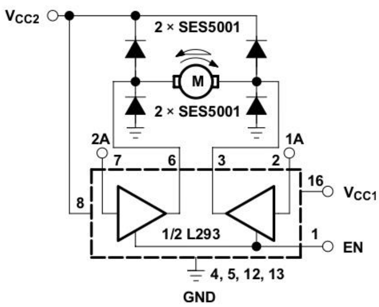


Figure 10. Bidirectional DC Motor Control

Table 3. Bidirectional DC Motor Control

EN	1A	2A	FUNCTION (1)
H	L	H	Turn right
H	H	L	Turn left

(1) L = low, H = high, X = don't care

Table 3. Bidirectional DC Motor Control (continued)

EN	1A	2A	FUNCTION (1)
H	L	L	Fast motor stop
H	H	H	Fast motor stop
L	X	X	Free-running motor stop

9.3.3 Bipolar Stepping-Motor Control

Figure 11 below depicts a typical setup for using the L293D as a two-phase motor driver. Refer to the *Recommended Operating Conditions* when considering the appropriate input high and input low voltage levels to enable each channel of the device.

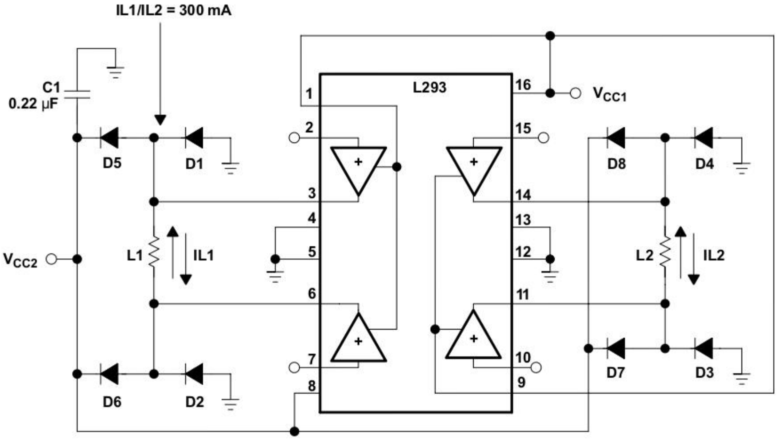


Figure 11. Bipolar Stepping-Motor Control

10 Power Supply Recommendations

V_{CC1} is 5 V ± 0.5 V and V_{CC2} can be same supply as V_{CC1} or a higher voltage supply with peak voltage up to 36 V. Bypass capacitors of 0.1 uF or greater should be used at V_{CC1} and V_{CC2} pins. There are no power up or power down supply sequence order requirements.

Properly heatsinking the L293 when driving high-current is critical to design. The Rthj-amp of the L293 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heat sink.

Figure 14 shows the maximum package power PTOT and the θJA as a function of the side of two equal square copper areas having a thickness of 35 µm (see Figure 14). In addition, an external heat sink can be used (see Figure 12).

During soldering, the pin temperature must not exceed 260°C, and the soldering time must not exceed 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

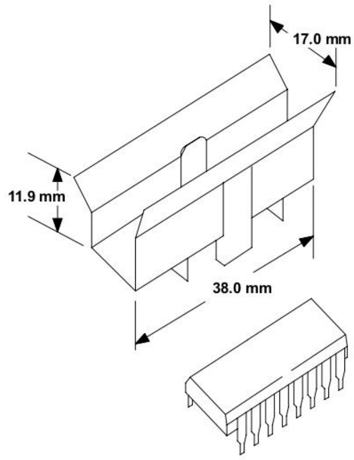


Figure 12. External Heat Sink Mounting Example (θ_{JA} = 25°C/W)

11 Layout

11.1 Layout Guidelines

Place the device near the load to keep output traces short to reduce EMI. Use solid vias to transfer heat from ground pins to ground plane of the printed-circuit-board.

11.2 Layout Example

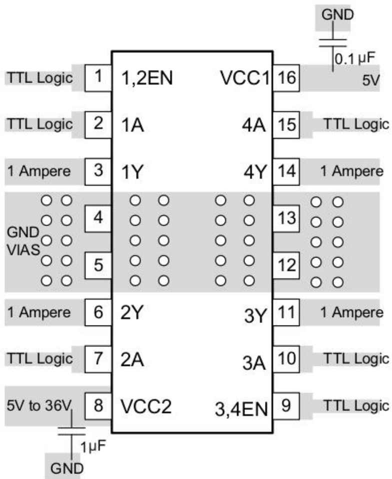


Figure 13. Layout Diagram

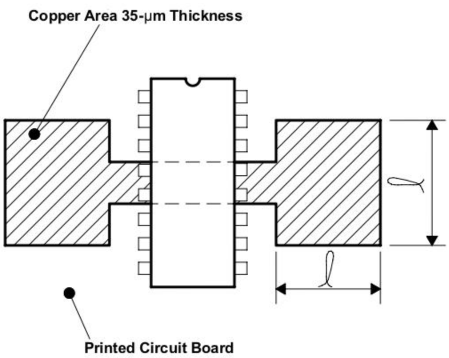


Figure 14. Example of Printed-Circuit-Board Copper Area (Used as Heat Sink)

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
L293	Click here	Click here	Click here	Click here	Click here
L293D	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TEXAS INSTRUMENTS

PACKAGE OPTION ADDENDUM

www.ti.com 17-Mar-2017

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
L293DNE	ACTIVE	PDIP	NE	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	L293DNE	Samples
L293DNEE4	ACTIVE	PDIP	NE	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	L293DNE	Samples
L293NE	ACTIVE	PDIP	NE	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	L293NE	Samples
L293NEE4	ACTIVE	PDIP	NE	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	L293NE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OPTION ADDENDUM

17-Mar-2017

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Anexo 1.7: Electroválvula

ANEXO 2: Código implementado

Anexo 2.1: Código Maestro

```
#include <VirtualWire.h>
//#include <VirtualWire_Config.h>

//Declaración de constantes
const int transmit_pin = 10; // Mensaje a modular.
const int receive_pin = 3; //Antes pin 11. Mensaje demodulada. 3**
const int CD4046 = 8; // Inhibit.


void setup() {

  Serial.begin(9600);
  vw_setup(220);

  vw_set_tx_pin(transmit_pin);
  vw_set_rx_pin(receive_pin);
  vw_rx_start();

  pinMode(CD4046, OUTPUT);
  digitalWrite(CD4046, LOW);

  delay(1000);

}

void loop() {

  uint8_t Mensaje_Correcto = 0;
  const char *msg1 = "T";
  const char *regar = "A";
  const char *no_regar = "C";
  int Numero_reenvios = 5;
  int reenvio_actual = 0;

  uint8_t buf[VW_MAX_MESSAGE_LEN];
  uint8_t buflen = VW_MAX_MESSAGE_LEN;

  Serial.println("Iniciando comunicacion");

  // While reenvioActual < N° reenvios
  while ((Mensaje_Correcto == 0) && (reenvio_actual < Numero_reenvios)) {

  digitalWrite(CD4046, LOW);
  delay(320);

  Serial.print("He enviado: ");
  vw_send((uint8_t *)msg1, strlen(msg1));
  vw_wait_tx();
  Serial.println(msg1);
  digitalWrite(CD4046, HIGH);

  reenvio_actual = reenvio_actual +1;
  Serial.print("Reenvio numero: ");
  Serial.println(reenvio_actual);
  long Tiempo_Maximo = 1000;
  long Tiempo_Envio = millis();
```

```
  while ((Mensaje_Correcto == 0) && (millis() - Tiempo_Envio < Tiempo_Maximo)) {

    if (vw_get_message((uint8_t *)buf, &buflen)) {
      Serial.print("He recibido ");
      Serial.print(buflen);
      Serial.print(" ");
      for( int i = 0; i < buflen; i++)
        Serial.print(buf[i], HEX);
        Serial.println();
      if (buflen == 2) {
          Mensaje_Correcto = 1;
      }
    }
    delay(50);
  }
  }

  if (Mensaje_Correcto == 1) {
    Serial.println("Mensaje correcto");
    int ValorSensor;
        ValorSensor = buf[0] << 8 | buf[1];
        Serial.print("Valor sensor recibido: ");
        Serial.println(ValorSensor);
    float Temperatura;
        Temperatura = (ValorSensor * 5.0)/(1024.0 * 0.01);
        Serial.print("Valor temperatura: ");
        Serial.println(Temperatura);

     if (Temperatura >= 28.0) {
        digitalWrite(CD4046, LOW);
        delay(320);
        Serial.println("Se debe regar");
        Serial.println("He enviado");
        vw_send((uint8_t *)regar, strlen(regar));
        vw_wait_tx();
        Serial.println(regar);
        digitalWrite(CD4046, HIGH);
      }
      if (Temperatura < 28.0) {
        digitalWrite(CD4046, LOW);
        delay(320);
        Serial.println("NO se debe regar");
        Serial.println("He enviado");
        vw_send((uint8_t *)no_regar, strlen(no_regar));
        vw_wait_tx();
        Serial.println(no_regar);
        digitalWrite(CD4046, HIGH);
      }

    }else
      Serial.println("Error de Conexion");
   delay(3000);

}
```

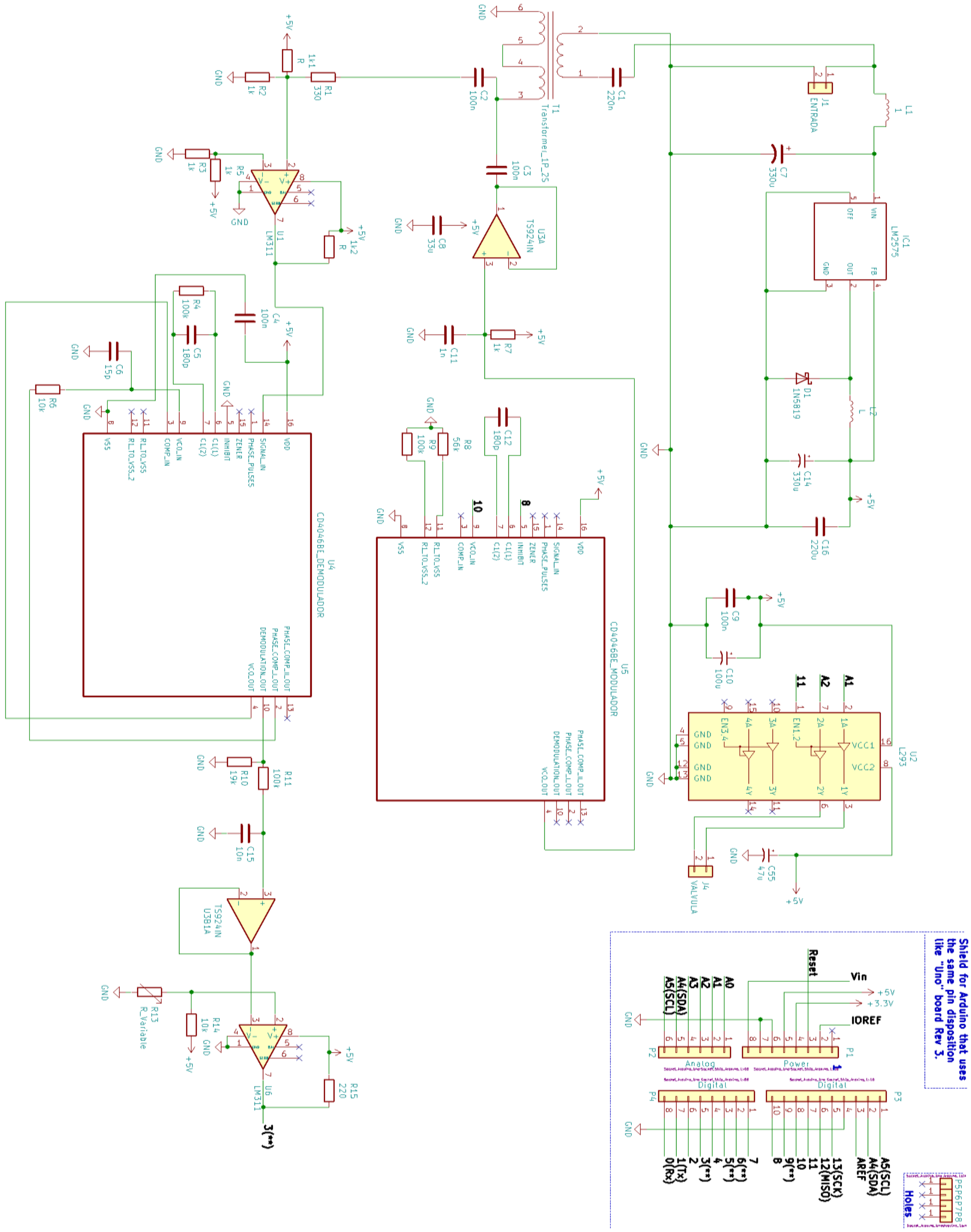
Anexo 2.2: Código Esclavo

```
#include <VirtualWire.h>

  const int transmit_pin = 10;
  const int receive_pin = 3;
  const int CD4046 = 8;
  const int ENABLEelectrovalvula = 11;
  const int Giro1 = A1;
  const int Giro2 = A2;

void setup() {

  Serial.begin(9600);
  vw_setup(220);

  vw_set_tx_pin(transmit_pin);

  vw_set_rx_pin(receive_pin);
  vw_rx_start();

  pinMode(ENABLEelectrovalvula, OUTPUT);
  digitalWrite(ENABLEelectrovalvula, false);///LOW

  pinMode(Giro1, OUTPUT);
  digitalWrite(Giro1, LOW);

  pinMode(Giro2, OUTPUT);
  digitalWrite(Giro2, LOW);

  pinMode(CD4046, OUTPUT);
  digitalWrite(CD4046, HIGH);

}


int Tiempo_mensaje = 0;

void loop() {

  uint8_t buf[VW_MAX_MESSAGE_LEN];
  uint8_t buflen = VW_MAX_MESSAGE_LEN;
  uint8_t Mensaje_Correcto = 0;
  int i;

    if (millis() - Tiempo_mensaje >= 200){
        Serial.println("Comprobando existencia mensaje");
        Tiempo_mensaje = millis();
    }

       if (vw_get_message(buf, &buflen)){
            Serial.println("Recibiendo mensaje");
            Serial.print("He recibido: ");
            for(i = 0; i < buflen; i++)
                Serial.print((char)buf[i]);
               Serial.println();
            if ((char)buf[0] == 'T') {
              Serial.println("Mensaje correcto");

              unsigned int ValorSensor = 0;
              float Voltaje = 0.0;
              float Temperatura = 0.0;
              Serial.print("Valor de sensor enviado: ");
              ValorSensor = analogRead(A5);
              Serial.println(ValorSensor);
```

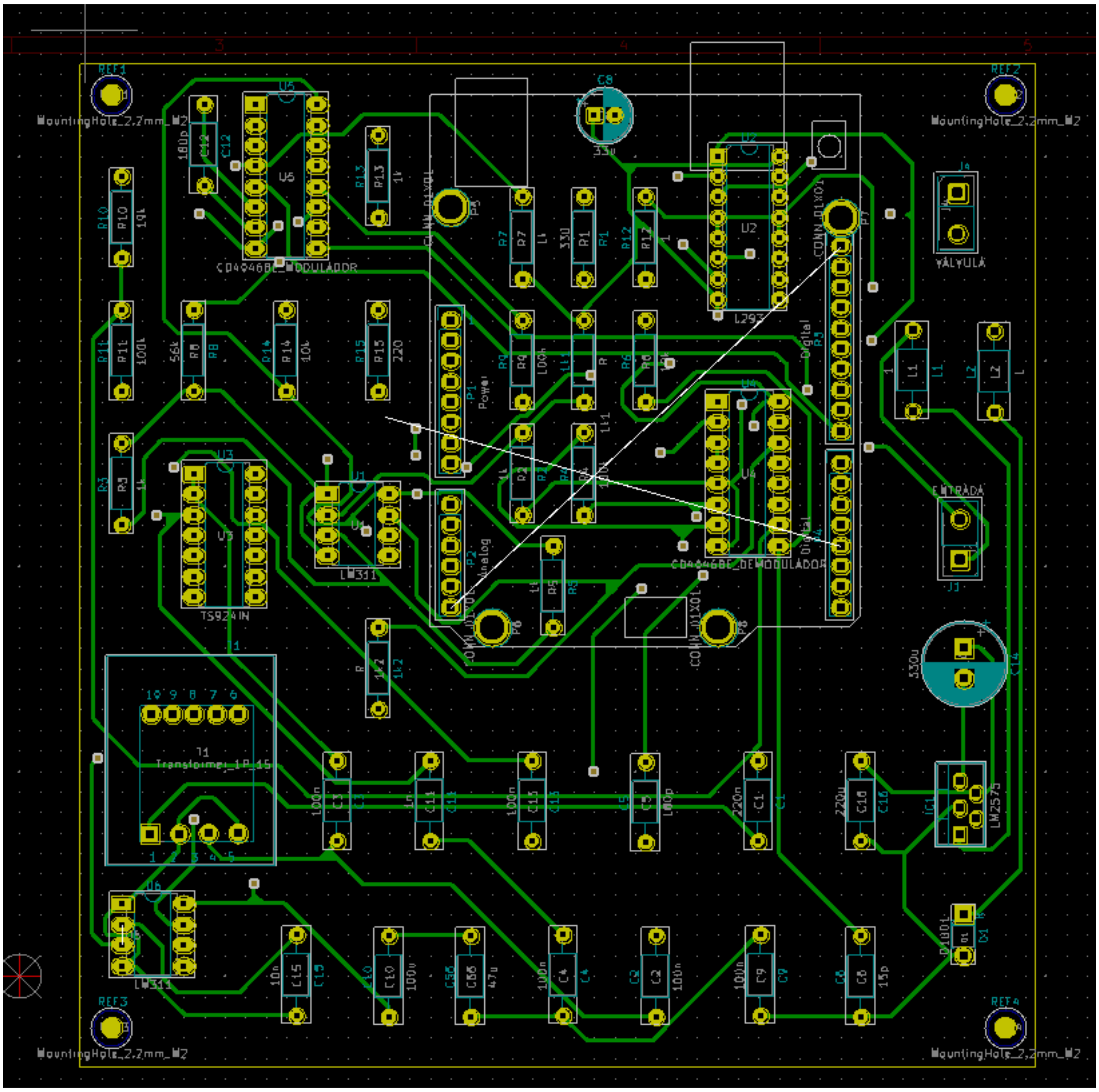
```
      Serial.print("Voltaje sensor: ");
      Voltaje = (ValorSensor* 5.0)/1024.0;

      Serial.println(Voltaje);

      Temperatura = Voltaje/0.01;
      Serial.print("Valor temperatura: ");
      Serial.println(Temperatura);

      uint8_t Envio[2];
      Envio[0] = (ValorSensor >> 8);
      Envio[1] = (ValorSensor & 0xFF);
      digitalWrite(CD4046, LOW);
      delay(50);
      vw_send((uint8_t *)Envio, 2);
      vw_wait_tx();
      Serial.print("Valor en HEXADECIMAL: ");
      Serial.print(Envio[0],HEX);
      Serial.println(Envio[1],HEX);
      digitalWrite(CD4046, HIGH);
    }

    //  Se añade acción electroválvula. Se modifica el código para comprobar el
    // funcionamiento de la electroválvula.
    if((char)buf[0] == 'A') {
     Serial.println("Se debe regar");
     digitalWrite(ENABLEelectrovalvula, true);
     digitalWrite(Giro1, HIGH); // Se abre la electroválvula.
     digitalWrite(Giro2, LOW);
     delay(20);
     digitalWrite(ENABLEelectrovalvula, true);
     digitalWrite(Giro2, HIGH); // Se cierra la electroválvula.
     digitalWrite(Giro1, LOW);
     delay(20);
     digitalWrite(Giro1, LOW);
     digitalWrite(Giro2, LOW);
     digitalWrite(ENABLEelectrovalvula, false);
     delay(2000);
    }
    if((char)buf[0] == 'C') {
      Serial.println("NO se debe regar");
      digitalWrite(ENABLEelectrovalvula, false);
    }else
      Serial.println("Mensaje no correcto");
  }
  delay(200);

}
```

ANEXO 3: ESQUEMAS DE LA PCB

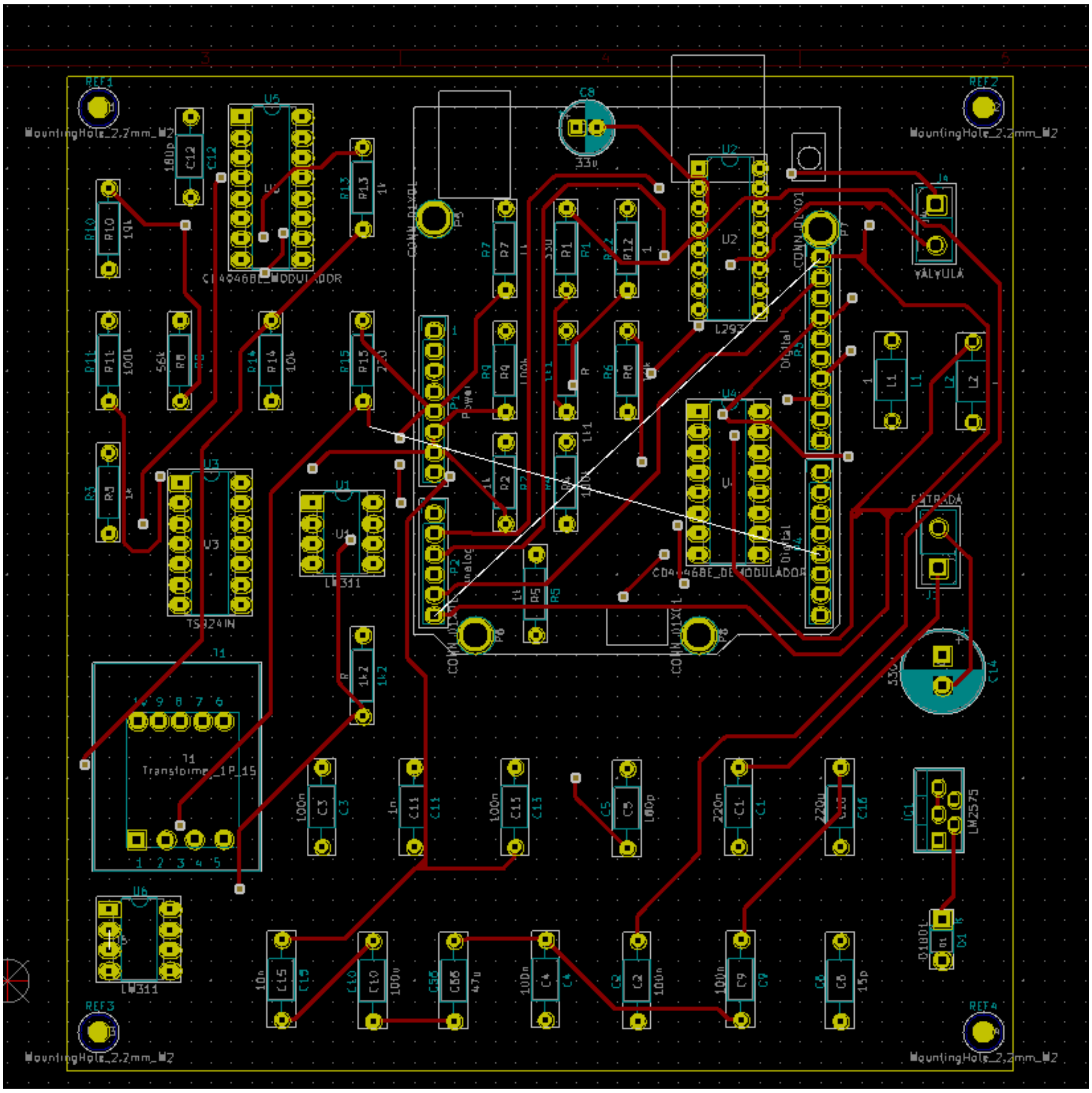
Anexo 3.1: Esquemático



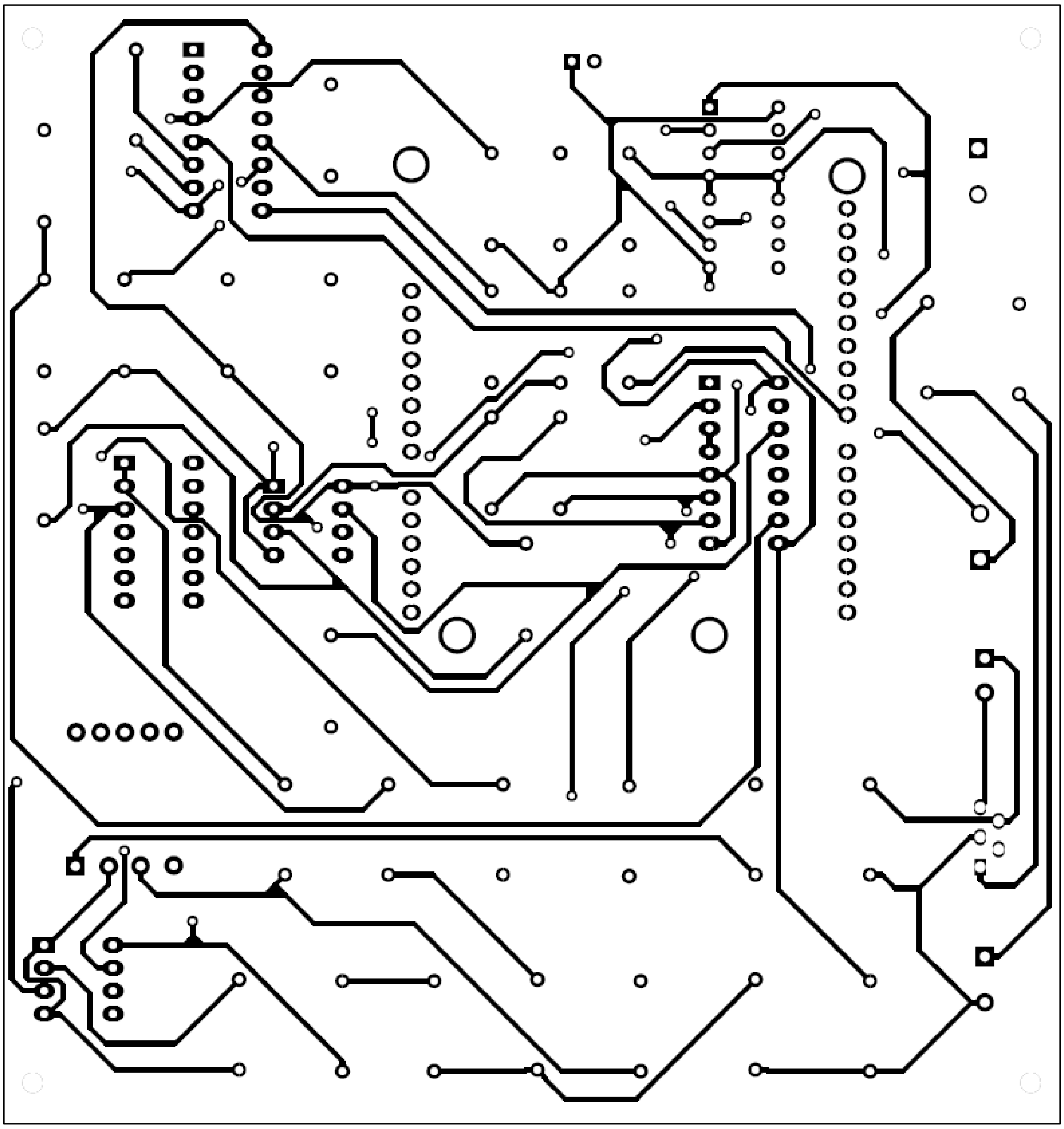
Anexo 3.2: Cara *botom*



Anexo 3.3: Cara *top*



Anexo 3.4: Transparencias cara *botom*



Anexo 3.5: Transparencias cara *top*