Escuela Superior
de Ingeniería y Tecnología
Universidad de La Laguna

TRABAJO FIN DE GRADO

Montaje, prueba y calibración de sistemas de encefalografía EEG OPEN-BCI

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Capítulo 0
Abstract, resumen y objetivos

0.1 ABSTRACT

The objective of this TFG was to assemble, test and calibrate two electroencephalography OPENBCI systems.

On the one hand, the OpenBCI 4-channel Headband and on the other hand the Ultracortex IV both 8-channel and 16-channel.

When the assembly was finished, different tests were carried out with different people, so that different responses obtained could be verified and analyzed.

Keywords:

Encephalography, OPENBCI

0.2 RESUMEN

El objetivo de este TFG fue montar, probar y calibrar dos sistemas de electroencefalografía de OpenBCI.

Por un lado, la Headband de OpenBCI de 4 canales y por otro lado el Ultracortex IV tanto de 8 canales como de 16.

Cuando el montaje se finalizado, se realizaron distintas pruebas con personas diferentes, de tal manera que se pudo comprobar y analizar las diferentes respuestas obtenidas.

Palabras clave:

Encefalografía, OPENBCI

0.3 OBJETIVOS

El objetivo principal de este trabajo fue montar, probar y calibrar dos sistemas OPENBCI.

- OpenBCI EEG Headband Kit
- OpenBCI Ultracortex Mark IV EEG Headset

Del primer sistema se trabajó con 4 canales y del segundo se trabajó tanto con 8 canales como con 16.

Finalmente, tras realizar varias pruebas, los resultados obtenidos fueron analizados.

Capítulo 1
Introducción

1. INTRODUCCIÓN

La electroencefalografía (EEG) es una técnica/prueba que se usa para el estudio de la actividad eléctrica cerebral mediante electrodos. Permite detectar alteraciones que afecten al sistema nervioso como por ejemplo epilepsia, depresión, traumatismos craneoencefálicos, tumores cerebrales…

En este TFG, vamos a trabajar con dos sistemas EEG:

- OpenBCI EEG Headband Kit
- OpenBCI Ultracortex Mark IV EEG Headset

1.1 Cerebro y neuronas:

Las células de nuestro celebro se comunican entre si mediante impulsos eléctricos y neurotransmisores generados en células del sistema nervioso. Estas células nerviosas se denominan neuronas y están activas todo el tiempo, incluso cuando dormimos.

El cerebro humano tiene entre 80 – 100 millones de neuronas. Todas ellas en conjunto forman redes neuronales y junto con las células gliales conforman el sistema nervioso.

1.2 Electroencefalografía

Un electroencefalograma, es una técnica/prueba que se usa para el estudio de la actividad eléctrica cerebral mediante electrodos.

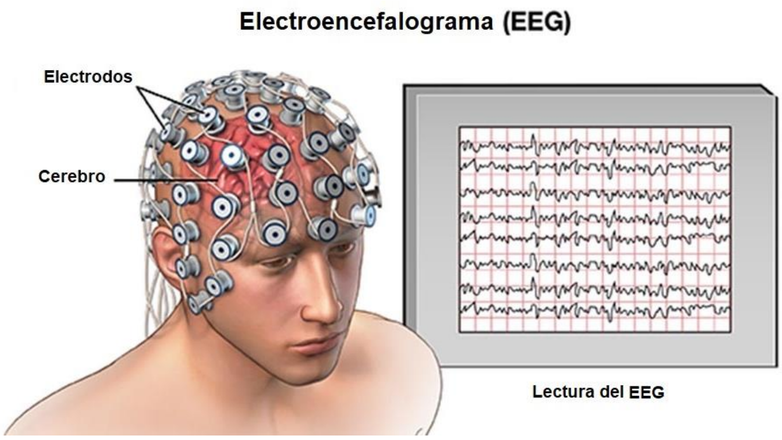


Figura 1 Electroencefalograma [1]

Permite detectar alteraciones que afecten al sistema nervioso como por ejemplo traumatismos craneoencefálicos, tumores cerebrales, cefaleas, enfermedades infecciosas, vasculares, degenerativas, consumo de drogas, intoxicaciones…

Comúnmente es utilizado para problemas del sueño, casos de epilepsia y depresión.

El análisis de esta prueba se puede observar en la lectura gráfica del EEG.

1.2.1 Ondas encefálicas:

Los electrodos son ubicados en diferentes zonas del cráneo y registran las ondas encefálicas.

Estas, también denominadas ondas cerebrales, se clasifican de acuerdo a su longitud de onda o su frecuencia (Hz).

Existen 5 tipos y se pueden organizar desde las más rapidas a las más len tas:

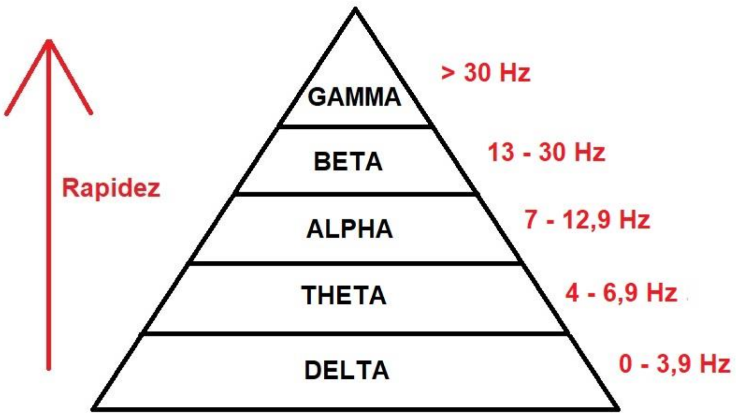
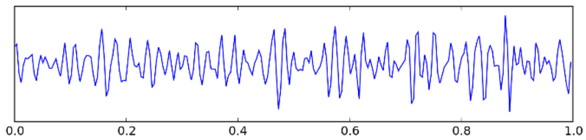
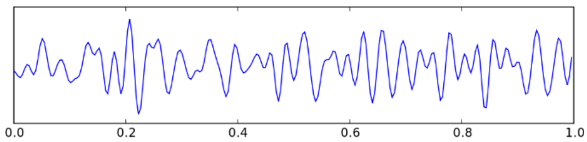
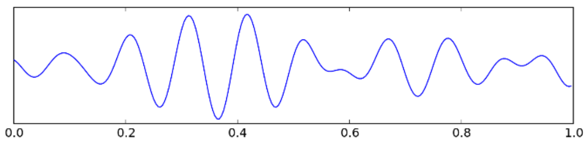
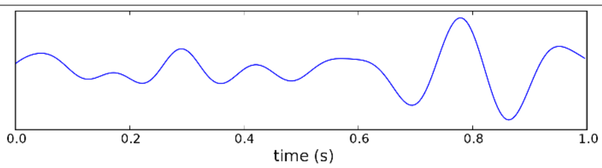
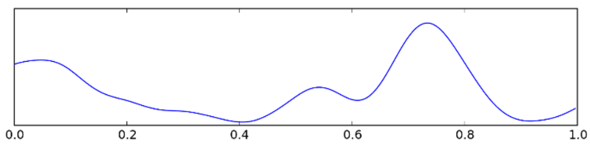


Figura 2 - Clasificación de ondas encefálicas según su rapidez

Tabla 1 - Características de las ondas cerebrales

Tipo de onda	Frecuencia (Hz)	Estados representativos	Forma de onda
Gamma	>30	Máximo nivel de estrés y confusión.	 *Figura 3 Onda Gamma [2]*
Beta	13 – 30	Estado de alerta y concentración profunda.	 *Figura 4 Onda Beta [3]*
Alpha	7 – 12,9	Estado de relajación, tranquilidad, creatividad. Actividad plena del hemisferio izquierdo, desconexion del derecho	 *Ilustración 5 Onda Alpha [4]*
Theta	4 – 6,9	Estado de vigilia, plenitud,armonía. Equilibrio entre ambos hemisferios	 *Figura 6 Onda Theta [4] [5]*
Delta	0 – 3,9	Estado hipnótico, sueño profundo, meditación… Hemisferio cerebral derecho totalmente activo.	 *Figura 7 Onda Delta [6]*

Capítulo 2
Software EEG utilizado (OpenBCI Hub y OpenBCI GUI)

OpenBCI Hub es un software utilizado para comunicarse con placas OpenBCI a través del protocolo de comando TCP / IP.

Las siglas TCP/IP se refieren a un conjunto de protocolos para comunicaciones de datos. Este conjunto toma su nombre de dos de sus protocolos más importantes, el protocolo TCP (Transmission Control Protocol) y el protocolo IP (Internet Protocol).

La GUI de OpenBCI es una herramienta de software para visualizar, grabar y transmitir datos EEG captados por las placas de OpenBCI. Los datos pueden mostrarse en tiempo real, reproducirse, guardarse en formato .txt, así como transmitirse en tiempo real a softwares de terceros como MATLAB.
Se puede iniciar como una aplicación independiente o mediante un lenguaje de programación basado en Java. [7]

Para cualquier placa que usemos primero se debe conectar el USB correspondiente, después abrir OpenBCI Hub y por último la GUI.

En este TFG he trabajado con la versión 3.3.1 (Mayo 2018) así como también con la 4.2.0 (Enero 2020). Para esta última versión, no hizo falta abrir Hub manualmente, ya que al abrir la herramienta GUI se ejecuta automáticamente.

En los capítulos siguientes explicaré las placas que hemos usado en este trabajo y qué se debe hacer para ejecutar la aplicación GUI correctamente con cada una.

Extracción de datos de OpenBCI GUI:

Cada vez que se transmiten datos de las placas a la GUI, se guardan automáticamente en formato .csv (valores separados por comas) o .txt (archivos de texto) en su ordenador.
Se puede seleccionar la preferencia que quiera el usuario en la pestaña "SavedData.pde" desde Java. Si no, por valor predeterminado, se guardarán como .txt.
Los datos y las grabaciones de la GUI se guardan en / Documentos / OpenBCI_GUI / Recordings / en todos los sistemas operativos.

Ejemplo (8 canales):

%Number of channels = 8 (Número de canales)
%Sample Rate = 250.0 Hz (Frecuencia de muestreo)
%First Column = SampleIndex
%Last Column = Timestamp
%Other Columns = EEG data in microvolts followed by Accel Data (in G) interleaved with Aux Data
0, 39083.86, -5400.40, -29377.25, -39752.26, -35053.10, -31536.37, -104373.28, -5372.64, 0.000, 0.000, 0.000, 15:26:19.224
1, 41962.49, -3918.98, -28189.44, -40297.15, -33924.70, -30291.42, -106796.41, -6910.38, 0.018, 0.678, 0.302, 15:26:19.225

Sample Index
Índice de muestra

EEG data in microvolts
Datos EEG en microvoltios

Accel data
Datos de aceleración

Timestamp
Marca de tiempo

Figura 8 - Datos recogidos en un archivo de texto (.txt) mediante la aplicación GUI y explicación de sus parámetros. (Sistema 8 electrodos)

Ejemplo (16 canales):

%OpenBCI Raw EEG Data

%Number of channels = 16

%Sample Rate = 125.0 Hz

%First Column = SampleIndex

%Last Column = Timestamp

%Other Columns = EEG data in microvolts followed by Accel Data (in G) interleaved with Aux Data

0, -187500.02, -187500.02, -172217.30, -171392.66, -187500.02, -187500.02, -187500.02, -187500.02, 75931.66, -93750.01, -93750.01, -83648.43, -83506.77, -93750.01, -82152.05, -81283.79, 0.044, 0.918, 0.334, 13:18:58.751

1, -93750.01, -93750.01, -89720.97, -90328.52, -93750.01, -93750.01, -93750.01, -93750.01, 155070.78, -187500.02, -187500.02, -176819.95, -168690.36, -187500.02, -169415.33, -170413.25, 0.000, 0.000, 0.000, 13:19:25.561

2, -187500.02, -187500.02, -176645.73, -178093.55, -187500.02, -187500.02, -187500.02, -187500.02, 155084.88, -187500.02, -187500.02, -175931.72, -170952.69, -187500.02, -169966.41, -169978.78, 0.000, 0.000, 0.000, 13:19:25.561

3, -187500.02, -187500.02, -175723.58, -175376.47, -187500.02, -187500.02, -187500.02, -187500.02, 155076.89, -187500.02, -187500.02, -176070.72, -170746.22, -187500.02, -169990.39, -170103.44, 0.000, 0.000, 0.000, 13:19:25.561

4, -187500.02, -187500.02, -176756.47, -178274.56, -187500.02, -187500.02, -187500.02, -187500.02, 155066.00, -187500.02, -187500.02, -176751.23, -168962.22, -187500.02, -169405.67, -170354.47, 0.044, 0.916, 0.346, 13:19:25.561

5, -187500.02, -187500.02, -180347.09, -180475.75, -187500.02, -187500.02, -187500.02, -187500.02, 155219.66, -187500.02, -187500.02, -175411.13, -172461.98, -187500.02, -170473.58, -169780.53, 0.000, 0.000, 0.000, 13:19:25.561

6, -187500.02, -187500.02, -177485.50, -177942.98, -187500.02, -187500.02, -187500.02, -187500.02, 155019.02, -187500.02, -187500.02, -176794.45, -168837.70, -187500.02, -169404.92, -170406.86, 0.000, 0.000, 0.000, 13:19:25.562

7, -187500.02, -187500.02, -174045.92, -175643.09, -187500.02, -187500.02, -187500.02, -187500.02, 155085.41, -187500.02, -187500.02, -175947.72, -170930.16, -187500.02, -169962.84, -169987.77, 0.000, 0.000, 0.000, 13:19:25.562

8, -187500.02, -187500.02, -178468.72, -177924.94, -187500.02, -187500.02, -187500.02, -187500.02, 155157.41, -187500.02, -187500.02, -176100.30, -170637.38, -187500.02, -170022.30, -170119.81, 0.000, 0.000, 0.000, 13:19:25.563

9, -187500.02, -187500.02, -179338.09, -180660.36, -187500.02, -187500.02, -187500.02, -187500.02, 155091.11, -187500.02, -187500.02, -176765.56, -168747.80, -187500.02, -169409.23, -170362.38, 0.044, 0.914, 0.342, 13:19:25.563

10, -187500.02, -187500.02, -177576.17, -177864.22, -187500.02, -187500.02, -187500.02, -187500.02, 155166.56, -187500.02, -187500.02, -175396.23, -172431.08, -187500.02, -170455.58, -169775.73, 0.000, 0.000, 0.000, 13:19:25.563

Figura 9 - Ejemplo de recogida de datos en un archivo de texto (.txt) mediante la aplicación GUI. (Sistema de 16 electrodos)

Capítulo 3
Dispositivo de 4 electrodos
(Open BCI EEG Headband Kit)

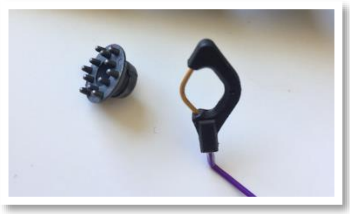
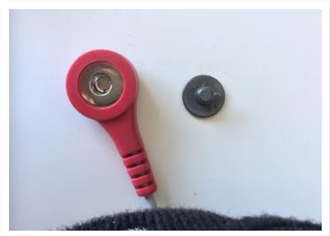
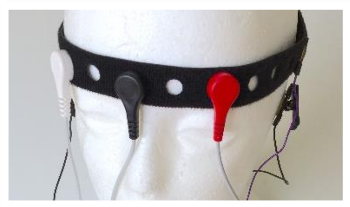
3.1 Especificaciones EEG Headband Kit

Figura 10 Uno de los sujetos participantes en las pruebas de este TFG con el sistema de 4 electrodos (Headband Kit)

El OpenBCI EEG Headband kit es un pack de inicio en forma de diadema para mediciones de EEG.

Los cables incluidos en este kit son compatibles con todas las placas de biosensores OpenBCI; Cyton, Ganglion y CytonDaisy.

Tabla 2 Componentes Headband Kit (Ref. [13])

	1. Dos electrodos con clip para las orejas.
	2. Cinco cables conductores estándar para electrodos puntiagudos, es decir, cables de alambre tipo clip.
	3. Tres cables conductores para electrodos planos. (Blanco, negro y rojo)
	4. Una diadema de velcro para la sujeción de los electrodos en la cabeza.

Además de lo expuesto en esta tabla, este kit también incluye: Electrodos de oreja de repuesto, electrodos planos de repuesto y electrodos puntiagudos de repuesto (2 mm).

3.2 Placa Ganglion y Hardware

- **Ganglion Board**

Ganglion board es una placa de cuatro canales de entrada que puede medir EEG / EMG / ECG y transmitir los datos a través de bluetooth.

Tabla 3 - Especificaciones generales placa Ganglion

Canales	4
Alimentación	3.3V-12V (Solo batería)
Consumo de corriente (inactivo)	14 mA
Consumo de corriente (Conectado y transmisión de datos)	15 mA
Transmisión	Simblee BLE (Bluetooh Low Energy) radio module (Compatible con arduino)
Amplificador de ganancia	AD8237
Nº bits ADC	24
Velocidad de muestreo	200 Hz en cada uno de los canales
Conexión y desconexión de las entradas a los pines de referencia	Interruptores manuales (switches)

Los electrodos se conectan al amplificador AD8237, ver figura 11. El AD8237 tiene una impedancia de entrada diferencial de 100 MΩ.

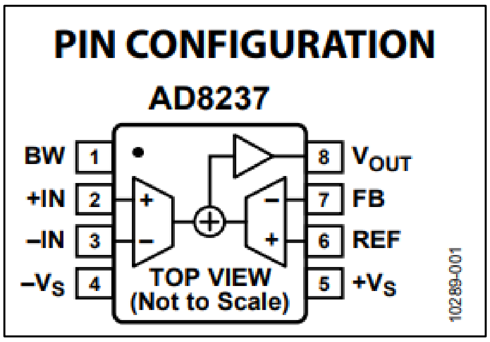


Figura 11 - Amplificador AD8237. Para ver el datasheet de este circuito, ver Anexo 1.

Este amplificador tiene entradas diferenciales. El data sheet de este circuito se puede encontrar en el Anexo 1.

La placa cuenta con una tierra activada, un suministro de voltaje positivo (Vdd) y un suministro de voltaje negativo (Vss)

Por otro lado, la digitalización se logra mediante el componente MCP3912. Este es un AFE (Analog-Front-End) de cuatro canales de 3V. Contiene cuatro convertidores de muestreo síncrono Delta-Sigma ADC (Analog-to-digital converter) y 24 bits diseñado para medidores de potencia. [10]

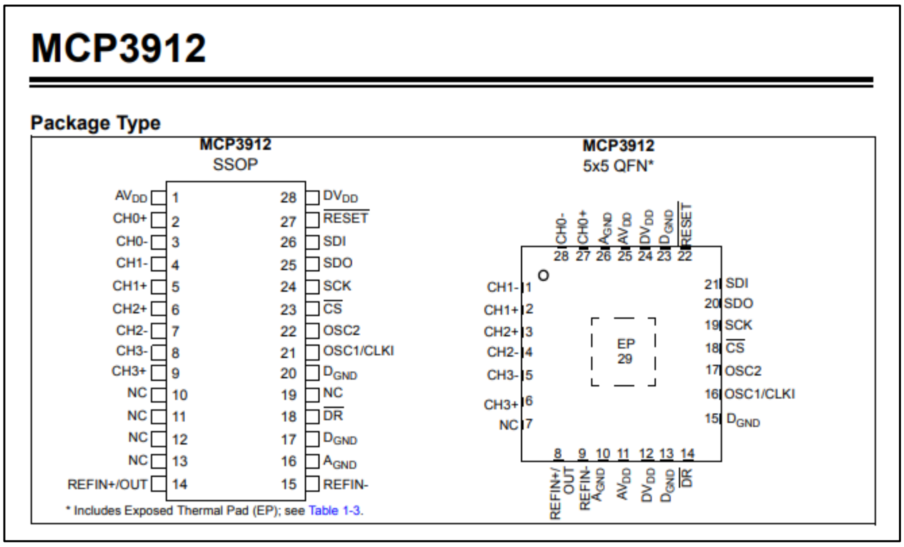


Figura 12 – MCP3912: Circuito integrado encargado de compensar el retardo de fase, así como también el error de la ganancia en los registros de calibración, entre otros (ver Anexo 2).

Los datos se muestrean en el conversor analógico-digital a 200Hz en cada uno de los cuatro canales de entrada de la placa.

Figura 13 Placa controladora del sistema EEG de 4 canales denominada Ganglion board [12]

Todas las placas OpenBCI se envían con un soporte de batería para 4 pilas tipo AA estándar, la cual hemos usado en este trabajo.

Aunque, se recomienda que compremos la batería y el cargador usb LiPo por su larga vida útil, tamaño compacto y compatibilidad con todas las placas OpenBCI.

La placa Ganglion viene con 4 piezas de plástico que se pueden encajar en los agujeros de su placa para proporcionar estabilidad adicional mientras trabajamos. [12]

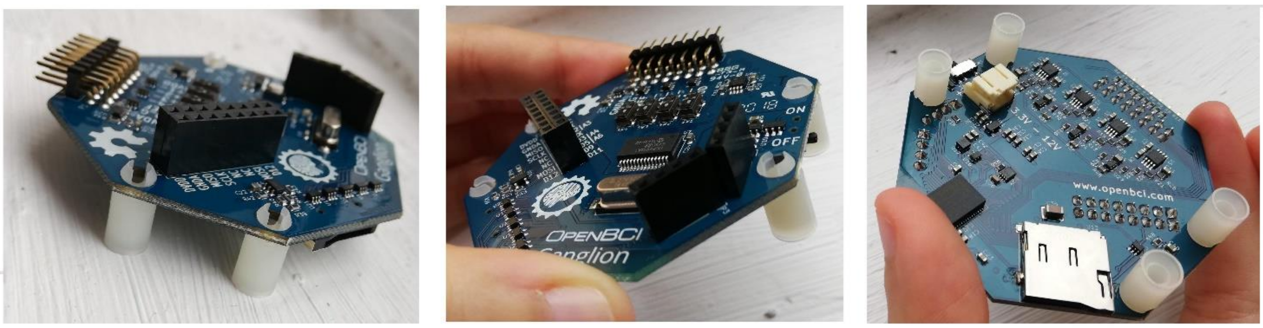


Figura 14 Piezas plásticas para mejorar la estabilidad de la placa Ganglion

- **Ganglion Dongle**

Figura 15 Bluetooh CSR 4.0 Dongle

CSR 4.0 Dongle es un adaptador mini USB bluetooth de versión 4.0 que cuenta con alta velocidad de transferencia y simple emparejamiento (Plug&Play). Es compatible con la mayoría de laptops y ordenadores, es rápido y fácil de configurar [13]. Además, incluye un disco pequeño para llevar a cabo la instalación del CSR Harmony Wireless Software Stack.

Este USB Dongle solo es necesario si vamos a usar una placa Ganglion con Mac, Windows o Linux. Si estamos trabajando con la placa Cyton, no necesitaríamos este dongle.

- **Alimentación Ganglion board**

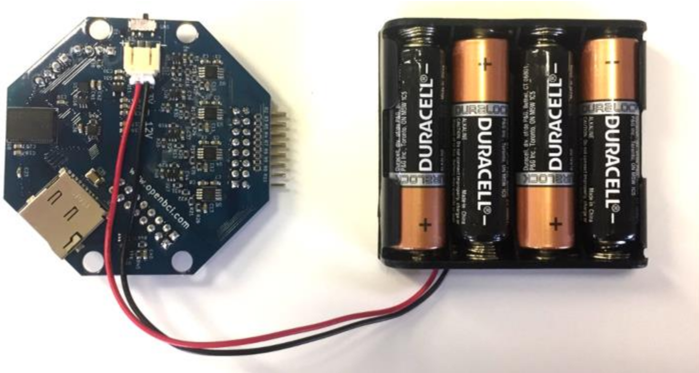


Figura 16 Conexión de la placa Ganglion (izquierda) con su alimentación (derecha) [12]

La placa Ganglion se alimenta conectándola con un paquete de 4 pilas AA. Cuando le damos al interruptor de encendido, vemos que el LED azul situado en D2 parpadea suavemente. El parpadeo significa que la radio BLE (Bluetooh Low Energy) no está conectada o emparejada con ningún ordenador o teléfono / tableta. Una vez que el Ganglion está conectado, el LED permanecerá encendido.

Aunque no fue nuestro caso, cabe remarcar que, si se usa un soporte de batería que no sea de OpenBCI, se debe verificar la polaridad (rojo + / negro -) antes de encender la placa OpenBCI. Pues, una polaridad invertida podría quemar la placa.

- **Hardware Ganglion**

En la placa Ganglion hay 4 interruptores deslizantes pequeños (SW1, SW2, SW3, SW4) que se pueden configurar para conectar las entradas a su pin asociado o al pin de referencia (REF). [15]

La posición predeterminada para estos interruptores cuando recibimos la placa es hacia arriba, que conecta cada entrada a su pin diferencial. Ver figura 17.

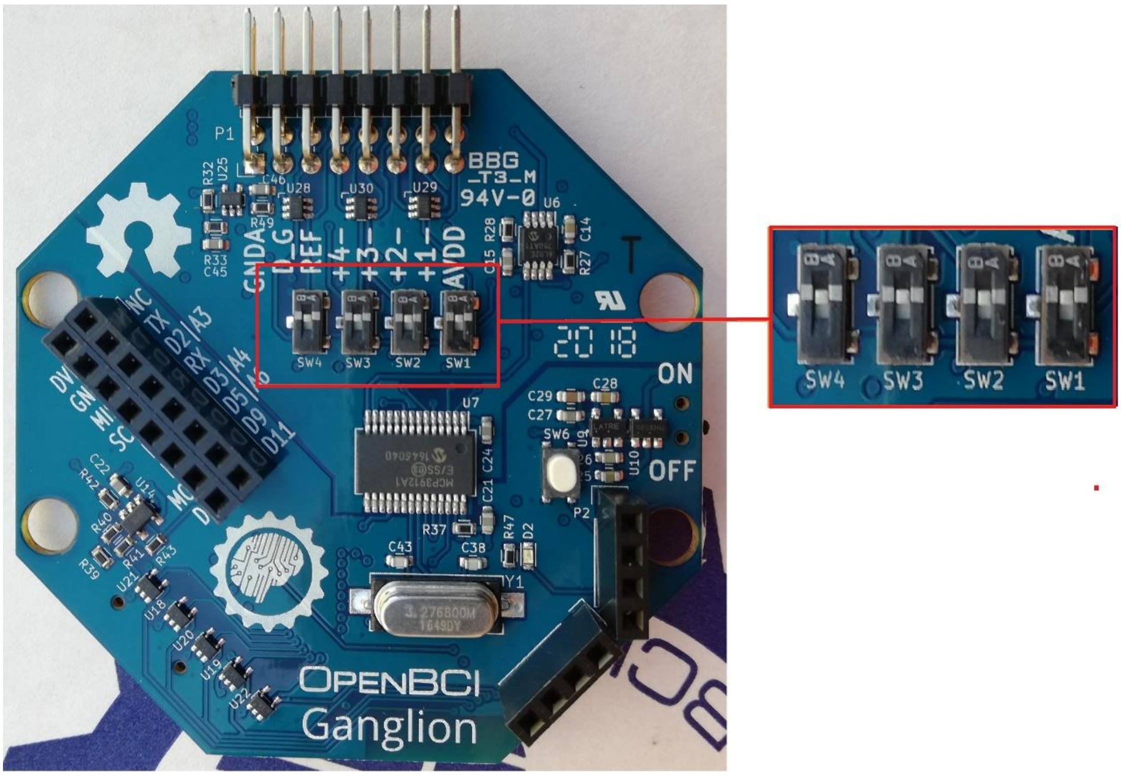


Figura 17 Interruptores en posición predeterminada (hacia arriba)

Para nuestro TFG tuvimos que mover los interruptores hacia abajo, así cada entrada – de cada canal asociado es conectado a su pin **REF**. Ver figura 18.

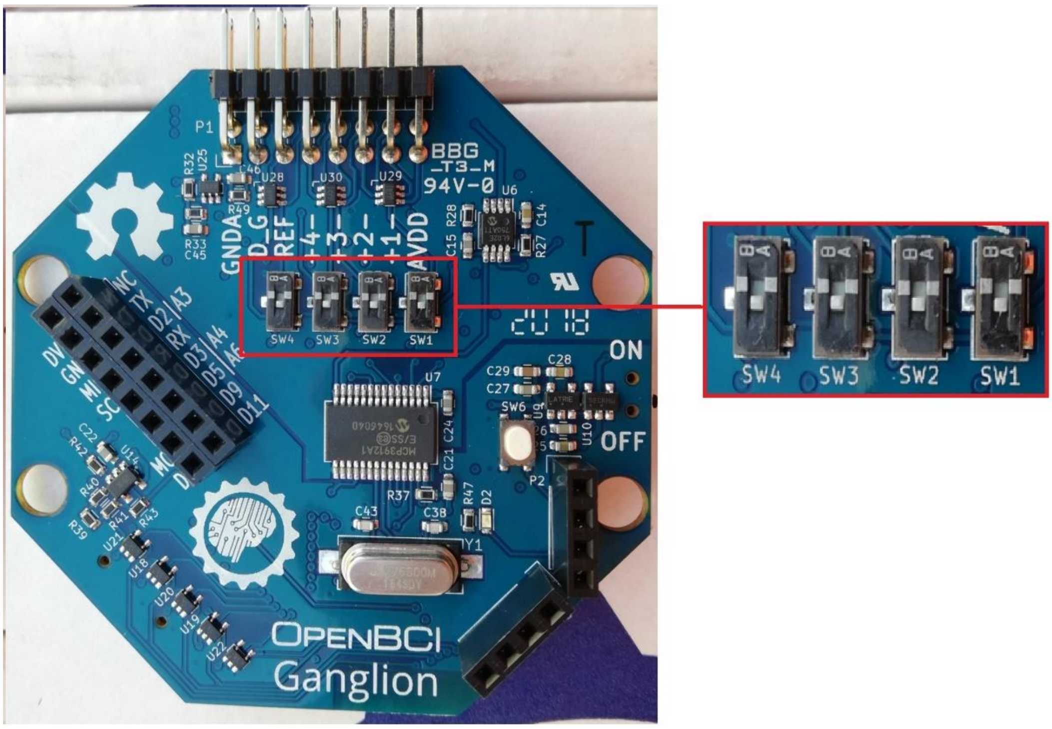


Figura 18 Interruptores en posición hacia abajo para conectar con pin REF

Esto nos permite 'agrupar' algunos o todos los pines juntos si estamos leyendo EEG, como fue nuestro caso, o por alguna otra razón para la cual queramos combinar dos o más pines.

Para entender más en profundidad el porqué de este paso de inversión de los interruptores, recomiendo que visiten las páginas del hardware Ganglion en las referencias [12] y [16], dónde también podemos encontrar los esquemas del circuito de la placa.

3.3 Montaje Headband Kit

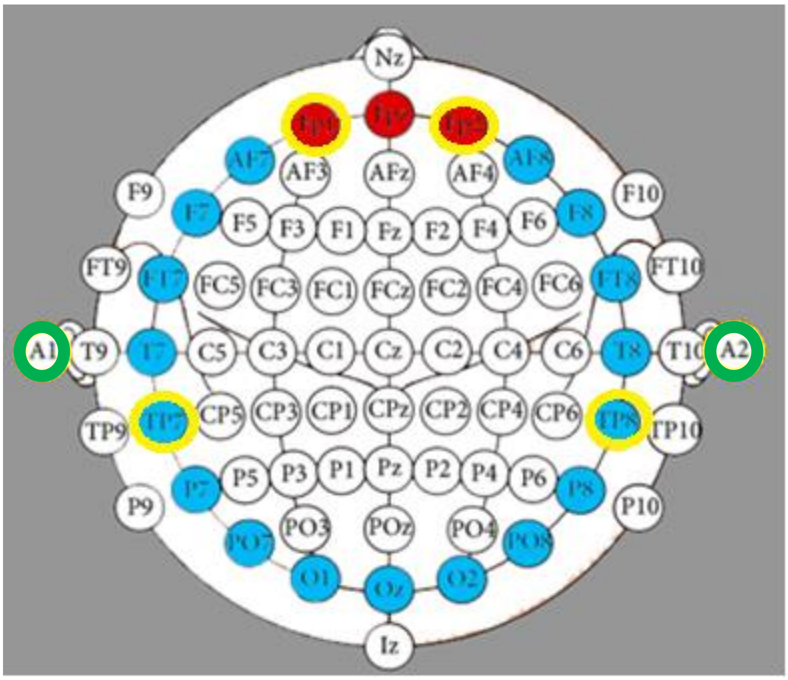


Figura 19 Distribución ubicaciones posibles de electrodos en la cabeza de la Headband (4 electrodos) según el sistema internacional "10-20 system" de posicionamiento de electrodos.. Redondeado en amarillo se muestran las posiciones elegidas para nuestro sistema, en verde (A1 y A2) se observa las posiciones de los clips de oreja. Se eligieron estas posiciones ya que son las recomendadas en la página de OpenBCI. [14]

Los círculos rojos representan áreas donde se pueden colocar electrodos planos, y los círculos azules donde se pueden colocar electrodos puntiagudos.

La distribución de estos depende de nosotros y de las áreas que queramos registrar.

La colocación realizada en este TFG fue la de los círculos en amarillo, siendo el A1 y A2 clips para oreja.

De los tres cables que disponíamos (rojo, blanco y negro) para electrodos planos, necesitamos únicamente dos cables. En mi caso, escogí aleatoriamente el rojo y el blanco, para posiciones FP1 y FP2.

En TP7 y TP8, se colocaron los cables tipo clip (violeta y azul) y electrodos puntiagudos.

- **Placa Ganglion para Headband Kit:**

Lo primero que se debe hacer es conectar el Dongle USB a nuestro ordenador e introducir el CD que también nos viene junto a este USB para realizar la instalación del mismo.
De esta forma se ejecutará el instalador para que nuestro ordenador tenga Bluetooth 4.0, y así poder conectar cualquier dispositivo de bluetooth. En nuestro caso, lo necesitamos para conectar nuestra placa Ganglion al ordenador de forma inalámbrica.
Más adelante, en el apartado 3.3.2 en “Procedimiento de preparación del CSR 4.0 USB”, veremos ciertas modificaciones que se deben hacer para tener preparado el CSR 4.0 para la conexión con la placa.

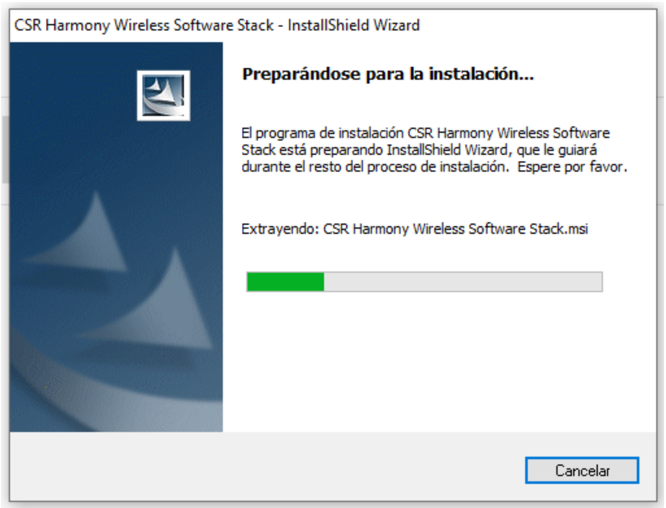


Figura 20 Captura de pantalla tomada al inicio de la instalación del Dongle USB

El siguiente paso fue descargar e instalar el software OpenBCI GUI y OpenBCIHub desde la página web oficial. [17-18] En mi caso, descargué la versión 3.0.1. [26]

- **Montaje de la placa con la headband [14]:**

Antes que nada, se debe tener en cuenta el proceso de inversión de los interruptores. (Ver apartado Hardware de la placa Ganglion)
Conectamos la alimentación de la placa, y para una mejor estabilidad los 4 soportes plásticos (Ver Figura 14 y 16).

Pasos de montaje:

1. Conectamos un clip de oreja al pin D_G superior (tierra activada).

2. Conectamos el segundo clip de oreja al pin REF superior.

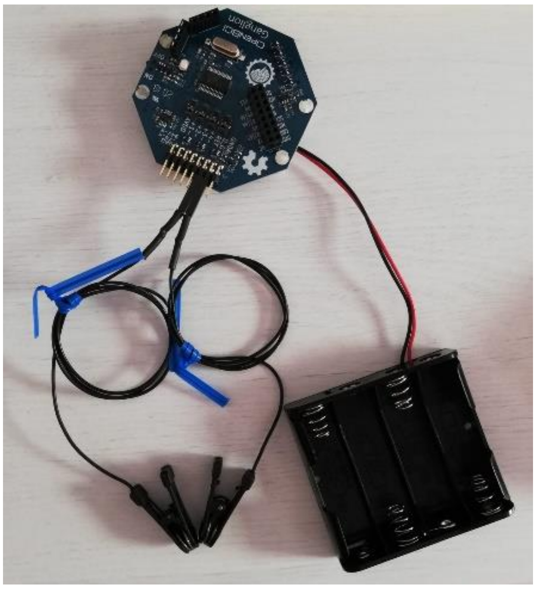


Figura 21 Conexiones de los clips de oreja: D_G superior y REF.

3. Conectamos las terminaciones hembra de los dos electrodos planos y dos electrodos puntiagudos a los pines superiores 1-4, como se muestra en la Figura siguiente. El orden de las conexiones de los pines depende de las preferencias del usuario.

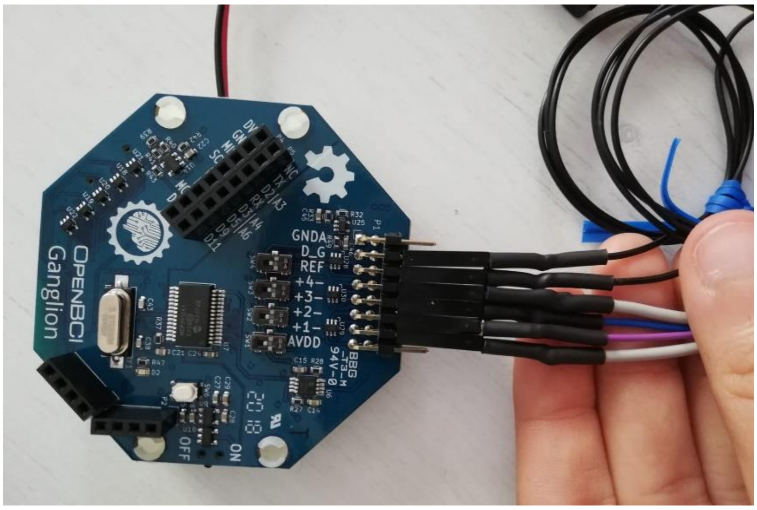


Figura 22 Conexiones placa Ganglion

4. Colocamos la diadema entre medio de un electrodo puntiagudo y el extremo tipo clip de un cable conductor violeta o azul, asegurándonos de alinearlo con el orificio de la diadema.

   De tal forma que, finalmente coloquemos el electrodo puntiagudo en el clip. Realizamos este paso para ambos cables, violeta y azul.

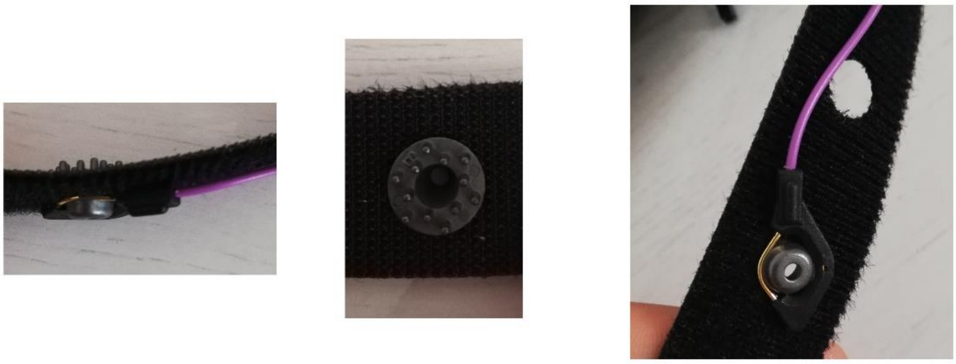


Figura 23 Procedimiento cables violeta y azul para electrodos puntiagudos

5. Finalmente, colocamos la diadema entre el electrodo plano y el extremo de un cable conductor de color (blanco, rojo o negro), asegurándonos de alinearlo con el orificio en la banda para la cabeza, ajustamos el electrodo en su lugar. Realizamos este paso para ambos cables, rojo y blanco.

Figura 24 Procedimiento cables rojo y blanco para electrodos planos.

De tal forma, que la situación final de montaje sería la siguiente:

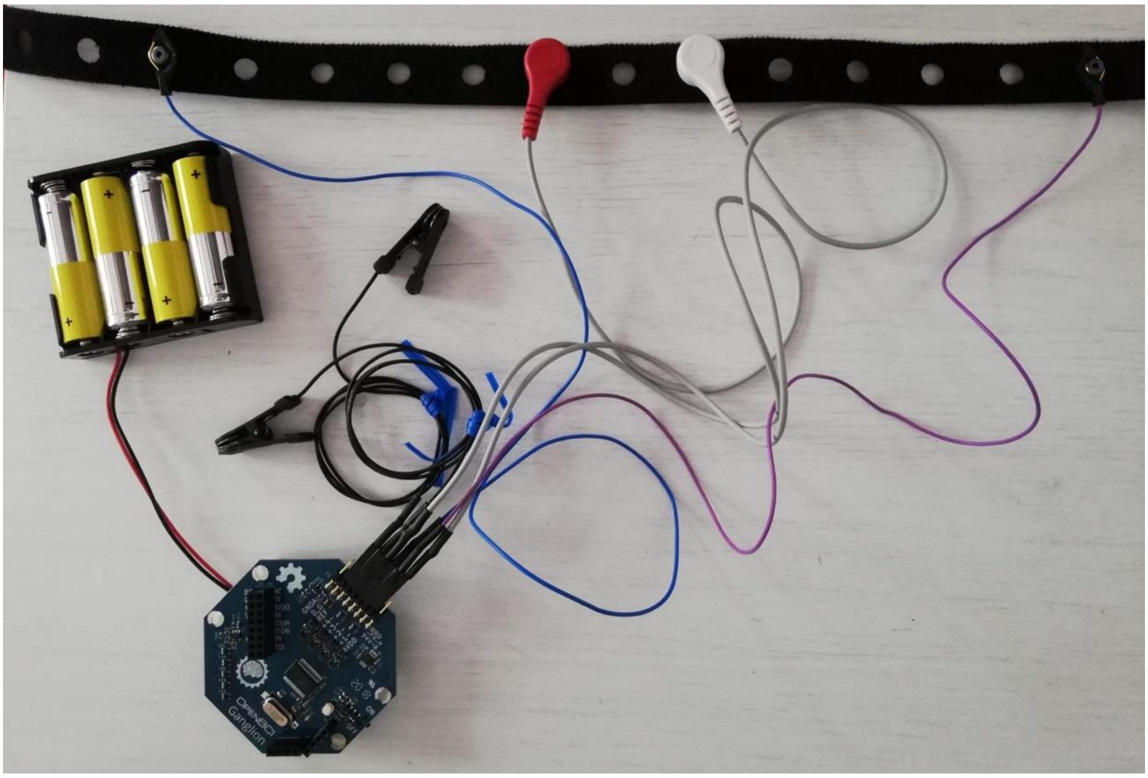


Figura 25 Situación final de montaje de la Headband (4 electrodos)

Recordemos que cuando le damos al interruptor de encendido, vemos que el LED azul parpadea suavemente. Una vez que el Ganglion está conectado a nuestro PC, el LED permanece encendido.

En un principio no conseguí que esto ocurriera, ya que a pesar de tener el USB dongle conectado, este no detectaba la placa Ganglion que estaba con el led azul parpadeando e intentándose comunicar.

La solución [19] de este problema es que debemos deshabilitar el bluetooh interno de nuestro portátil para que el USB dongle funcione. Ya que, no se puede tener dos sistemas de bluetooh activos en el PC. A continuación, veremos cómo se ha resuelto este inconveniente.

- **Procedimiento de preparación del CSR 4.0 USB:**

Primero debemos de tener el USB Dongle desconectado de nuestro PC.

1. En el cuadro de búsqueda de Windows en la parte inferior de la pantalla, escribimos "Administrador de dispositivos" y lo abrimos. Ver Figura 26.
2. Expandimos la sección de Bluetooh. Hacemos clic derecho en nuestra radio Bluetooth existente y seleccionamos "Deshabilitar dispositivo" de las opciones disponibles. Nos aparecerá el siguiente mensaje que debemos de aceptar:

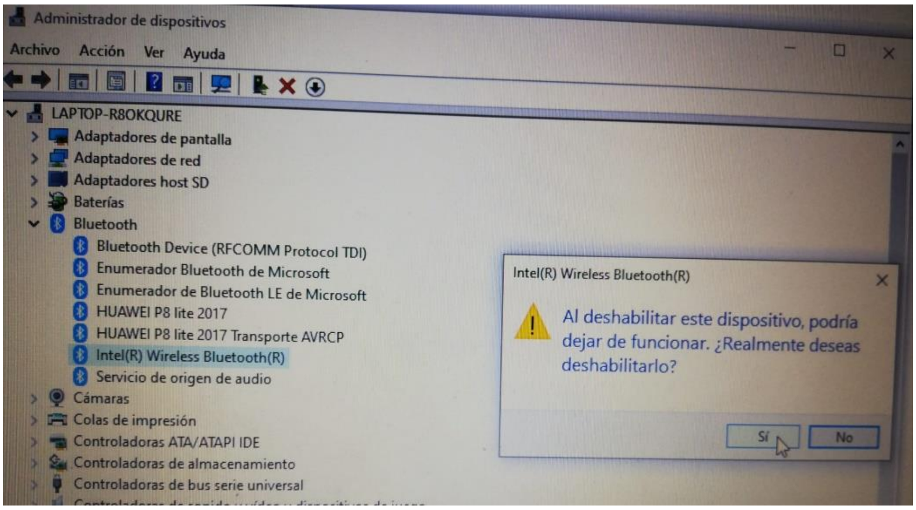


Figura 26 Pantalla vista al deshabilitar el bluetooh interno

3. Tras este paso, debemos reiniciar el PC para que el cambio se aplique.
4. Ya cuando hemos iniciado de nuevo el ordenador, conectamos el USB Dongle.
5. Descargamos el programa Zadig para cambiar el drive del dongle CSR 4.0 a WinUSB. (Recomiendo seguir los pasos de la referencia [19]). Finalmente, reiniciamos el ordenador.

   Ya tendremos el Dongle preparado para cuando vayamos a encender y conectar vía bluetooh la placa.

Otra forma mucho más sencilla para resolver este inconveniente es comprar el USB: BLED 112. Este es compatible tanto con la versión antigua 3.3.1 (Mayo 2018) como con la última actualmente: 4.2.0 (Enero 2020).

3.4 Pruebas

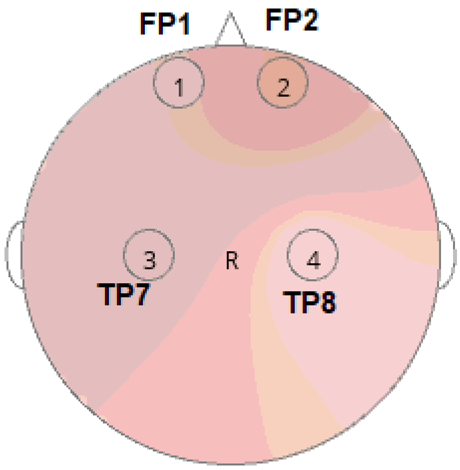


Figura 27 - Representación ubicación de cada electrodo respecto a cada canal en GUI para sistema de 4 electrodos

- **<u>Prueba inicial:</u>**

Pasos para iniciar la obtención de información en nuestro PC de nuestro sistema EEG:

1. Instalar el Dongle USB (Seguir pasos del apartado "Procedimiento de preparación del CSR 4.0 USB)
2. Con el CSR 4.0 conectado, abrimos OpenBCIhub
3. Arrancamos OpenBCI GUI
4. Clicamos en "Live (from Ganglion)" → "BLE (on Win from Dongle)" → "Search"

De esta forma debería de detectarnos nuestra placa Ganglion como en la Figura 28. Hay que recordar que el led de nuestra placa se debe de quedar fijo, no intermitente, de esa forma sabremos que se ha conectado correctamente con nuestro PC.

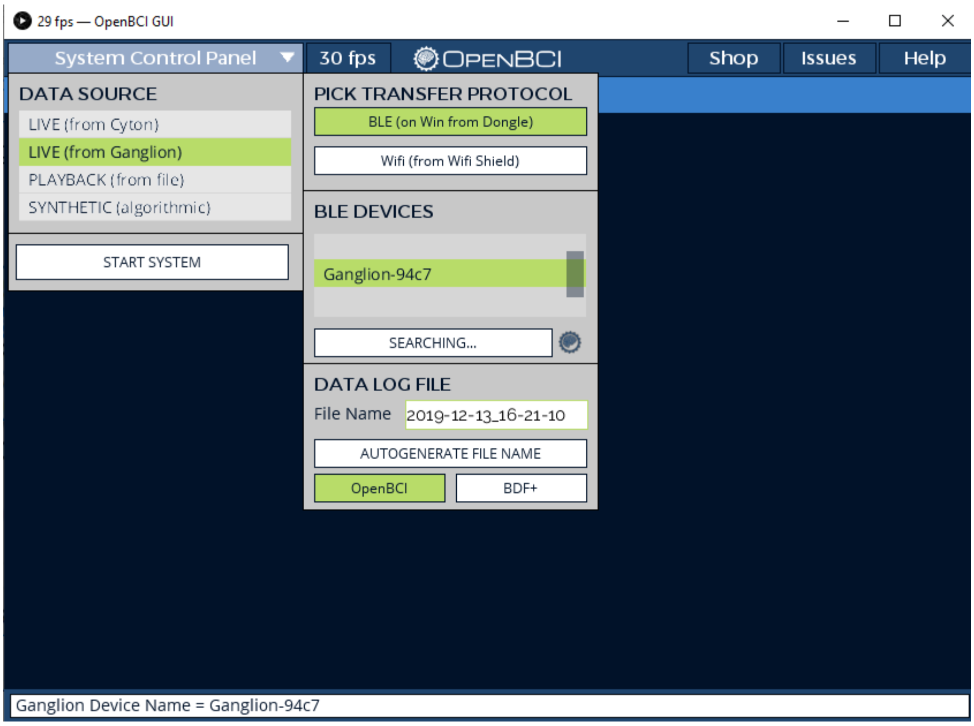


Figura 28 Conexión placa Ganglion y OpenBCI GUI para sistema de 4 electrodos.

Por último, le damos a "Start system" y ya tendríamos el programa trabajando con la placa Ganglion y la headband.

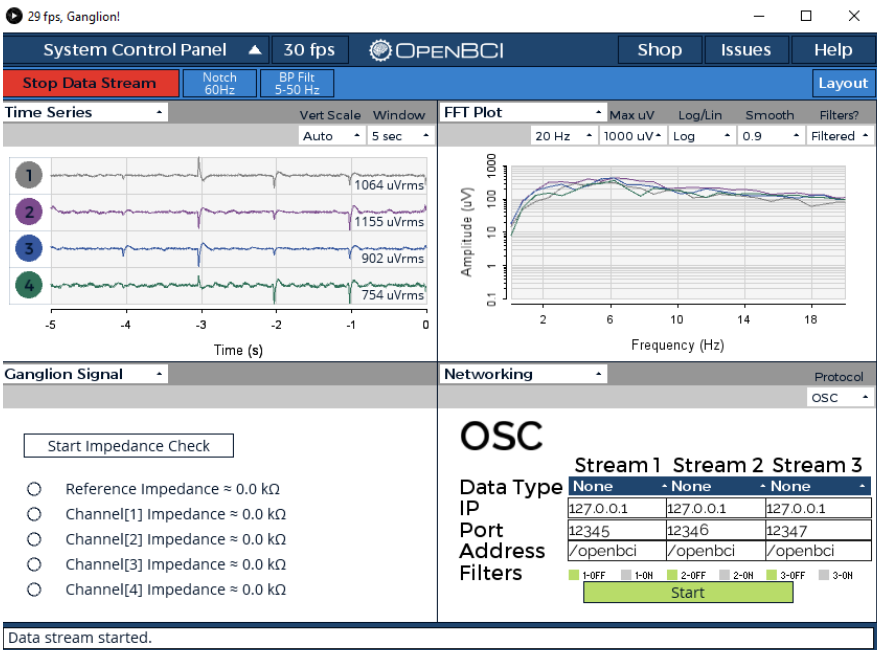


Figura 29 Prueba de funcionamiento de la headband (4 electrodos) haciendo click en Start Data Stream

En los ficheros de texto que obtenemos al recoger datos con la aplicación GUI, los electrodos están ordenados por columnas del 1-4, ese orden es equivalente a la figura 27.

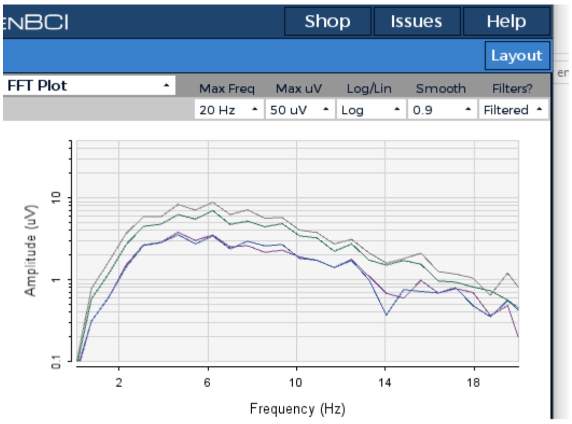
Otras pruebas:

Todas las pruebas se han realizado con el mismo sujeto:

Datos: Mujer, 23 años, 1.63 m, 60 Kg

Las pruebas realizadas.

- Proceso de meditación
- Escribir en el ordenador
- Escuchar música



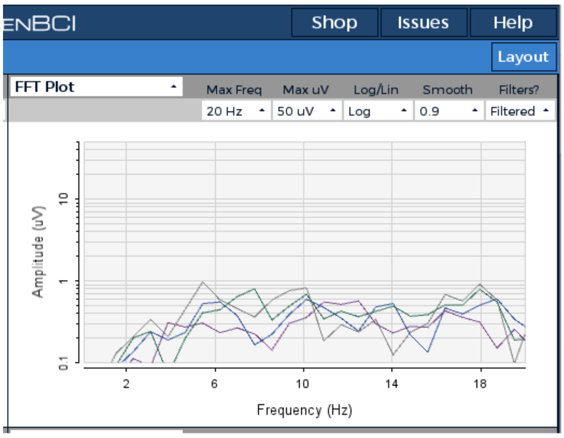


Figura 30 – Prueba de meditación. En la primera gráfica podemos observar el FFT Plot con las respuestas de amplitud en uV de los cuatro electrodos antes de realizar el proceso de meditación, y en la segunda gráfica vemos las respuestas cuando ya se está realizando la prueba. En un principio se está en un estado de alerta, podemos ver como comienza a crecer amplitud a partir de 1 Hz, pero, después de la meditación, las ondas encefalográficas comienzan a crecer a partir de los 5-6 Hz.

Comparando ambas imágenes podemos observar una gran diferencia en las gráficas de Amplitud/Frecuencia.

Este resultado, proviene de un proceso de meditación. Donde se aprecia claramente como se reduce la amplitud a lo largo de la frecuencia, tras entrar en un estado de calma, relajación, tranquilidad y creatividad.

Observando la figura 30: En la primer gráfica, en estado de alerta, podemos ver como comienza a crecer amplitud a partir de 1 Hz. Y en la segunda gráfica, después de la meditación, las ondas encefalográficas comienzan a crecer a partir de los 5-6 Hz.

Figura 31 Escribiendo en el ordenador

Figura 32 Escuchando música

Estas dos últimas pruebas se realizaron a partir de dos situaciones distintas con la misma persona.

La primera, escribiendo en el ordenador, podemos destacar que cuantas más rápido se parpadeaba, la amplitud de las ondas en uV y la frecuencia aumentaban.

En la segunda, volviendo a un estado de relajación escuchando música tranquilamente, se aprecia una disminución en la amplitud.

El widget de potencia de banda (Band Power) muestra los voltajes relativos de las diversas categorías de ondas cerebrales. Cada tipo de onda cerebral representa un subconjunto de frecuencias, que representan diferentes estados de actividad. El widget es una excelente visión "rápida" de la actividad del cerebro.

Durante la prueba de escribir en el ordenador se aprecia que son muchas más ondas cerebrales las que están presentes con mayor intensidad (Delta, Theta, Alpha, Beta y Gamma) que en la prueba de escuchar música dónde las más destacadas son la Beta y la Gamma.

En ambas pruebas las ondas cerebrales a destacar son las siguientes:

- Beta (13-32 Hz): Significa conciencia de alerta normal y pensamiento activo. Ocurre cuando uno se enfoca en el trabajo, resuelve un problema, aprende un nuevo concepto o entabla una conversación activa.

- Gamma: Significa una mayor percepción, el aprendizaje y las tareas de resolución de problemas, así como el estado de alerta. Ocurre cuando hay un procesamiento de información simultáneo de múltiples partes del cerebro.

Capítulo 4
Dispositivo de 8 y 16 electrodos
(OpenBCI Ultracortex Mark IV EEG Headset)

4.1 Especificaciones comunes para dispositivos Ultracortex Mark IV EEG Headset

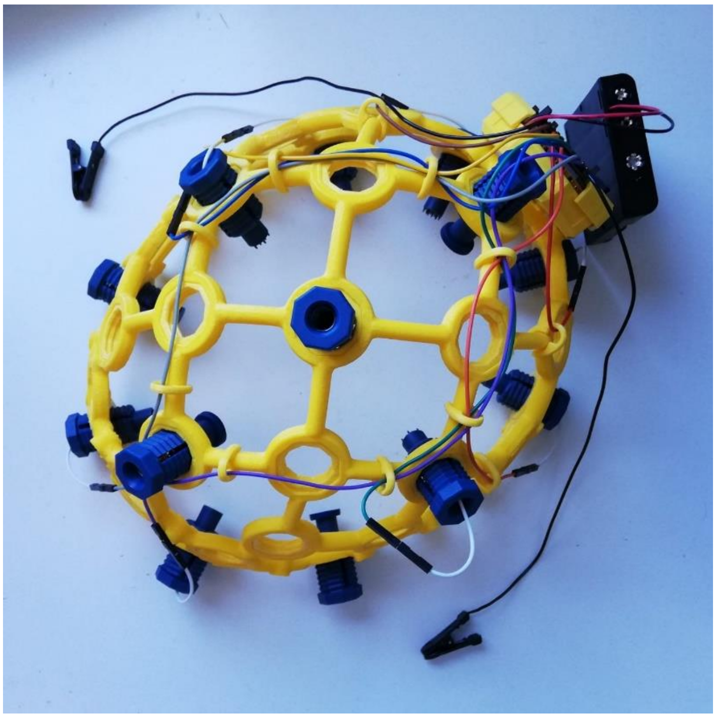


Figura 33 Montaje Biosensing Starter Kit (8 canales)

El OpenBCI Ultracortex es un dispositivo de código abierto, imprimible en 3D y diseñado para trabajar con cualquier placa OpenBCI.

Es de libre acceso, por lo tanto, puede ser adquirido comprándolo por la página web, pero también puede ser impreso en cualquier parte del mundo ya que sus creadores permiten que cualquier persona se pueda descargar el diseño para imprimirlo en 3D.

En este TFG hemos trabajado con un casco impreso en nuestra universidad (ULL)

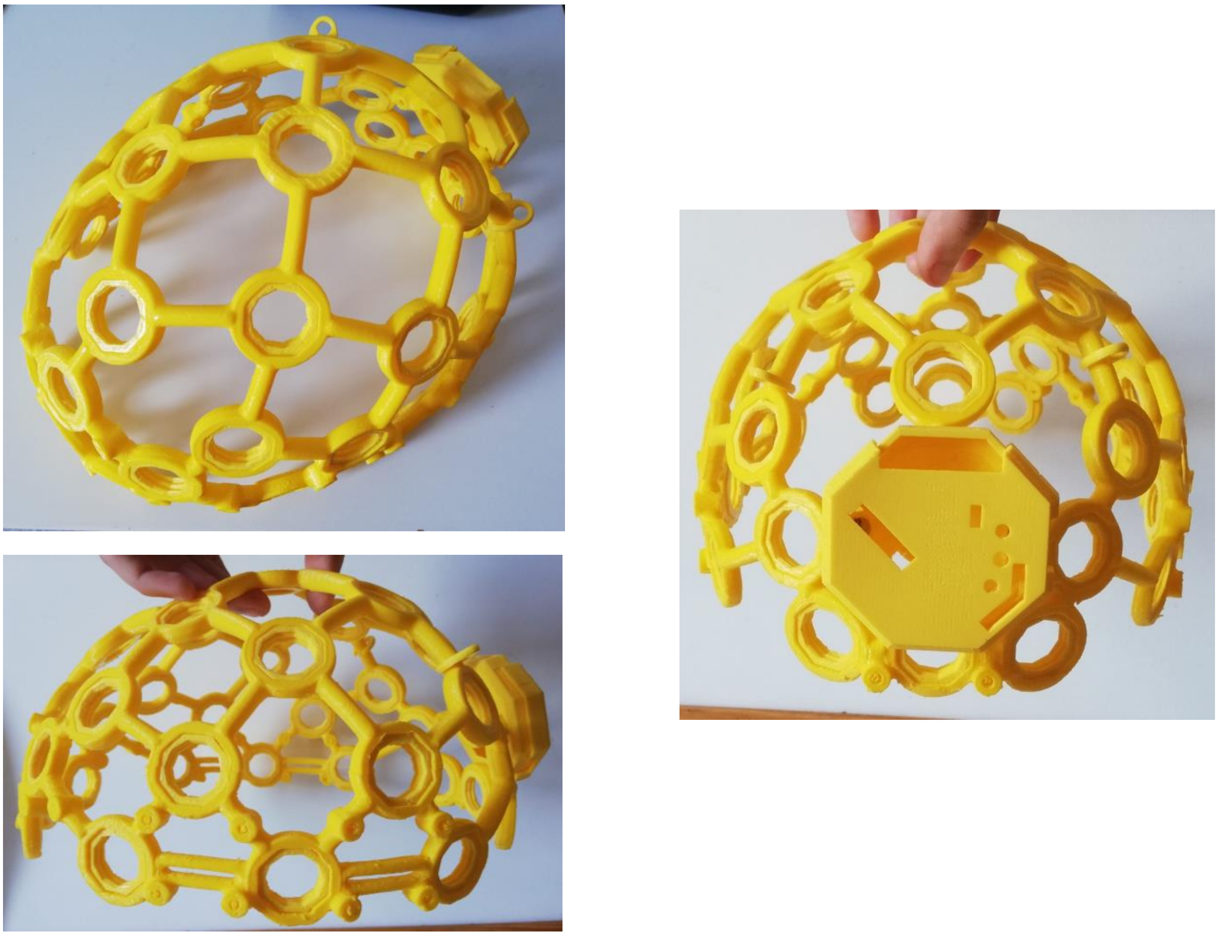
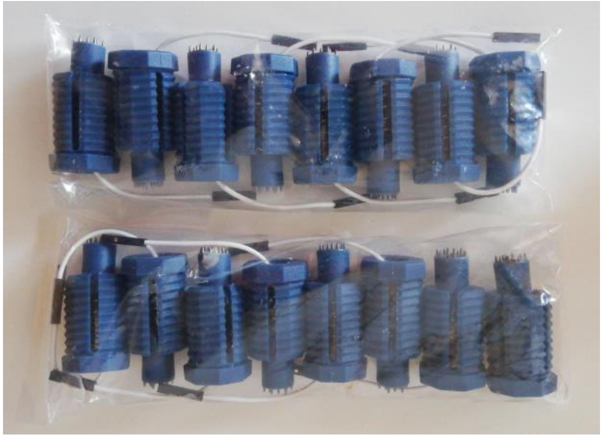


Figura 34 - Casco Ultracortex Mark IV impreso en la ULL

En este TFG se ha trabajdo tanto con 8 como con 16 canales, por lo tanto, se ha contado con los siguientes componentes:

Tabla 2 Componentes empleados con el casco Ultracortex Mark IV

	**Electrodos con clip para las orejas (2). Principalmente hacen la función de referencia y de tierra (GND)**



**Spikey units (16)
Electrodos empleados para zonas con pelo.**

**Flat units (4)
Electrodos empleados principalmente para zonas sin pelo, por ejemplo, la frente.**

**Confort units (14)
Piezas usadas para distribuir mejor el peso del casco en la cabeza.**

- Conjuntos de cables ribbon, de distintos tamaños para poder llegar bien a conectar todos los electrodos desde cualquier posición permitida a la placa empleada.
- Tornillos (2) para asegurar la placa al casco.

Dependiendo de si trabajamos con 8 canales o 16 canales, tendremos que tener en cuenta:

Tabla 4 - Cantidad de componentes según trabajemos con 8 o 16 electrodos [20]

Términos en español	**Términos en inglés**	**Sistema 8 electrodos**	**Sistema 16 electrodos**
Electrodos puntiagudos	Spikey Units	8	16
Electrodos planos	Flat Units	2	4
Piezas de confort	Confort Units	7	14
3 conjuntos de cables planos paralelos	3 Ribbon cables	1	1
Clips de oreja	Ear clips	2	2
Tornillos	Screws	2	2

Para 8 canales se trabajaría con la placa Cyton únicamente, en cambio, para 16 canales debemos tener la Cyton más la placa Daisy Biosensing.

4.2 Ultracortex Mark IV (8 canales)

4.2.1 Cyton Board

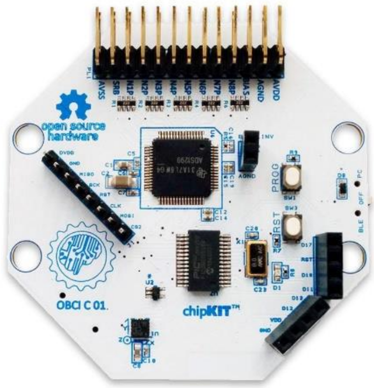


Figura 35 - Placa Cyton

La placa Cyton OpenBCI es una interfaz neuronal de 8 señales con un procesador de 32 bits, compatible con Arduino.

Esta placa implementa el microcontrolador PIC32MX250F128B, dándole mucha memoria local (128 KB) y velocidades de procesamiento rápidas (hasta 50 MHz).

También cuenta con un circuito integrado ADS1299 [21], este es capaz de amplificar por distintos valores (1, 2, 4, 8, 12 y 24) y digitalizar a distintas tasas de muestreo hasta 8 señales de EEG con una resolución de 24 bits.

Figura 36 - Microcontrolador PIC32MX250F128B

Figura 37 - Amplificador ADS1299

Tabla 5 - Especificaciones generales placa Cyton

Canales / Electrodos	8
Alimentación	3-6V DC (Solo batería)
Transmisión	RFduino BLE (Bluetooh Low Energy) radio (OpenBCI USB Dongle)
Amplificador de ganancia	ADS1299
Nº bits ADC	24 (ADS1299)
Velocidad de muestreo	250 Hz
Microcontrolador	PIC32MX250F128B

4.2.2 Montaje 8 electrodos

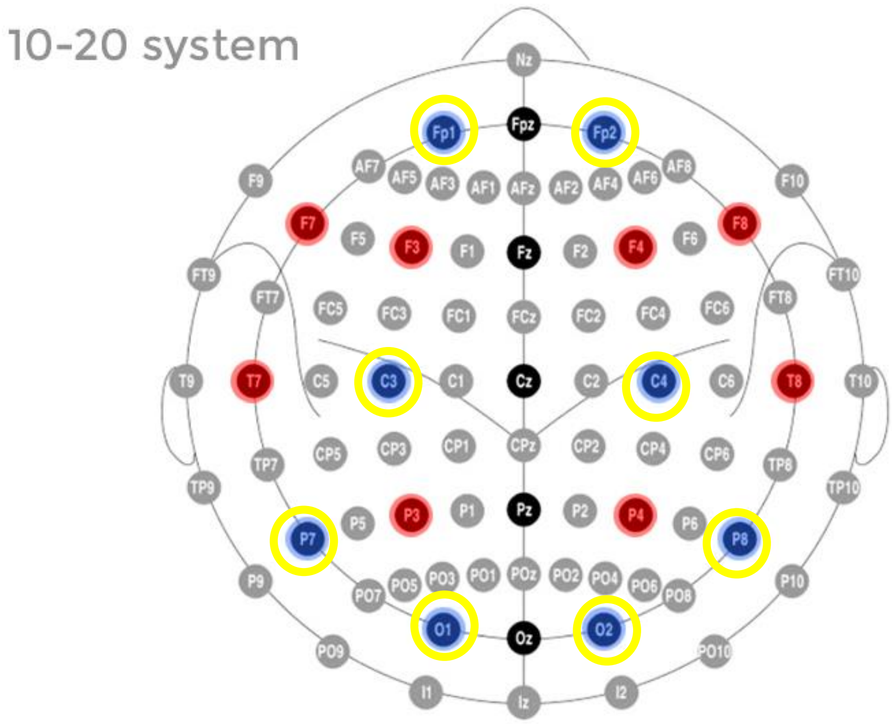


Figura 36 – Ubicaciones posibles de los electrodos para el Ultracortex IV. En amarillo se muestran las elegidas para nuestro sistema de 8 canales. Los nodos azules indican las 8 ubicaciones predeterminadas de la Cyton Board y los nodos rojos indican las ubicaciones predeterminadas cuando queremos añadir más electrodos si pasamos a trabajar con 16 canales.

Los nodos azules indican las 8 ubicaciones predeterminadas de la Cyton Board. Los nodos rojos indican las ubicaciones predeteminadas cuando tenemos que añadir más electrodos si trabajamos con 16 canales.[22]

Nosotros hemos trabajado con las ubicaciones redondeadas en amarillo en la figura 39, basado en el sistema estándar de encefalografía “10-20 system”.

Tabla 6 - Distribuciones electrodos

Canal	Ubicación electrodo	Color del cable	Pin en la placa Cyton
Channel 1	Fp1	Violeta	N1P
Channel 2	Fp2	Gris	N2P
Channel 3	C3	Verde	N3P
Channel 4	C4	Azul	N4P
Channel 5	P7	Naranja	N5P
Channel 6	P8	Amarillo	N6P
Channel 7	O1	Rojo	N7P
Channel 8	O2	Marrón	N8P
Clip oreja 1	-	Negro	SRB
Clip oreja 2	-	Negro	BIAS

Pasos de montaje (Ver tabla 3 para saber cuales son los componentes que vamos a emplear):

1. Colocamos 2 electrodos planos (flat) en los dos huecos frontales del casco: FP1, FP2.
2. Colocamos 6 electrodos puntiagudos (spikey) en los huecos correspondientes a: C3, C4, P7, P8, O1, O2.
3. Colocamos 5 piezas de confort (confort units) dónde creamos que nos va a dar mayor sujeción

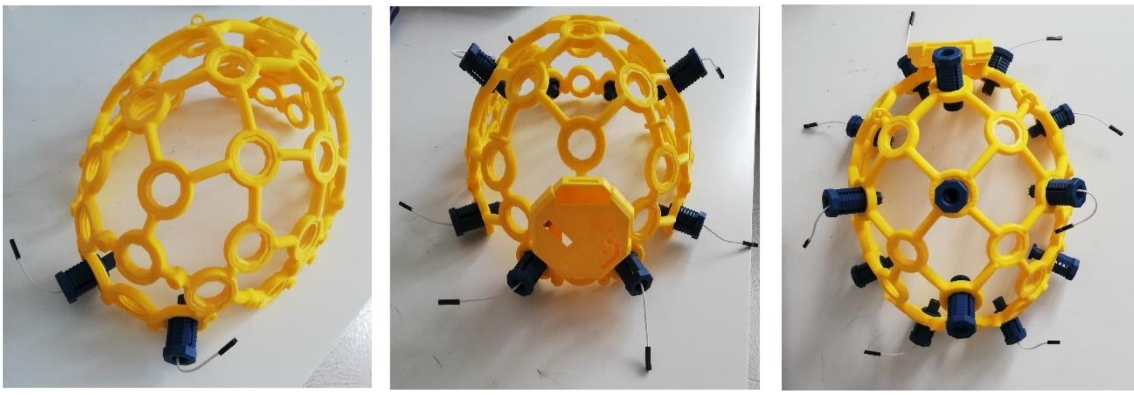


Figura 37 - Pasos de montaje de piezas y electrodos para Ultracortex IV de 8 electrodos,

Conexión cables entre placa y electrodos:

Despegamos el gris y el violeta de los cables más largos. El azul, verde, naranja y amarillo del conjunto de cables mediano. Por último, el rojo y marrón de los cables más cortos. Conectamos los cables y los clips de oreja según la tabla comentada previamente (Ver tabla 5). Y finalmente, conectamos la alimentación de la placa.

El resultado es el siguiente:

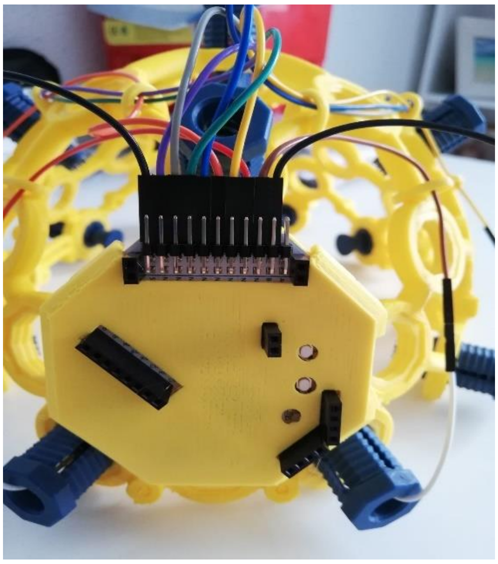


Figura 38 - Resultado final de montaje UltraCortex IV (8 canales)

Figura 39 – Ejemplo de montaje sistema de 8 electrodos en casco Ultracortex

4.2.3 OpenBCI GUI con 8 electrodos

Antes de comenzar con la aplicación GUI se tuvo que tener en cuenta qué representaba cada electrodo del programa en relación con las ubicaciones de estos en el cerebro.

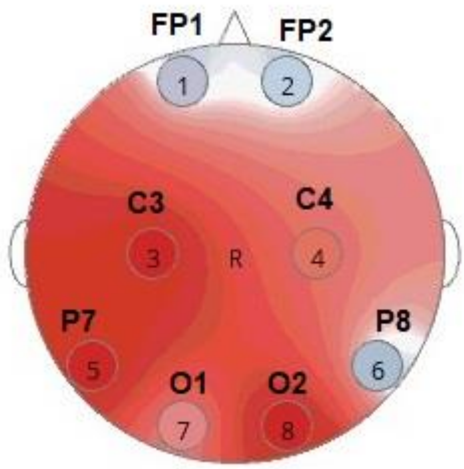


Figura 40 – Representación ubicación de cada electrodo respecto a cada canal en GUI para sistema de 8 electrodos

Pasos para ejecutar la aplicación GUI con el sistema de 8 electrodos:

1. Conectamos el USB dongle de Cyton en el ordenador y esperamos que se instale.
   Deberíamos ver un LED azul encendido permanente, así como un LED rojo parpadeando.

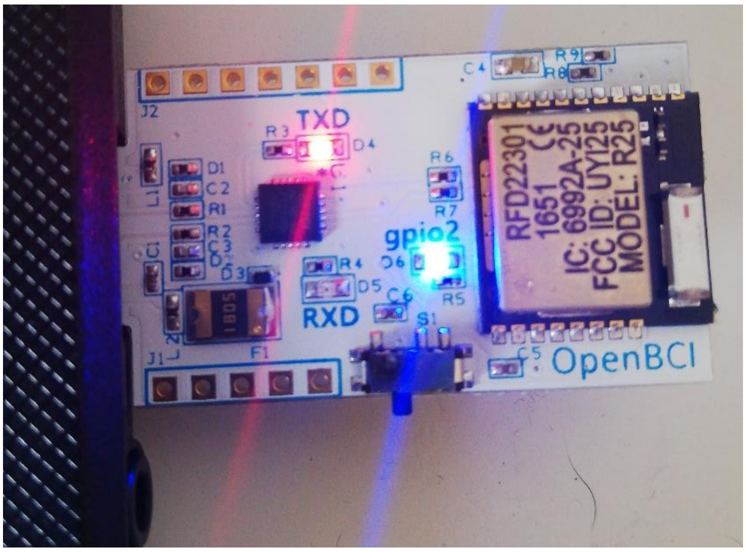


Figura 41 - Conexión USB OpenBCI para emparejar la placa Cyton con el ordenador vía bluetooh.

2. Abrimos OpenBCIHub
3. Abrimos OpenBCI GUI (En este caso, versión 3.3.1 May 2018)
4. Encendemos la placa, moviendo el interruptor de apagado “OFF” hacia “PC”.

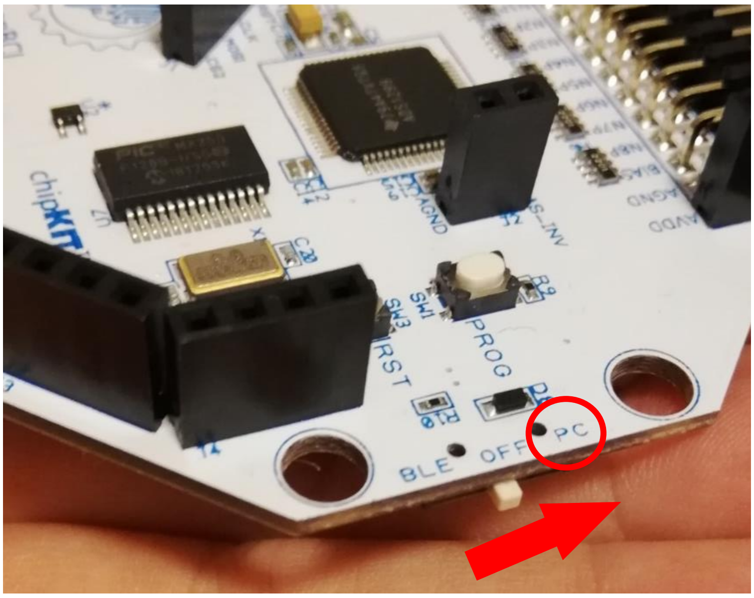


Figura 42 - Interruptor de encendido placa Cyton. Desplazamos hacia PC para conectarlo a nuestro ordenador.

5. Clicamos en LIVE (from Cyton), después en Serial (from dongle). Por último, elegimos el correspondiente que nos sale, en nuestro caso COM6 y seleccionamos 8 channels.

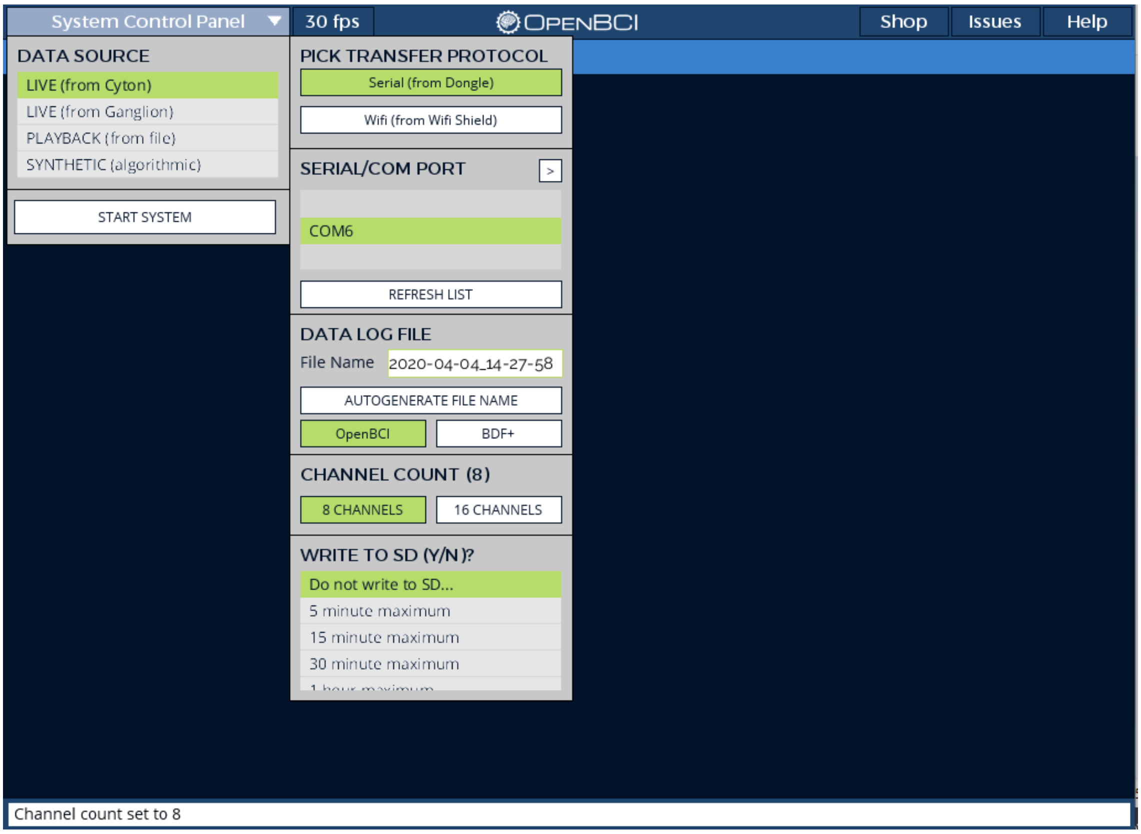


Figura 43 - OpenBCI GUI detectando la Cyton board (8 canales)

En los ficheros de texto que obtenemos al recoger datos con la aplicación GUI, los electrodos están ordenados por columnas del 1-8, ese orden es equivalente a la figura 40.

4.3 Ultracortex Mark IV (16 canales)

4.3.1 Cyton Board + Módulo Daisy

OpenBCI Cyton Board y OpenBCI Daisy Module (que se conecta a la placa Cyton, ver figura 44) se pueden usar para muestrear hasta 16 canales de actividad cerebral (EEG), actividad muscular (EMG) y actividad cardíaca (ECG).

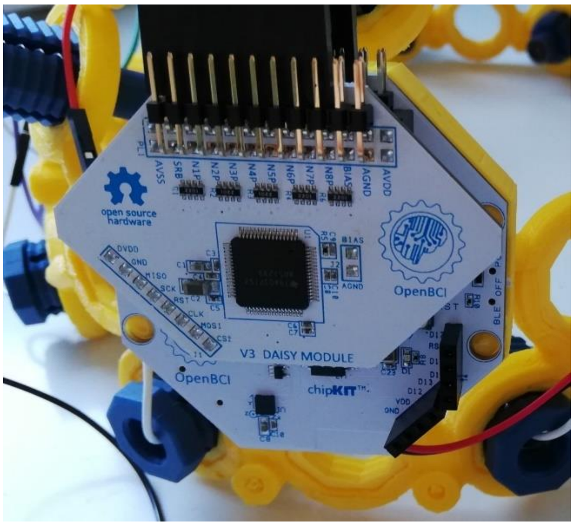


Figura 44 - Unión placa Cyton con el módulo Daisy

El sistema se comunica de forma inalámbrica a una ordenador a través del USB OpenBCI (no confudir con el USB CSR Dongle). También se puede comunicar de forma inalámbrica a cualquier dispositivo móvil o tablet compatible con BLE.

La combinación Cyton-Daisy muestrea datos a 125 Hz en cada uno de sus 16 canales [23] Es decir, a la mitad de muestreo de la placa Cyton (250 Hz).

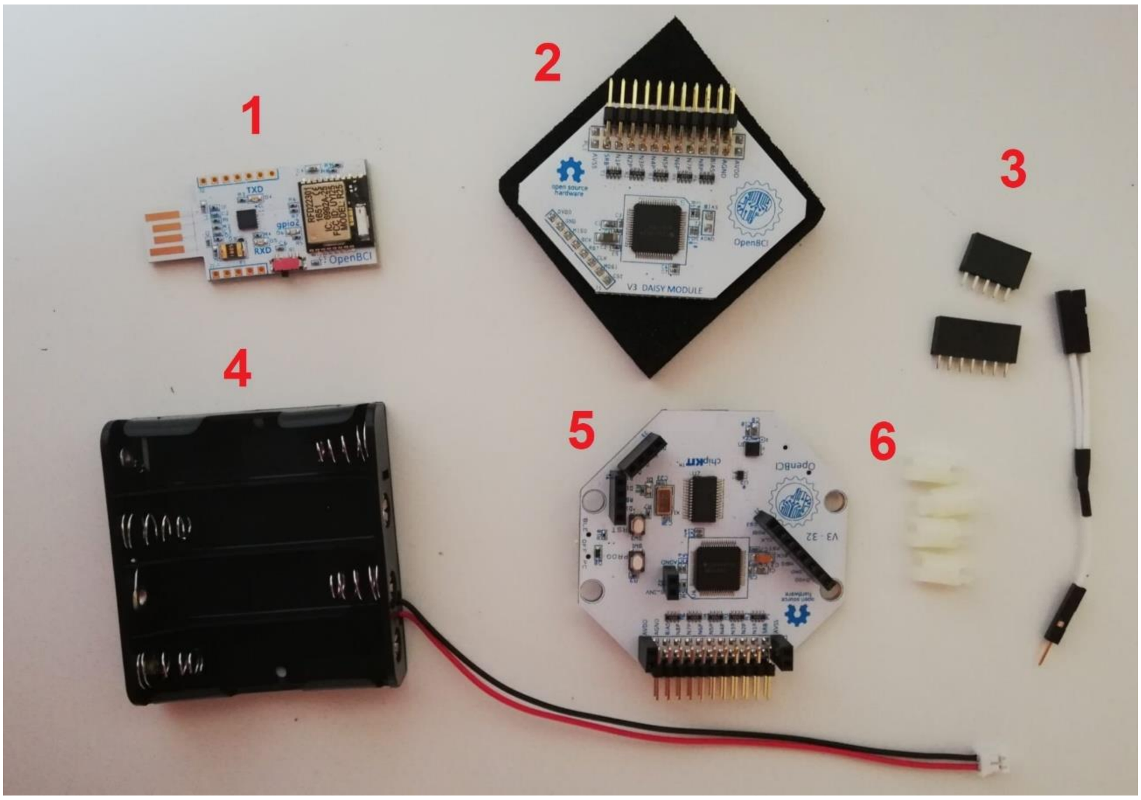


Figura 45 – Componentes: 1. OpenBCI USB Dongle USB, 2. Módulo Daisy, 3. componentes varios + cable unión en Y, 4. Alimentación de la placa (6V AA), 5. Placa Cyton, 6. Piezas plásticas para estabilizar la placa)

4.3.2 Montaje 16 electrodos

Como comentamos previamente, si tenemos la extensión Cyton Daisy, podemos pasar de trabajar con 8 electrodos a 16.

Para ello se añaden al montaje de 8 electrodos: 8 electrodos spiky.
Sustituimos las dos piezas de confort frontales (F7, F8) por dos electrodos spiky. Ver figura 46.

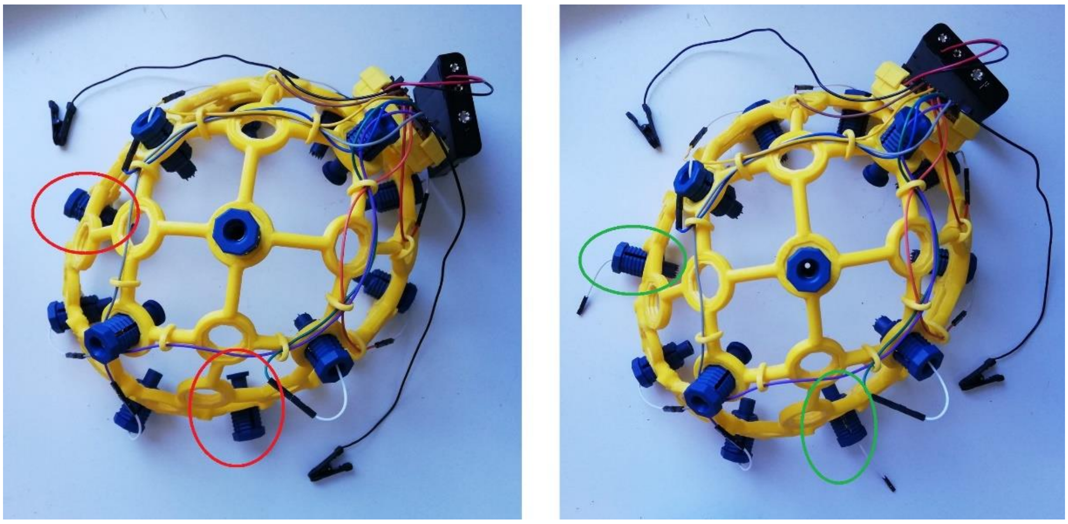


Figura 46 – Modificación sistema de 8 electrodos para pasar a trabajar con 16 electrodos. La figura nos muestra la sustitución de las dos piezas de confort frontales (círculos en rojo) por dos electrodos spiky (círculos en verde)

Añadimos los otros 6 electrodos spiky restantes en las siguientes ubicaciones: F3, F4, T7, T8, P3, P4.

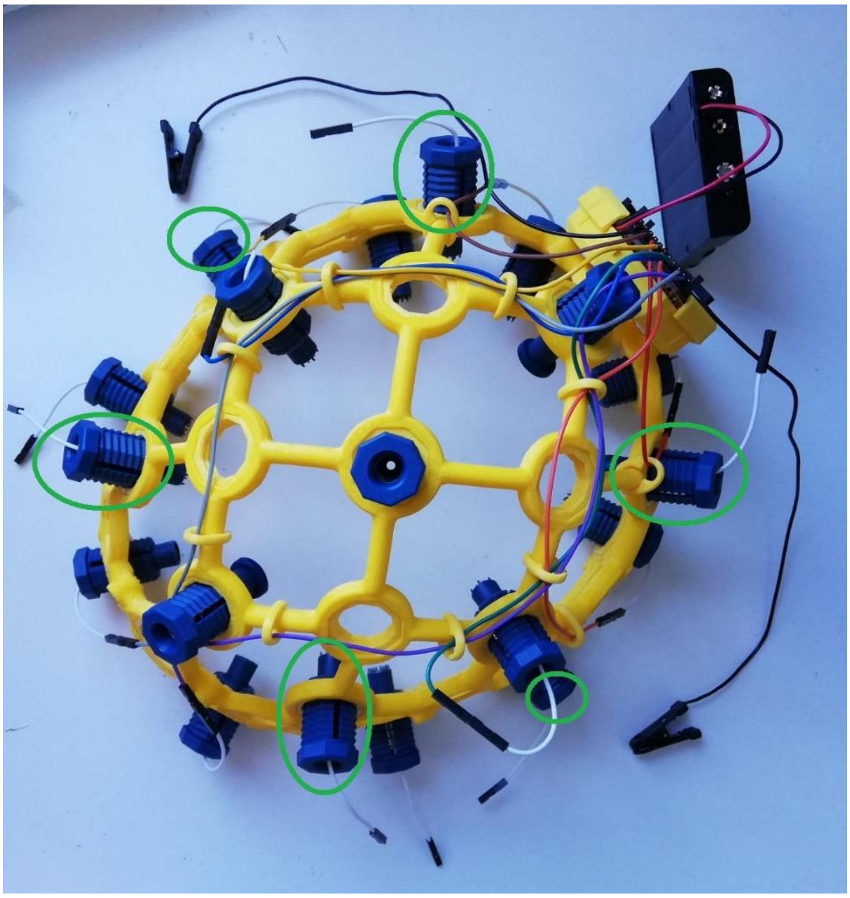


Figura 47 - Ubicación de los 6 electrodos spiky restantes para completar nuestro montaje de 16 electrodos.

Ya tendríamos nuestro casco con 16 electrodos preparado. Ahora faltaría conectar los 8 nuevos añadidos a la placa mediante el módulo Daisy

<u>Conexión cables entre placa y electrodos:</u>

- Cogemos el gris y el violeta de los cables medianos y de los cortos, y los unimos (violeta con violeta y gris con gris). Colocamos el gris en F8 y el violeta en F7.

  Ahora, cogemos el azul, el verde, el naranja y el amarillo de los cables largos. Colocamos el verde en F3, el azul en F4, el naranja en T8, y el amarillo en T3.

  Por último, de los cables medianos cogemos y colocamos el marrón en P4 y el rojo en P3.

- Le quitamos la alimentación a la placa y los dos clips de oreja, pero mantenemos la placa conectada con cada uno de los 8 electrodos de igual forma que vimos previamente. Ver Figura 41 y tabla 4.

- Unimos el módulo Daisy a la placa Cyton:

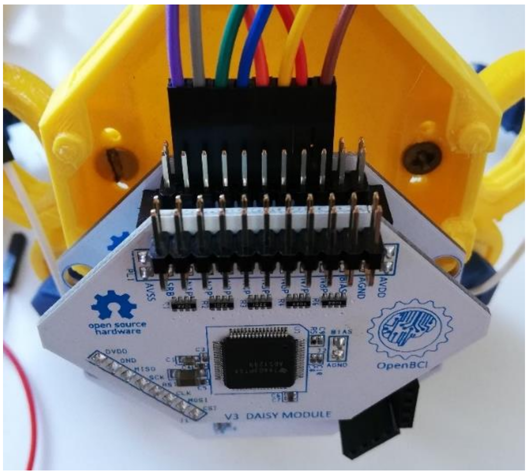


Figura 48 - Conexiones placa Cyton para Ultracortex Mark IV (16 electrodos)

Se debe seguir la siguiente tabla para conectar los 8 electrodos que faltan conectar al módulo Daisy y así tener nuestro sistema de 16 canales finalizado.

Tabla 7 – Conexiones entre la placa Cyton y el módulo Daisy con los electrodos y sus respectivas ubicaciones

Canal	Ubicación electrodo	Color del cable	Pines (placa)
Channel 1	Fp1	Violeta	N1P (Cyton)
Channel 2	Fp2	Gris	N2P(Cyton)
Channel 3	C3	Verde	N3P(Cyton)
Channel 4	C4	Azul	N4P(Cyton)
Channel 5	P7	Naranja	N5P(Cyton)
Channel 6	P8	Amarillo	N6P(Cyton)
Channel 7	O1	Rojo	N7P(Cyton)
Channel 8	O2	Marrón	N8P(Cyton)
-	-	-	-
Channel 9	P4	Marrón	N8P (Daisy)
Channel 10	P3	Rojo	N7P (Daisy)
Channel 11	T4	Amarillo	N6P (Daisy)
Channel 12	T3	Naranja	N5P (Daisy)
Channel 13	F4	Azul	N4P (Daisy)
Channel 14	F3	Verde	N3P (Daisy)
Channel 15	F8	Gris	N2P (Daisy)
Channel 16	F7	Violeta	N1P (Daisy)
-	-	-	-
Clip oreja 1	-	Negro	SRB
Clip oreja 2	-	Negro	BIAS

El resultado es el siguiente:

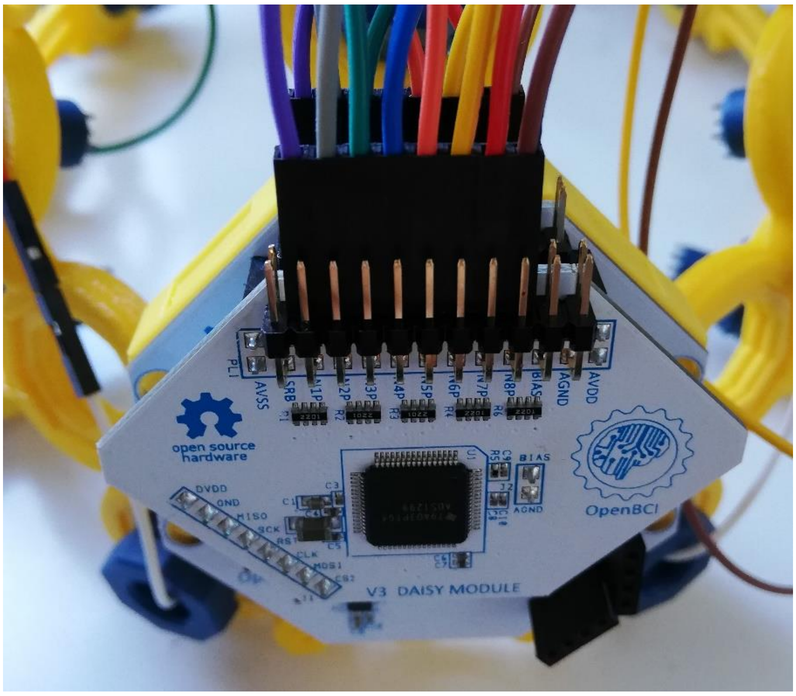


Figura 49 - Conexiones placa Cyton y módulo Daisy para Ultracortex Mark IV (16 electrodos)

Por último, unimos con el cable Y, el pin SRB de la placa Cyton con el pin SRB del módulo Daisy y con un clip de oreja. Como se ve en la siguiente imagen:

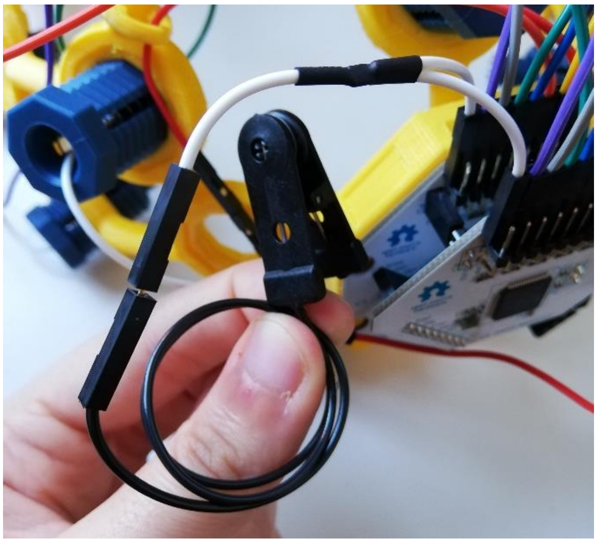


Figura 50 - Conexión clip de oreja entre la placa Cyton y el módulo Daisy con la conexión en Y.

Y el otro clip de oreja lo conectamos a BIAS de la placa Cyton.

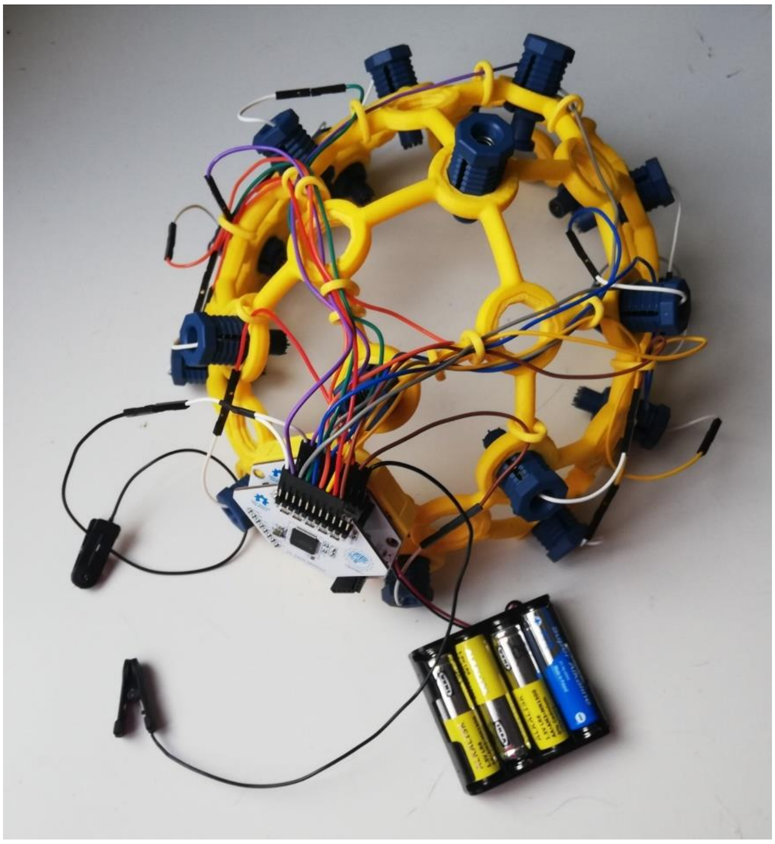


Figura 51 - Situación final de montaje Ultracortex Mark IV (16 canales)

4.3.3 OpenBCI GUI con 16 electrodos

Antes de comenzar con la aplicación GUI debemos tener en cuenta qué representa cada electrodo del programa en relación con las ubicaciones de estos en el cerebro.

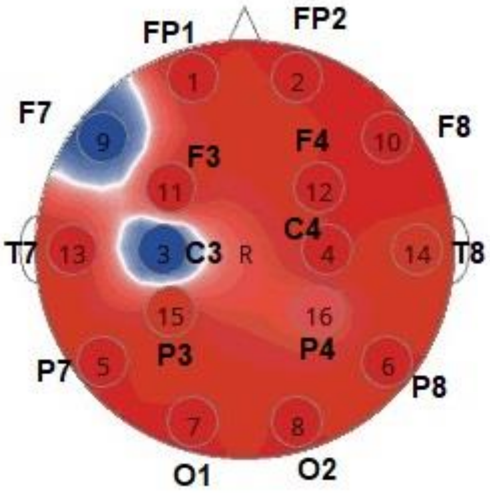


Figura 52 – Representación ubicación de cada electrodo respecto a cada canal en GUI para sistema de 16 electrodos

Tras esto, los pasos a seguir son los siguientes:

1. Conectamos el USB dongle de Cyton en el ordenador
2. Abrimos OpenBCIHub
3. Abrimos OpenBCI GUI (En este caso, versión 3.3.1 May 2018)
4. Encendemos la placa, clicamos en LIVE (from Cyton), después en Serial (from dongle). Por último, elegimos el correspondiente que nos sale, en nuestro caso COM6 y seleccionamos 16 channels.

En los ficheros de texto que obtenemos al recoger datos con la aplicación GUI, los electrodos están ordenados por columnas del 1-16, ese orden es equivalente a la figura 52.

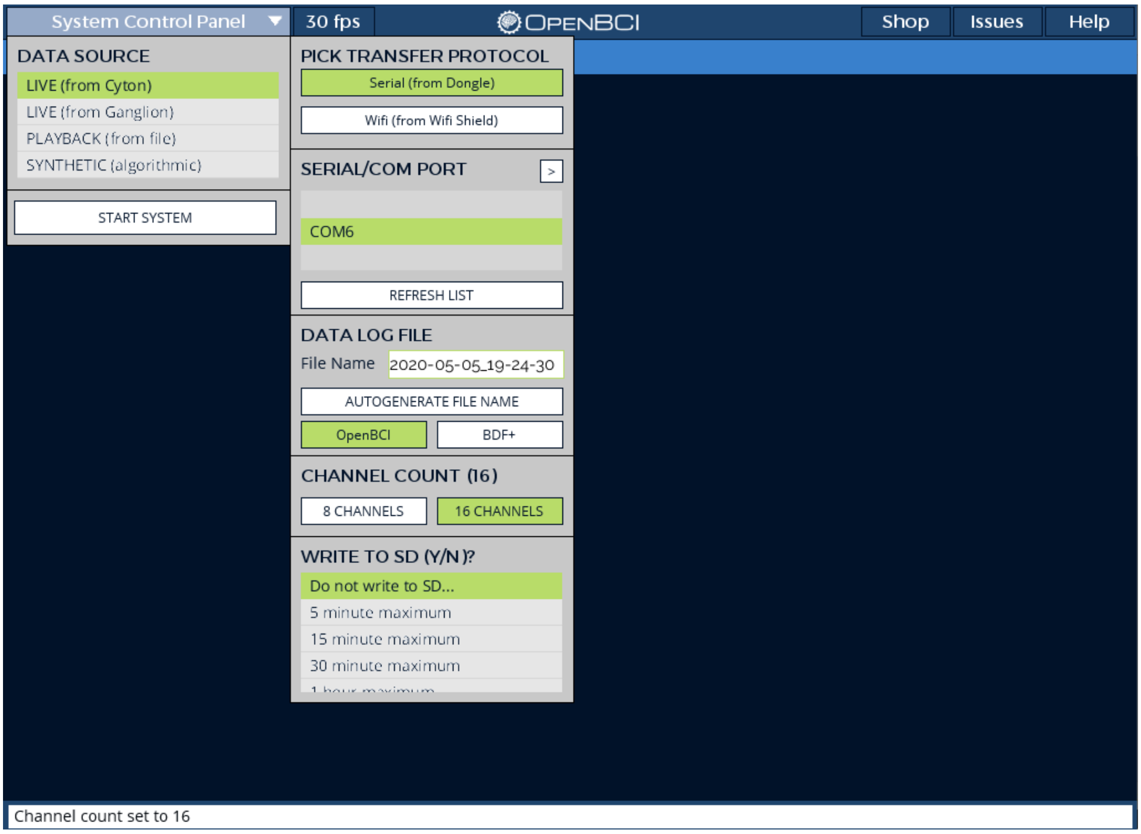


Figura 53 - OpenBCI GUI detectando la Cyton board + módulo Daisy

4.4 Pruebas de calibración

4.4.1 Pruebas de calibración EEG con 8 electrodos

Para la calibración se han realizado dos pruebas obtenidas del canal oficial del Co-fundador y CEO de OpenBCI, Conor Russomanno [24]. Las he realizado con el sistema de 8 electrodos.

- 1ª prueba de calibración: Cerrar los ojos y comprobar tras ello si se ha realizado un aumento de amplitud sobre los 10 Hz. (Observar el FFT plot)

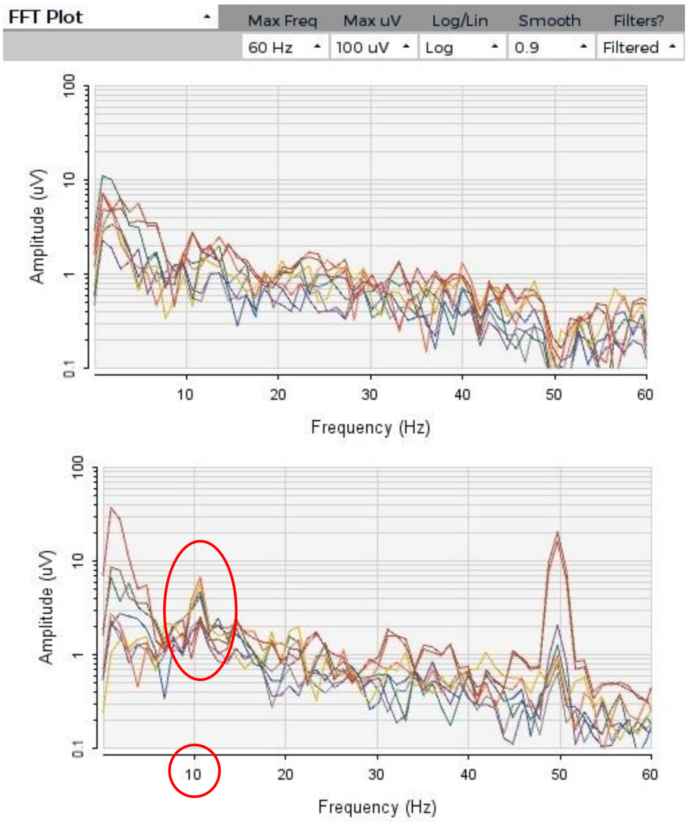


Figura 54 - Prueba de calibración: Cerrar los ojos y comprobar que tras ello se ha realizado un aumento de amplitud sobre los 10 Hz. La figura superior es la situación inicial, previa a cerrar los ojos; la inferior nos muestra la situación después de cerrar los ojos, efectivamente ha ocurrido lo esperado. (Gráficas tomada de la pantalla del programa GUI)

Como hemos podido observar, efectivamente se cumple ese aumento de amplitud sobre la frecuencia de los 10 Hz. Por lo tanto, podemos dar el resultado por aceptado.

- 2ª de calibración: Apretar los dientes abriendo y cerrando la boca, observando que tras ello se ven alteradas todas las ondas encefálicas que tenemos en cada uno de los 8 canales.

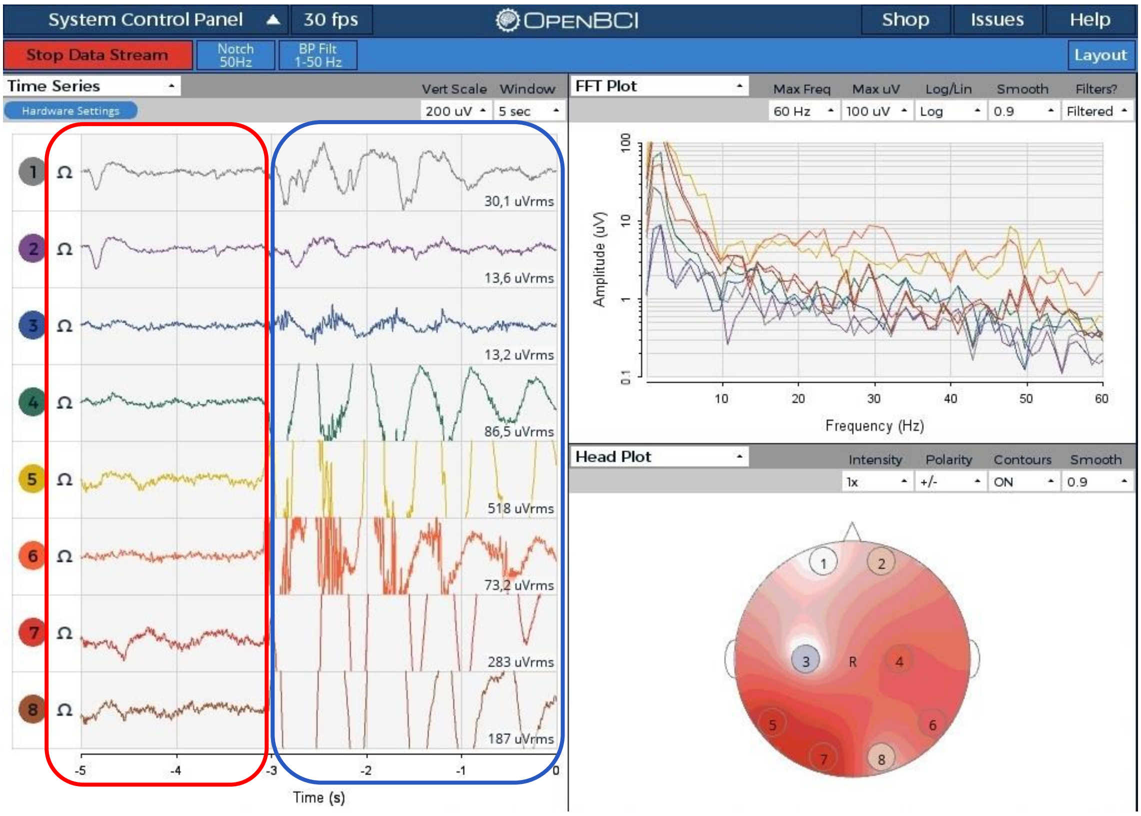


Figura 55 – Resultado prueba de calibración 2: Apretar los dientes abriendo y cerrando la boca, observando que tras ello se ven alteradas todas las ondas encefálicas que tenemos en cada uno de los 8 canales. En recuadro rojo: momentos previos a iniciar la prueba. En recuadro azul: realización de la prueba. (Gráfica tomada de la pantalla del programa GUI)

En este caso también se cumple, ya que podemos ver perfectamente la diferencia entre cada una de las ondas de los ocho canales, antes y después de realizar la prueba. Se han visto alteradas unas más que otros, pero, al fin y al cabo, todas han sido modificadas.

4.4.2 Prueba de concentración con 16 electrodos mediante un widget de OpenBCI GUI

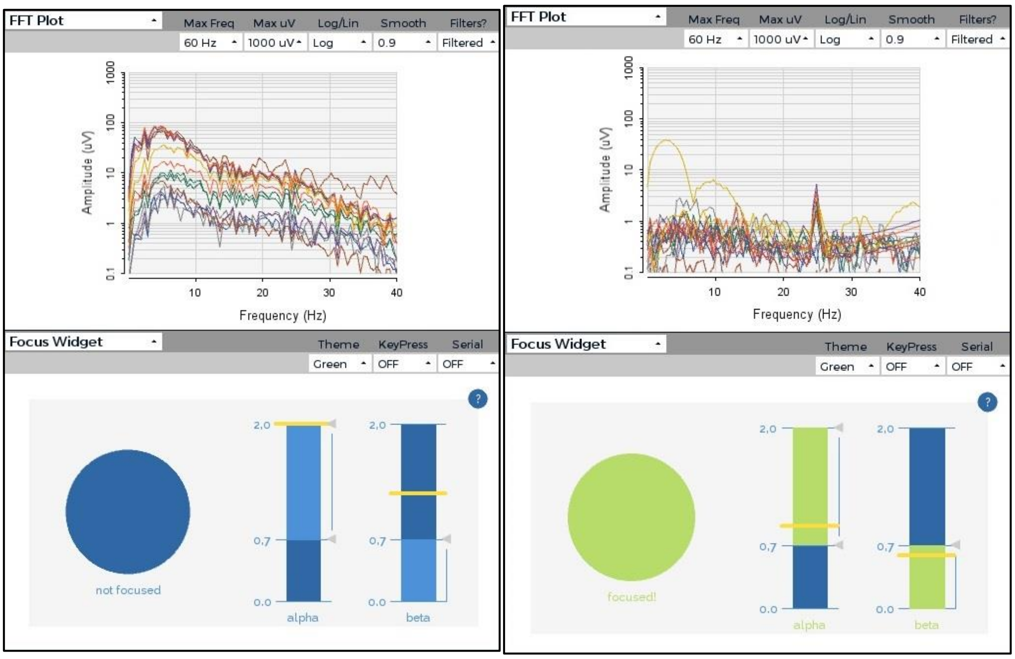


Figura 56 – Prueba de concentración mediante un widget de OpenBCI GUI. Observando los niveles de las ondas alfa y beta podemos saber si estamos en el punto de concentración óptimo. Este se basa en investigaciones de OpenBCI que respaldan estados enfocados que se alinean con niveles alfa entre 0.7-2.0 µV y los niveles beta entre 0.0-0.7 µv. (Gráficas tomadas de la pantalla del programa GUI)

El widget [25] reconoce un estado mental "enfocado" al observar los niveles de las onda alfa y beta en los canales 1 y 2. Se basa en investigaciones que respaldan estados enfocados que se alinean con niveles alfa entre 0.7-2.0 µV y los niveles beta entre 0.0-0.7 µV. Si nuestros datos están fuera de esta relación, el algoritmo indica que no está enfocado.

4.5 Acelerómetro

4.5.1 Definición y especificaciones

Cada placa de OpenBCI está equipada con un acelerómetro de tres ejes, cuyos datos son transmitidos al widget "Accelerometer" de OpenBCI GUI.

Este acelerómetro mide la aceleración de la placa en los ejes xyz, y se muestra visualmente la aceleración xyz relativa en el momento actual en un gráfico como el que se añade a continuación:

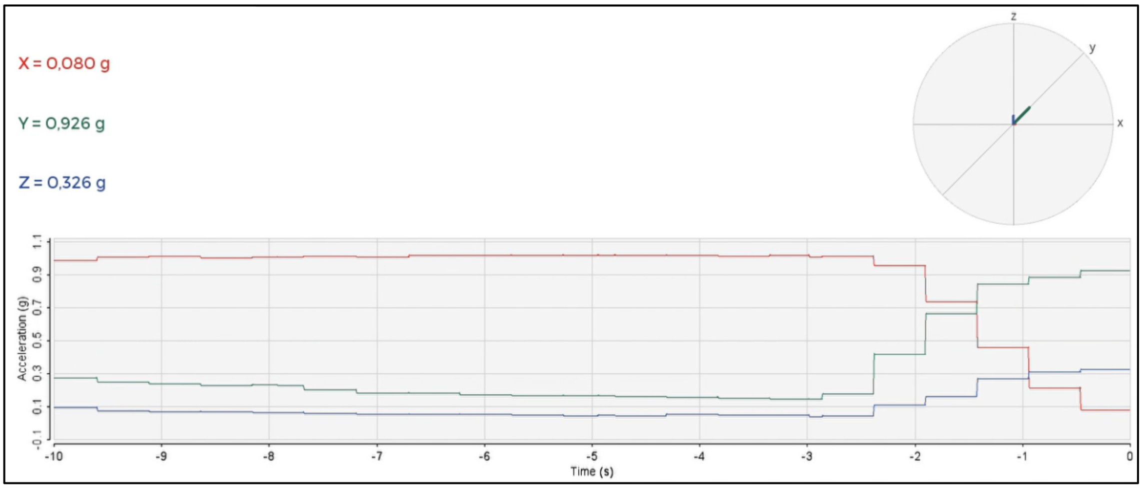


Figura 57 - Visión del acelerómetro en la aplicación GUI. Eje X (rojo), eje Y (verde), eje Z (azul). (Gráfica tomada de la pantalla del programa GUI)

La gráfica aceleración/tiempo nos indica las aceleraciones xyz relativas a lo largo del tiempo, codificadas por los colores de los ejes.

Rojo: Eje X Verde: Eje Y Azul: Eje Z

4.5.2 Prueba de funcionamiento del acelerómetro

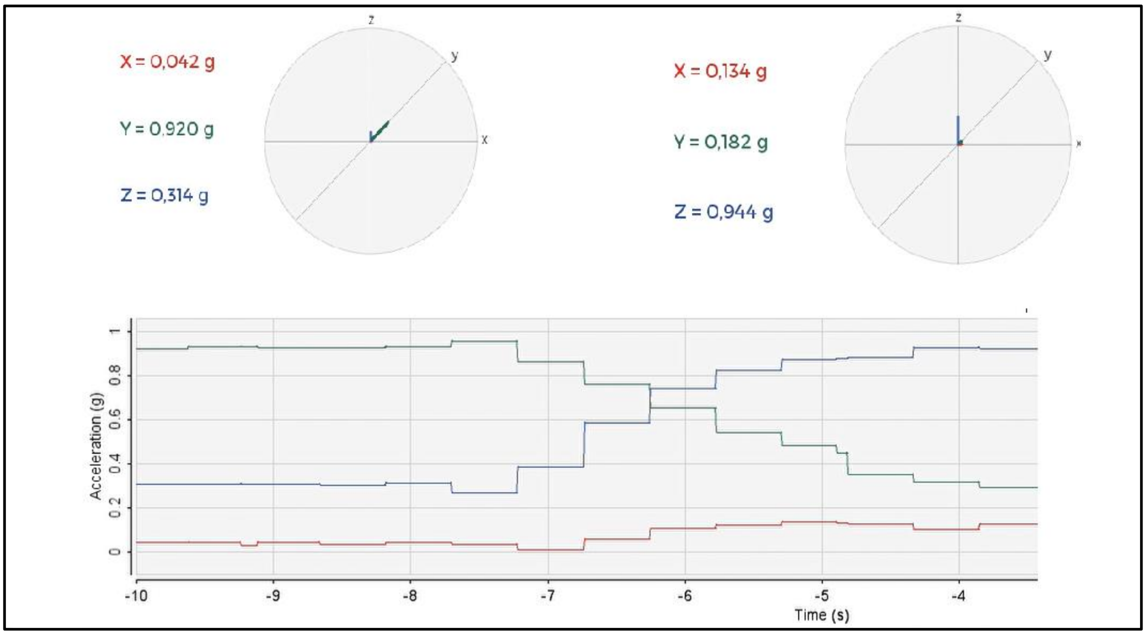


Figura 58 – En la parte izquierda superior podemos observar los valores iniciales de los ejes del acelerómetro (positivo en Y ya que la placa esta ligeramente inclinada y no perpendicular al casoc) y en la superior derecha el cambio de los mismos tras realizar un giro hacia delante del dispositivo UltraCortex Mark IV. Esto demuestra que, si movemos nuestra cabeza hacia delante, como haciendo una reverencia, abajo en dirección frontal con el casco puesto, nos estamos moviendo en positivo en el eje Z.

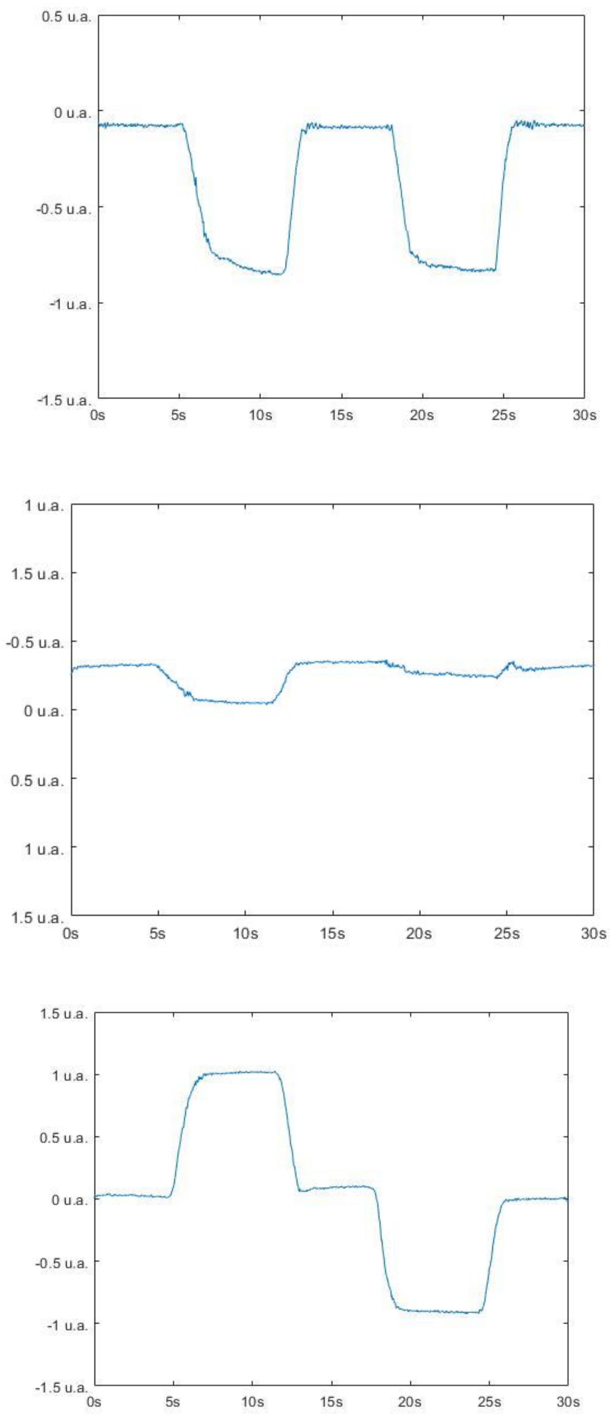


Figura 59 - Respuesta acelerómetro en eje x,y,z respectivamente. La prueba consiste en mover el casco hacia delante (sin tenerlo en la cabeza, simplemente agarrando el casco con las manos. Es decir, estamos haciendo un giro del casco en dirección frontal. Y después realizarlo, hacemos el mismo movimiento hacia atrás. (Gráfica a partir de fichero de datos)

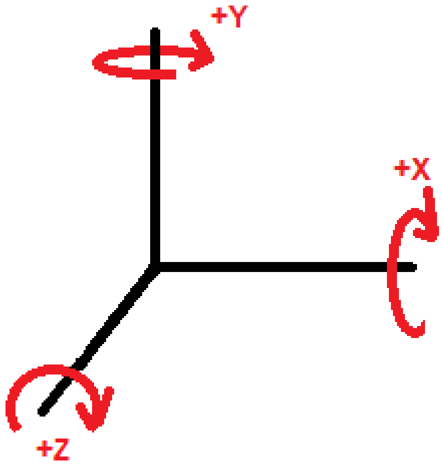


Figura 60 - Dirección de los giros del acelerómetro. El eje x en el casco controla el giro hacia la derecha (--X) o izquierda (+X), el Z, si hacemos movimientos hacia delante (+Z) o hacia atrás (-Z) con el casco. Y el eje Y teniendo el casco puesto no variaba mucho, pero me di cuenta que varía según tengamos el casco girado totalmente hacia arriba (-Y) o colocado normal recto (+Y).

Capítulo 5
Pruebas solicitadas

5.1 Pruebas recomendadas por el neurólogo Dr. Jesús Llabrés

Las siguientes pruebas se han realizado con este sujeto:

- Hombre, 55 años, 178 cm, 86 Kg.

- <u>Filtro empleado en las gráficas de las pruebas:</u>

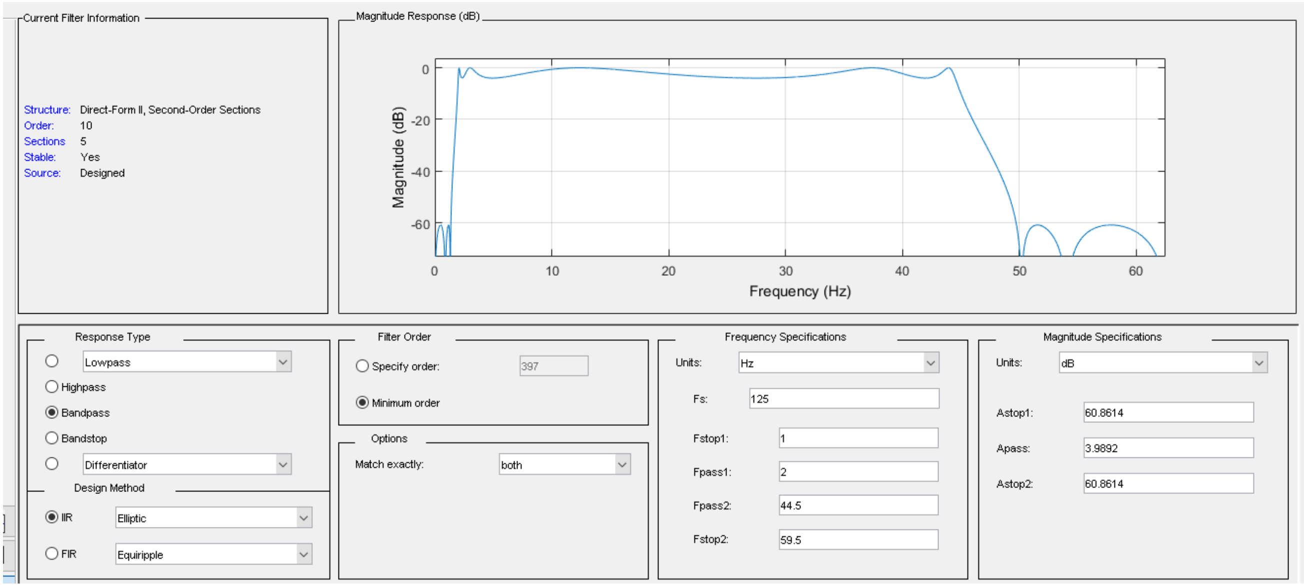


Figura 63 - Filtro utilizado para filtrar las gráficas de las pruebas

- <u>Script del filtro:</u>

```
function Hd = F2
%F2 Returns a discrete-time filter object.

% MATLAB Code
% Generated by MATLAB(R) 8.6 and the DSP System Toolbox 9.1.
% Generated on: 10-Jun-2020 18:50:25

% Elliptic Bandpass filter designed using FDESIGN.BANDPASS.

% All frequency values are in Hz.
Fs = 125;  % Sampling Frequency

Fstop1 = 1;       % First Stopband Frequency
Fpass1 = 2;       % First Passband Frequency
Fpass2 = 44.5;    % Second Passband Frequency
Fstop2 = 59.5;    % Second Stopband Frequency
```

```
Astop1 = 60.8614;  % First Stopband Attenuation (dB)
Apass  = 3.9892;   % Passband Ripple (dB)
Astop2 = 60.8614;  % Second Stopband Attenuation (dB)
match  = 'both';   % Band to match exactly

% Construct an FDESIGN object and call its ELLIP method.
h  = fdesign.bandpass(Fstop1, Fpass1, Fpass2, Fstop2, Astop1, Apass, ...
                  Astop2, Fs);
Hd = design(h, 'ellip', 'MatchExactly', match);

% [EOF]
```

5.1.1 Ojos abiertos / Ojos cerrados

Esta prueba consiste en alternar estados de ojos abiertos y cerrados durante 10 segundos cada uno, y observar si se captan las ondas alfa en 10 Hz en los electrodos occipitales.

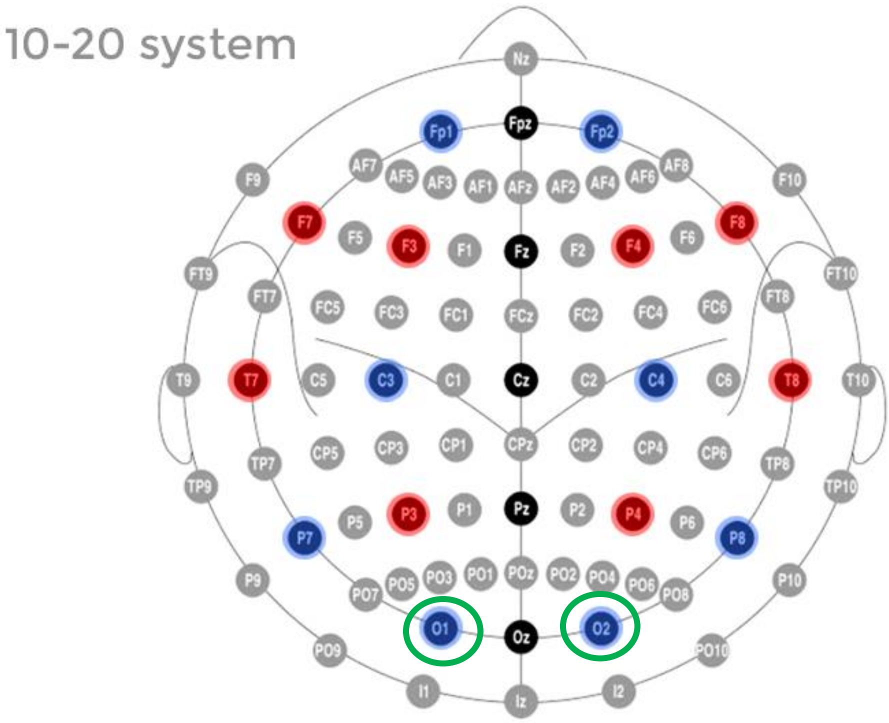


Figura 64 – En verde se ven las ubicaciones de los electrodos occipitales O1 y O2, de interés para la prueba de registro de ojos abiertos / ojos cerrados. En rojo y en azul, se pueden observar las posiciones elegidas de los electrodos para nuestro sistema de 16 canales.

Para ello hay que hacer un registro alternando ojos abiertos y cerrados cada 10 segundos: 10 segundos abiertos, 10 segundos cerrados, 10 segundos abiertos… Así durante 1 minuto.

Se ha realizado la siguiente secuencia:

```
COMIENZO DE LA PRUEBA

Abiertos: 13:51:44
          13:51:54

Cerrados: 13:51:54
          13:52:04

Abiertos: 13:52:04
          13:52:14

Cerrados: 13:52:14
          13:52:24

Abiertos: 13:52:24
          13:52:34

Cerrados: 13:52:34
          13:52:44

FIN DE LA PRUEBA
```

Ilustración 65 - Secuencia empleada para la prueba ojos abiertos y cerrados

Situación ojos abiertos:

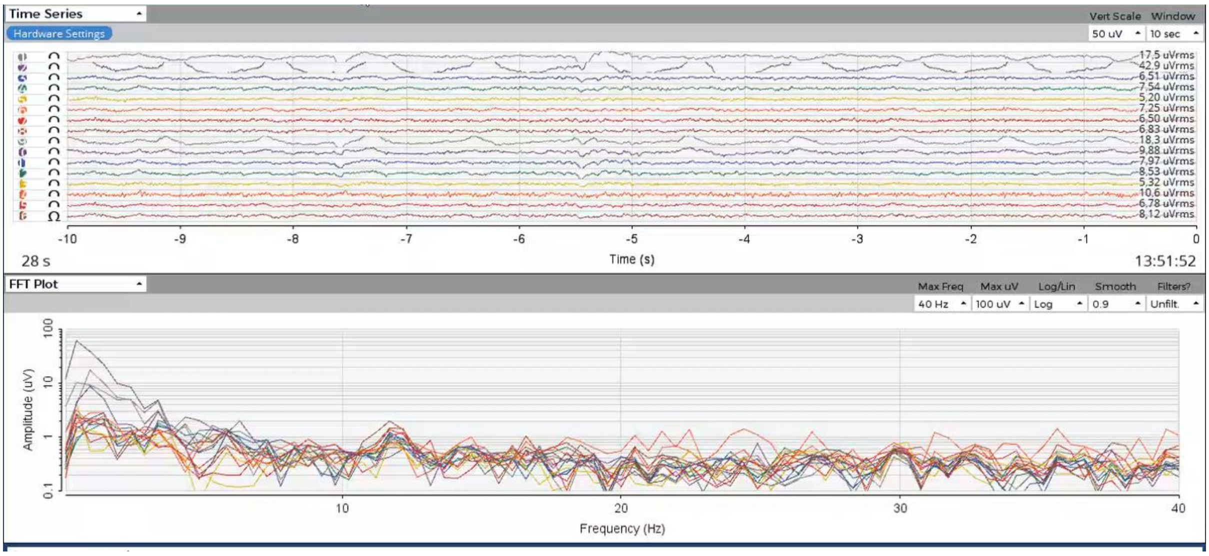


Figura 66 - Situación inicial con los ojos abiertos (Gráfica tomada de la pantalla del programa GUI)

Situación ojos cerrados:

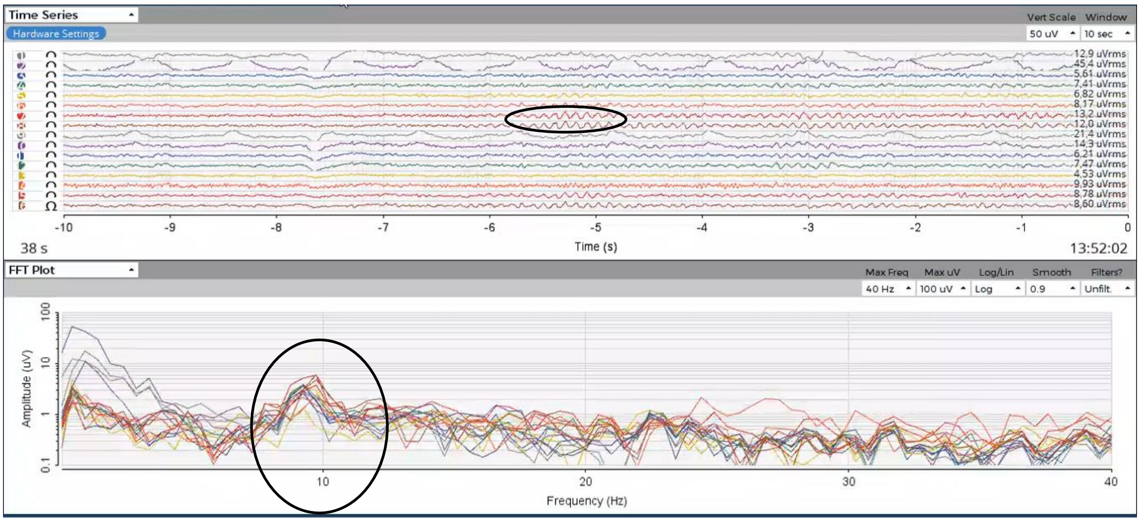


Ilustración 67 - Situación con ojos cerrados. Se observa el aumento de amplitud sobre los 10 Hz y la aparición de las ondas alfa en los electrodos occipitales O1 y O2. (O1 en el programa es el electrodo 7 y O2 es el electrodo 8) (Gráfica tomada de la pantalla del programa GUI)

Podemos observar claramente el aumento de amplitud alrededor de los 10 Hz y cómo empiezan a cambiar las ondas occipitales cuando se cierran los ojos.

Si ampliamos para observar los electrodos occipitales: 7 (rojo) y 8 (marrón) podríamos apreciar claramente como se muestran las ondas alfa:

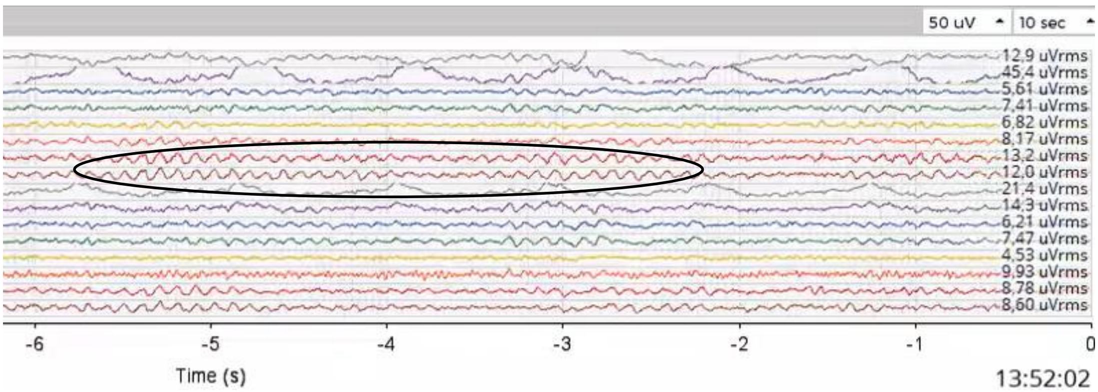


Figura 68 - Situación con ojos cerrados. Se observa la aparición de las ondas alfa en los electrodos occipitales O1 y O2. (O1 en el programa es el electrodo 7-rojo y O2 es el electrodo 8-marrón) (Gráfica tomada de la pantalla del programa GUI)

Con el registro de los datos en .txt se ha podido realizar la siguiente gráfica representativa donde se puede apreciar las ondas alfa:

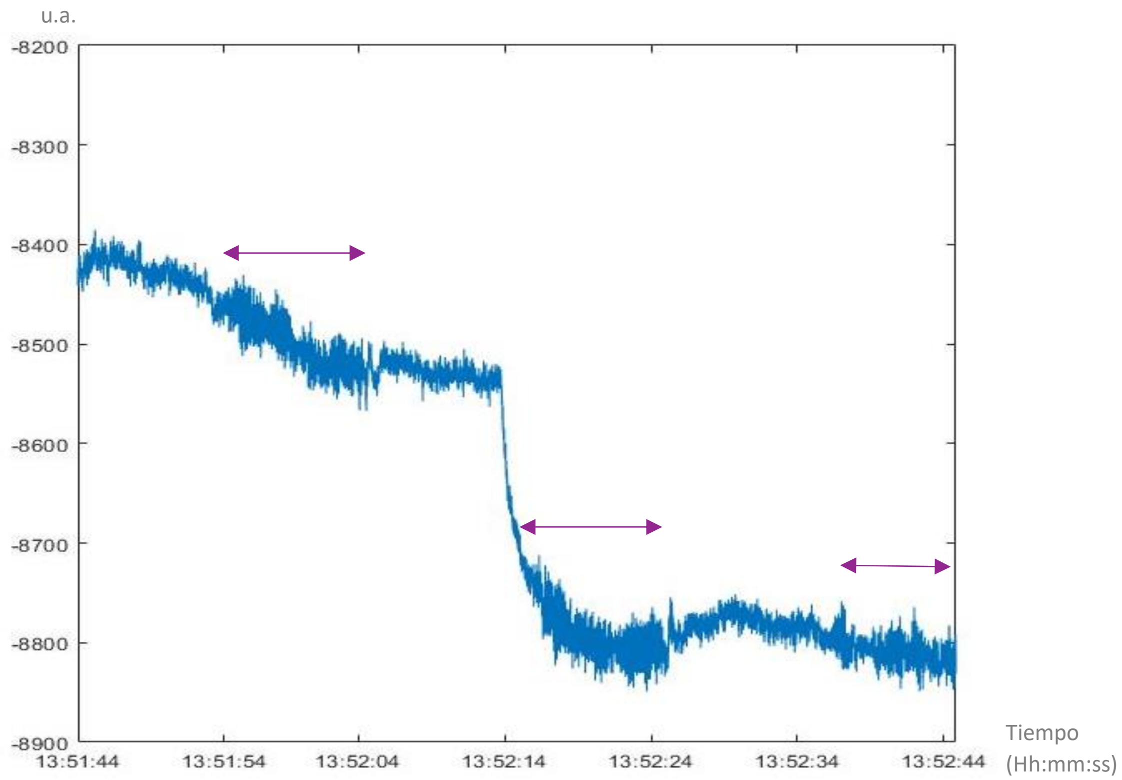


Figura 69 – Representación electrodo occipital O1 (nº7 en GUI). En violeta se observan los periodos de los ojos cerrados, en el resto se tiene los ojos abiertos. Se puede apreciar perfectamente la aparición de las ondas alfa durante los ojos cerrados. (Gráfica a partir de fichero de datos, sin filtro)

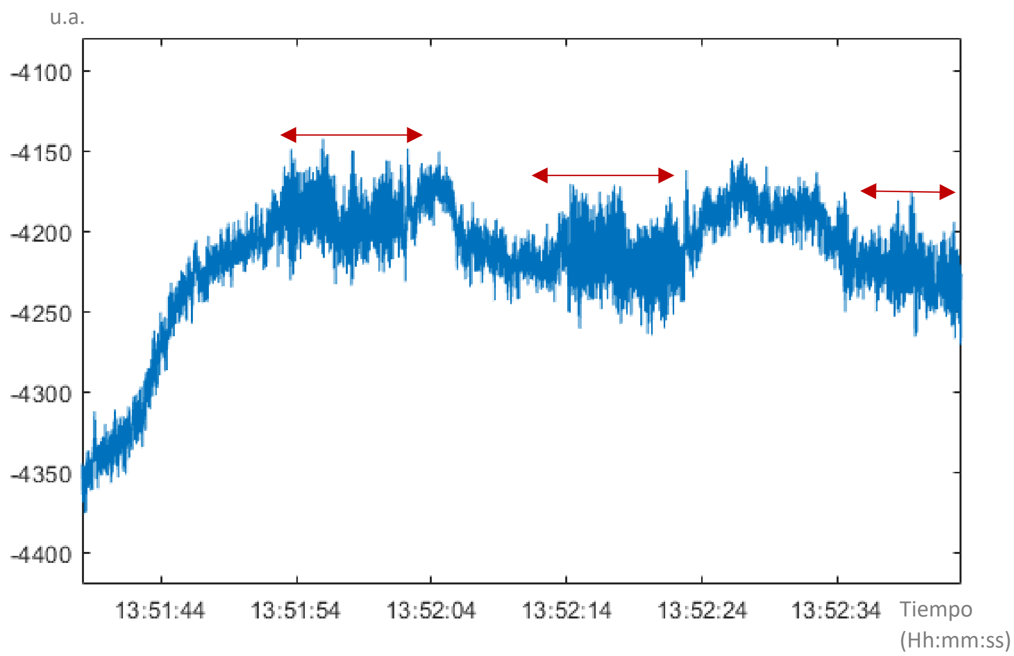


Figura 70 - Representación electrodo occipital O2 (nº8 en GUI). En rojo se observan los periodos de los ojos cerrados, en el resto se tiene los ojos abiertos. Se puede apreciar perfectamente la aparición de las ondas alfa durante los ojos cerrados. (Gráfica a partir de fichero de datos, sin filtro)

En los periodos que se representan con las flechas violetas y rojas en ambos gráficos, es donde podemos observar las ondas alfa durante las partes de la prueba con los ojos cerrados. El resto, es con los ojos abiertos.

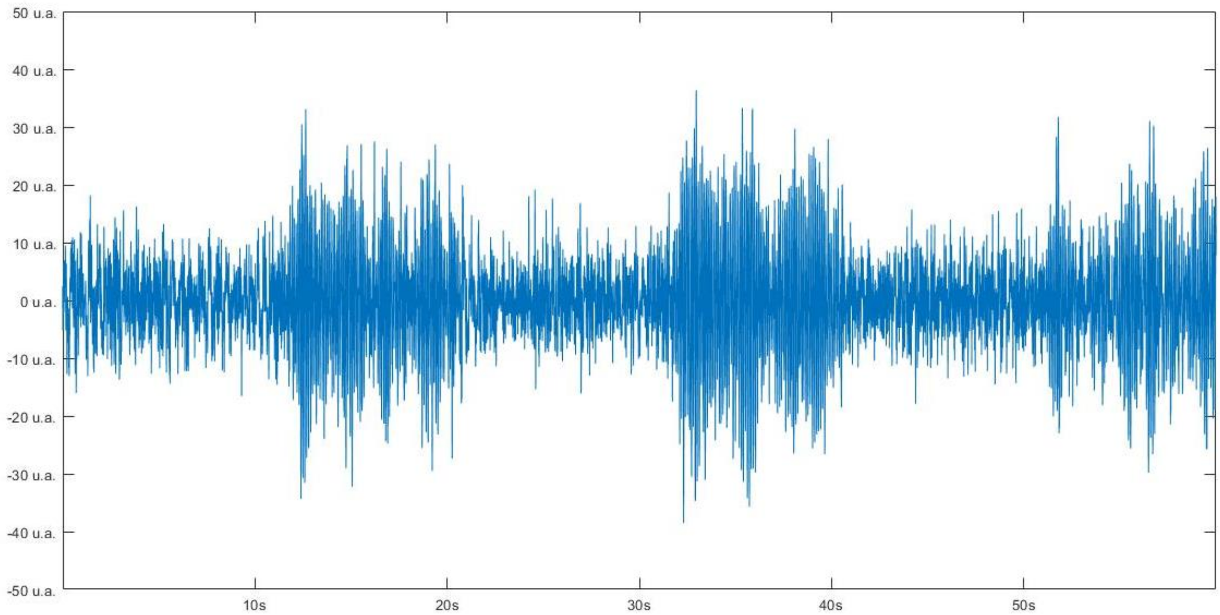


Figura 71 - Gráfica con filtro de la prueba ojos cerrados/abiertos en función del tiempo. Se puede observar claramente las ondas alfa en los periodos de ojos cerrados. (Gráfica a partir de fichero de datos, electrodo 7 (O1)).

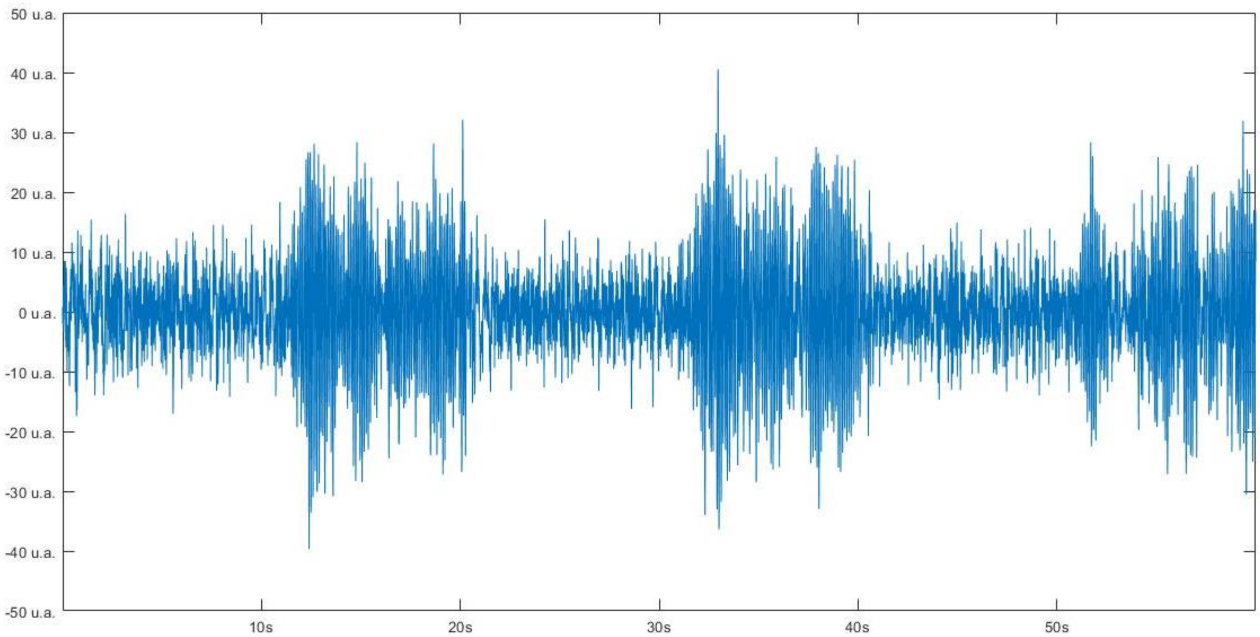


Figura 72 - Gráfica con filtro de la prueba ojos cerrados/abiertos en función del tiempo. Se puede observar claramente las ondas alfa en los periodos de ojos cerrados. (Gráfica a partir de fichero de datos, electrodo 8 (O2)).

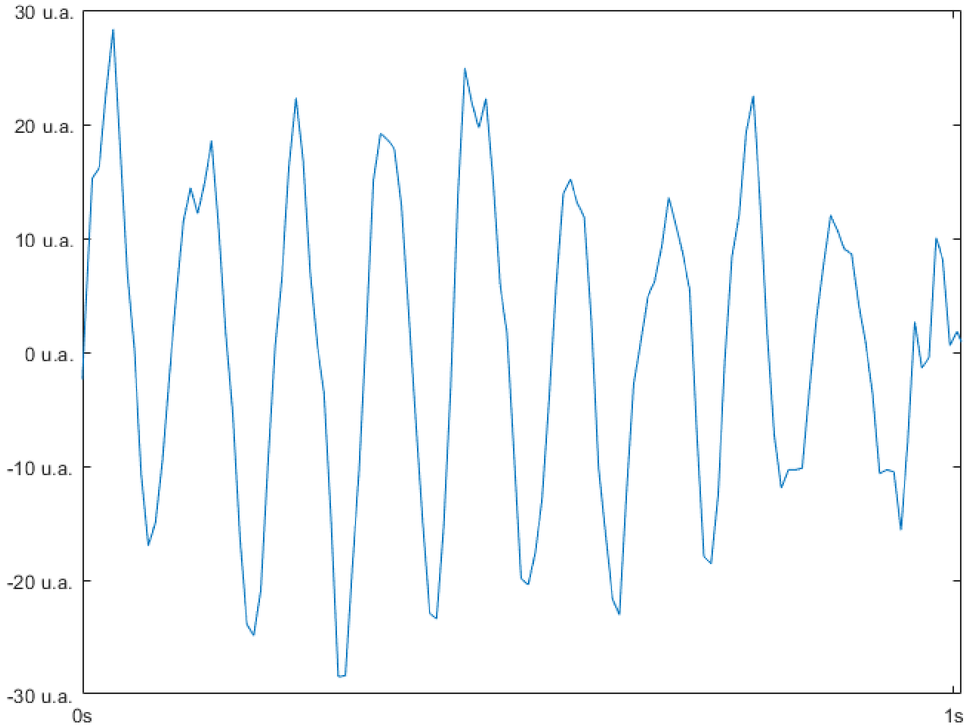


Ilustración 73 - Gráfica con filtro de la prueba ojos cerrados/abiertos en función del tiempo. Se puede observar los 10 ciclos a lo largo de 1 segundo.

5.1.2 Registro parpadeo

En esta prueba, se desea captar el comportamiento en electrodos FP1 y FP2, situados en la zona frontal, durante el proceso de parpadeo, ver figura 67.

La prueba consiste en durante 5 segundos parpadear, los 5 segundos siguientes descanso… así sucesivamente durante 30 segundos.

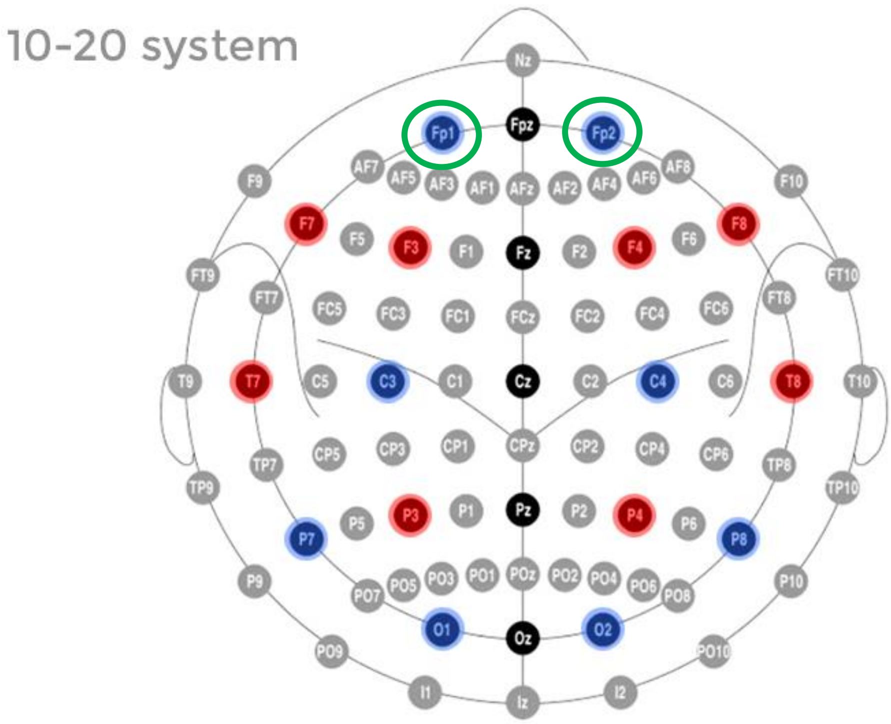


Figura 74 – En verde podemos ver las ubicaciones electrodos FP1 y FP2, de interés para la prueba de registro de parpadeo. En azul y en rojo, se muestran las posiciones elegidas para nuestro sistema de 16 electrodos.

Se ha realizado la siguiente secuencia:

```
INICIO PRUEBA

Parpadeo 13:56:55
         13:57:00

Parar    13:57:00
         13:57:05

Parpadeo 13:57:05
         13:57:10

Parar    13:57:10
         13:57:15

Parpadeo 13:57:15
         13:57:20

Parar    13:57:20
         13:57:25

FIN PRUEBA
```

Figura 75 - Secuencia empleada para prueba de parpadeo

En la siguiente imagen podemos observar:

-En verde: Cuando no se realiza parpadeo

-En rojo: Cuando se está parpadeando

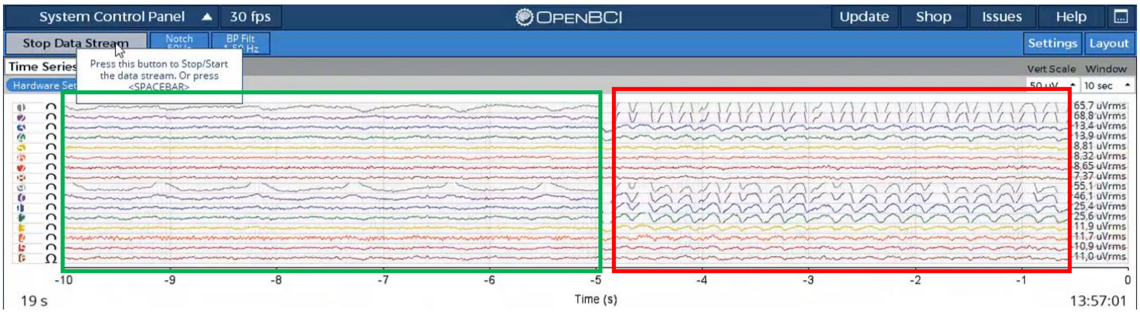


Figura 76 - Diferencia entre periodo sin parpadear (izquierda, recuadro verde) y periodo parpadeando (derecha, recuadro rojo) (Gráfica tomada de la pantalla del programa GUI)

Al abrirse los ojos, el movimiento del globo ocular hacia abajo hace que la córnea (que tiene carga positiva) se aleje de los electrodos Fp1 y Fp2, haciéndolos más negativos y, por lo tanto, genera una onda negativa; el cierre de los ojos hace que los electrodos Fp1 y Fp2 se hagan más positivos, por el acercamiento de la córnea hacia ellos, lo que resulta en una deflexión positiva [26].

De ahí que veamos esa secuencia en 1 (gris) y 2 (violeta) tan clara similar a una oscilación.

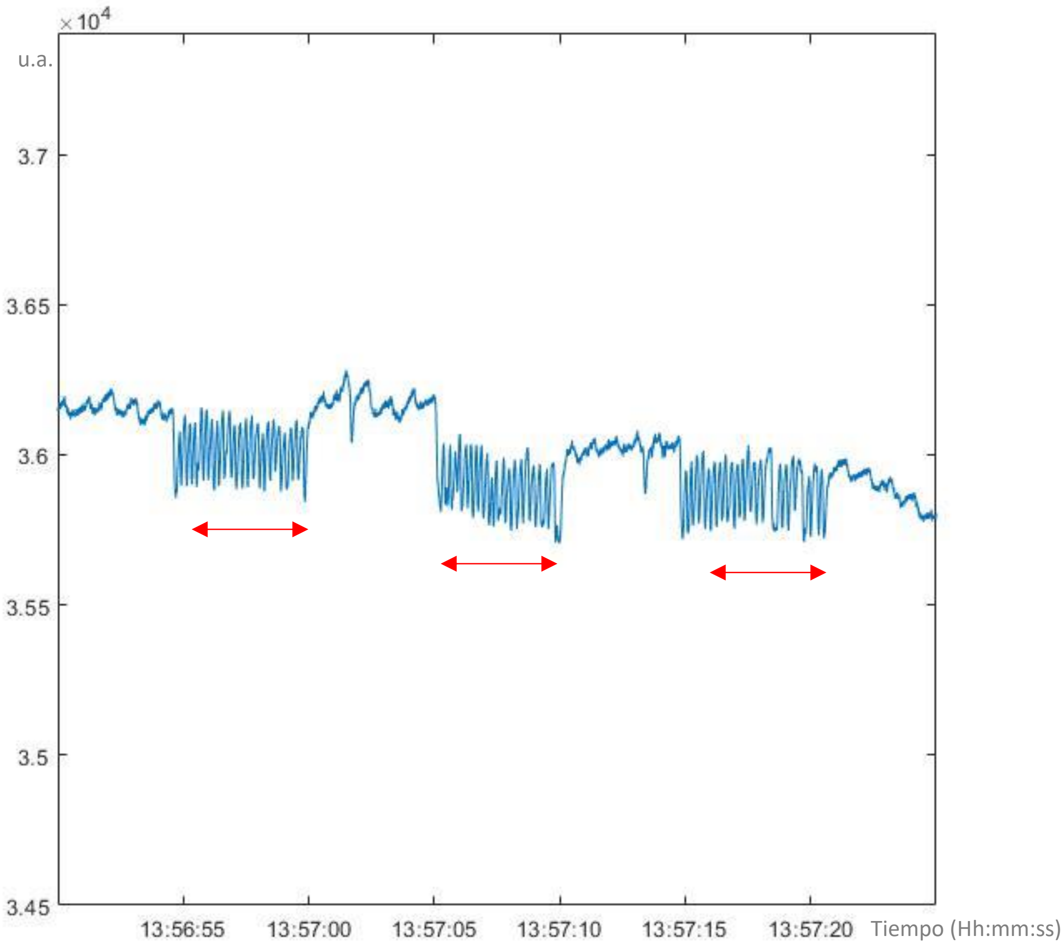


Figura 77 - En rojo se puede apreciar perfectamente el periodo de parpadeo, el resto es una situación normal sin constante parpadeo. (Gráfica a partir de fichero de datos, sin filtro)

Podemos observar, destacado con las flechas en rojo, los periodos en dónde se realiza el parpadeo.

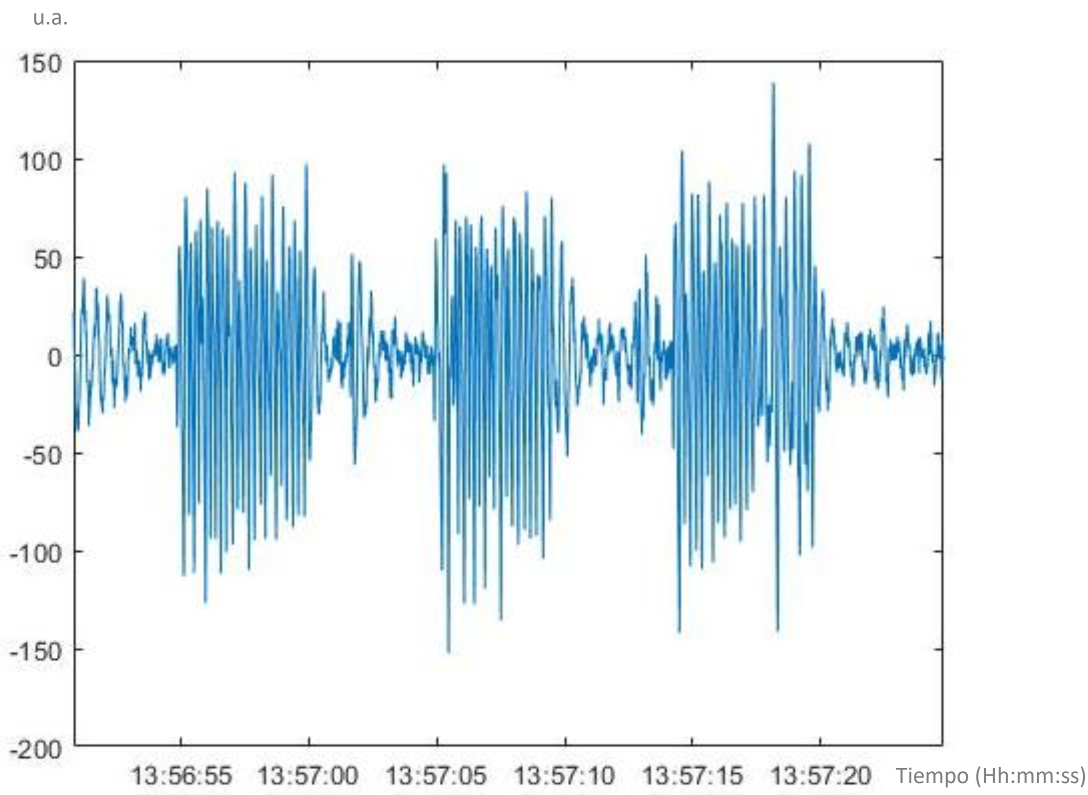


Figura 78 - Gráfica con filtro de la prueba parpadeo siguiendo la secuencia de tiempo comentada previamente. Se puede observar claramente 7 periodos: 4 en situación normal y 3 parpadeando. (Gráfica a partir de fichero de datos)

5.1.3 Mirar alternativamente izquierda-derecha

Esta prueba tiene una duración de 1 minuto y consiste en mirar alternativamente a derecha e izquierda sin mover la cabeza, 5 segundos a cada lado de forma cómoda. Tenemos que fijarnos en el comportamiento de los electrodos F7 y F8, deberían ir en contrafase.

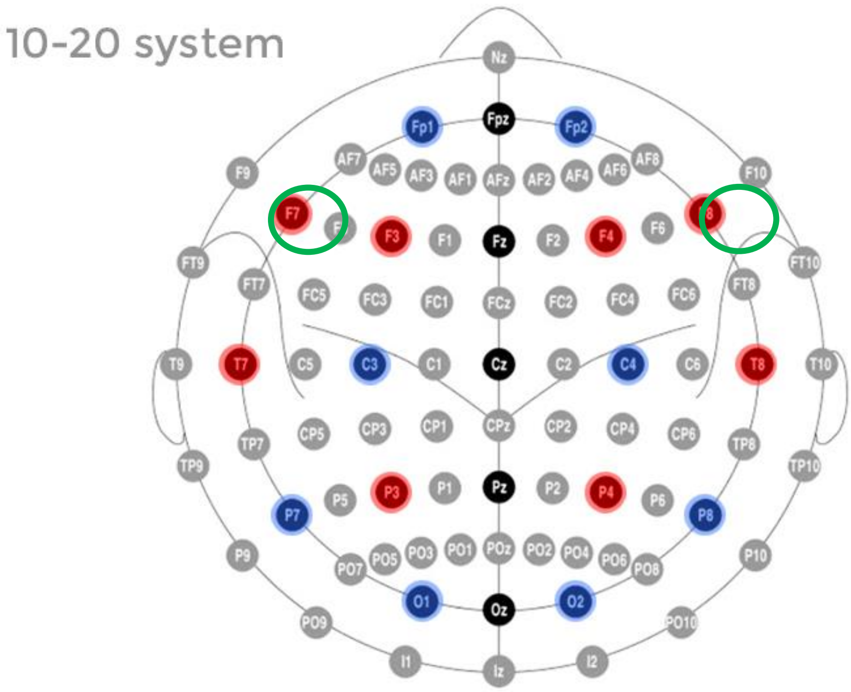


Figura 79 - Ubicaciones electrodos F7 y F8, de interés para la prueba de mirar a izquierda y derecha alternativamente.

Se ha realizado la siguiente secuencia:

```
INICIO PRUEBA

Mirar a la derecha   13:55:10
                     13:55:15

Mirar a la izquierda 13:55:15
                     13:55:20

Mirar a la derecha   13:55:20
                     13:55:25

Mirar a la izquierda 13:55:25
                     13:55:30

Mirar a la derecha   13:55:30
                     13:55:35

Mirar a la izquierda 13:55:35
                     13:55:40

Mirar a la derecha   13:55:40
                     13:55:45

Mirar a la izquierda 13:55:45
                     13:55:50

Mirar a la derecha   13:55:50
                     13:55:55

Mirar a la izquierda 13:55:55
                     13:56:00

Mirar a la derecha   13:56:00
                     13:56:05

Mirar a la izquierda 13:56:05
                     13:56:10

FIN PRUEBA
```

Figura 80 - Secuencia empleada para prueba de mirar alternativamente a izquierda y derecha.

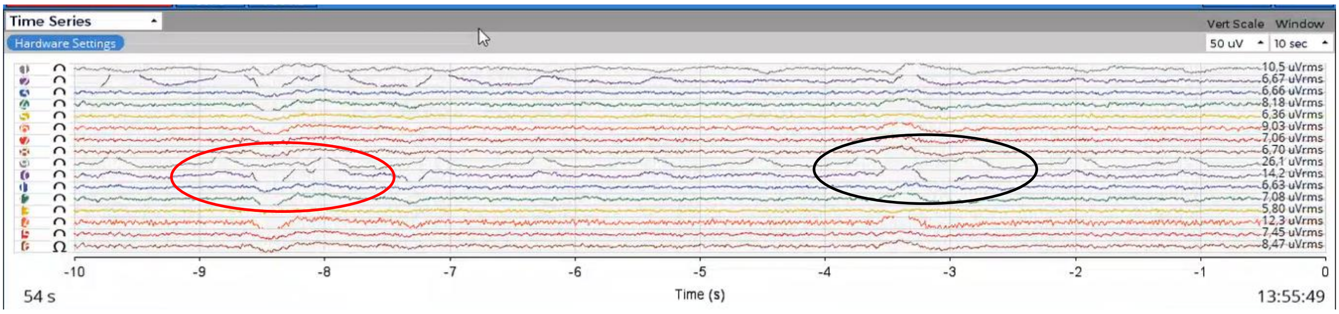


Figura 81 -En rojo podemos aprecias el momento en que el sujeto mira a la derecha, y en negro cuando mira a la izquierda. Se observa que ambas ondas (Onda en F7 y onda en F8) van en contrafase como era de esperar.

Redondeado en color rojo podemos ver la respuesta al estímulo de mirar hacia la derecha en los electrodos F7 y F8 (en el programa electrodo nº9-color gris y nº10-color violeta respectivamente).

Y en color negro la respuesta cuando el sujeto mira a la izquierda.

Podemos concluir que efectivamente van en contrafase, y se nota más claramente a la hora de mirar hacia la derecha.

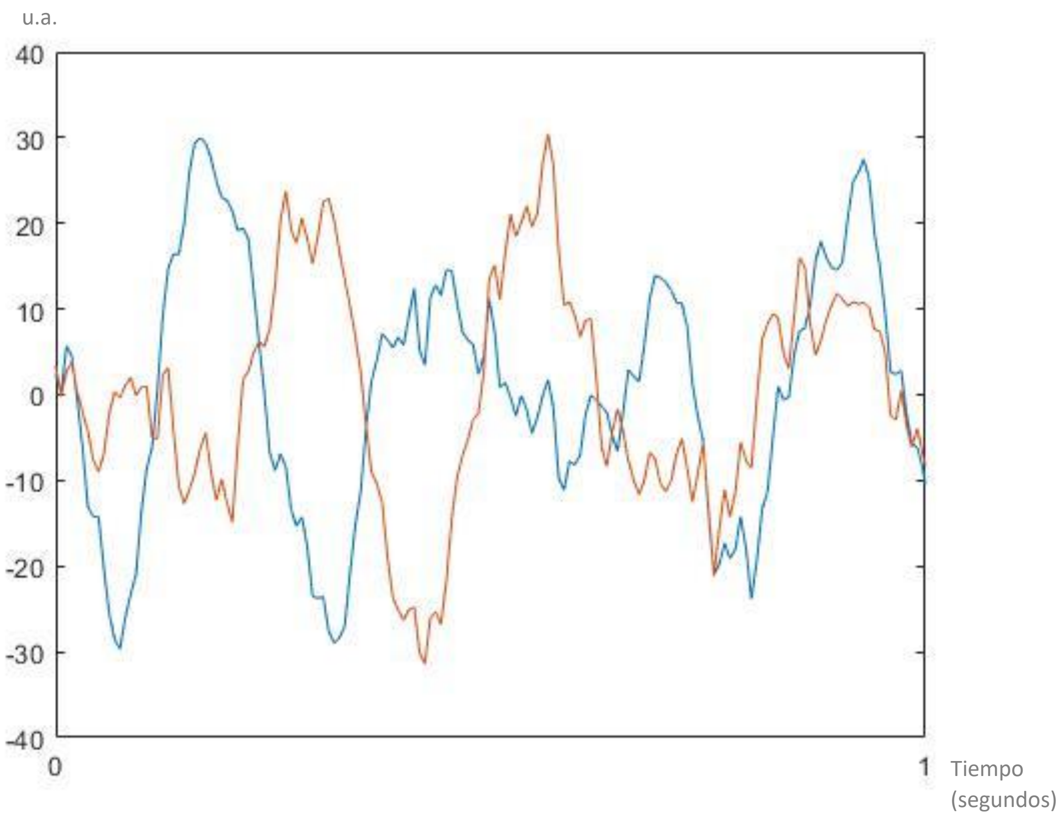


Figura 82 - Gráfica con filtro resultado de la prueba mirar a izquierda y derecha alternativamente. En azul: respuesta F7. En rojo: Respuesta electrodo F8. Se puede ver claramente que van a contrafase.

5.2 Prueba recomendada por el profesor Sergio Elías (16 canales)

Las siguientes pruebas han sido realizadas con 3 sujetos con los siguientes datos:

- Sujeto 1: Mujer, 28 años. Nivel de estudios: Universitario

- Sujeto 2: Mujer, 58 años. Nivel de estudios: COU

- Sujeto 3: Hombre, 26 años. Nivel de estudios: Universitario

5.2.1 Detección de estado de meditación por electroencefalografía

En esta prueba se desea registrar una meditación guiada.

Consiste en poner el casco al voluntario y que vea un vídeo de meditación.

El vídeo tiene primero una parte teórica [27] y luego una meditación guiada [28].

El vídeo de meditación guiada dura aproximadamente 10 minutos.

Al final de la prueba, se le ha realizado un cuestionario sobre la misma a cada uno de los sujetos. Los resultados se muestran a continuación.

Sujeto 1:

Edad: 28

Género: mujer

Nivel de estudios acabados: Universitario

Cuestionario meditación. Valoraciones de 0 (nada) a 5 (excelente):

Tabla 8 - Cuestionario meditación (Sujeto 1)

Interés en la meditación	4
¿Pudo seguir las instrucciones?	3
Percibió brisa fresca en las manos (0 nada-5 muy claro)	3 (Mano derecha)
Percibió brisa fresca parte superior de la cabeza (fontanela) (0-5 muy claro)	3
Percibió calor en las manos (yemas de los dedos) (0-5 muy claro)	2 (Mano izquierda)
Percibió calor en la parte superior de la cabeza (fontanela) (0-5 muy claro):	2

Comentarios: Se desconcentró un poco cuando tuvo que hacer los movimientos de las manos sobre la cabeza, ya que con el casco es imposible tener contacto directo sobre la misma. Dado esto, no pudo seguir exactamente las instrucciones que se le pedían.

Le gustó mucho la experiencia, se sintió relajada durante la prueba y al final.

Sujeto 2:

Edad: 58

Género: mujer

Nivel de estudios acabados: COU

Cuestionario meditación. Valoraciones de 0 (nada) a 5 (excelente):

Tabla 9 - Cuestionario meditación (Sujeto 2)

Interés en la meditación	3
¿Pudo seguir las instrucciones?	4 (Muy bien explicado)
Percibió brisa fresca en las manos (0 nada-5 muy claro)	2 (Sensación de hormigueo)
Percibió brisa fresca parte superior de la cabeza (fontanela) (0-5 muy claro)	0
Percibió calor en las manos (yemas de los dedos) (0-5 muy claro)	0
Percibió calor en la parte superior de la cabeza (fontanela) (0-5 muy claro):	0

Comentarios: Una experiencia agradable y relajante. Misma opinión que el sujeto 1, que fue una pena que no pudiera tener contacto directo su mano con su cabeza por el casco.

Sujeto 3:

Edad: 26

Género: Hombre

Nivel de estudios acabados: Universitario

Cuestionario meditación. Valoraciones de 0 (nada) a 5 (excelente):

Tabla 10 - Cuestionario meditación (Sujeto 3)

Interés en la meditación	3
¿Pudo seguir las instrucciones?	3 (Dificultad al repetir frases continuamente en poco tiempo)
Percibió brisa fresca en las manos (0 nada-5 muy claro)	2 (Mano derecha)
Percibió brisa fresca parte superior de la cabeza (fontanela) (0-5 muy claro)	0
Percibió calor en las manos (yemas de los dedos) (0-5 muy claro)	0
Percibió calor en la parte superior de la cabeza (fontanela) (0-5 muy claro):	0

Comentarios: Una experiencia no tan relajante como esperaba. Se desconcentro en ocasiones como por ejemplo cuando tenía que repetir algunas frases y contarlas a la vez. Pensaba tanto en contar cuantas estaba diciendo que en la relajación en sí. Misma opinión que los otros dos sujetos, hubiese estado mejor la meditación si no hubieran llevado el casco encima.

Capítulo 6
Conclusiones

El objetivo de este TFG fue montar, probar y calibrar dos sistemas de electroencefalografía de OpenBCI. Por un lado, se trabajó con la Headband de 4 canales y por otro lado con el Ultracortex IV tanto de 8 canales como de 16.

Con el dispositivo de 4 y 8 canales se pudieron realizar pruebas de concentración, así como de situaciones cotidianas como escribir, escuchar música… Pudiendo analizar las respuestas obtenidas en la aplicación GUI de OpenBCI, así como los cambios del voltaje y frecuencia de las ondas encefalográficas a través de los electrodos.

Cuando se realizó el montaje y la prueba con el dispositivo de 16 electrodos, pudimos ver que llegamos a controlar más en profundidad lo que estaba ocurriendo en nuestro cerebro, ya que teníamos más puntos donde recoger datos. Es por eso que, las pruebas más completas se realizaron con este último dispositivo, por ejemplo: detectar las ondas alfa en los electrodos occipitales con claridad durante la prueba de ojos abiertos/cerrados y el aumento de la amplitud (uV) sobre los 10 Hz, observar el comportamiento de las ondas en los electrodos de las posiciones FP1 y FP2 en la prueba de parpadeo, F7 y F8 yendo a contrafase si miramos a izquierda y a derecha alternativamente… Así como, la realización de una prueba de meditación guiada dónde se pudo recoger las valoraciones de la misma a través de un cuestionario a los sujetos que participaron en ella.

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Anexos

Anexo 1

Hojas de datos: Circuito integrado amplificador AD8237

Micropower, Zero Drift, True Rail-to-Rail Instrumentation Amplifier

Data Sheet **AD8237**

FEATURES

- Gain set with 2 external resistors
  - Can achieve low gain drift at all gains
- Ideal for battery powered instruments
  - Supply current: 115 µA
  - Rail-to-rail input and output
  - Zero input crossover distortion
- Designed for excellent dc performance
  - Minimum CMRR: 106 dB
  - Maximum offset voltage drift: 0.3 µV/°C
  - Maximum gain error: 0.005% (all gains)
  - Maximum gain drift: 0.5 ppm/°C (all gains)
  - Input bias current: 1 nA guaranteed to 125°C
- Bandwidth mode pin (BW) to adjust compensation
- 8 kV HBM ESD rating
- RFI filter on-chip
- Single-supply operation: 1.8 V to 5.5 V
- 8-lead MSOP package

APPLICATIONS

- Bridge amplification
- Pressure measurement
- Medical instrumentation
- Thermocouple interface
- Portable systems
- Current measurement

PIN CONFIGURATION

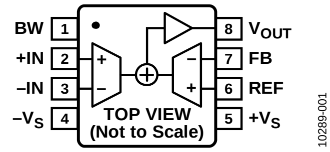

Figure 1.

Table 1. Instrumentation Amplifiers by Category[1]

General Purpose	Zero Drift	Military Grade	Micropower	Digital Gain
AD8421	AD8237	AD620	AD8237	AD8250
AD8221/AD8222	AD8231	AD621	AD8420	AD8251
AD8220/AD8224	AD8293	AD524	AD8235/AD8236	AD8253
AD8228	AD8553	AD526	AD627	AD8231
AD8295	AD8556	AD624		
AD8226	AD8557			

[1] See www.analog.com for the latest instrumentation amplifiers.

GENERAL DESCRIPTION

The AD8237 is a micropower, zero drift, rail-to-rail input and output instrumentation amplifier. The relative match of two resistors sets any gain from 1 to 1000. The AD8237 has excellent gain accuracy performance that can be preserved at any gain with two ratio-matched resistors.

The AD8237 employs the indirect current feedback architecture to achieve a true rail-to-rail capability. Unlike conventional in-amps, the AD8237 can fully amplify signals with common-mode voltage at or even slightly beyond its supplies. This enables applications with high common-mode voltages to use smaller supplies and save power.

The AD8237 is an excellent choice for portable systems. With a minimum supply voltage of 1.8 V, a 115 µA typical supply current, and wide input range, the AD8237 makes full use of a limited power budget, yet offers bandwidth and drift performance suitable for bench-top systems.

The AD8237 is available in an 8-lead MSOP package. Performance is specified over the full temperature range of −40°C to +125°C.

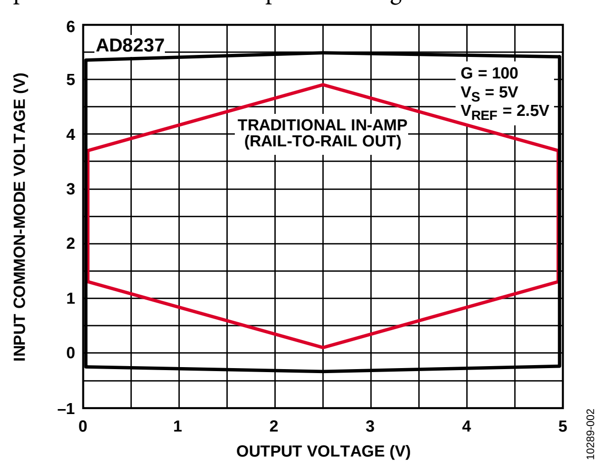

Figure 2. Input Common-Mode Voltage vs. Output Voltage, $+V_S = 5$ V, G = 100

Rev. 0

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Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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REVISION HISTORY

8/12—Revision 0: Initial Version

SPECIFICATIONS

$+V_S = +5$ V, $-V_S = 0$ V, $V_{REF} = 2.5$ V, $V_{CM} = 2.5$ V, $T_A = 25°C$, G = 1 to 1000, $R_L = 10$ kΩ to ground, specifications referred to input, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	$V_{CM} = 0.1$ V to 4.9 V				
CMRR at DC					
G = 1, G = 10		106	120		dB
G = 100, G = 1000		114	140		dB
Over Temperature (G = 1)	$T_A = -40°C$ to $+125°C$	104			dB
CMRR at 1 kHz			80		dB
NOISE					
Voltage Noise					
Spectral Density	f = 1 kHz		68		nV/√Hz
Peak to Peak	f = 0.1 Hz to 10 Hz		1.5		μV p-p
Current Noise					
Spectral Density	f = 1 kHz		70		fA/√Hz
Peak to Peak	f = 0.1 Hz to 10 Hz		3		pA p-p
VOLTAGE OFFSET					
Offset			30	75	μV
Average Temperature Coefficient	$T_A = -40°C$ to $+125°C$			0.3	μV/°C
Offset RTI vs. Supply (PSR)		100			dB
INPUTS[1]	Valid for REF and FB pair, as well as +IN and −IN				
Input Bias Current	$T_A = +25°C$		250	650	pA
Over Temperature	$T_A = -40°C$ to $+125°C$			1	nA
Average Temperature Coefficient			0.5		pA/°C
Input Offset Current	$T_A = +25°C$		250	650	pA
Over Temperature	$T_A = -40°C$ to $+125°C$			1	nA
Average Temperature Coefficient			0.5		pA/°C
Input Impedance					
Differential			100‖5		MΩ‖pF
Common Mode			800‖10		MΩ‖pF
Differential Input Operating Voltage	$T_A = -40°C$ to $+125°C$		±3.85		V
Input Operating Voltage (+IN, −IN, or REF)	$T_A = +25°C$	$-V_S - 0.3$		$+V_S + 0.3$	V
	$T_A = -40°C$ to $+125°C$	$-V_S - 0.2$		$+V_S + 0.2$	V
DYNAMIC RESPONSE					
Small Signal Bandwidth	−3 dB				
Low Bandwidth Mode	Pin 1 connected to $-V_S$				
G = 1			200		kHz
G = 10			20		kHz
G = 100			2		kHz
G = 1000			0.2		kHz
High Bandwidth Mode	Pin 1 connected to $+V_S$				
G = 10			100		kHz
G = 100			10		kHz
G = 1000			1		kHz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Settling Time 0.01%	4 V output step				
Low Bandwidth Mode	Pin 1 connected to $-V_S$				
G = 1			80		µs
G = 10			100		µs
G = 100			440		µs
G = 1000			4		ms
High Bandwidth Mode	Pin 1 connected to $+V_S$				
G = 10			80		µs
G = 100			100		µs
G = 1000			820		µs
Slew Rate					
Low Bandwidth Mode			0.05		V/µs
High Bandwidth Mode			0.15		V/µs
EMI Filter Frequency			6		MHz
GAIN[2]	G = 1 + (R2/R1)				
Gain Range[3]		1		1000	V/V
Gain Error	V_{OUT} = 0.1 V to 4.9 V, G = 1 to G = 1000			0.005	%
Gain Error vs. V_{CM}			15		ppm/V
Gain vs. Temperature	T_A = −40°C to +125°C			0.5	ppm/°C
Gain Nonlinearity	V_{OUT} = 0.2 V to 4.8 V, R_L = 10 kΩ to ground				
G = 1, G = 10			3		ppm
G = 100			6		ppm
G = 1000			10		ppm
OUTPUT					
Output Swing					
R_L = 10 kΩ to Midsupply	T_A = +25°C	$-V_S$ + 0.05		$+V_S$ − 0.05	V
	T_A = −40°C to 125°C	$-V_S$ + 0.07		$+V_S$ − 0.07	V
R_L = 100 kΩ to Midsupply	T_A = +25°C	$-V_S$ + 0.02		$+V_S$ − 0.02	V
	T_A = −40°C to 125°C	$-V_S$ + 0.03		$+V_S$ − 0.03	V
Short-Circuit Current			4		mA
POWER SUPPLY					
Operating Range		1.8		5.5	V
Quiescent Current	T_A = +25°C		115	130	µA
	T_A = −40°C to +125°C			150	µA
TEMPERATURE RANGE					
Specified		−40		+125	°C

[1] Specifications apply to input voltages between 0 V and 5 V. When measuring voltages beyond the supplies, there is additional offset error, bias currents increase, and input impedance decreases, especially at higher temperatures.
[2] For G > 1, errors from the external resistors, R1 and R2, must be added to these specifications, including error from the FB pin bias current.
[3] The AD8237 has only been characterized for gains of 1 to 1000; however, higher gains are possible.

$+V_S = 1.8$ V, $-V_S = 0$ V, $V_{REF} = 0.9$ V, $V_{CM} = 0.9$ V, $T_A = 25°C$, G = 1 to 1000, $R_L = 10$ kΩ to ground, specifications referred to input, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	V_{CM} = 0.2 V to 1.6 V				
CMRR at DC					
G = 1, G = 10		100	120		dB
G = 100, G = 1000		114	140		dB
Over Temperature (G = 1)	T_A = −40°C to +125°C	94			dB
CMRR at 1 kHz			80		dB
NOISE					
Voltage Noise					
Spectral Density	f = 1 kHz, V_{DIFF} ≤ 100 mV		68		nV/√Hz
Peak to Peak	f = 0.1 Hz to 10 Hz, V_{DIFF} ≤ 100 mV		1.5		μV p-p
Current Noise					
Spectral Density	f = 1 kHz		70		fA/√Hz
Peak to Peak	f = 0.1 Hz to 10 Hz		3		pA p-p
VOLTAGE OFFSET					
Offset			25	75	μV
Average Temperature Coefficient	T_A = −40°C to +125°C			0.3	μV/°C
Offset RTI vs. Supply (PSR)		100			dB
INPUTS[1]	Valid for REF and FB pair, as well as +IN and −IN				
Input Bias Current	T_A = +25°C		250	650	pA
Over Temperature	T_A = −40°C to +125°C			1	nA
Average Temperature Coefficient			0.5		pA/°C
Input Offset Current	T_A = +25°C		250	650	pA
Over Temperature	T_A = −40°C to +125°C			1	nA
Average Temperature Coefficient			0.5		pA/°C
Input Impedance					
Differential			100‖5		MΩ‖pF
Common Mode			800‖10		MΩ‖pF
Differential Input Operating Voltage	T_A = −40°C to +125°C		± 0.75		V
Input Operating Voltage (+IN, −IN, REF, or FB)	T_A = +25°C	$-V_S - 0.3$		$+V_S + 0.3$	V
	T_A = −40°C to +125°C	$-V_S - 0.2$		$+V_S + 0.2$	V
DYNAMIC RESPONSE					
Small Signal Bandwidth	−3 dB				
Low Bandwidth Mode	Pin 1 connected to $-V_S$				
G = 1			200		kHz
G = 10			20		kHz
G = 100			2		kHz
G = 1000			0.2		kHz
High Bandwidth Mode	Pin 1 connected to $+V_S$				
G = 10			100		kHz
G = 100			10		kHz
G = 1000			1		kHz
Slew Rate					
Low Bandwidth Mode			0.05		V/μs
High Bandwidth Mode			0.15		V/μs
EMI Filter Frequency			6		MHz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GAIN[2]	G = 1 + (R2/R1)				
Gain Range[3]		1		1000	V/V
Gain Error	V_{OUT} = 0.2 V to 1.6 V, G = 1 to G = 1000			0.005	%
Gain Error vs. V_{CM}			15		ppm/V
Gain vs. Temperature	T_A = −40°C to +125°C			0.5	ppm/°C
Gain Nonlinearity	V_{OUT} = 0.2 V to 1.6 V				
G = 1, G = 10			3		ppm
G = 100			6		ppm
G = 1000			10		ppm
OUTPUT					
Output Swing					
R_L = 10 kΩ to Midsupply	T_A = +25°C	$-V_S + 0.05$		$+V_S - 0.05$	V
	T_A = −40°C to 125°C	$-V_S + 0.07$		$+V_S - 0.07$	V
R_L = 100 kΩ to Midsupply	T_A = +25°C	$-V_S + 0.02$		$+V_S - 0.02$	V
	T_A = −40°C to 125°C	$-V_S + 0.03$		$+V_S - 0.03$	V
Short-Circuit Current			4		mA
POWER SUPPLY					
Operating Range		1.8		5.5	V
Quiescent Current	T_A = +25°C		115	130	µA
	T_A = −40°C to +125°C			150	µA
TEMPERATURE RANGE					
Specified		−40		+125	°C

[1] Specifications apply to input voltages between 0 V and 1.8 V. When measuring voltages beyond the supplies, there is additional offset error, bias currents increase, and input impedance decreases, especially at higher temperatures.
[2] For G > 1, errors from the external resistors, R1 and R2, must be added to these specifications, including error from the FB pin bias current.
[3] The AD8237 has only been characterized for gains of 1 to 1000; however, higher gains are possible.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	6 V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage at −IN, +IN, FB, or REF[1]	$+V_S$ + 0.5 V
Minimum Voltage at −IN, +IN, FB, or REF[1]	$−V_S$ − 0.5 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature Range	−65°C to +150°C
ESD	
Human Body Model	8 kV
Charge Device Model	1.25 kV
Machine Model	0.2 kV

[1] If input voltages beyond the specified minimum or maximum voltages are expected, place resistors in series with the inputs to limit the current to 5 mA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

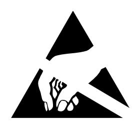
THERMAL RESISTANCE

θ_{JA} is specified for a device in free air.

Table 5.

Package	θ_{JA}	Unit
8-Lead MSOP, 4-Layer JEDEC Board	145.7	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

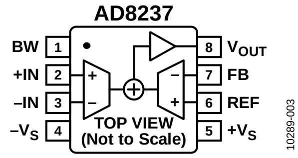


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BW	For high bandwidth mode, connect this pin to $+V_S$, or for low bandwidth mode, connect this pin to $-V_S$. Do not leave this pin floating.
2	+IN	Positive Input.
3	−IN	Negative Input.
4	$-V_S$	Negative Supply.
5	$+V_S$	Positive Supply.
6	REF	Reference Input.
7	FB	Feedback Input.
8	V_{OUT}	Output.

TYPICAL PERFORMANCE CHARACTERISTICS

$+V_S = +5$ V, $-V_S = 0$ V, $V_{REF} = 2.5$ V, $T_A = 25°C$, $R_L = 10$ kΩ to ground, unless otherwise noted.

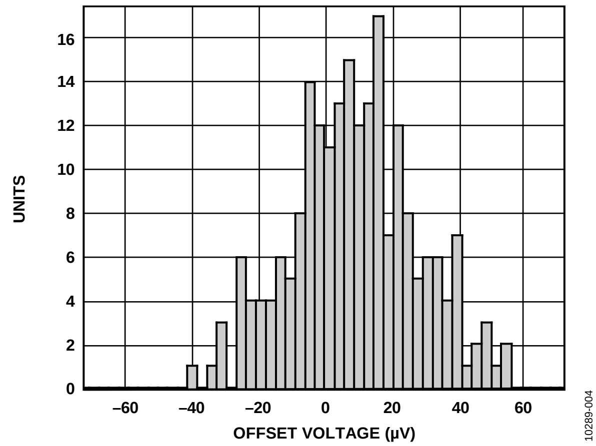


Figure 4. Typical Distribution of Offset Voltage

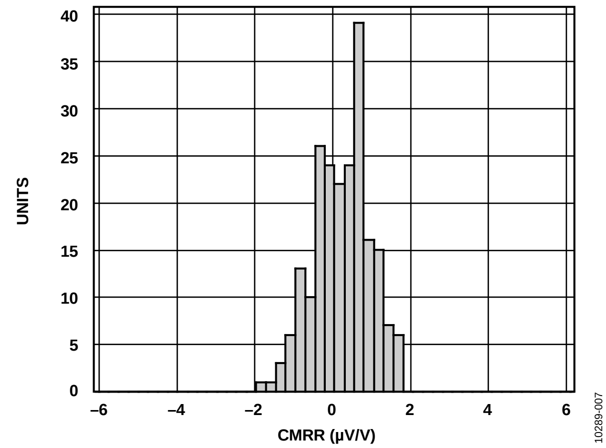


Figure 7. Typical Distribution of CMRR

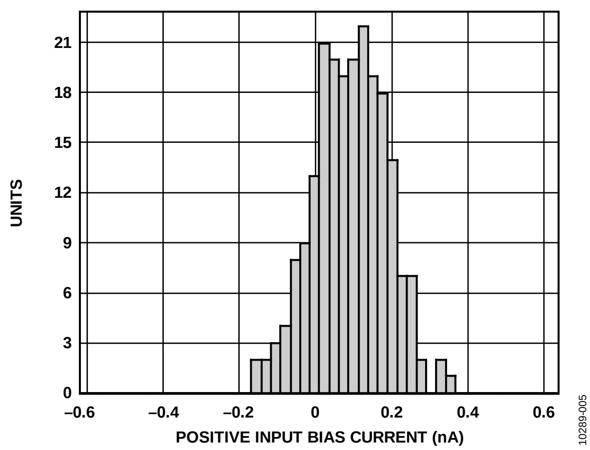


Figure 5. Typical Distribution of Input Bias Current

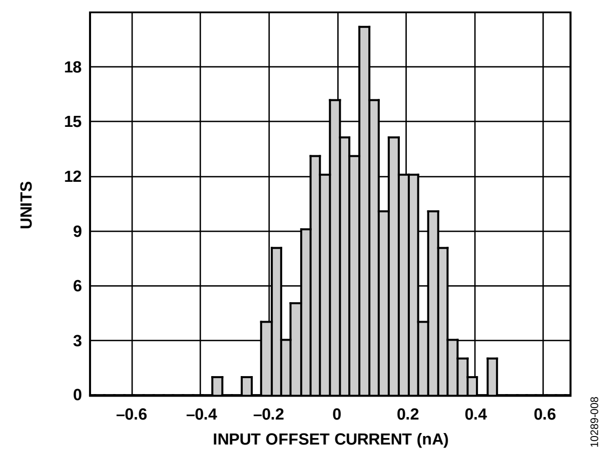


Figure 8. Typical Distribution of Input Offset Current

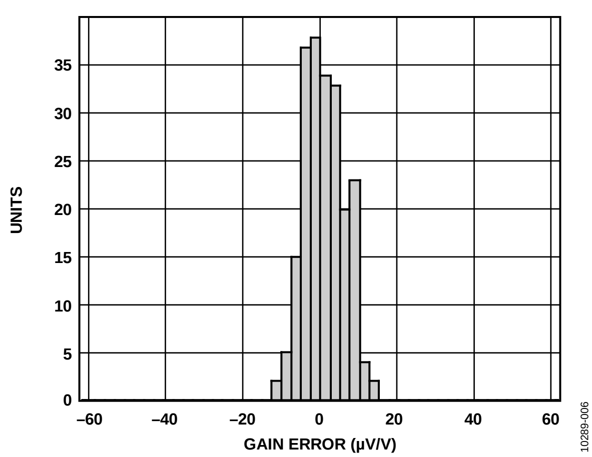


Figure 6. Typical Distribution of Gain Error (G = 1)

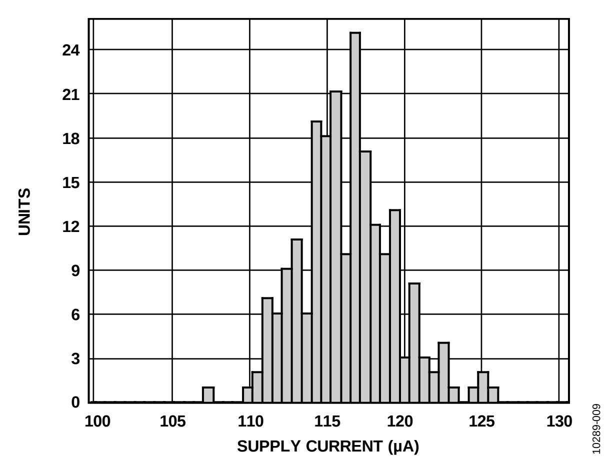


Figure 9. Typical Distribution of Supply Current

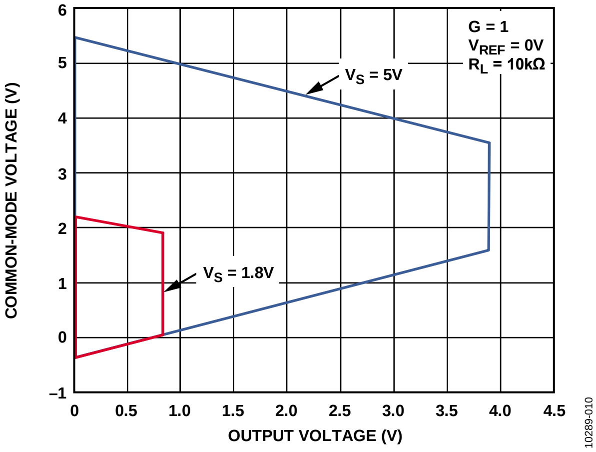


Figure 10. Input Common-Mode Voltage vs. Output Voltage, G = 1, V_{REF} = 0 V, V_S = 5 V and V_S = 1.8 V, R_L = 10 kΩ to Ground

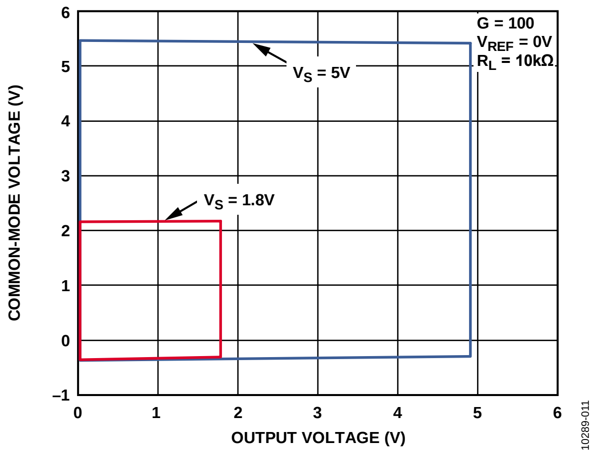


Figure 11. Input Common-Mode Voltage vs. Output Voltage, G = 100, V_{REF} = 0 V, V_S = 5 V and V_S = 1.8 V, R_L = 10 kΩ to Ground

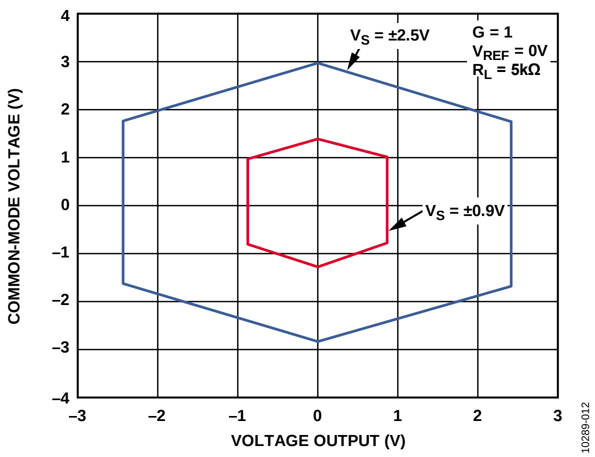


Figure 12. Input Common-Mode Voltage vs. Output Voltage, G = 1, V_{REF} = 0 V, V_S = ±2.5 V and V_S = ±0.9 V, R_L = 5 kΩ to Ground

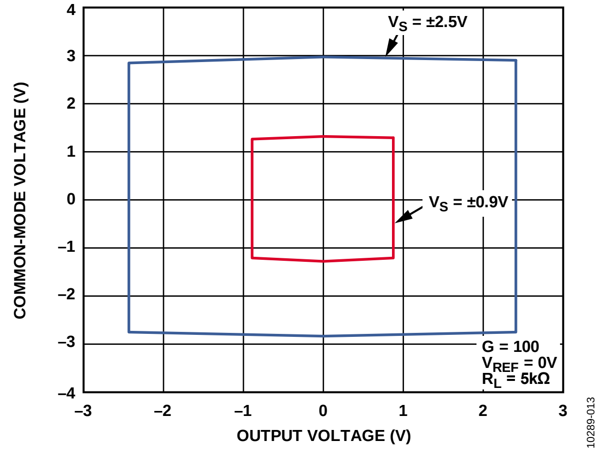


Figure 13. Input Common-Mode Voltage vs. Output Voltage, G = 100, V_{REF} = 0 V, V_S = ±2.5 V and V_S = ±0.9 V, R_L = 5 kΩ to Ground

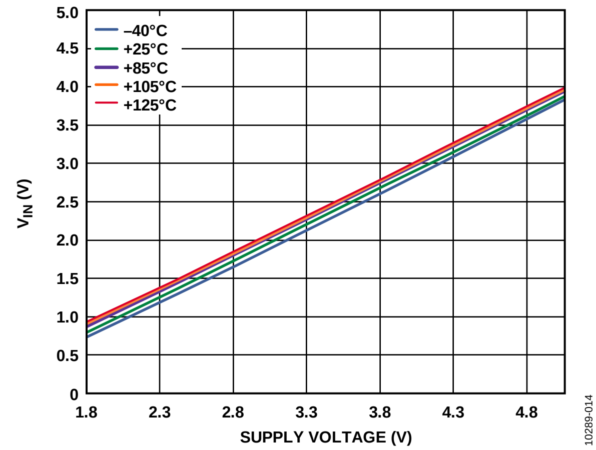


Figure 14. Maximum Differential Input vs. Supply Voltage

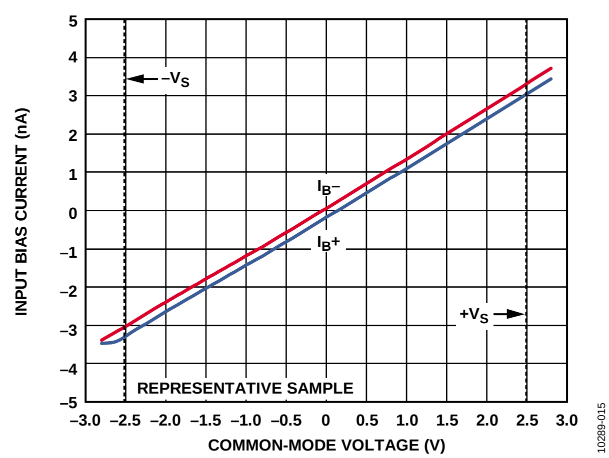


Figure 15. Input Bias Current vs. Common-Mode Voltage

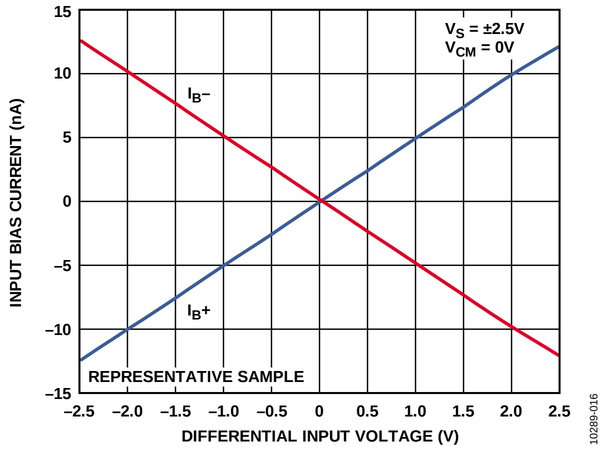


Figure 16. Input Bias Current vs. Differential Input Voltage

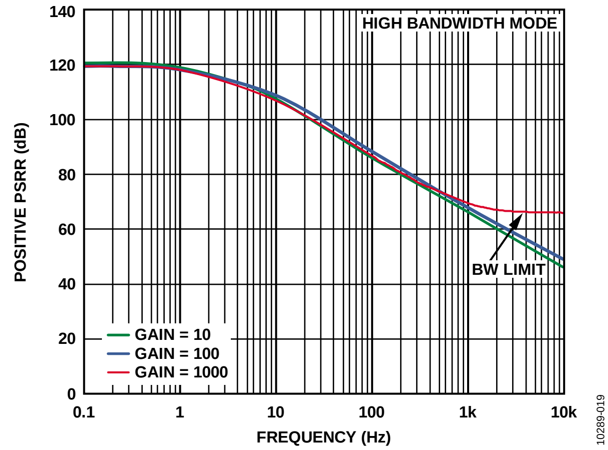


Figure 19. Positive PSRR vs. Frequency, RTI, High Bandwidth Mode

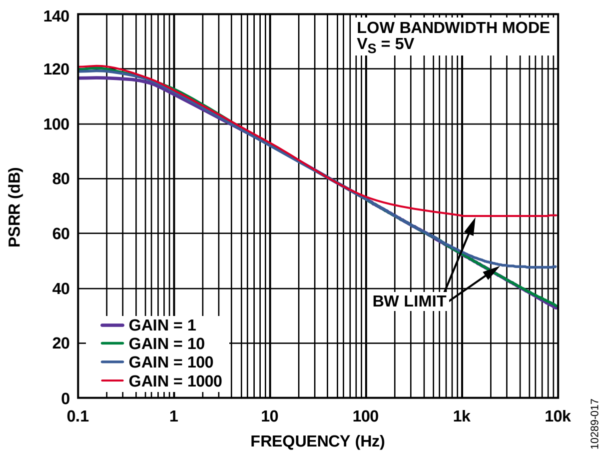


Figure 17. Positive PSRR vs. Frequency, RTI, Low Bandwidth Mode, $V_S = 5$ V

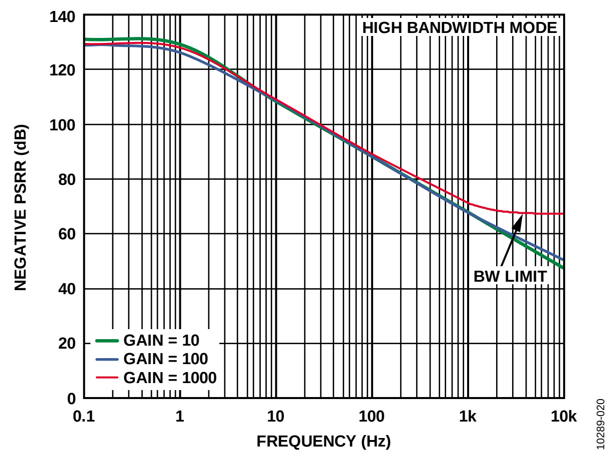


Figure 20. Negative PSRR vs. Frequency, RTI, High Bandwidth Mode

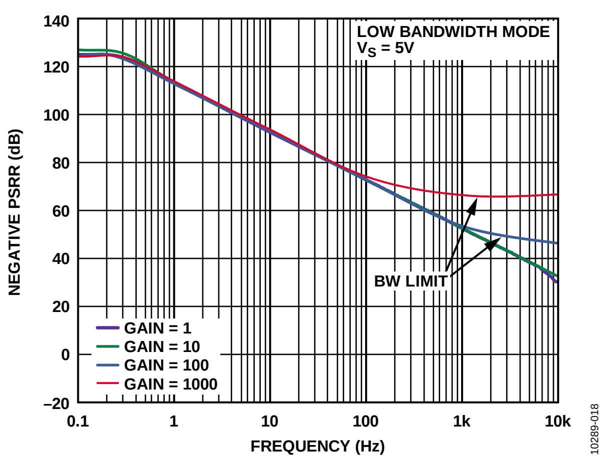


Figure 18. Negative PSRR vs. Frequency, RTI, Low Bandwidth Mode, $V_S = 5$ V

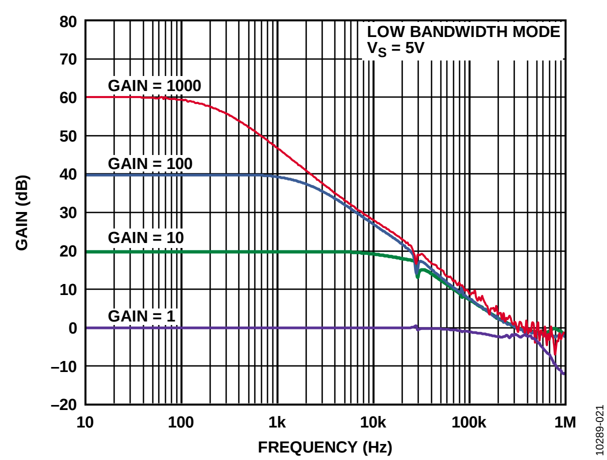


Figure 21. Gain vs. Frequency, Low Bandwidth Mode, $V_S = 5$ V

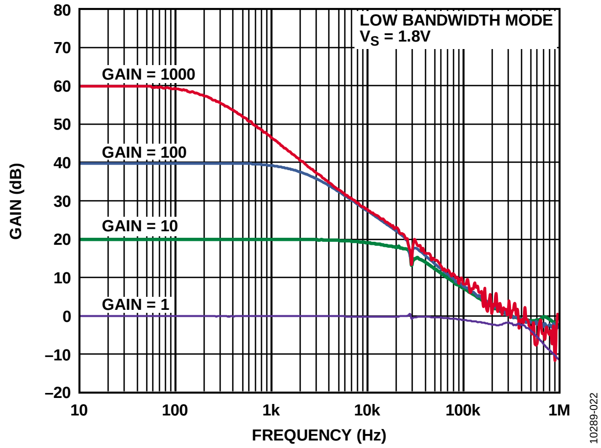


Figure 22. Gain vs. Frequency, Low Bandwidth Mode, V_S = 1.8 V

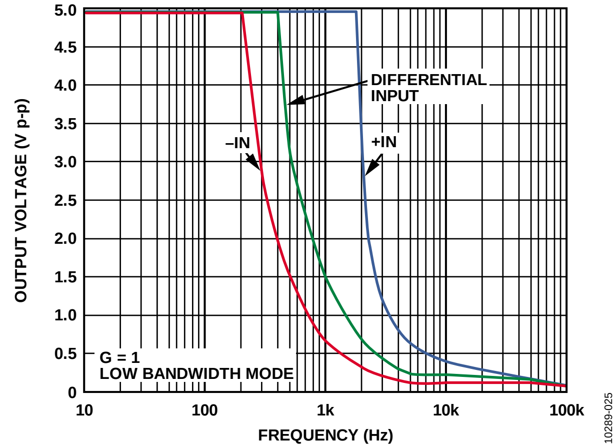


Figure 25. Large Signal Frequency Response, Low Bandwidth Mode, G = 1

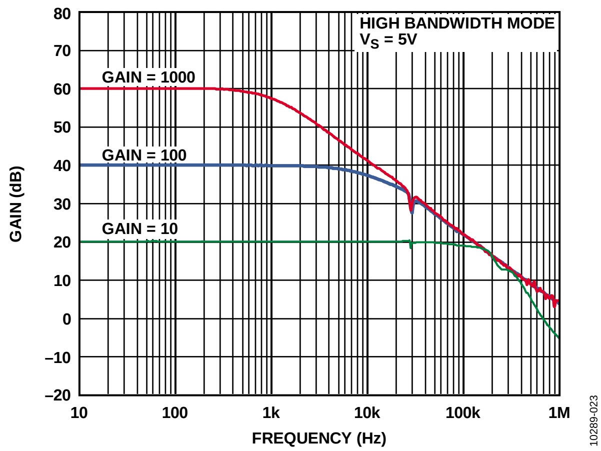


Figure 23. Gain vs. Frequency, High Bandwidth Mode, V_S = 5 V

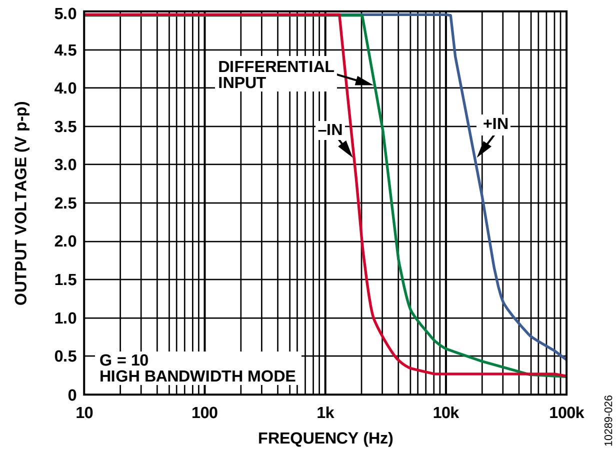


Figure 26. Large Signal Frequency Response, High Bandwidth Mode, G = 10

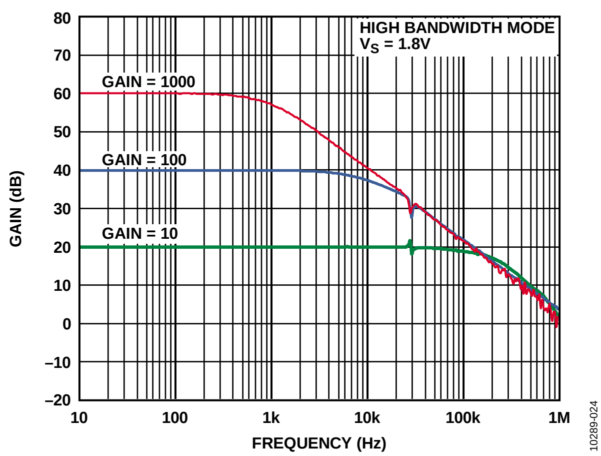


Figure 24. Gain vs. Frequency, High Bandwidth Mode, V_S = 1.8 V

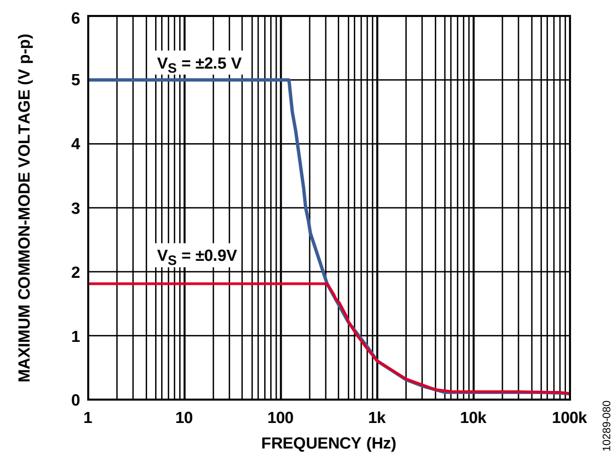


Figure 27. Maximum Common-Mode Voltage vs. Frequency

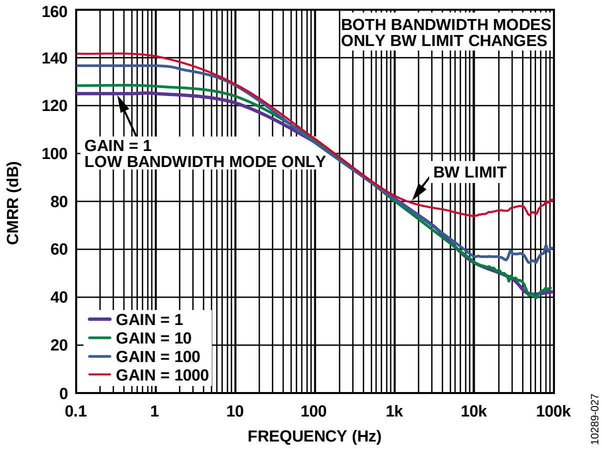


Figure 28. CMRR vs. Frequency

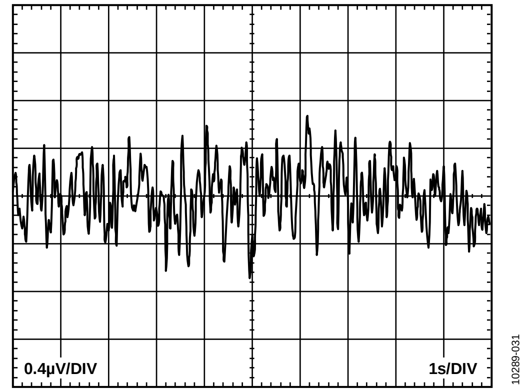


Figure 31. 0.1 Hz to 10 Hz RTI Voltage Noise

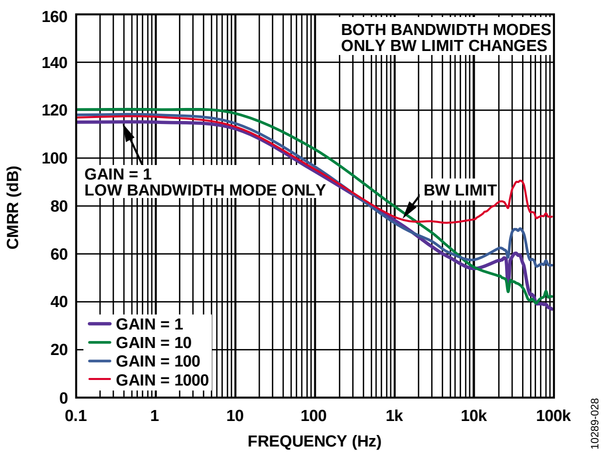


Figure 29. CMRR vs. Frequency, 1 kΩ Source Imbalance

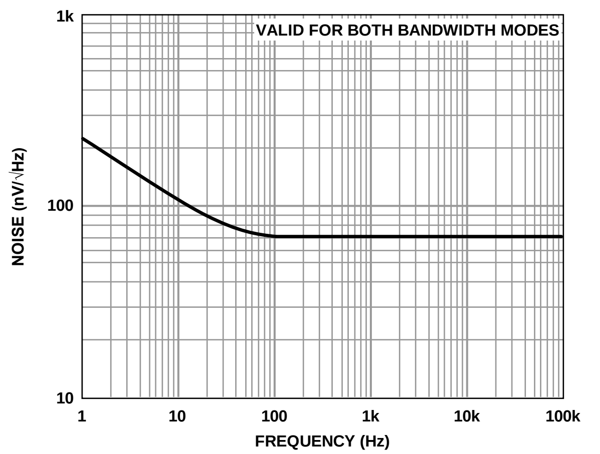


Figure 32. Current Noise Spectral Density vs. Frequency

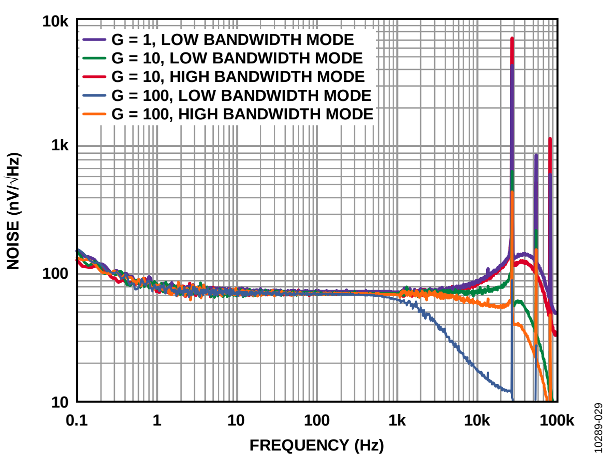


Figure 30. Voltage Noise Spectral Density vs. Frequency

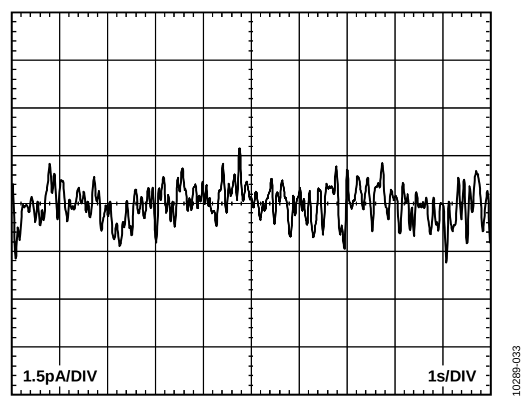


Figure 33. 0.1 Hz to 10 Hz RTI Current Noise

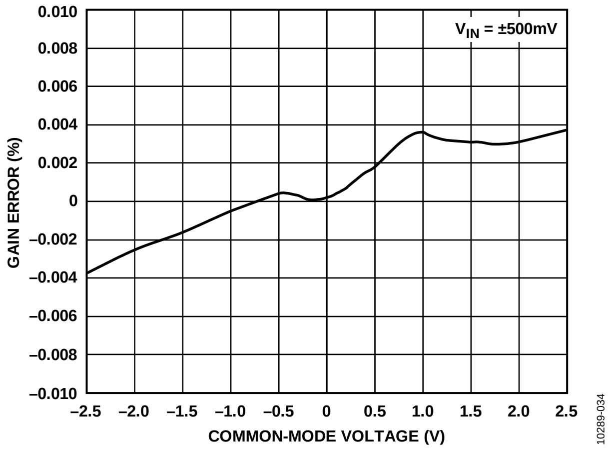


Figure 34. Gain Error vs. Common-Mode Voltage, G = 1

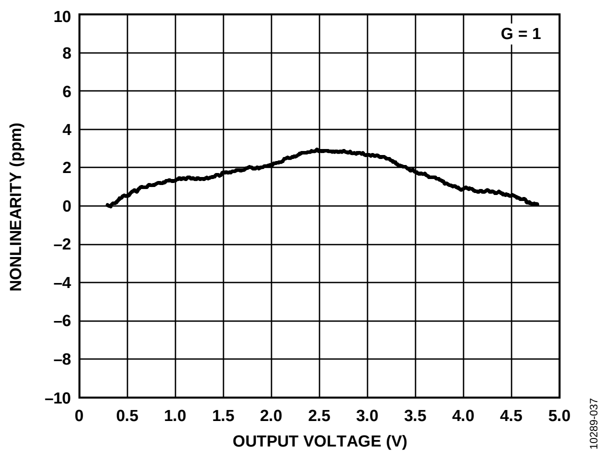


Figure 35. Gain Nonlinearity, G = 1, V_S = 5 V, R_L = 10 kΩ to Ground, Low Bandwidth Mode

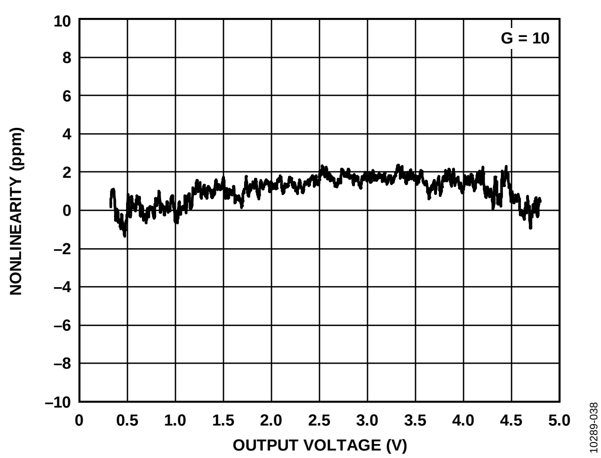


Figure 36. Gain Nonlinearity, G = 10, V_S = 5 V, R_L = 10 kΩ to Ground

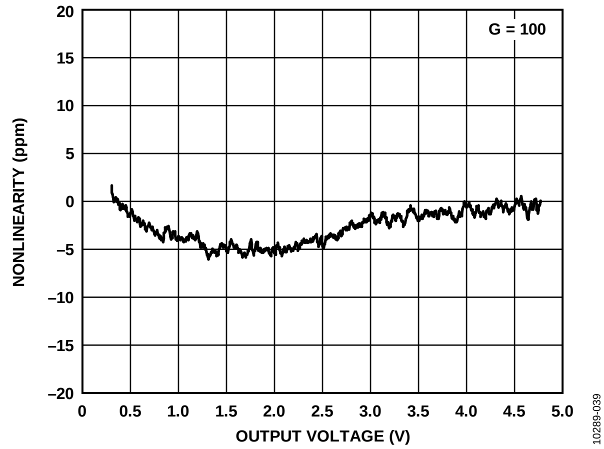


Figure 37. Gain Nonlinearity, G = 100, V_S = 5 V, R_L = 10 kΩ to Ground

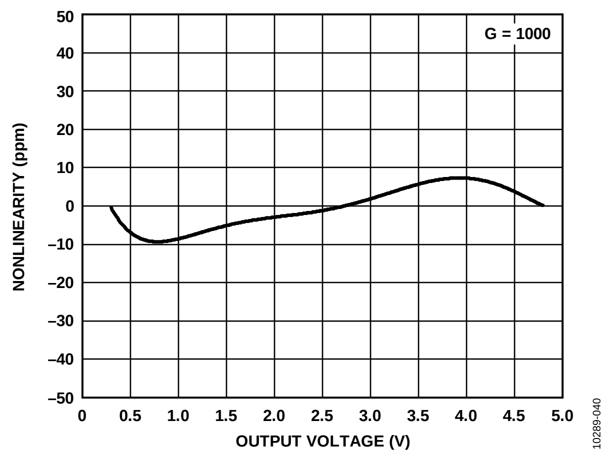


Figure 38. Gain Nonlinearity, G = 1000, V_S = 5 V, R_L = 10 kΩ to Ground

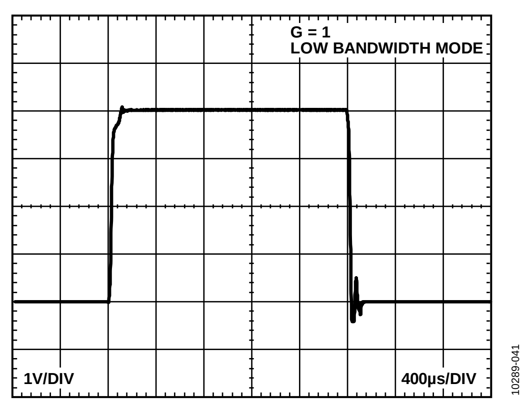


Figure 39. Large Signal Pulse Response, Low Bandwidth Mode, G = 1, R_L = 10 kΩ, C_L = 10 pF

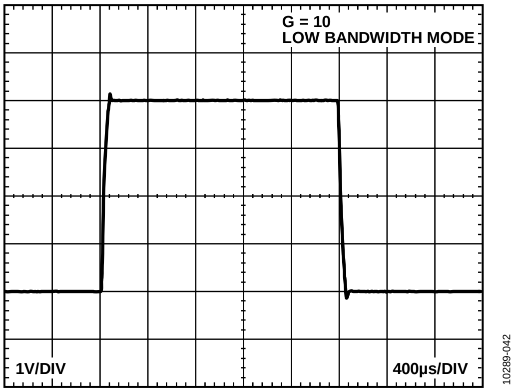


Figure 40. Large Signal Pulse Response, Low Bandwidth Mode, G = 10, R_L = 10 kΩ, C_L = 10 pF

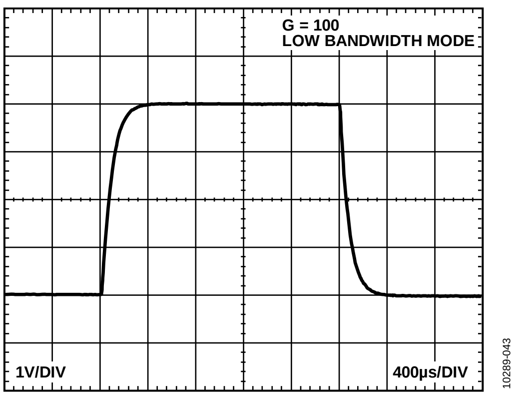


Figure 41. Large Signal Pulse Response, Low Bandwidth Mode, G = 100, R_L = 10 kΩ, C_L = 10 pF

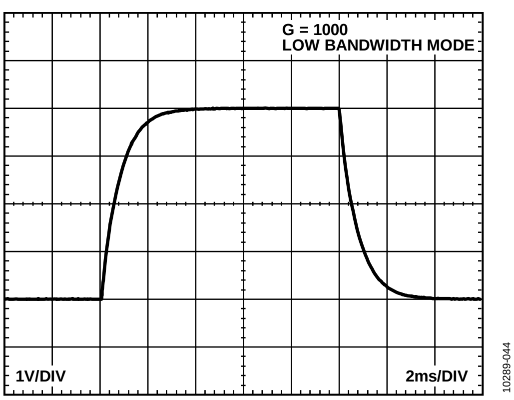


Figure 42. Large Signal Pulse Response, Low Bandwidth Mode, G = 1000, R_L = 10 kΩ, C_L = 10 pF

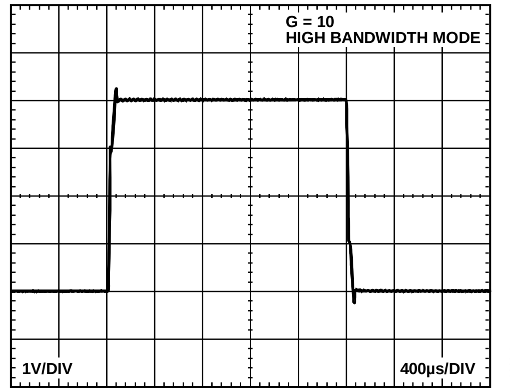


Figure 43. Large Signal Pulse Response, High Bandwidth Mode, G = 10, R_L = 10 kΩ, C_L = 10 pF

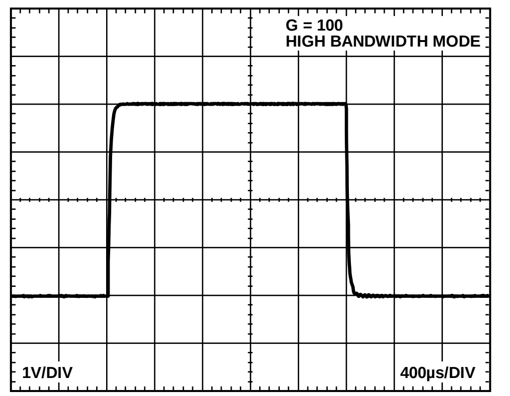


Figure 44. Large Signal Pulse Response, High Bandwidth Mode, G = 100, R_L = 10 kΩ, C_L = 10 pF

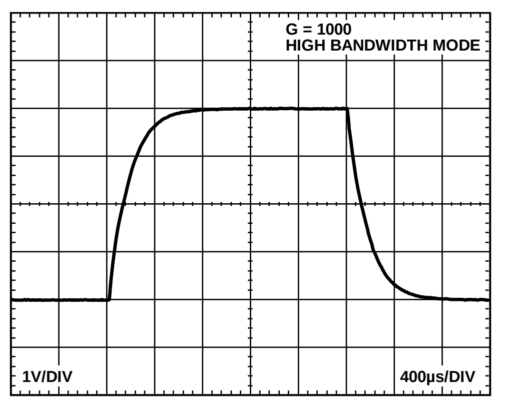


Figure 45. Large Signal Pulse Response, High Bandwidth Mode, G = 1000, R_L = 10 kΩ, C_L = 10 pF

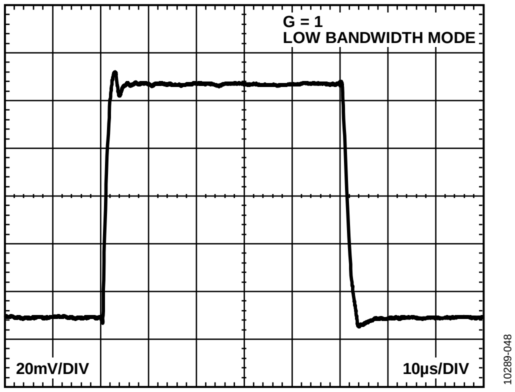


Figure 46. Small Signal Pulse Response, G = 1, R_L = 10 kΩ, C_L = 100 pF, Low Bandwidth Mode

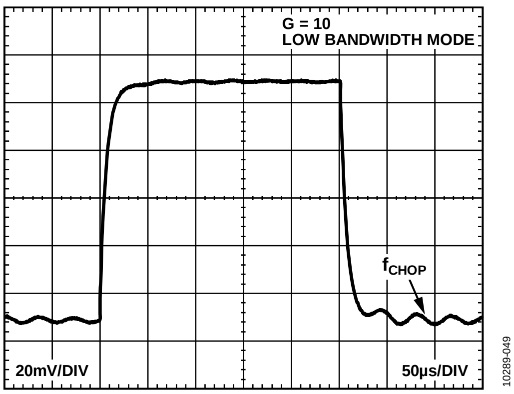


Figure 47. Small Signal Pulse Response, G = 10, R_L = 10 kΩ, C_L = 100 pF, Low Bandwidth Mode

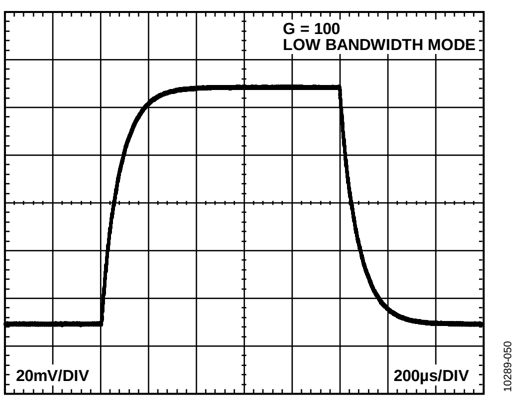


Figure 48. Small Signal Pulse Response, G = 100, R_L = 10 kΩ, C_L = 100 pF, Low Bandwidth Mode

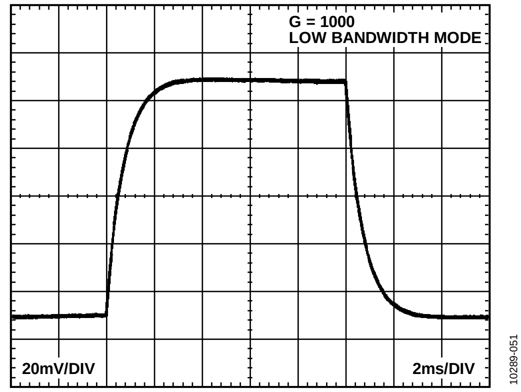


Figure 49. Small Signal Pulse Response, G = 1000, R_L = 10 kΩ, C_L = 100 pF, Low Bandwidth Mode

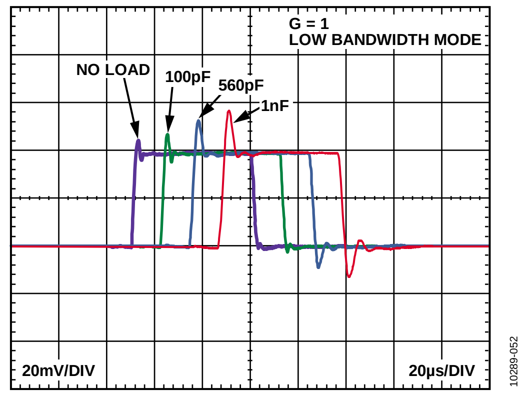


Figure 50. Small Signal Pulse Response with Various Capacitive Loads, G = 1, R_L = Infinity, Low Bandwidth Mode

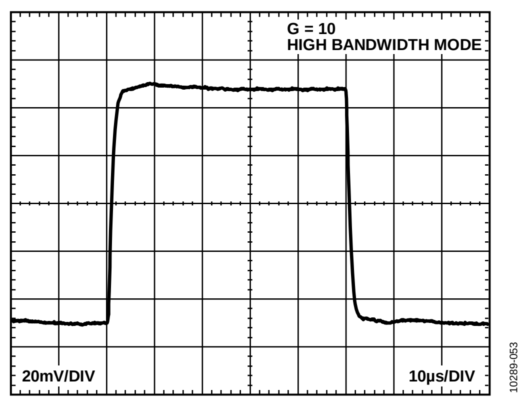


Figure 51. Small Signal Pulse Response, G = 10, R_L = 10 kΩ, C_L = 100 pF, High Bandwidth Mode

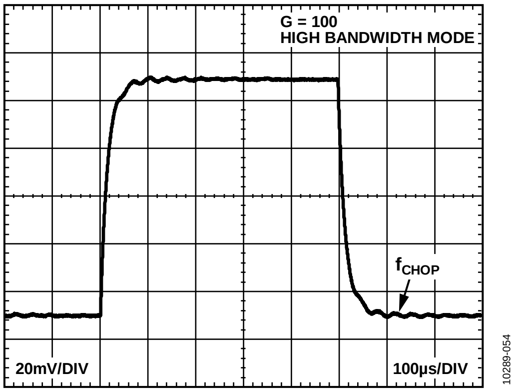


Figure 52. Small Signal Pulse Response, G = 100, R_L = 10 kΩ, C_L = 100 pF, High Bandwidth Mode

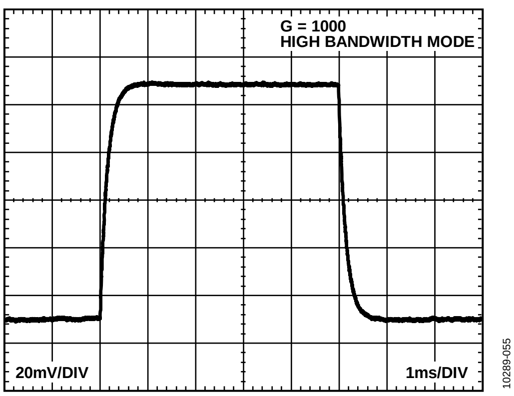


Figure 53. Small Signal Pulse Response, G = 1000, R_L = 10 kΩ, C_L = 100 pF, High Bandwidth Mode

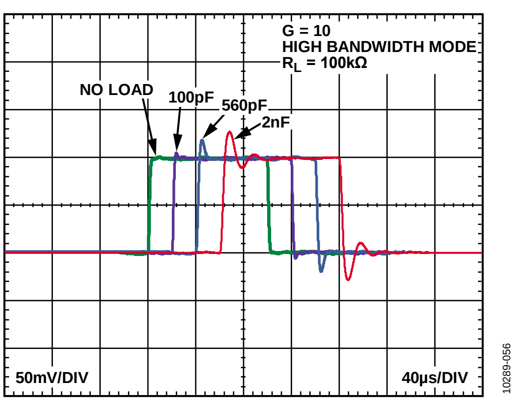


Figure 54. Small Signal Pulse Response with Various Capacitive Loads, G = 10, R_L = 100 kΩ, High Bandwidth Mode

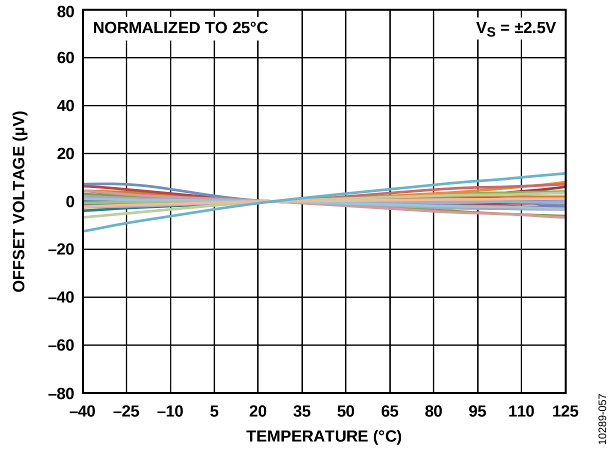


Figure 55. Offset Voltage vs. Temperature

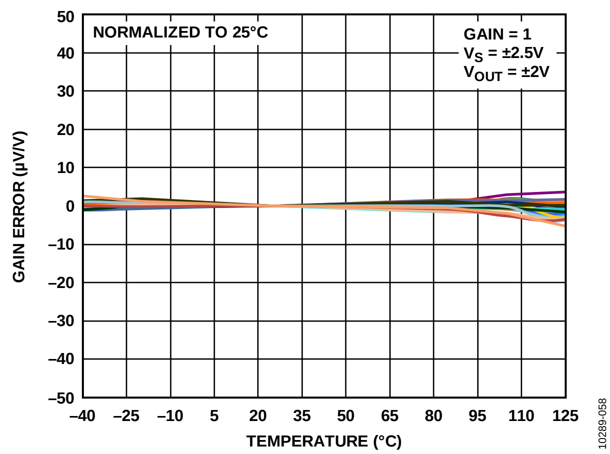


Figure 56. Gain vs. Temperature

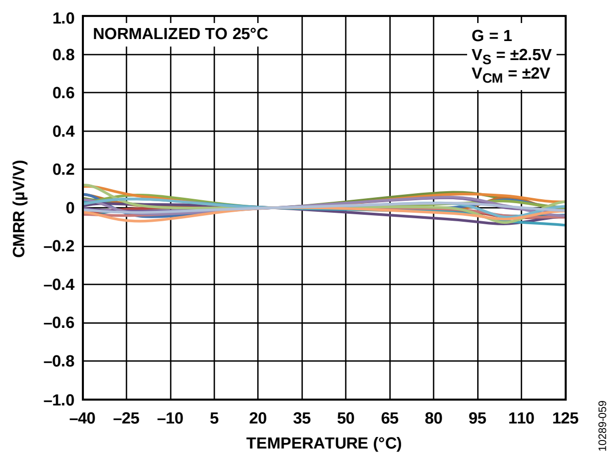


Figure 57. CMRR vs. Temperature

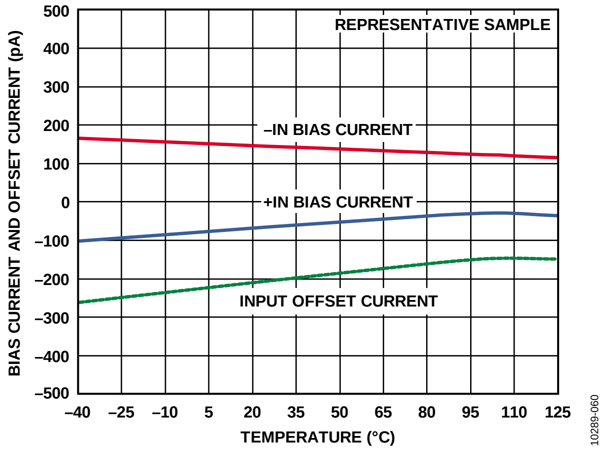


Figure 58. Input Bias Current and Input Offset Current vs. Temperature

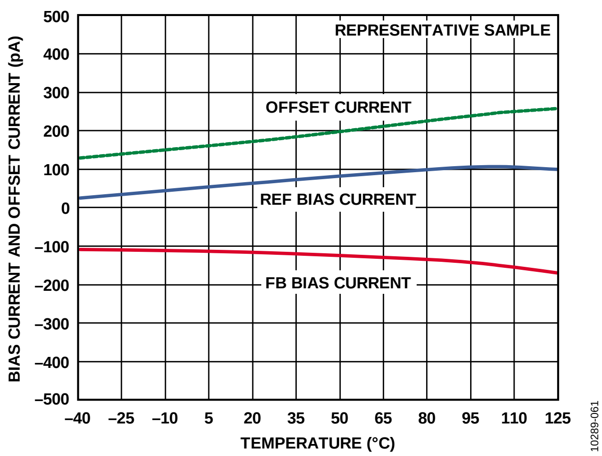


Figure 59. REF Input Bias Current, FB Input Bias Current, and Offset Current vs. Temperature

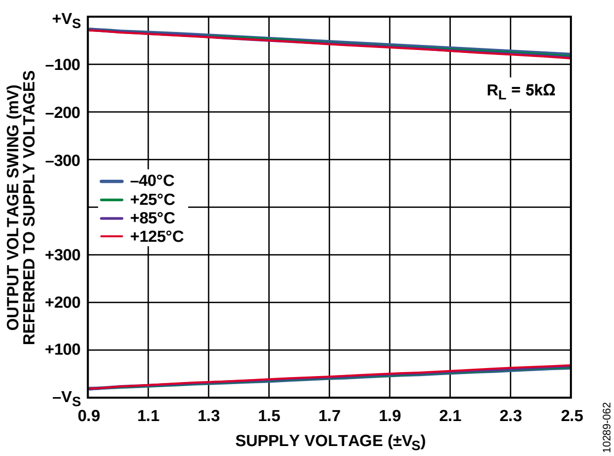


Figure 60. Output Voltage Swing vs. Supply Voltage

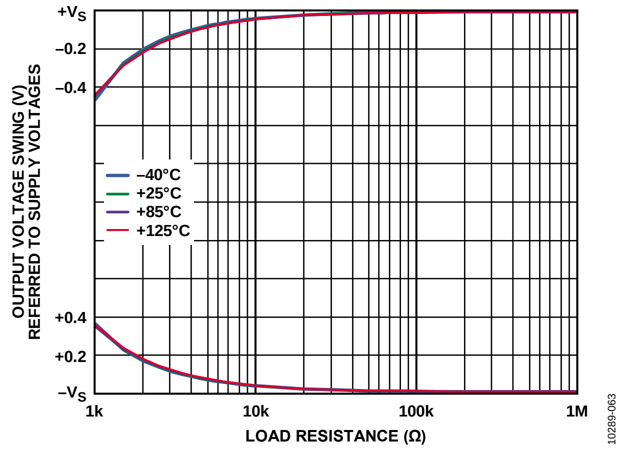


Figure 61. Output Voltage Swing vs. Load Resistance, V_S = ±2.5 V

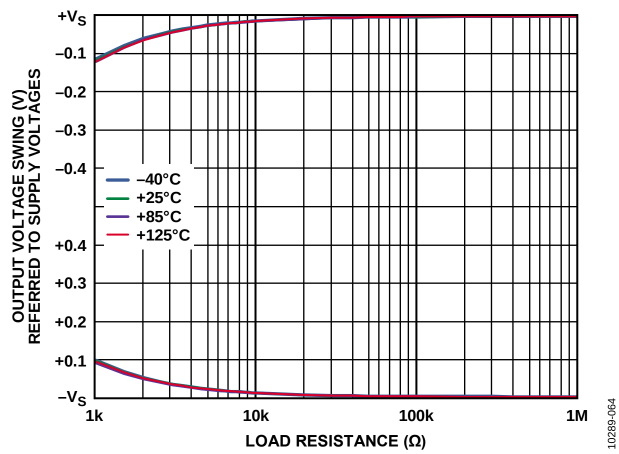


Figure 62. Output Voltage Swing vs. Load Resistance, V_S = ±0.9 V

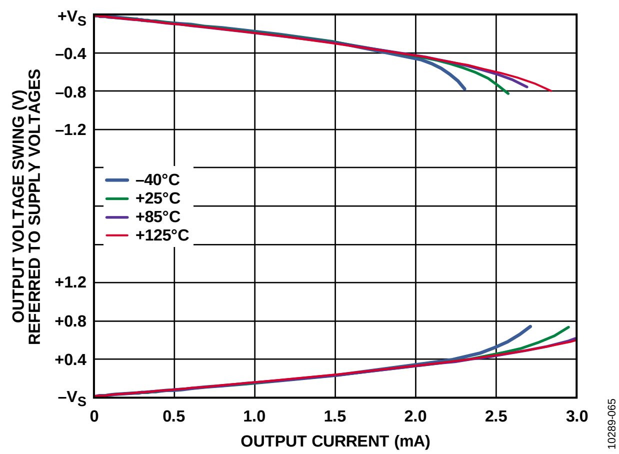


Figure 63. Output Voltage Swing vs. Output Current

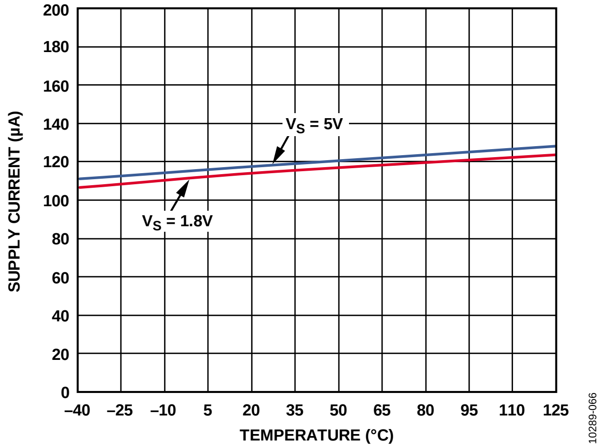


Figure 64. Supply Current vs. Temperature, V_S = 5 V, V_S = 1.8 V

THEORY OF OPERATION

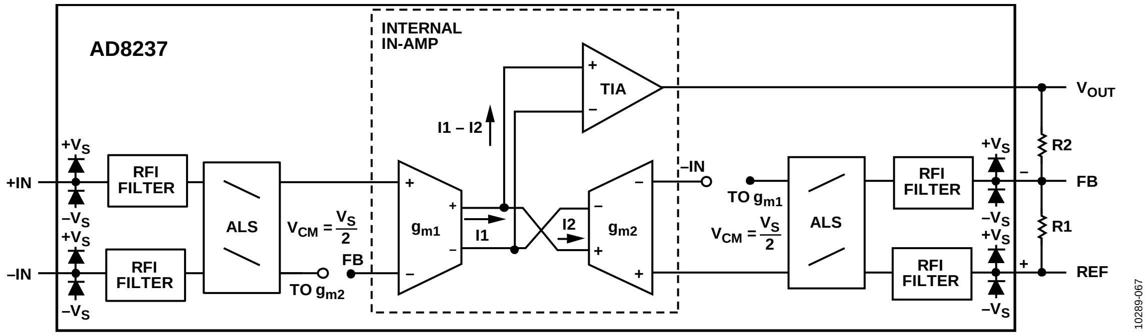


Figure 65. Simplified Schematic

ARCHITECTURE

The AD8237 is based on an indirect current feedback topology consisting of three amplifiers: two matched transconductance amplifiers that convert voltage to current, and one transimpedance amplifier, TIA, that converts current to voltage.

To understand how the AD8237 works, first consider only the internal in-amp. Assume a positive differential voltage is applied across the inputs of the transconductance amplifier, g_{m1}. This input voltage is converted into a differential current, I1, by the g_m. Initially, I2 is zero; therefore, I1 is fed into the TIA, causing the output to increase. If there is feedback from the output of the TIA to the negative terminal of g_{m2}, and the positive terminal is held constant, the increasing output of the TIA causes I2, as shown, to increase. When it is assumed that the TIA has infinite gain, the loop is satisfied when I2 equals I1. Because the gain of g_{m1} and g_{m2} are matched, this means that the differential input voltage across g_m1 appears across the inputs of g_{m2}. This behavioral model is all that is needed for proper operation of the AD8237, and the rest of the circuit is for performance optimization.

The AD8237 employs a novel adaptive level shift (ALS) technique. This switched capacitor method shifts the common-mode level of the input signal to the optimal level for the in-amp while preserving the differential signal. Once this is accomplished, additional performance benefits can be achieved by using the internal in-amp to compare +IN to FB and −IN to REF. This is only practical because the signals emitting from the ALS blocks are all referred to the same common-mode potential.

In traditional instrumentation amplifiers, the input common-mode voltage can limit the available output swing, typically depicted in a hexagon plot of the input common-mode vs. the output voltage. Because of this limit, very few instrumentation amplifiers can measure small signals near either supply rail. Using the indirect current feedback topology and ALS, the AD8237 achieves a truly rail-to-rail characteristic. This increases power efficiency in many applications by allowing for power supply reduction.

The AD8237 includes an RFI filter to remove high frequency out-of-band signals without affecting input impedance and CMRR over frequency. Additionally, there is a bandwidth mode pin to adjust the compensation. For gains greater than or equal to 10, the bandwidth mode pin (BW) can be tied to $+V_S$ to change the compensation and increase the gain bandwidth product of the amplifier to 1 MHz. Otherwise, connect BW to $-V_S$ for a 200 kHz gain bandwidth product.

SETTING THE GAIN

There are several ways to configure the AD8237. The transfer function of the AD8237 in the configuration in Figure 65 is

$$V_{OUT} = G(V_{+IN} - V_{-IN}) + V_{REF}$$

where:

$$G = 1 + \frac{R2}{R1}$$

Table 7. Suggested Resistors for Various Gains (1% Resistors)

R1 (kΩ)	R2 (kΩ)	Gain
None	Short	1.00
49.9	49.9	2.00
20	80.6	5.03
10	90.9	10.09
5	95.3	20.06
2	97.6	49.8
1	100	101
1	200	201
1	499	500
1	1000	1001

Whereas the ratio of R2 to R1 sets the gain, the designer determines the absolute value of the resistors. Larger values reduce power consumption and output loading; smaller values limit the FB input bias current and input impedance errors. If the parallel combination of R1 and R2 is greater than about 30 kΩ, the resistors start to contribute to the noise. For best output swing and linearity, keep $(R1 + R2) \| R_L \geq 10$ kΩ.

The bias current at the FB pin is dependent on the common-mode and differential input impedance. FB bias current errors from the common-mode input impedance can be reduced by placing a resistor value of R1||R2 in series with the REF terminal, as shown in Figure 66. At higher gains, this resistor can simply be the same value as R1.

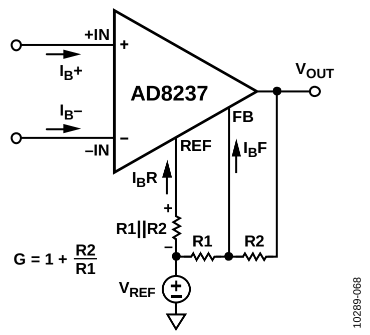


Figure 66. Cancelling Error from FB Input Bias Current

Some applications may be able to take advantage of the symmetry of the input transconductance amplifiers by canceling the differential input impedance errors, as shown in Figure 67. If the source resistance is well known, setting the parallel combination of R1 and R2 equal to R_S accomplishes this. If practical resistor values force the parallel combination of R1 and R2 to be less than R_S, add a series resistor to the FB input to make up for the difference.

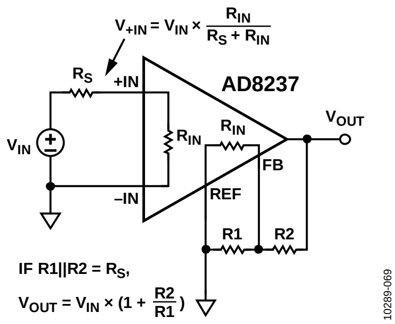


Figure 67. Canceling Input Impedance Errors

GAIN ACCURACY

Unlike most instrumentation amplifiers, the relative match of the two gain setting resistors determines the gain accuracy of the AD8237 rather than a single external resistor. For example, if two resistors have exactly the same absolute error, there is no error in gain. Conversely, two 1% resistors can cause approximately 2% maximum gain error at high gains. Temperature coefficient mismatch of the gain setting resistors increases the gain drift of the instrumentation amplifier circuit according to the gain equation. Because these external resistors do not have to match any on-chip resistors, resistors with good TCR tracking can achieve excellent gain drift without the need for a low absolute TCR.

For the best performance, keep the two input pairs (+IN and −IN, and FB and REF) at similar dc and ac common-mode potentials. This has two benefits. For dc common-mode, this minimizes the gain error of the AD8237. For ac common-mode, this yields improved frequency response. There is a maximum rate at which the ALS circuit can shift the common-mode voltage, which is shown in Figure 27. Because of this limit, the best large signal frequency response is achieved when the ac common-mode voltage of the two input pairs are matched. For example, if the negative input is at a fixed voltage and the positive input is driven with a signal, the feedback input moves with the positive input; therefore, the ac common-mode voltage of the two input pairs is the same. The effect of this is shown in Figure 25 and Figure 26.

CLOCK FEEDTHROUGH

The AD8237 uses nonoverlapping clocks to perform the chopping and ALS functions. The input voltage-to-current amplifiers are chopped at approximately 27 kHz.

Although there is internal ripple-suppression circuitry, trace amounts of these clock frequencies and their harmonics can be observed at the output in some configurations. These ripples are typically 100 μV RTI when the bandwidth is greater than the clock frequency. They can be larger after a transient pulse but settle back to nominal, which is included in the settling time specifications. The amount of feedthrough at the output is dependent upon the gain and bandwidth mode. The worst case is in high bandwidth mode when the gain can be almost 40 before the clock ripple is outside the bandwidth of the amplifier. For some applications, it may be necessary to use additional filtering after the AD8237 to remove this ripple.

INPUT VOLTAGE RANGE

The allowable input range of the AD8237 is much simpler than traditional architectures. For the transfer function of the AD8237 to be valid, the input voltage must follow two rules

- Keep the differential input voltage within the limits shown in Figure 14; approximately ±(Total Supply Voltage – 1.2) V.
- Keep the voltage of the inputs (including the REF and FB pins) and the output within the specified voltage range, which are approximately the supply rails.

Because the output swing is completely independent of the input common-mode voltage, there are no hexagonal figures or complicated formulas to follow, and no limitation for the output swing the amplifier has for input signals with changing common mode.

INPUT PROTECTION

If no external protection is used, keep the inputs of the AD8237 within the voltages specified in the absolute maximum ratings. If the application requires voltages beyond these ratings, input protection resistors can be placed in series with the inputs of the AD8237 to limit the current to 5 mA. For example, if $+V_S$ is 3 V and a 10 V overload voltage can occur at the inputs, place a protection resistor of at least (10 V − 3 V)/5 mA = 1.4 kΩ in series with the inputs.

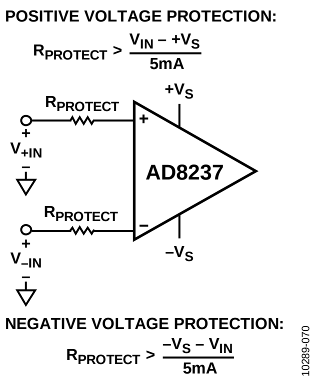


Figure 68. Protection Resistors for Large Input Voltages

FILTERING RADIO FREQUENCY INTERFERENCE

The AD8237 contains an on-chip RFI filter that is sufficient for a majority of applications. For applications where additional radio frequency immunity is needed, an external RFI filter can also be applied as shown in Figure 69.

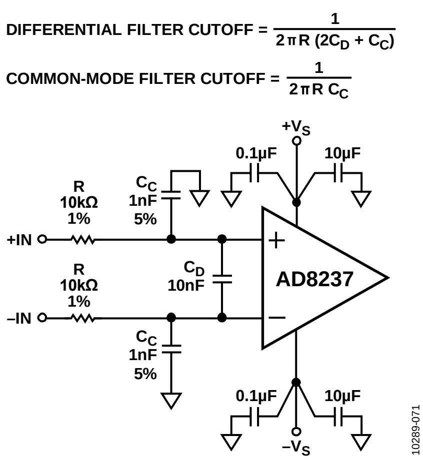


Figure 69. Adding Extra RFI Filtering

USING THE REFERENCE PIN

In general, instrumentation amplifier reference pins can be useful for a few reasons. They provide a means of physically separating the input and output grounds to reject ground bounce common to the inputs. They can also be used to precisely level shift the output signal. In the configuration shown in Figure 65 through Figure 67, the gain of the reference pin to the output is unity, as is common in a typical in-amp. Because the reference pin is functionally no different from the positive input, it can be used with gain, as shown in Figure 70.

This configuration can be very useful in certain cases, such as dc removal servo loops, which typically use an inverting integrator to drive REF and compensate for a dc offset. This requires special attention to the input range (especially at REF) and the output range. All three input voltages are referred to the one ground shown, which may need to be a low impedance midsupply.

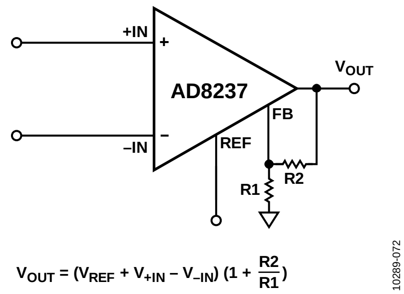


Figure 70. Applying Gain to the Reference Voltage

Traditional instrumentation amplifier architectures require the reference pin to be driven with a low impedance source. In these traditional architectures, impedance at the reference pin degrades both CMRR and gain accuracy. With the AD8237 architecture, resistance at the reference pin has no effect on CMRR.

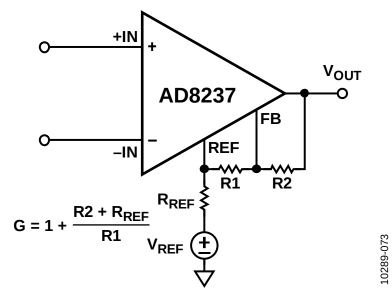


Figure 71. Calculating Gain with Reference Resistance

Resistance at the reference pin does affect the gain of the AD8237; however, if this resistance is constant, the gain setting resistors can be adjusted to compensate. For example, the AD8237 can be driven with a voltage divider, as shown in Figure 72.

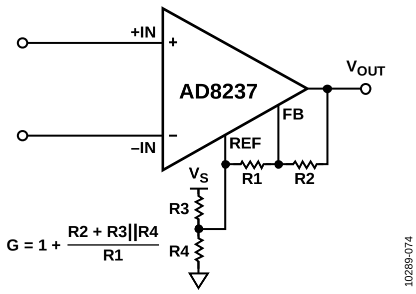


Figure 72. Using Voltage Divider to Set Reference Voltage

LAYOUT

Common-Mode Rejection Ratio over Frequency

Poor layout can cause some of the common-mode signal to be converted to a differential signal before reaching the in-amp. This conversion can occur when the path to the positive input pin has a different frequency response than the path to the negative input pin. For best CMRR vs. frequency performance, closely match the impedance of each path. Place additional source resistance in the input path (for example, for input protection) close to the in-amp inputs to minimize interaction between the resistors and the parasitic capacitance from the printed circuit board (PCB) traces.

Power Supplies

Use a stable dc voltage to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. For more information, see the PSRR performance curves in Figure 17 through Figure 20.

Place a 0.1 μF capacitor as close as possible to each supply pin. As shown in Figure 73, a 10 μF tantalum capacitor can be used farther away from the part. This capacitor, which is intended to be effective at low frequencies, can usually be shared by other precision integrated circuits. Keep the traces between these integrated circuits short to minimize interaction of the trace parasitic inductance with the shared capacitor. If a single supply is used, decoupling capacitors at $-V_S$ can be omitted.

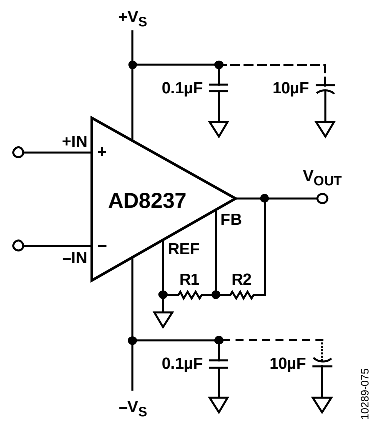


Figure 73. Supply Decoupling, REF, and Output Referred to Local Ground

Reference

The output voltage of the AD8237 is developed with respect to the potential on the reference terminal. Take care to tie REF to the appropriate local ground.

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8237 must have a return path to ground. When the source, such as a thermocouple, cannot provide a return current path, create one, as shown in Figure 74.

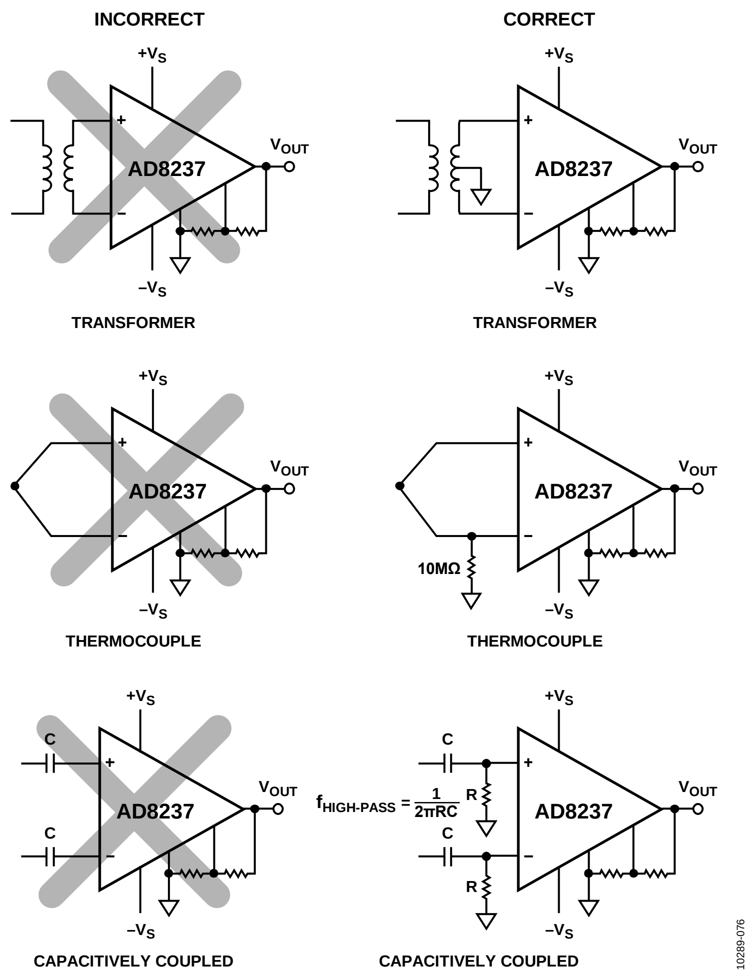


Figure 74. Creating an I_{BIAS} Path

APPLICATIONS INFORMATION

BATTERY CURRENT MONITOR

The micropower current consumption, unique topology, and rail-to-rail input of the AD8237 make it ideal for battery-powered current sensing applications. When configured as shown in Figure 75, the AD8237 is able to obtain an accurate high-side current measurement for both charging and discharging. Depending on the nature of the load, $+V_S$ may require RC decoupling. Use Kelvin sensing methods to achieve the most accurate results.

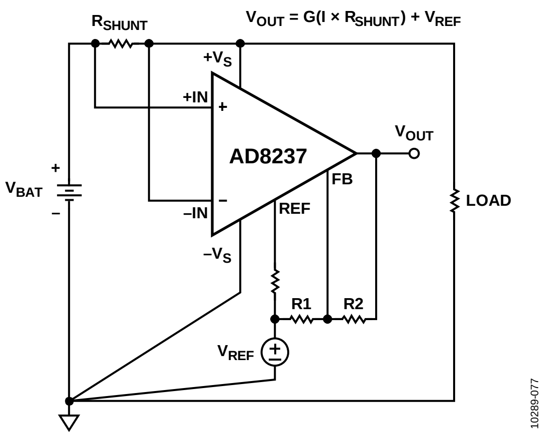


Figure 75. Battery-Powered Current Sense

PROGRAMMABLE GAIN IN-AMP

Most integrated circuit instrumentation amplifiers use a single resistor to set the gain, which is in a low impedance path. Any component placed between the gain setting pins has current flowing through it, which adds to the gain resistance. Typical CMOS switches have on resistance, R_{ON}. R_{ON} is not well controlled, is nonlinear with input voltage, and has high drift. This creates large gain errors and distortion at the output of the in-amp. This R_{ON} problem has made it difficult to build a precision programmable gain in-amp in the past. With the AD8237 topology, the switches can be placed in a high impedance sense path, eliminating the parasitic resistance effects. Figure 76 shows one way to accomplish programmable gain. Some applications may benefit from using a digital potentiometer instead of a multiplexer.

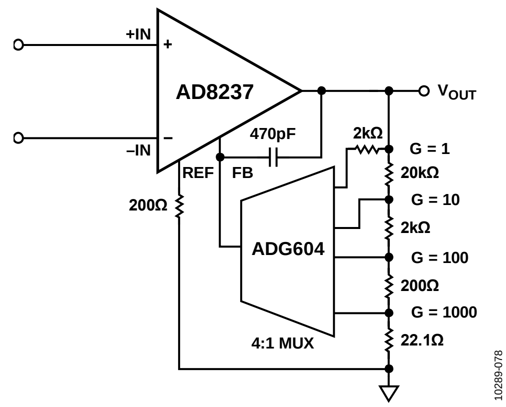


Figure 76. Programmable Gain with a Multiplexer

AD8237 IN AN ECG FRONT END

Electrocardiogram (ECG) circuits must operate with a differential dc offset due to the half-cell potential of the electrodes. The tolerance for this over potential is typically ±300 mV; however, it can be a volt or more in some situations. As ECG circuits move to lower supply voltages, the half-cell potential problem becomes more difficult, strictly limiting the gain that can be applied in the first stage. The AD8237 architecture provides a unique solution to this problem. If the REF pin is left unconnected to the gain setting network, a low frequency inverting integrator can be connected from the output to the REF pin. Because the AD8237 applies gain to the integrator output, the integrator only has to swing as far as the dc offset to compensate for it, rather than the dc offset multiplied by the gain.

With this system architecture, large gains can be applied at the in-amp stage, and the requirements of the rest of the system can be greatly reduced. This also reduces noise and offset error contributions from devices after the in-amp in the signal path. The circuit in Figure 77 illustrates the core concept. Additional op amps can be added for improved performance, such as input buffering, filtering, and driven lead, if it is required by the system. Proper decoupling is not shown.

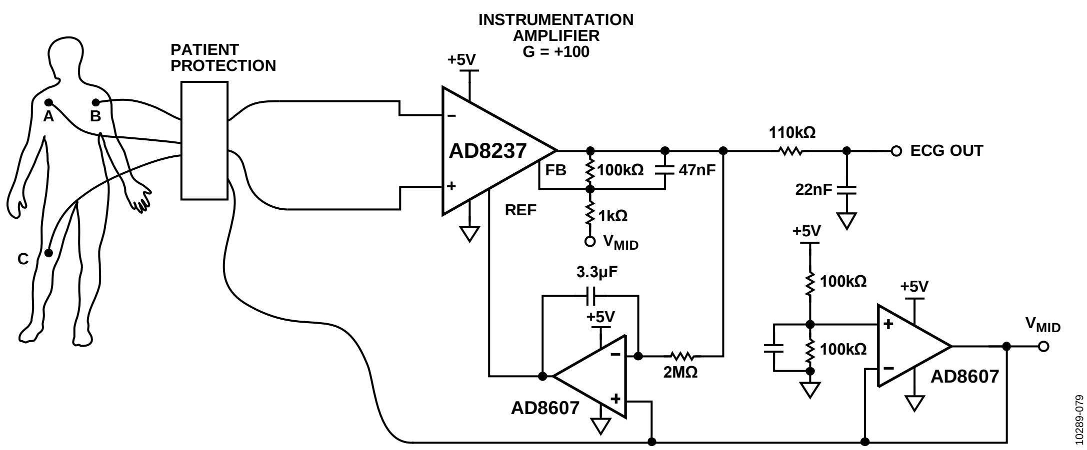


Figure 77. AD8237 in ECG

OUTLINE DIMENSIONS

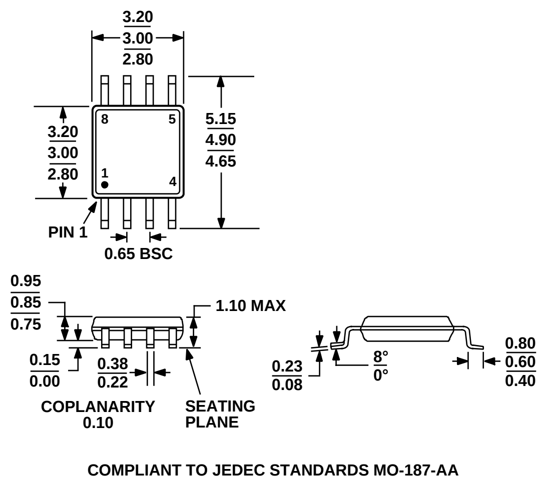


Figure 78. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package	Branding
AD8237ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP], Tube	RM-8	Y4H
AD8237ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP], 7-Inch Tape and Reel	RM-8	Y4H
AD8237ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP], 13-Inch Tape and Reel	RM-8	Y4H

[1] Z = RoHS Compliant Part.

NOTES

Anexo 2

Hojas de datos: Circuito integrado microcontrolador MCP3912

MCP3912

3V Four-Channel Analog Front End

Features:

- Four Synchronous Sampling 24-bit Resolution Delta-Sigma A/D Converters
- 93.5 dB SINAD, -107 dBc Total Harmonic Distortion (THD) (up to 35^{th} Harmonic), 112 dBFS SFDR for Each Channel
- Enables 0.1% Typical Active Power Measurement Error over a 10,000:1 Dynamic Range
- Advanced Security Features:
  - 16-Bit Cyclic Redundancy Check (CRC) Checksum on All Communications for Secure Data Transfers
  - 16-Bit CRC Checksum and Interrupt Alert for Register Map Configuration
  - Register Map lock with 8-Bit Secure Key
- 2.7V-3.6V AV_{DD}, DV_{DD}
- Programmable Data Rate up to 125 ksps:
  - 4 MHz Maximum Sampling Frequency
  - 16 MHz Maximum Master Clock
- Oversampling Ratio up to 4096
- Ultra-Low Power Shutdown Mode with < 10 µA
- -122 dB Crosstalk between Channels
- Low-Drift 1.2V Internal Voltage Reference: 9 ppm/°C
- Differential Voltage Reference Input Pins
- High Gain PGA on Each Channel (up to 32 V/V)
- Phase Delay Compensation with 1 µs Time Resolution
- Separate Data Ready Pin for Easy Synchronization
- Individual 24-Bit Digital Offset and Gain Error Correction for Each Channel
- High-Speed 20 MHz SPI Interface with Mode 0,0 and 1,1 Compatibility
- Continuous Read/Write Modes for Minimum Communication Time with Dedicated 16/32-Bit Modes
- Available in 28-Lead QFN and 28-Lead SSOP Packages
- Extended Temperature Range: -40°C to +125°C

Description:

The MCP3912 is a 3V four-channel Analog Front End (AFE) containing four synchronous sampling delta-sigma, Analog-to-Digital Converters (ADC), four PGAs, phase delay compensation block, low-drift internal voltage reference, digital offset and gain error calibration registers and high-speed 20 MHz SPI-compatible serial interface.

The MCP3912 ADCs are fully configurable, with features such as 16/24-bit resolution, Oversampling Ratio (OSR) from 32 to 4096, gain from 1x to 32x, independent Shutdown and Reset, dithering and auto-zeroing. The communication is largely simplified with 8-bit commands, including various continuous read/write modes and 16/24/32-bit data formats that can be accessed by the Direct Memory Access (DMA) of an 8/16- or 32-bit MCU, and with the separate Data Ready pin that can directly be connected to an Interrupt Request (IRQ) input of an MCU.

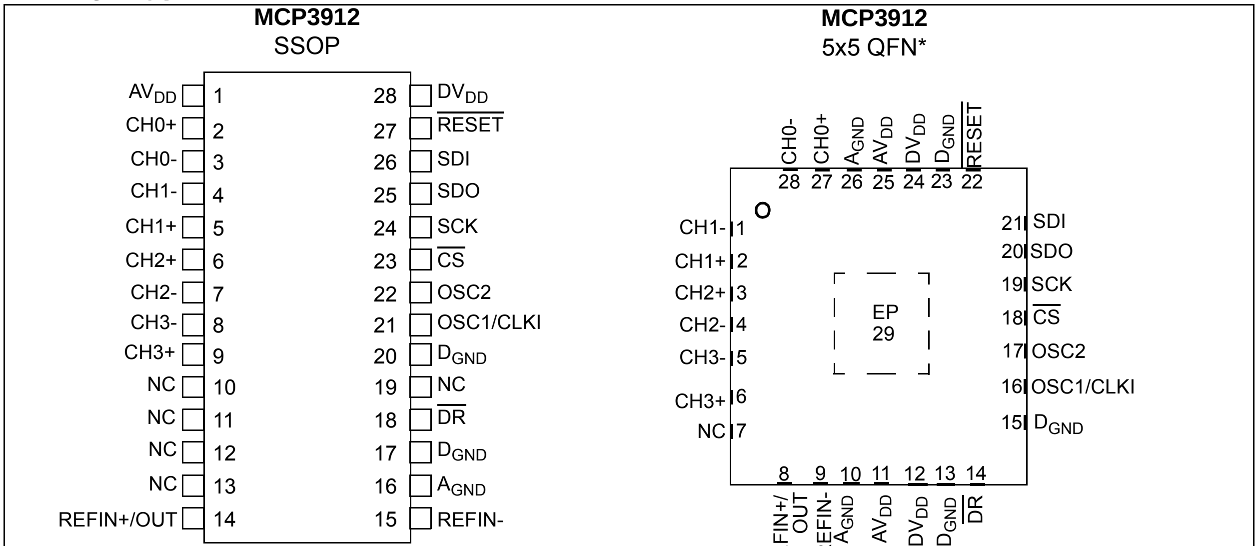
The MCP3912 includes advanced security features to secure the communications and the configuration settings, such as a CRC-16 checksum on both serial data outputs and static register map configuration. It also includes a register-map lock through an 8-bit secure key to stop unwanted write commands from processing.

The MCP3912 is capable of interfacing with a variety of voltage and current sensors, including shunts, current transformers, Rogowski coils and Hall-effect sensors.

Applications:

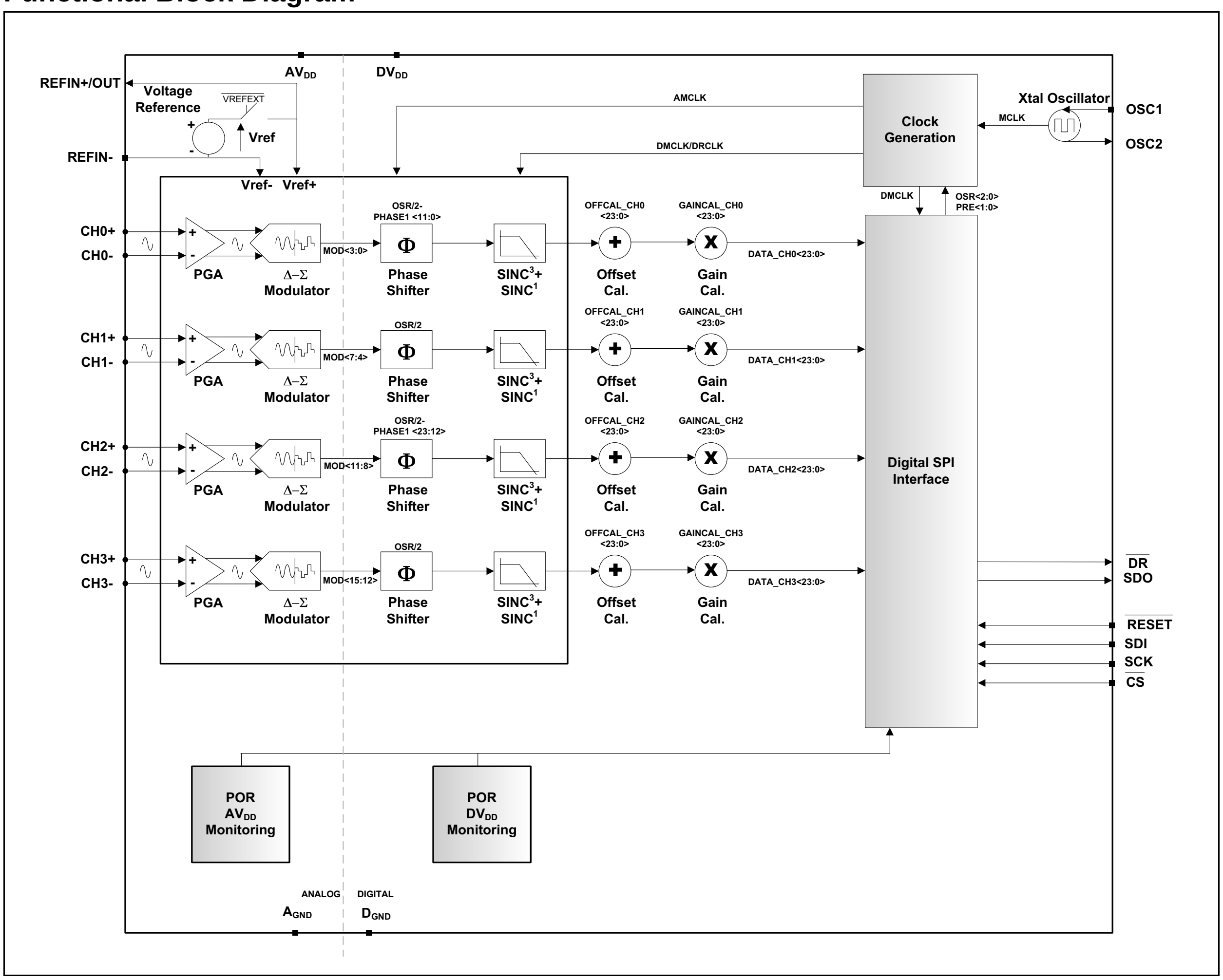
- Polyphase Energy Meters
- Energy Metering and Power Measurement
- Automotive
- Portable Instrumentation
- Medical and Power Monitoring
- Audio/Voice Recognition

Package Type



* Includes Exposed Thermal Pad (EP); see Table 1-3.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} .... -0.3V to 4.0V
Digital inputs and outputs w.r.t. A_{GND} .... -0.3V to 4.0V
Analog input w.r.t. A_{GND} .... -2V to +2V
V_{REF} input w.r.t. A_{GND} .... -0.6V to V_{DD} +0.6V
Storage temperature .... -65°C to +150°C
Ambient temp. with power applied .... -65°C to +125°C
Soldering temperature of leads (10 seconds) .... +300°C
ESD on all pins (HBM,MM) .... 4 kV, 300V

† **Notice**: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 Electrical Specifications

TABLE 1-1: ANALOG SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 3V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, DITHER<1:0> = 11; BOOST<1:0> = 10, V_{CM} = 0V; T_A = -40°C to +125°C; V_{IN} = -0.5 dBFS @ 50/60 Hz on all channels.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
ADC Performance						
Resolution (No missing codes)		24	—	—	bits	OSR = 256 or greater
Sampling Frequency	f_S(DMCLK)	—	1	4	MHz	For maximum condition, BOOST<1:0> = 11
Output Data Rate	f_D(DRCLK)	—	4	125	ksps	For maximum condition, BOOST<1:0> = 11, OSR = 32
Analog Input Absolute Voltage on CHn+/- pins, n between 0 and 3	CHn+/-	-1	—	+1	V	All analog input channels, measured to A_{GND}
Analog Input Leakage Current	I_{IN}	—	+/-1	—	nA	RESET<3:0> = 1111, MCLK running continuously
Differential Input Voltage Range	$(CH_{n+}-CH_{n-})$	-600/GAIN	—	+600/GAIN	mV	V_{REF} = 1.2V, proportional to V_{REF}
Offset Error	V_{OS}	-1	0.2	1	mV	**Note 5**
Offset Error Drift		—	0.5	—	µV/°C	
Gain Error	GE	-5	—	+5	%	**Note 5**
Gain Error Drift		—	1	—	ppm/°C	

Note 1: Dynamic Performance specified at -0.5 dB below the maximum differential input value, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz, V_{REF} = 1.2V. See **Section 4.0 “Terminology And Formulas”** for definition. This parameter is established by characterization and not 100% tested.

2: For these operating currents, the following configuration bit settings apply: SHUTDOWN<3:0> = 0000, RESET<3:0> = 0000, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following configuration bit settings apply: SHUTDOWN<3:0> = 1111, VREFEXT = 1, CLKEXT = 1.

4: Measured on one channel versus all others channels. The average of crosstalk performance over all channels (see Figure 2-32 for individual channel performance).

5: Applies to all gains. Offset and gain errors depend on PGA gain setting, see typical performance curves for typical performance.

6: Outside of this range, ADC accuracy is not specified. An extended input range of +/-2V can be applied continuously to the part with no damage.

7: For proper operation and for optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2, as a function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

8: This parameter is established by characterization and not 100% tested.

TABLE 1-1: ANALOG SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 3V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, DITHER<1:0> = 11; BOOST<1:0> = 10, V_{CM} = 0V; T_A = -40°C to +125°C; V_{IN} = -0.5 dBFS @ 50/60 Hz on all channels.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Integral Nonlinearity	INL	—	5	—	ppm	
Measurement Error	ME	—	0.1	—	%	Measured with a 10,000:1 dynamic range (from 600 mV_{Peak} to 60 μV_{Peak}), AV_{DD} = DV_{DD} = 3V, measurement points averaging time: 20 seconds, measured on each channel pair (CH0/1, CH2/3)
Differential Input Impedance	Z_{IN}	232	—	—	kΩ	G = 1, proportional to 1/AMCLK
		142	—	—	kΩ	G = 2, proportional to 1/AMCLK
		72	—	—	kΩ	G = 4, proportional to 1/AMCLK
		38	—	—	kΩ	G = 8, proportional to 1/AMCLK
		36	—	—	kΩ	G = 16, proportional to 1/AMCLK
		33	—	—	kΩ	G = 32, proportional to 1/AMCLK
Signal-to-Noise and Distortion Ratio (**Note 1**)	SINAD	92	93.5	—	dB	
Total Harmonic Distortion (**Note 1**)	THD	—	-107	-103	dBc	Includes the first 35 harmonics
Signal-to-Noise Ratio (**Note 1**)	SNR	92	94	—	dB	
Spurious Free Dynamic Range (**Note 1**)	SFDR	—	112	—	dBFS	
Crosstalk (50, 60 Hz)	CTALK	—	-122	—	dB	**Note 4**
AC Power Supply Rejection	AC PSRR	—	-73	—	dB	AV_{DD} = DV_{DD} = 3V + $0.6V_{PP}$ 50/60 Hz, 100/120 Hz
DC Power Supply Rejection	DC PSRR	—	-73	—	dB	AV_{DD} = DV_{DD} = 2.7V to 3.6V
DC Common Mode Rejection	DC CMRR	—	-100	—	dB	V_{CM} from -1V to +1V

Note 1: Dynamic Performance specified at -0.5 dB below the maximum differential input value, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz, V_{REF} = 1.2V. See **Section 4.0 "Terminology And Formulas"** for definition. This parameter is established by characterization and not 100% tested.

2: For these operating currents, the following configuration bit settings apply: SHUTDOWN<3:0> = 0000, RESET<3:0> = 0000, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following configuration bit settings apply: SHUTDOWN<3:0> = 1111, VREFEXT = 1, CLKEXT = 1.

4: Measured on one channel versus all others channels. The average of crosstalk performance over all channels (see Figure 2-32 for individual channel performance).

5: Applies to all gains. Offset and gain errors depend on PGA gain setting, see typical performance curves for typical performance.

6: Outside of this range, ADC accuracy is not specified. An extended input range of +/-2V can be applied continuously to the part with no damage.

7: For proper operation and for optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2, as a function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

8: This parameter is established by characterization and not 100% tested.

TABLE 1-1: ANALOG SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 3V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, DITHER<1:0> = 11; BOOST<1:0> = 10, V_{CM} = 0V; T_A = -40°C to +125°C; V_{IN} = -0.5 dBFS @ 50/60 Hz on all channels.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Internal Voltage Reference						
Tolerance	V_{REF}	1.176	1.2	1.224	V	VREFEXT = 0, T_A = +25°C only
Temperature Coefficient	TCV_{REF}	—	9	—	ppm/°C	T_A = -40°C to +125°C, VREFEXT = 0, VREFCAL<7:0> = 0x50
Output Impedance	$ZOUTV_{REF}$	—	0.6	—	kΩ	VREFEXT = 0
Internal Voltage Reference Operating Current	$AI_{DD}V_{REF}$	—	54	—	µA	VREFEXT = 0, SHUTDOWN<3:0> = 1111
Voltage Reference Input						
Input Capacitance		—	—	10	pF	
Differential Input Voltage Range (V_{REF+} – V_{REF-})	V_{REF}	1.1	—	1.3	V	VREFEXT = 1
Absolute Voltage on REFIN+ pin	V_{REF+}	V_{REF-} + 1.1	—	V_{REF-} + 1.3	V	VREFEXT = 1
Absolute Voltage REFIN- pin	V_{REF-}	-0.1	—	+0.1	V	REFIN- should be connected to A_{GND} when VREFEXT = 0
Master Clock Input						
Master Clock Input Frequency Range	f_{MCLK}	—	—	20	MHz	CLKEXT = 1, **(Note 7)**
Crystal Oscillator Operating Frequency Range	f_{XTAL}	1	—	20	MHz	CLKEXT = 0, **(Note 7)**
Analog Master Clock	AMCLK	—	—	16	MHz	**(Note 7)**
Crystal Oscillator Operating Current	DIDDXTAL	—	80	—	µA	CLKEXT = 0
Power Supply						
Operating Voltage, Analog	AV_{DD}	2.7	—	3.6	V	
Operating Voltage, Digital	DV_{DD}	2.7	—	3.6	V	

Note 1: Dynamic Performance specified at -0.5 dB below the maximum differential input value, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz, V_{REF} = 1.2V. See **Section 4.0 "Terminology And Formulas"** for definition. This parameter is established by characterization and not 100% tested.

2: For these operating currents, the following configuration bit settings apply: SHUTDOWN<3:0> = 0000, RESET<3:0> = 0000, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following configuration bit settings apply: SHUTDOWN<3:0> = 1111, VREFEXT = 1, CLKEXT = 1.

4: Measured on one channel versus all others channels. The average of crosstalk performance over all channels (see Figure 2-32 for individual channel performance).

5: Applies to all gains. Offset and gain errors depend on PGA gain setting, see typical performance curves for typical performance.

6: Outside of this range, ADC accuracy is not specified. An extended input range of +/-2V can be applied continuously to the part with no damage.

7: For proper operation and for optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2, as a function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

8: This parameter is established by characterization and not 100% tested.

TABLE 1-1: ANALOG SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = DV_{DD} = 3V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, DITHER<1:0> = 11; BOOST<1:0> = 10, V_{CM} = 0V; T_A = -40°C to +125°C; V_{IN} = -0.5 dBFS @ 50/60 Hz on all channels.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Operating Current, Analog (**Note 2**)	$I_{DD,A}$	—	2.8	4	mA	BOOST<1:0> = 00
		—	3.4	4.5	mA	BOOST<1:0> = 01
		—	4.7	6.4	mA	BOOST<1:0> = 10
		—	8.1	11.8	mA	BOOST<1:0> = 11
Operating Current, Digital	$I_{DD,D}$	—	0.28	0.6	mA	MCLK = 4 MHz, proportional to MCLK (**Note 2**)
		—	1.1	—	mA	MCLK = 16 MHz, proportional to MCLK (**Note 2**)
Shutdown Current, Analog	$I_{DDS,A}$	—	0.01	2	µA	AV_{DD} pin only (**Note 3**) (**Note 8**)
Shutdown Current, Digital	$I_{DDS,D}$	—	0.01	4	µA	DV_{DD} pin only (**Note 3**) (**Note 8**)
Pull-down Current on OSC2 Pin (External Clock mode only)	I_{OSC2}	—	35	—	µA	CLKEXT = 1

Note 1: Dynamic Performance specified at -0.5 dB below the maximum differential input value, V_{IN} = 1.2 V_{PP} = 424 mV_{RMS} @ 50/60 Hz, V_{REF} = 1.2V. See **Section 4.0 "Terminology And Formulas"** for definition. This parameter is established by characterization and not 100% tested.

2: For these operating currents, the following configuration bit settings apply: SHUTDOWN<3:0> = 0000, RESET<3:0> = 0000, VREFEXT = 0, CLKEXT = 0.

3: For these operating currents, the following configuration bit settings apply: SHUTDOWN<3:0> = 1111, VREFEXT = 1, CLKEXT = 1.

4: Measured on one channel versus all others channels. The average of crosstalk performance over all channels (see Figure 2-32 for individual channel performance).

5: Applies to all gains. Offset and gain errors depend on PGA gain setting, see typical performance curves for typical performance.

6: Outside of this range, ADC accuracy is not specified. An extended input range of +/-2V can be applied continuously to the part with no damage.

7: For proper operation and for optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2, as a function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

8: This parameter is established by characterization and not 100% tested.

1.2 Serial Interface Characteristics

TABLE 1-2: SERIAL DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, C_{LOAD} = 30 pF, applies to all digital I/O.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
High-Level Input Voltage	V_{IH}	0.7 DV_{DD}	—	—	V	Schmitt-Triggered
Low-Level Input Voltage	V_{IL}	—	—	0.3 DV_{DD}	V	Schmitt-Triggered
Input Leakage Current	I_{LI}	—	—	±1	µA	$\overline{CS}$ = DV_{DD}, V_{IN} = D_{GND} to DV_{DD}
Output Leakage Current	I_{LO}	—	—	±1	µA	$\overline{CS}$ = DV_{DD}, V_{OUT} = D_{GND} or DV_{DD}
Hysteresis Of Schmitt-Trigger Inputs	V_{HYS}	—	500	—	mV	DV_{DD} = 3.3V only, **Note 2**
Low-Level Output Voltage	V_{OL}	—	—	0.2 DV_{DD}	V	I_{OL} = +1.7 mA

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is established by characterization and not production tested.

TABLE 1-2: SERIAL DC CHARACTERISTICS (CONTINUED)

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Electrical Specifications: Unless otherwise indicated, all parameters apply at DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, C_{LOAD} = 30 pF, applies to all digital I/O.						
High-Level Output Voltage	V_{OH}	0.75 DV_{DD}	—	—	V	I_{OH} = -1.7 mA
Internal Capacitance (All Inputs And Outputs)	C_{INT}	—	—	7	pF	T_A = +25°C, SCK = 1.0 MHz, DV_{DD} =3.3V (**Note 1**)

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is established by characterization and not production tested.

TABLE 1-3: SERIAL AC CHARACTERISTICS TABLE

Electrical Specifications: Unless otherwise indicated, all parameters apply at DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, GAIN = 1, C_{LOAD} = 30 pF						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Serial Clock Frequency	f_{SCK}	—	—	20	MHz	
$\overline{CS}$ Setup Time	t_{CSS}	25	—	—	ns	
$\overline{CS}$ Hold Time	t_{CSH}	50	—	—	ns	
$\overline{CS}$ Disable Time	t_{CSD}	50	—	—	ns	
Data Setup Time	t_{SU}	5	—	—	ns	
Data Hold Time	t_{HD}	10	—	—	ns	
Serial Clock High Time	t_{HI}	20	—	—	ns	
Serial Clock Low Time	t_{LO}	20	—	—	ns	
Serial Clock Delay Time	t_{CLD}	50	—	—	ns	
Serial Clock Enable Time	t_{CLE}	50	—	—	ns	
Output Valid from SCK Low	t_{DO}	—	—	25	ns	
Output Hold Time	t_{HO}	0	—	—	ns	Note 1
Output Disable Time	t_{DIS}	—	—	25	ns	Note 1
Reset Pulse Width ($\overline{RESET}$)	t_{MCLR}	100	—	—	ns	
Data Transfer Time to $\overline{DR}$ (Data Ready)	t_{DODR}	—	—	25	ns	Note 2
Data Ready Pulse Low Time	t_{DRP}	—	1/(2 x DMCLK)	—	µs	

Note 1: This parameter is periodically sampled and not 100% tested.
2: This parameter is established by characterization and not production tested.

TABLE 1-4: TEMPERATURE SPECIFICATIONS TABLE

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = 2.7 to 3.6V, DV_{DD} = 2.7 to 3.6V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units.**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	Note 1
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 28L SSOP	θ_{JA}	—	80	—	°C/W	
Thermal Resistance, 28L QFN	θ_{JA}	—	41	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

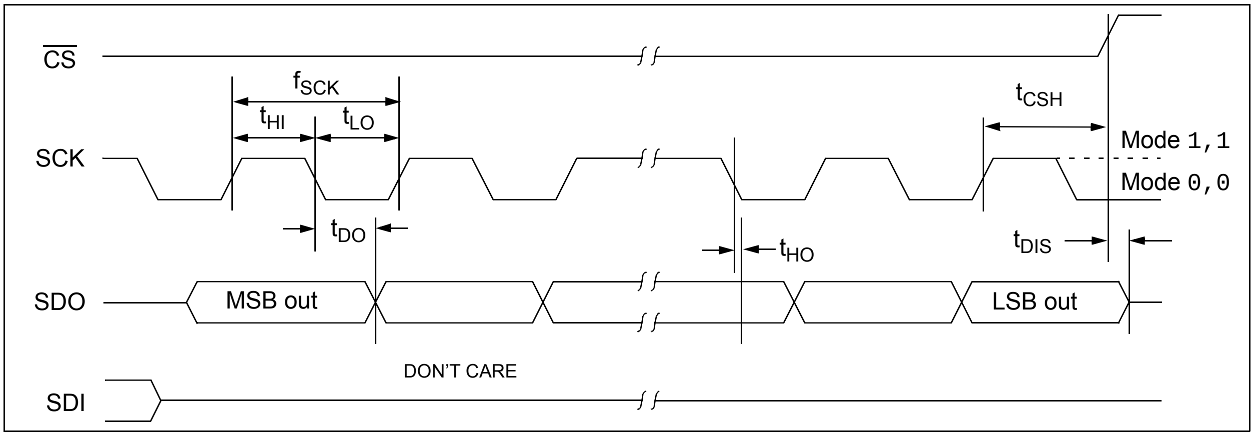


FIGURE 1-1: *Serial Output Timing Diagram.*

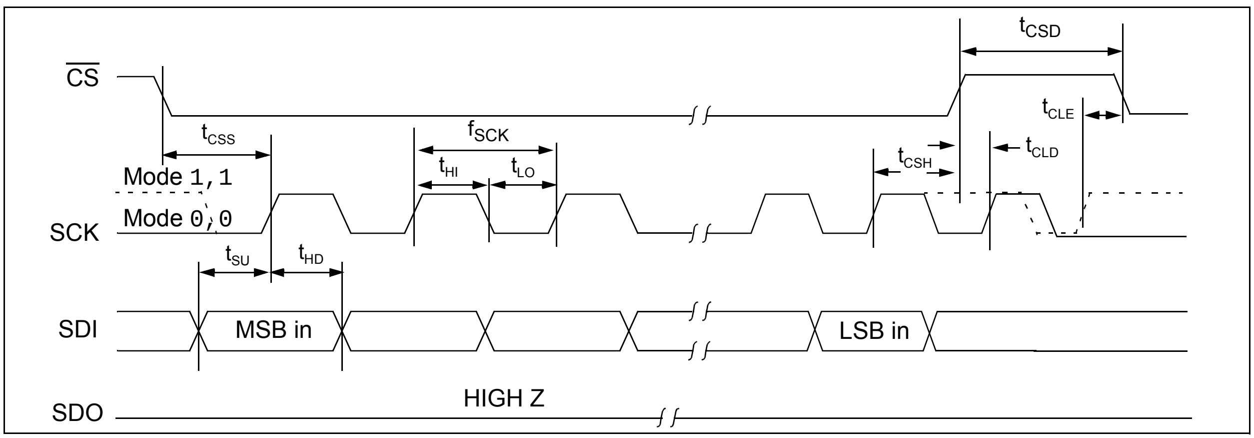


FIGURE 1-2: *Serial Input Timing Diagram.*

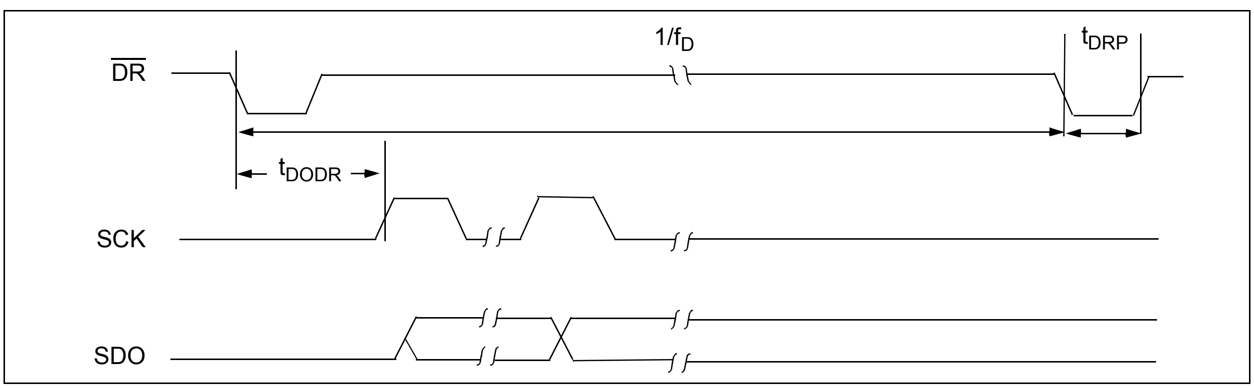


FIGURE 1-3: *Data Ready Pulse / Sampling Timing Diagram.*

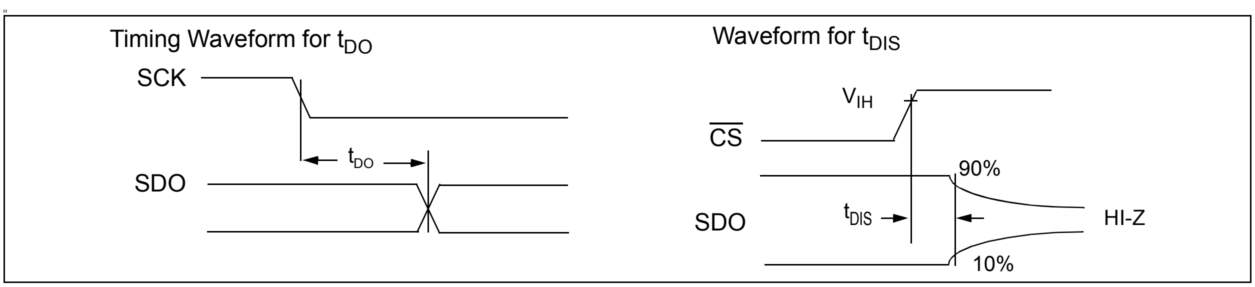


FIGURE 1-4: *Timing Diagrams, continued.*

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

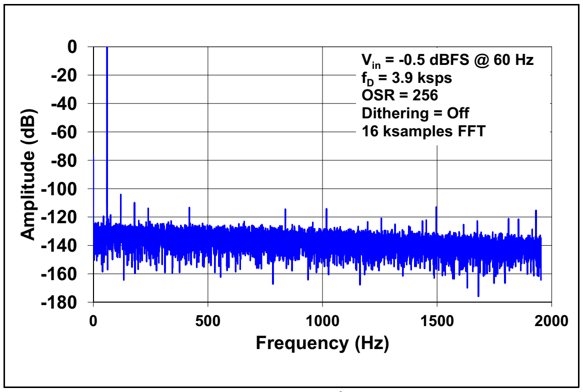


FIGURE 2-1: *Spectral Response.*

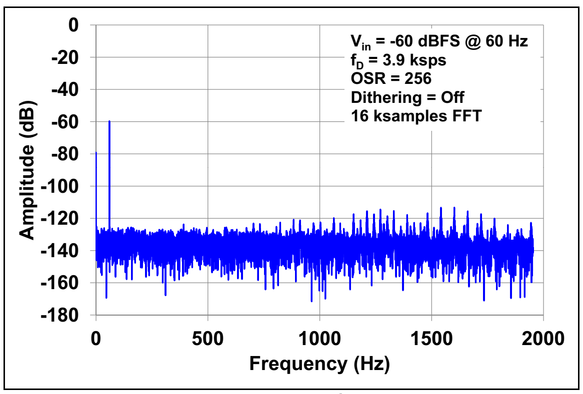


FIGURE 2-2: *Spectral Response.*

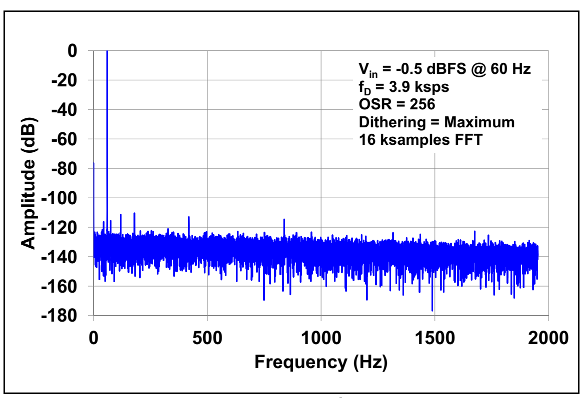


FIGURE 2-3: *Spectral Response.*

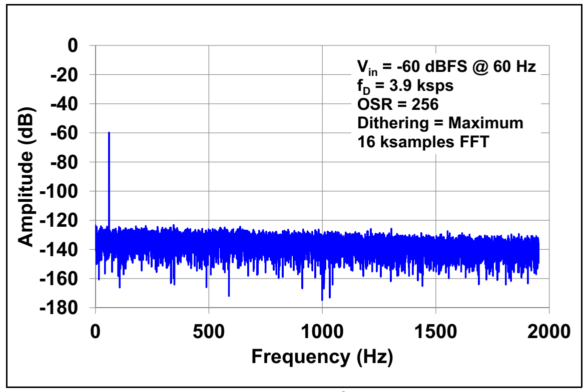


FIGURE 2-4: *Spectral Response.*

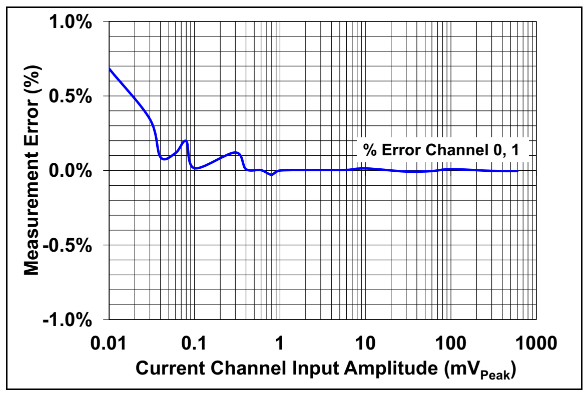


FIGURE 2-5: *Measurement Error with 1-Point Calibration.*

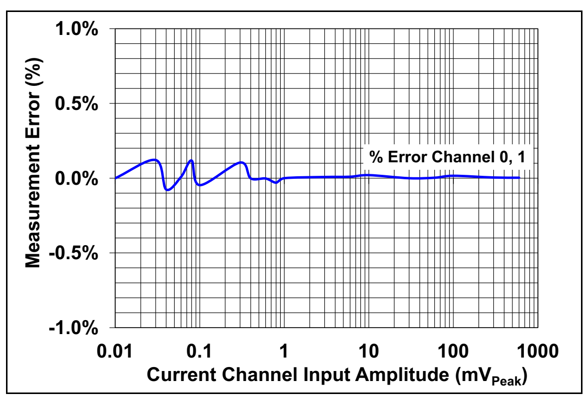


FIGURE 2-6: *Measurement Error with 2-Point Calibration.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

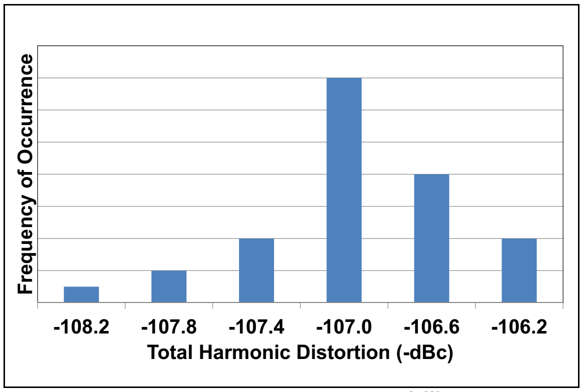


FIGURE 2-7: *THD Repeatability Histogram.*

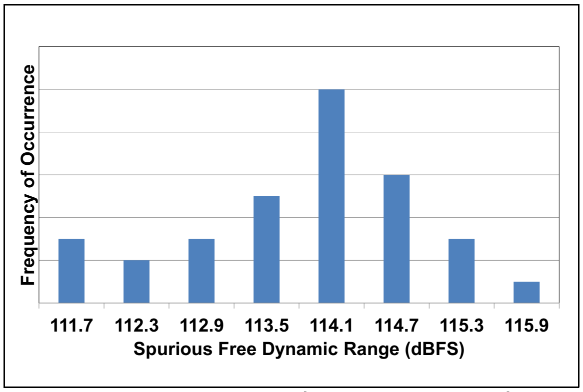


FIGURE 2-8: *Spurious Free Dynamic Range Repeatability Histogram.*

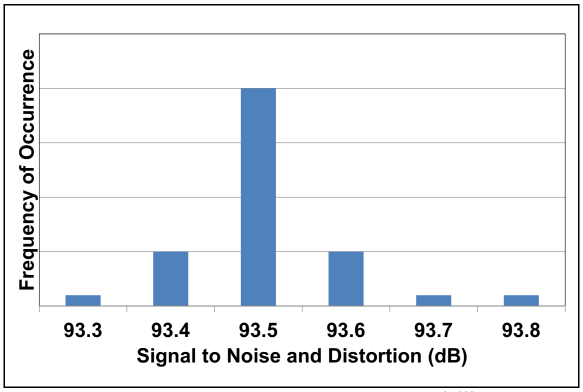


FIGURE 2-9: *SINAD Repeatability Histogram.*

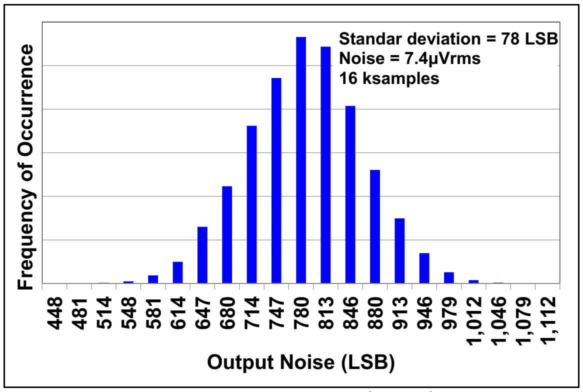


FIGURE 2-10: *Output Noise Histogram.*

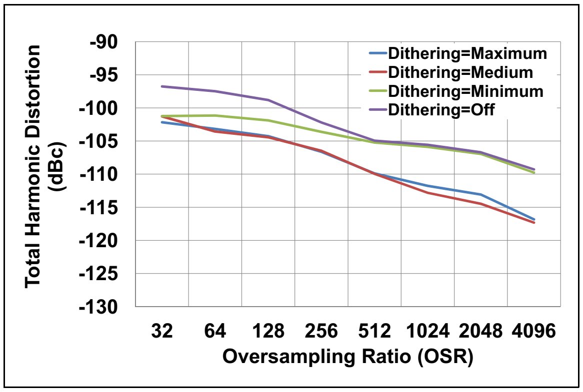


FIGURE 2-11: *THD vs.OSR.*

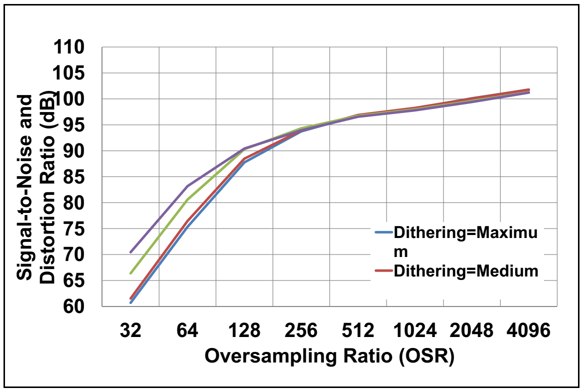


FIGURE 2-12: *SINAD vs. OSR.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

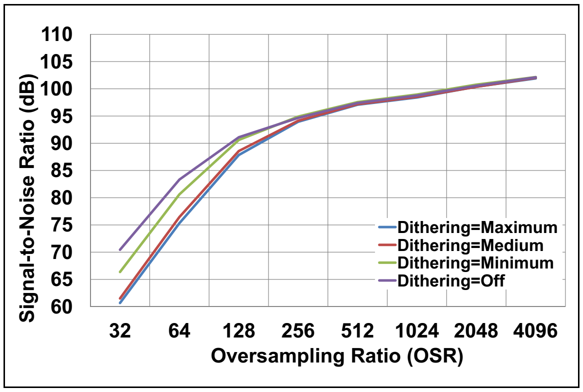


FIGURE 2-13: *SNR vs.OSR.*

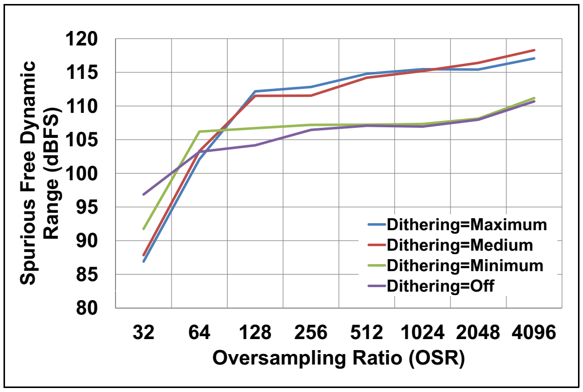


FIGURE 2-14: *SFDR vs. OSR.*

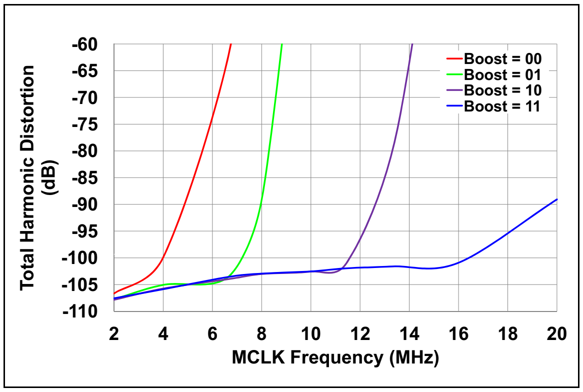


FIGURE 2-15: *THD vs. MCLK.*

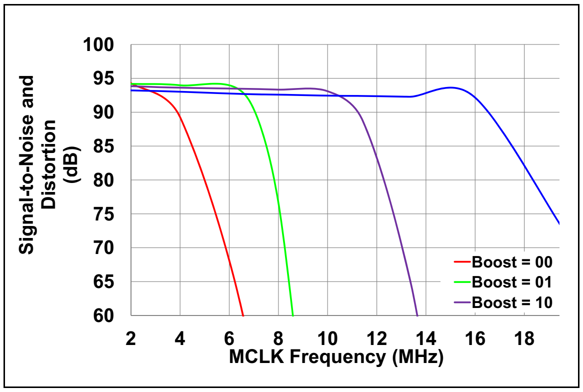


FIGURE 2-16: *SINAD vs. MCLK.*

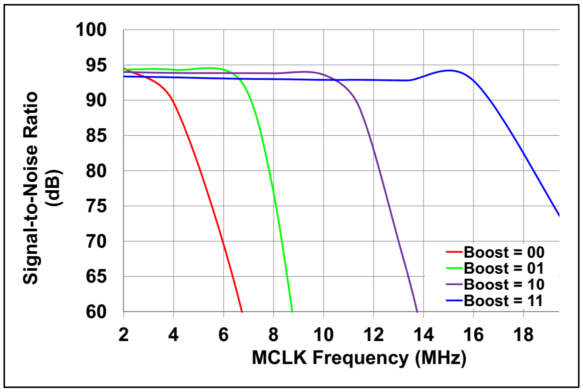


FIGURE 2-17: *SNR vs. MCLK.*

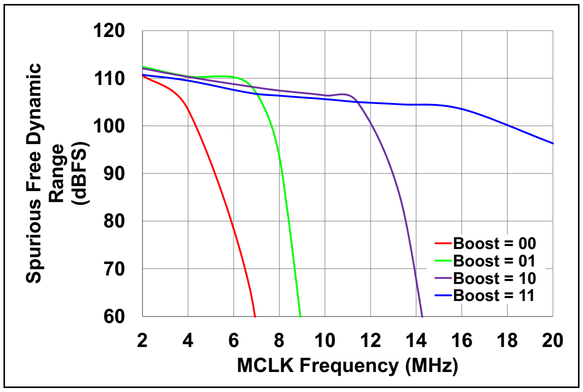


FIGURE 2-18: *SFDR vs. MCLK.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

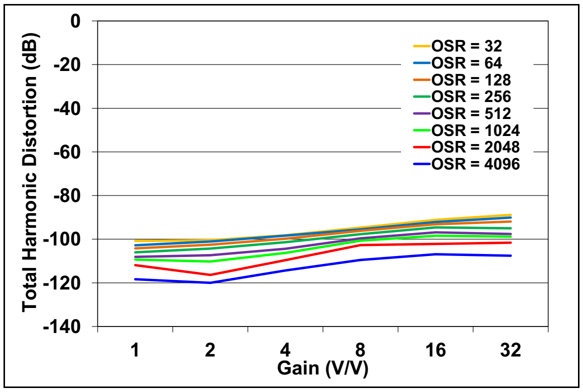


FIGURE 2-19: *THD vs. GAIN.*

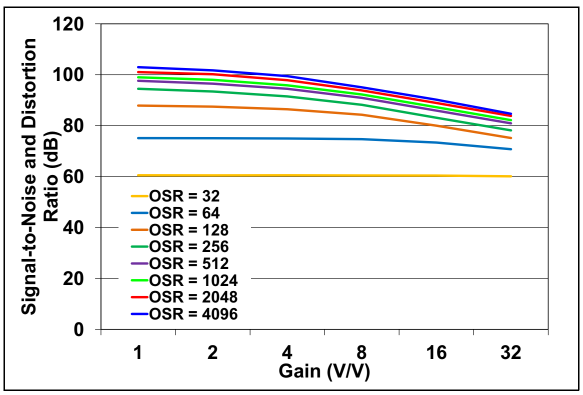


FIGURE 2-20: *SINAD vs. GAIN.*

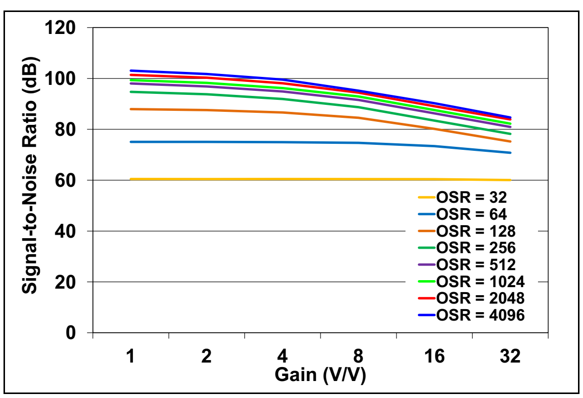


FIGURE 2-21: *SNR vs. GAIN.*

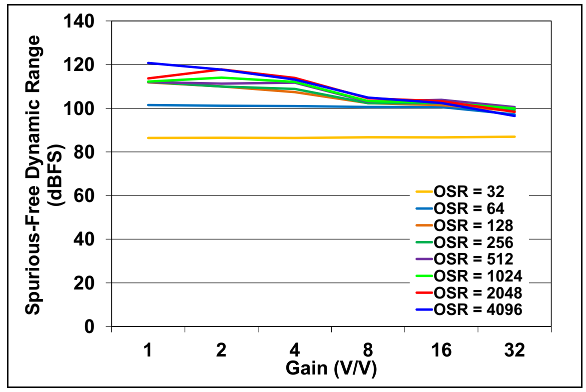


FIGURE 2-22: *SFDR vs. GAIN.*

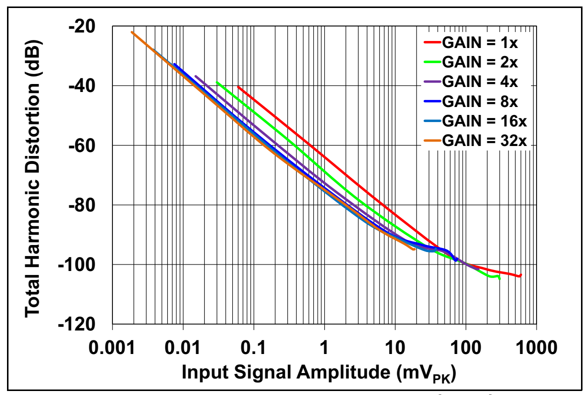


FIGURE 2-23: *THD vs. Input Signal Amplitude.*

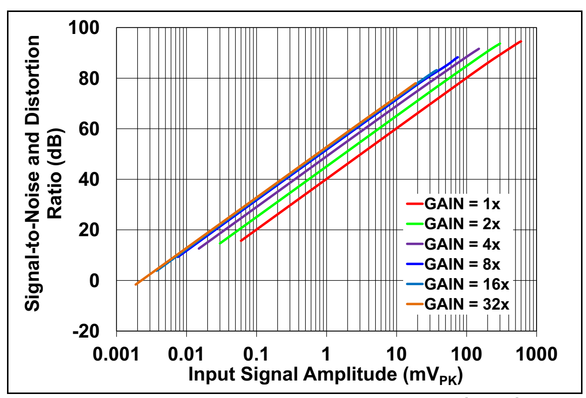


FIGURE 2-24: *SINAD vs. Input Signal Amplitude.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

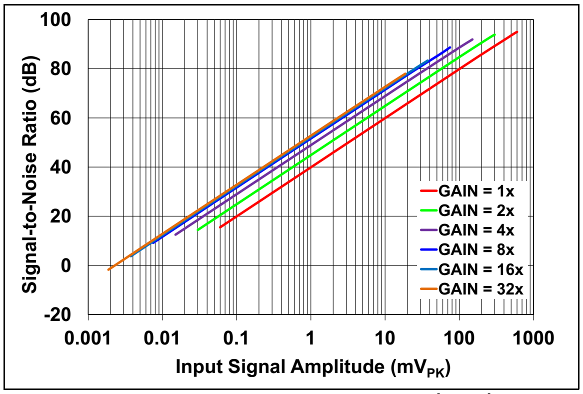


FIGURE 2-25: *SNR vs. Input Signal Amplitude.*

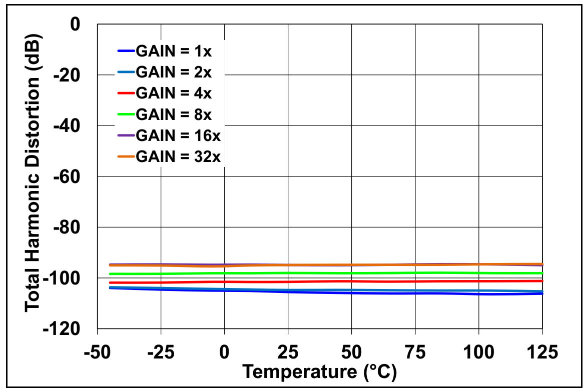


FIGURE 2-28: *THD vs. Temperature.*

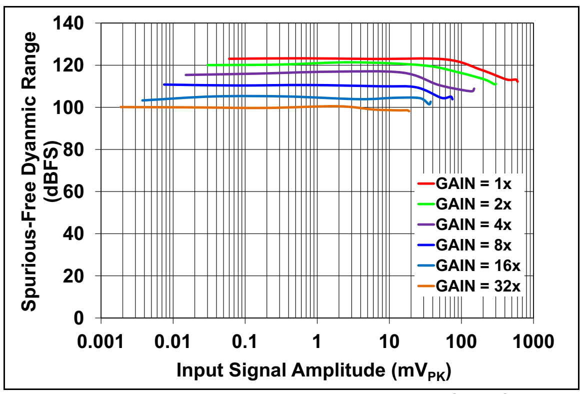


FIGURE 2-26: *SFDR vs. Input Signal Amplitude.*

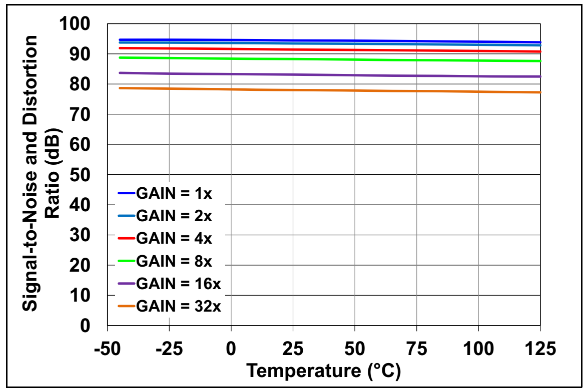


FIGURE 2-29: *SINAD vs. Temperature.*

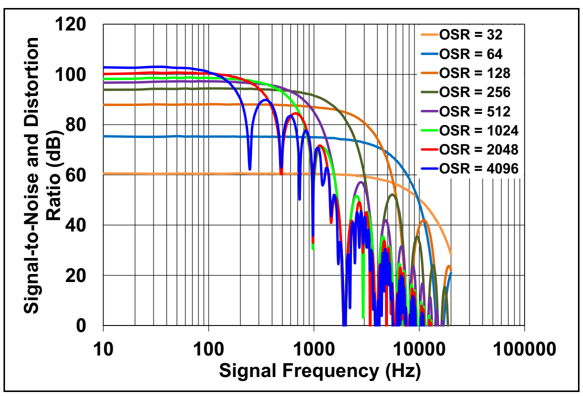


FIGURE 2-27: *SINAD vs. Input Frequency.*

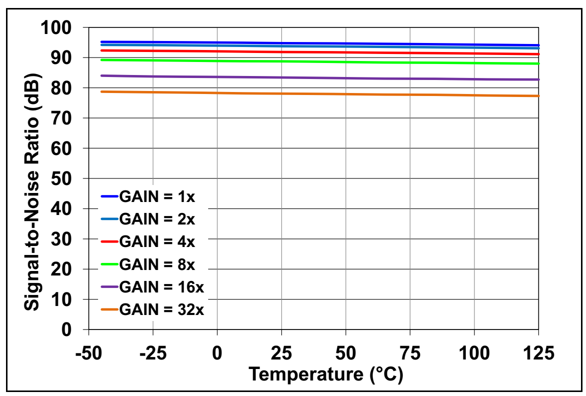


FIGURE 2-30: *SNR vs. Temperature.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

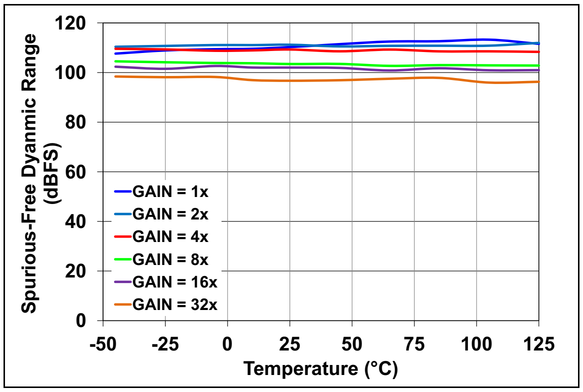


FIGURE 2-31: *SFDR vs. Temperature.*

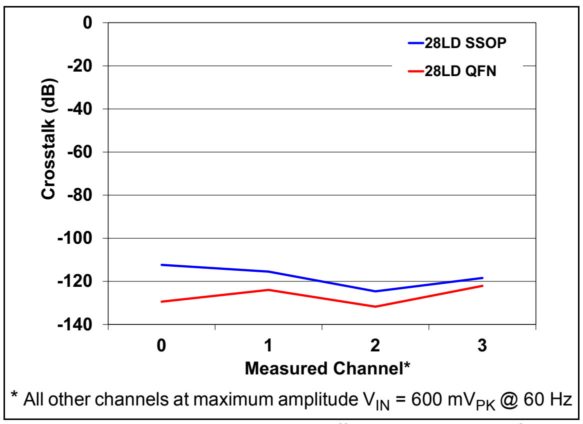


FIGURE 2-32: *Crosstalk vs. Measured Channel.*

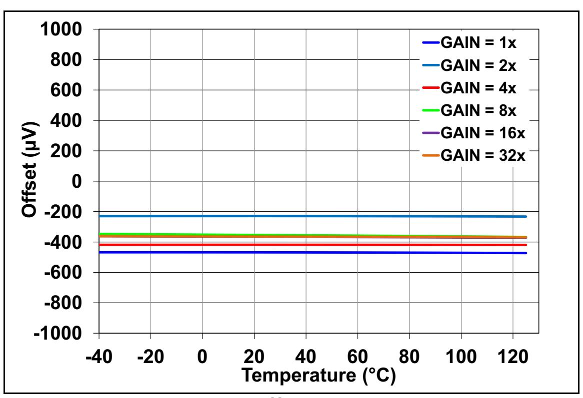


FIGURE 2-33: *Offset vs. Temperature vs. Gain.*

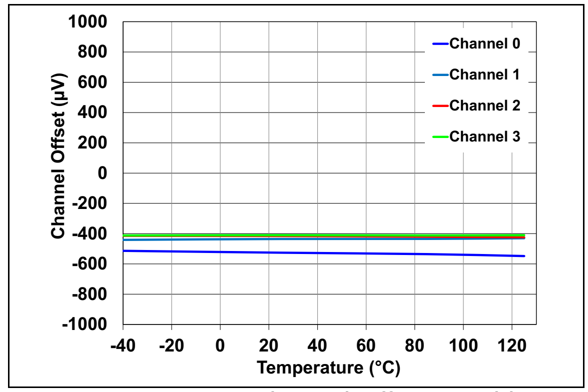


FIGURE 2-34: *Channel Offset Matching vs. Temperature.*

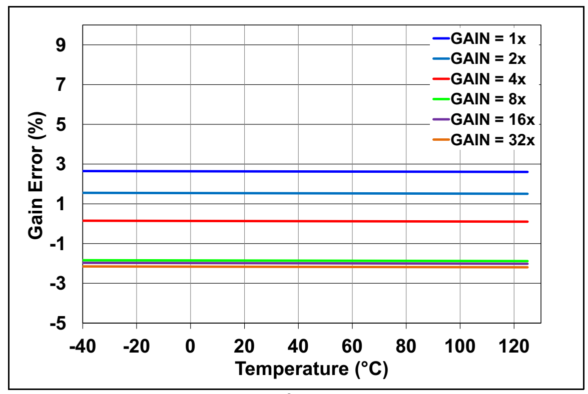


FIGURE 2-35: *Gain Error vs. Temperature vs. Gain.*

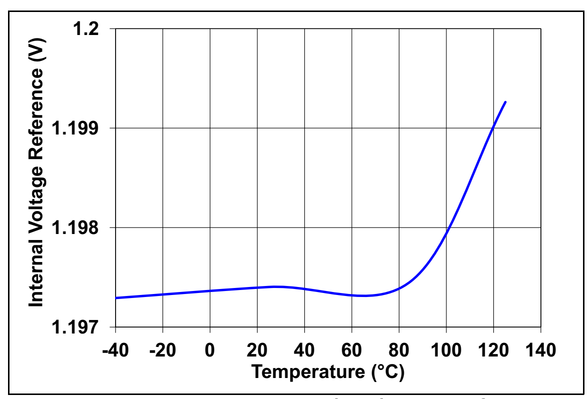


FIGURE 2-36: *Internal Voltage Reference vs. Temperature.*

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; V_{IN} = -0.5 dBFS @ 60 Hz on all channels, VREFEXT = 0; CLKEXT = 1; BOOST<1:0> = 10.

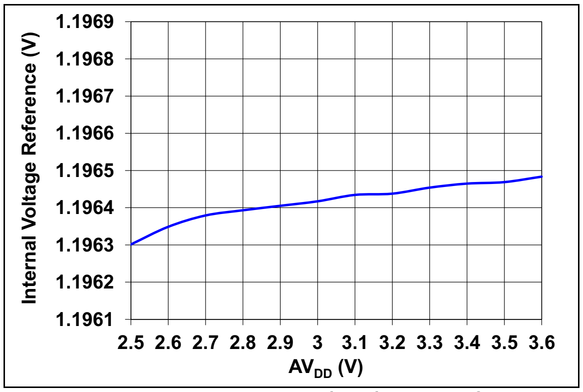


FIGURE 2-37: *Internal Voltage Reference vs. Supply Voltage.*

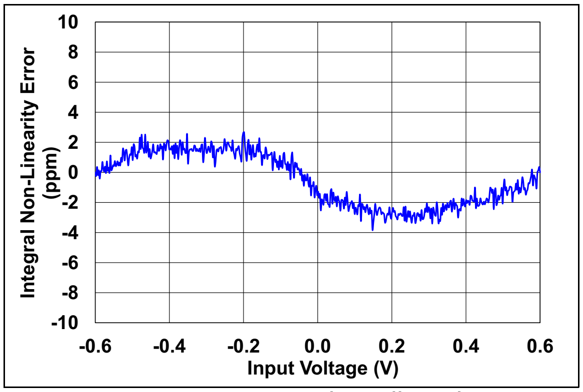


FIGURE 2-38: *Integral Nonlinearity (Dithering Maximum).*

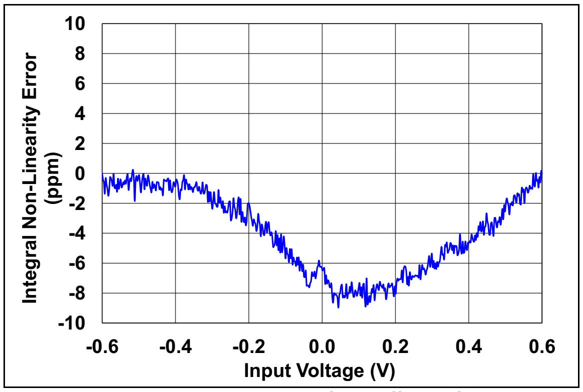


FIGURE 2-39: *Integral Nonlinearity (Dithering Off).*

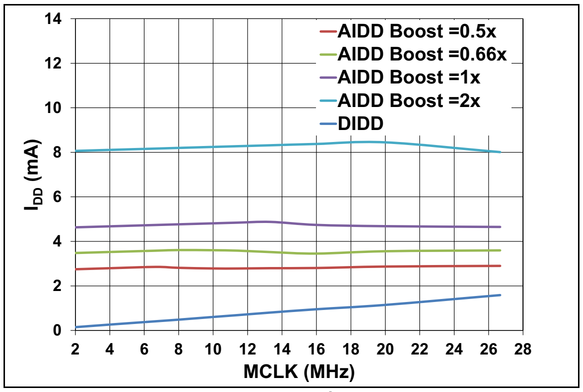


FIGURE 2-40: *Operating Current vs. MCLK Frequency vs. Boost, V_{DD} = 3V.*

NOTES:

3.0 PIN DESCRIPTION

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: FOUR CHANNEL MCP3912 PIN FUNCTION TABLE

MCP3912 SSOP	MCP3912 QFN	Symbol	Function
1	25, 11	AV_{DD}	Analog Power Supply Pin
2	27	CH0+	Noninverting Analog Input Pin for Channel 0
3	28	CH0-	Inverting Analog Input Pin for Channel 0
4	29	CH1-	Inverting Analog Input Pin for Channel 1
5	2	CH1+	Noninverting Analog Input Pin for Channel 1
6	3	CH2+	Noninverting Analog Input Pin for Channel 2
7	4	CH2-	Inverting Analog Input Pin for Channel 2
8	5	CH3-	Inverting Analog Input Pin for Channel 3
9	6	CH3+	Noninverting Analog Input Pin for Channel 3
10, 11, 12, 13, 19	7	NC	No Connect (for better EMI results connect to A_{GND})
14	8	REFIN+/OUT	Noninverting Voltage Reference Input and Internal Reference Output Pin
15	9	REFIN-	Inverting Voltage Reference Input Pin
16	10, 26	A_{GND}	Analog Ground Pin, Return Path for Internal Analog Circuitry
17, 20	13, 15, 23	D_{GND}	Digital Ground Pin, Return Path for Internal Digital Circuitry
18	14	$\overline{DR}$	Data Ready Signal Output Pin
21	16	OSC1/CLKI	Oscillator Crystal Connection Pin or External Clock Input Pin
22	17	OSC2	Oscillator Crystal Connection Pin
23	18	$\overline{CS}$	Serial Interface Chip Select Input Pin
24	19	SCK	Serial Interface Clock Input Pin for SPI
25	20	SDO	Serial Interface Data Output Pin
26	21	SDI	Serial Interface Data Input Pin
27	22	$\overline{RESET}$	Master Reset Logic Input Pin
28	12, 14	DV_{DD}	Digital Power Supply Pin
—	29	EP	Exposed Thermal Pad. Must be connected to A_{GND} or floating.

3.1 Analog Power Supply (AV_{DD})

AV_{DD} is the power supply voltage for the analog circuitry within the MCP3912. It is distributed on several pins (pins 11 and 25 in the QFN-28 package, one pin only in the SSOP-28 package). For optimal performance, connect these pins together using a star connection, and connect the appropriate bypass capacitors (typically a 10 µF in parallel with a 0.1 µF ceramic). AV_{DD} should be maintained between 2.7V and 3.6V for specified operation.

To ensure proper functionality of the device, at least one of these pins must be properly connected. To ensure optimal performance of the device, all the pins must be properly connected. If any of these pins are left floating, the accuracy and noise specifications are not ensured.

3.2 ADC Differential Analog Inputs (CHn+/CHn-)

The CHn+/- pins (n comprised between 0 and 3) are the four fully-differential analog voltage inputs for the delta-sigma ADCs.

The linear and specified region of the channels is dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each CHn+/- input pin is ±1V with no distortion, and ±2V with no breaking after continuous voltage. This maximum absolute voltage is not proportional to the V_{REF} voltage.

3.3 Noninverting Reference Input, Internal Reference Output (REFIN+/OUT)

This pin is the noninverting side of the differential voltage reference input for all ADCs or the internal voltage reference output.

When VREFEXT = `1`, an external voltage reference source can be used, and the internal voltage reference is disabled. When using an external differential voltage reference, it should be connected to its V_{REF+} pin. When using an external single-ended reference, it should be connected to this pin.

When VREFEXT = `0`, the internal voltage reference is enabled and connected to this pin through a switch. This voltage reference has minimal drive capability and thus needs proper buffering and bypass capacitances (a 0.1 µF ceramic capacitor is sufficient in most cases) if used as a voltage source.

If the voltage reference is only used as an internal V_{REF}, adding bypass capacitance on REFIN+/OUT is not necessary for keeping ADC accuracy, but a minimal 0.1 µF ceramic capacitance can be connected to avoid EMI/EMC susceptibility issues due to the antenna created by the REFIN+/OUT pin if left floating.

3.4 Inverting Reference Input (REFIN-)

This pin is the inverting side of the differential voltage reference input for all ADCs. When using an external differential voltage reference, it should be connected to its V_{REF-} pin. When using an external single-ended voltage reference, or when VREFEXT = `0` (default) and using the internal voltage reference, the pin should be directly connected to A_{GND}.

3.5 Analog Ground (A_{GND})

A_{GND} is the ground reference voltage for the analog circuitry within the MCP3912. It is distributed on several pins (pins 10 and 26 in the QFN-28 package, one pin only in the SSOP-28 package). For optimal performance, it is recommended to connect these pins together using a star connection, and to connect it to the same ground node voltage as D_{GND} with a star connection.

At least one of these pins needs to be properly connected to ensure proper functionality of the device. All of these pins need to be properly connected to ensure optimal performance of the device. If any of these pins are left floating, the accuracy and noise specifications are not ensured. If an analog ground plane is available, it is recommended that these pins be tied to this plane of the PCB. This plane should also reference all other analog circuitry in the system.

3.6 Digital Ground (D_{GND})

D_{GND} is the ground reference voltage for the digital circuitry within the MCP3912. It is distributed on several pins (pins 13, 15 and 23 in the QFN-28 package, two pins only in the SSOP-28 package). For optimal performance, connect these pins together using a star connection and connect it to the same ground node voltage as A_{GND} with a star connection.

At least one of these pins needs to be properly connected to ensure proper functionality of the device. All of these pins need to be properly connected to ensure optimal performance of the device. If any of these pins are left floating, the accuracy and noise specifications are not ensured. If a digital ground plane is available, it is recommended that these pins be tied to this plane of the Printed Circuit Board (PCB). This plane should also reference all other digital circuitry in the system.

3.7 Data Ready Output ($\overline{\text{DR}}$)

The Data Ready pin indicates if a new conversion result is ready to be read. The default state of this pin is logic high when $\overline{\text{DR\_HIZ}}$ = `1`, and is high-impedance when $\overline{\text{DR\_HIZ}}$ = `0` (default). After each conversion is finished, a logic low pulse will take place on the data ready pin to indicate the conversion result is ready as an interrupt. This pulse is synchronous with the master clock and has a defined and constant width.

The Data Ready pin is independent of the SPI interface and acts like an interrupt output. The Data Ready pin state is not latched, and the pulse width (and period) are both determined by the MCLK frequency, over-sampling rate and internal clock prescale settings. The data ready pulse width is equal to half a DMCLK period, and the frequency of the pulses is equal to DRCLK (see Figure 1-3).

> **Note:** This pin should not be left floating when the $\overline{\text{DR\_HIZ}}$ bit is low; a 100 kΩ pull-up resistor connected to DV_{DD} is recommended.

3.8 Oscillator and Master Clock Input Pin (OSC1/CLKI)

OSC1/CLKI and OSC2 provide the master clock for the device. When CLKEXT = `0`, a resonant crystal or clock source with a similar sinusoidal waveform must be placed across the OSC1 and OSC2 pins to ensure proper operation.

The typical clock frequency specified is 4 MHz. For proper operation and for optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2 for the function of the BOOST and PGA setting chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2. Appropriate load capacitance should be connected to these pins for proper operation.

> **Note:** When CLKEXT = `1`, the crystal oscillator is disabled. OSC1 becomes the master clock input CLKI, a direct path for an external clock source. One example would be a clock source generated by an MCU.

3.9 Crystal Oscillator (OSC2)

When CLKEXT = `0`, a resonant crystal or clock source with a similar sinusoidal waveform must be placed across the OSC1 and OSC2 pins to ensure proper operation. Appropriate load capacitance should be connected to these pins for proper operation.

When CLKEXT = `1`, this pin should be connected to D_{GND} at all times (an internal pull-down operates this function if the pin is left floating).

3.10 Chip Select ($\overline{\text{CS}}$)

This pin is the Serial Peripheral Interface (SPI) chip select that enables serial communication. When this pin is logic high, no communication can take place. A chip select falling edge initiates serial communication, and a chip select rising edge terminates the communication. No communication can take place even when $\overline{\text{CS}}$ is logic low if $\overline{\text{RESET}}$ is also logic low.

This input is Schmitt-triggered.

3.11 Serial Data Clock (SCK)

This is the serial clock pin for SPI communication. Data is clocked into the device on the rising edge of SCK. Data is clocked out of the device on the falling edge of SCK.

The MCP3912 SPI interface is compatible with SPI 0,0 and 1,1 modes. SPI modes can be changed during a $\overline{\text{CS}}$ high time.

The maximum clock speed specified is 20 MHz. SCK and MCLK are two different and asynchronous clocks; SCK is only required when a communication happens, while MCLK is continuously required when the part is converting analog inputs.

This input is Schmitt-triggered.

3.12 Serial Data Output (SDO)

This is the SPI data output pin. Data is clocked out of the device on the falling edge of SCK.

This pin remains in a high-impedance state during the command byte. It also stays high-impedance during the entire communication for write commands when the $\overline{\text{CS}}$ pin is logic high or when the $\overline{\text{RESET}}$ pin is logic low. This pin is active only when a read command is processed. The interface is half-duplex (inputs and outputs do not happen at the same time).

3.13 Serial Data Input (SDI)

This is the SPI data input pin. Data is clocked into the device on the rising edge of SCK. When $\overline{\text{CS}}$ is logic low, this pin is used to communicate with a series of 8-bit commands. The interface is half-duplex (inputs and outputs do not happen at the same time).

Each communication starts with a chip select falling edge followed by an 8-bit command word entered through the SDI pin. Each command is either a read or a write command. Toggling SDI after a read command or when $\overline{\text{CS}}$ is logic high has no effect.

This input is Schmitt-triggered.

3.14 Master Reset ($\overline{\text{RESET}}$)

This pin is active-low and places the entire chip in a Reset state when active.

When $\overline{\text{RESET}}$ is logic low, all registers are reset to their default value, no communication can take place and no clock is distributed inside the part, except in the input structure if MCLK is applied (if MCLK is idle, then no clock is distributed). This state is equivalent to a Power-On Reset (POR) state.

Since the default state of the ADCs is on, the analog power consumption when $\overline{\text{RESET}}$ is logic low is equivalent to when $\overline{\text{RESET}}$ is logic high. Only the digital power consumption is largely reduced, because this current consumption is essentially dynamic and is reduced drastically when there is no clock running.

All the analog biases are enabled during a Reset, so that the part is fully operational just after a $\overline{\text{RESET}}$ rising edge if MCLK is applied when $\overline{\text{RESET}}$ is logic low. If MCLK is not applied, there is a time after a hard reset when the conversion may not accurately correspond to the start-up of the input structure.

This input is Schmitt-triggered.

3.15 Digital Power Supply (DV_{DD})

DV_{DD} is the power supply voltage for the digital circuitry within the MCP3912. It is distributed on several pins (pins 12 and 24 in the QFN-28 package, one pin only in the SSOP-28 package). For optimal performance, it is recommended to connect these pins together using a star connection and to connect appropriate bypass capacitors (typically a 10 µF in parallel with a 0.1 µF ceramic). DV_{DD} should be maintained between 2.7V and 3.6V for specified operation.

At least one of these pins needs to be properly connected to ensure proper functionality of the device. All of these pins need to be properly connected to ensure optimal performance of the device. If any of these pins are left floating, the accuracy and noise specifications are not ensured.

3.16 Exposed Thermal Pad

This pin must be connected to A_{GND} or left floating for proper operation. Connecting it to A_{GND} is preferable for lowest noise performance and best thermal behavior.

4.0 TERMINOLOGY AND FORMULAS

This section defines the terms and formulas used throughout this data sheet. The following terms are defined:

- MCLK – Master Clock
- AMCLK – Analog Master Clock
- DMCLK – Digital Master Clock
- DRCLK – Data Rate Clock
- OSR – Oversampling Ratio
- Offset Error
- Gain Error
- Integral Nonlinearity Error
- Signal-to-Noise Ratio (SNR)
- Signal-To-Noise Ratio And Distortion (SINAD)
- Total Harmonic Distortion (THD)
- Spurious-Free Dynamic Range (SFDR)
- MCP3912 Delta-Sigma Architecture
- Idle Tones
- Dithering
- Crosstalk
- PSRR
- CMRR
- ADC Reset Mode
- Hard Reset Mode (RESET = 0)
- ADC Shutdown Mode
- Full Shutdown Mode
- Measurement Error

4.1 MCLK – Master Clock

This is the fastest clock present on the device. This is the frequency of the crystal placed at the OSC1/OSC2 inputs when CLKEXT = 0, or the frequency of the clock input at the OSC1/CLKI when CLKEXT = 1. See Figure 4-1.

4.2 AMCLK – Analog Master Clock

AMCLK is the clock frequency that is present on the analog portion of the device after prescaling has occurred via the CONFIG0 PRE<1:0> register bits (see Equation 4-1). The analog portion includes the PGAs and the delta-sigma modulators.

EQUATION 4-1:

$$AMCLK = \frac{MCLK}{PRESCALE}$$

TABLE 4-1: MCP3912 OVERSAMPLING RATIO SETTINGS

CONFIG0 PRE<1:0>		Analog Master Clock Prescale
0	0	AMCLK = MCLK/1 (default)
0	1	AMCLK = MCLK/2
1	0	AMCLK = MCLK/4
1	1	AMCLK = MCLK/8

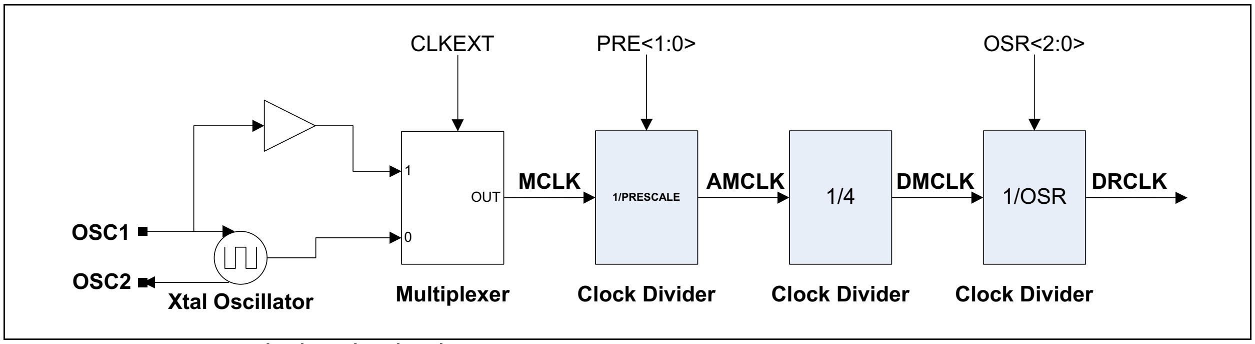


FIGURE 4-1: Clock Sub-Circuitry.

4.3 DMCLK – Digital Master Clock

This is the clock frequency that is present on the digital portion of the device after prescaling and division by four (Equation 4-2). This is also the sampling frequency, which is the rate at which the modulator outputs are refreshed. Each period of this clock corresponds to one sample and one modulator output. See Figure 4-1.

EQUATION 4-2:

$$DMCLK = \frac{AMCLK}{4} = \frac{MCLK}{4 \times PRESCALE}$$

4.4 DRCLK – Data Rate Clock

This is the output data rate, i.e., the rate at which the ADCs output new data. New data is signaled by a data ready pulse on the $\overline{DR}$ pin.

This data rate is depending on the OSR and the prescaler with the formula in Equation 4-3.

EQUATION 4-3:

$$DRCLK = \frac{DMCLK}{OSR} = \frac{AMCLK}{4 \times OSR} = \frac{MCLK}{4 \times OSR \times PRESCALE}$$

Since this is the output data rate, and because the decimation filter is a SINC (or notch) filter, there is a notch in the filter transfer function at each integer multiple of this rate.

Table 4-2 describes the various combinations of OSR and PRESCALE, and their associated AMCLK, DMCLK and DRCLK rates.

TABLE 4-2: DEVICE DATA RATES IN FUNCTION OF MCLK, OSR AND PRESCALE, MCLK = 4 MHZ

PRE<1:0>		OSR<2:0>			OSR	AMCLK	DMCLK	DRCLK	DRCLK (ksps)	SINAD (dB) Note 1	ENOB from SINAD (bits) Note 1
1	1	1	1	1	4096	MCLK/8	MCLK/32	MCLK/131072	.035	102.5	16.7
1	1	1	1	1	2048	MCLK/8	MCLK/32	MCLK/65536	.061	100	16.3
1	1	1	1	1	1024	MCLK/8	MCLK/32	MCLK/32768	.122	97	15.8
1	1	1	1	1	512	MCLK/8	MCLK/32	MCLK/16384	.244	96	15.6
1	1	0	1	1	256	MCLK/8	MCLK/32	MCLK/8192	0.488	94	15.3
1	1	0	1	0	128	MCLK/8	MCLK/32	MCLK/4096	0.976	90	14.7
1	1	0	0	1	64	MCLK/8	MCLK/32	MCLK/2048	1.95	83	13.5
1	1	0	0	0	32	MCLK/8	MCLK/32	MCLK/1024	3.9	70	11.3
1	0	1	1	1	4096	MCLK/4	MCLK/16	MCLK/65536	.061	102.5	16.7
1	0	1	1	1	2048	MCLK/4	MCLK/16	MCLK/32768	.122	100	16.3
1	0	1	1	1	1024	MCLK/4	MCLK/16	MCLK/16384	.244	97	15.8
1	0	1	1	1	512	MCLK/4	MCLK/16	MCLK/8192	.488	96	15.6
1	0	0	1	1	256	MCLK/4	MCLK/16	MCLK/4096	0.976	94	15.3
1	0	0	1	0	128	MCLK/4	MCLK/16	MCLK/2048	1.95	90	14.7
1	0	0	0	1	64	MCLK/4	MCLK/16	MCLK/1024	3.9	83	13.5
1	0	0	0	0	32	MCLK/4	MCLK/16	MCLK/512	7.8125	70	11.3
0	1	1	1	1	4096	MCLK/2	MCLK/8	MCLK/32768	.122	102.5	16.7
0	1	1	1	1	2048	MCLK/2	MCLK/8	MCLK/16384	.244	100	16.3
0	1	1	1	1	1024	MCLK/2	MCLK/8	MCLK/8192	.488	97	15.8
0	1	1	1	1	512	MCLK/2	MCLK/8	MCLK/4096	.976	96	15.6
0	1	0	1	1	256	MCLK/2	MCLK/8	MCLK/2048	1.95	94	15.3
0	1	0	1	0	128	MCLK/2	MCLK/8	MCLK/1024	3.9	90	14.7
0	1	0	0	1	64	MCLK/2	MCLK/8	MCLK/512	7.8125	83	13.5
0	1	0	0	0	32	MCLK/2	MCLK/8	MCLK/256	15.625	70	11.3
0	0	1	1	1	4096	MCLK	MCLK/4	MCLK/16384	.244	102.5	16.7
0	0	1	1	0	2048	MCLK	MCLK/4	MCLK/8192	.488	100	16.3
0	0	1	0	1	1024	MCLK	MCLK/4	MCLK/4096	.976	97	15.8
0	0	1	0	0	512	MCLK	MCLK/4	MCLK/2048	1.95	96	15.6
0	0	0	1	1	256	MCLK	MCLK/4	MCLK/1024	3.9	94	15.3
0	0	0	1	0	128	MCLK	MCLK/4	MCLK/512	7.8125	90	14.7
0	0	0	0	1	64	MCLK	MCLK/4	MCLK/256	15.625	83	13.5
0	0	0	0	0	32	MCLK	MCLK/4	MCLK/128	31.25	70	11.3

Note 1: For OSR = 32 and 64, DITHER = None. For OSR = 128 and higher, DITHER = Maximum. The SINAD values are given from GAIN = 1.

4.5 OSR – Oversampling Ratio

This is the ratio of the sampling frequency to the output data rate; OSR = DMCLK/DRCLK. The default OSR<2:0> is 256, or with MCLK = 4 MHz, PRESCALE = 1, AMCLK = 4 MHz, f_S = 1 MHz and f_D = 3.90625 ksps. The OSR<2:0> bits in Table 4-3 in the CONFIG0 register are used to change the oversampling ratio (OSR).

TABLE 4-3: MCP3912 OVERSAMPLING RATIO SETTINGS

OSR<2:0>			Oversampling Ratio OSR
0	0	0	32
0	0	1	64
0	1	0	128
0	1	1	256 (Default)
1	0	0	512
1	0	1	1024
1	1	0	2048
1	1	1	4096

4.6 Offset Error

This is the error induced by the ADC when the inputs are shorted together (V_{IN} = 0V). The specification incorporates both PGA and ADC offset contributions. This error varies with PGA and OSR settings. The offset is different on each channel and varies from chip-to-chip. The offset is specified in µV. The offset error can be digitally compensated independently on each channel through the OFFCAL_CHn registers with a 24-bit calibration word.

The offset on the MCP3912 has a low-temperature coefficient.

4.7 Gain Error

This is the error induced by the ADC on the slope of the transfer function. It is the deviation expressed in a percentage, compared to the ideal transfer function defined in Equation 5-3. The specification incorporates both PGA and ADC gain error contributions, but not the V_{REF} contribution (it is measured with an external V_{REF}).

This error varies with PGA and OSR settings. The gain error can be digitally compensated independently on each channel through the GAINCAL_CHn registers with a 24-bit calibration word.

The gain error on the MCP3912 has a low temperature coefficient.

4.8 Integral Nonlinearity Error

Integral nonlinearity error is the maximum deviation of an ADC transition point from the corresponding point of an ideal transfer function, with the offset and gain errors removed or with the end points equal to zero.

It is the maximum remaining error after calibration of offset and gain errors for a DC input signal.

4.9 Signal-to-Noise Ratio (SNR)

For the MCP3912 ADCs, the signal-to-noise ratio is a ratio of the output fundamental signal power to the noise power (not including the harmonics of the signal) when the input is a sine wave at a predetermined frequency (see Equation 4-4). It is measured in dB. Usually, only the maximum signal-to-noise ratio is specified. The SNR figure depends mainly on the OSR and DITHER settings of the device.

EQUATION 4-4: SIGNAL-TO-NOISE RATIO

$$SNR(dB) = 10\log\left(\frac{SignalPower}{NoisePower}\right)$$

4.10 Signal-To-Noise Ratio And Distortion (SINAD)

The most important Figure of Merit for analog performance of the ADCs present on the MCP3912 is the Signal-to-Noise And Distortion (SINAD) specification.

The Signal-to-Noise And Distortion ratio is similar to signal-to-noise ratio, with the exception that you must include the harmonic's power in the noise power calculation (see Equation 4-5). The SINAD specification depends mainly on the OSR and DITHER settings.

EQUATION 4-5: SINAD EQUATION

$$SINAD(dB) = 10\log\left(\frac{SignalPower}{Noise + HarmonicsPower}\right)$$

The calculated combination of SNR and THD per the following formula also yields SINAD (see Equation 4-6).

EQUATION 4-6: SINAD, THD AND SNR RELATIONSHIP

$$SINAD(dB) = 10\log\left[10^{\left(\frac{SNR}{10}\right)} + 10^{\left(\frac{-THD}{10}\right)}\right]$$

4.11 Total Harmonic Distortion (THD)

The total harmonic distortion is the ratio of the output harmonics power to the fundamental signal power for a sine wave input, and is defined in Equation 4-7.

EQUATION 4-7:

$$THD(dB) = 10\log\left(\frac{HarmonicsPower}{FundamentalPower}\right)$$

The THD calculation includes the first 35 harmonics for the MCP3912 specifications. The THD is usually measured only with respect to the ten first harmonics, which leads artificially to better figures. THD is sometimes expressed in a percentage. Equation 4-8 converts the THD in percentages.

EQUATION 4-8:

$$THD(\%) = 100 \times 10^{\frac{THD(dB)}{20}}$$

This specification depends mainly on the DITHER setting.

4.12 Spurious-Free Dynamic Range (SFDR)

Spurious-Free Dynamic Range, or SFDR, is the ratio between the output power of the fundamental and the highest spur in the frequency spectrum (see Equation 4-9). The spur frequency is not necessarily a harmonic of the fundamental, even though it is usually the case. This figure represents the dynamic range of the ADC when a full-scale signal is used at the input. This specification depends mainly on the DITHER setting.

EQUATION 4-9:

$$SFDR(dB) = 10\log\left(\frac{FundamentalPower}{HighestSpurPower}\right)$$

4.13 MCP3912 Delta-Sigma Architecture

The MCP3912 incorporates four delta-sigma ADCs with a multi-bit architecture. A delta-sigma ADC is an oversampling converter that incorporates a built-in modulator, which digitizes the quantity of charges integrated by the modulator loop (see Figure 5-1). The quantizer is the block that is performing the analog-to-digital conversion. The quantizer is typically 1-bit, or a simple comparator, which helps maintain the linearity performance of the ADC (the DAC structure is, in this case, inherently linear).

Multi-bit quantizers help to lower the quantization error (the error fed back in the loop can be very large with 1-bit quantizers) without changing the order of the modulator or the OSR, which leads to better SNR figures. However, typically, the linearity of such architectures is more difficult to achieve since the DAC linearity is as difficult to attain, and its linearity limits the THD of such ADCs.

The quantizer present in each ADC channel in the MCP3912 is a Flash ADC composed of four comparators arranged with equally spaced thresholds and a thermometer coding. The MCP3912 also includes proprietary five-level DAC architecture that is inherently linear for improved THD figures.

4.14 Idle Tones

A delta-sigma converter is an integrating converter. It also has a finite quantization step (LSB) that can be detected by its quantizer. A DC input voltage that is below the quantization step should only provide an all zeros result, since the input is not large enough to be detected. As an integrating device, any delta-sigma ADC will show idle tones. This means that the output will have spurs in the frequency content that depend on the ratio between quantization step voltage and the input voltage. These spurs are the result of the integrated sub-quantization step inputs that will eventually cross the quantization steps after a long enough integration. This will induce an AC frequency at the output of the ADC, and can be shown in the ADC output spectrum.

These idle tones are residues that are inherent to the quantization process and the fact that the converter is integrating at all times without being reset. They are residues of the finite resolution of the conversion process. They are very difficult to attenuate and they are heavily signal dependent. They can degrade the SFDR and THD of the converter, even for DC inputs. They can be localized in the baseband of the converter and are thus difficult to filter from the actual input signal.

For power metering applications, idle tones can be very disturbing, because energy can be detected even at the 50 or 60 Hz frequency, depending on the DC offset of the ADCs, while no power is really present at the inputs. The only practical way to suppress or attenuate the idle tones phenomenon is to apply dithering to the ADC. The amplitudes of the idle tones are a function of the order of the modulator, the OSR and the number of levels in the quantizer of the modulator. A higher order, a higher OSR or a higher number of levels for the quantizer will attenuate the amplitudes of the idle tones.

4.15 Dithering

In order to suppress or attenuate the idle tones present in any delta-sigma ADCs, dithering can be applied to the ADC. Dithering is the process of adding an error to the ADC feedback loop in order to “decorrelate” the outputs and “break” the idle tone’s behavior. Usually a random or pseudo-random generator adds an analog or digital error to the feedback loop of the delta-sigma ADC in order to ensure that no tonal behavior can happen at its outputs. This error is filtered by the feedback loop and typically has a zero average value so that the converter static transfer function is not disturbed by the dithering process. However, the dithering process slightly increases the noise floor (it adds noise to the part) while reducing its tonal behavior and thus improving SFDR and THD. The dithering process scrambles the idle tones into baseband white noise and ensures that dynamic specs (SNR, SINAD, THD, SFDR) are less signal dependent. The MCP3912 incorporates a proprietary dithering algorithm on all ADCs in order to remove idle tones and improve THD, which is crucial for power metering applications.

4.16 Crosstalk

Crosstalk is defined as the perturbation caused on one ADC channel by all the other ADC channels present in the chip. It is a measurement of the isolation between each channel present in the chip.

This measurement is a two-step procedure:

1. Measure one ADC input with no perturbation on the other ADC (ADC inputs shorted).
2. Measure the same ADC input with a perturbation sine wave signal on all the other ADCs at a certain predefined frequency.

Crosstalk is the ratio between the output power of the ADC when the perturbation is and is not present, divided by the power of the perturbation signal. A lower crosstalk value implies more independence and isolation between the channels.

The measurement of this signal is performed under the default conditions of MCLK = 4 MHz:

- GAIN = 1
- PRESCALE = 1
- OSR = 256
- MCLK = 4 MHz

Step 1 for CH0 Crosstalk Measurement:

- CH0+ = CH0- = AGND
- CHn+ = CHn- = AGND
  n comprised between 1 and 3

Step 2 for CH0 Crosstalk Measurement:

- CH0+ = CH0-=AGND
- CHn+ - CHn- = 1.2V_{P-P} @ 50/60 Hz (full-scale sine wave), n comprised between 1 and 3

The crosstalk for Channel 0 is then calculated with the formula in Equation 4-10.

EQUATION 4-10:

$$CTalk(dB) = 10log\left(\frac{\Delta CH0Power}{\Delta CHnPower}\right)$$

The crosstalk depends slightly on the position of the channels in the MCP3912 device. This dependency is shown in the Figure 2-32, where the inner channels show more crosstalk than the outer channels, since they are located closer to the perturbation sources. The outer channels have the preferred locations to minimize crosstalk.

4.17 PSRR

This is the ratio between a change in the power supply voltage and the ADC output codes. It measures the influence of the power supply voltage on the ADC outputs.

The PSRR specification can be DC (the power supply is taking multiple DC values) or AC (the power supply is a sine wave at a certain frequency with a certain common mode). In AC, the amplitude of the sine wave represents the change in the power supply. It is defined in Equation 4-11.

EQUATION 4-11:

$$PSRR(dB) = 20log\left(\frac{\Delta V_{OUT}}{\Delta AV_{DD}}\right)$$

Where: V_{OUT} is the equivalent input voltage that the output code translates to, with the ADC transfer function.

In the MCP3912 specification for DC PSRR, AV_{DD} varies from 2.7V to 3.6V, and for AC PSRR, a 50/60 Hz sine wave is chosen centered around 3.0V with a maximum 300 mV amplitude. The PSRR specification is measured with $AV_{DD} = DV_{DD}$.

4.18 CMRR

CMRR is the ratio between a change in the common-mode input voltage and the ADC output codes. It measures the influence of the common-mode input voltage on the ADC outputs.

The CMRR specification can be DC (the common-mode input voltage is taking multiple DC values) or AC (the common-mode input voltage is a sine wave at a certain frequency with a certain common mode). In AC, the amplitude of the sine wave represents the change in the power supply. It is defined in Equation 4-12.

EQUATION 4-12:

$$CMRR(dB) = 20log\left(\frac{\Delta V_{OUT}}{\Delta V_{CM}}\right)$$

Where: V_{CM} = (CHn+ + CHn-)/2 is the common-mode input voltage, and V_{OUT} is the equivalent input voltage that the output code translates to, with the ADC transfer function.

In the MCP3912 specification, VCM varies from -1V to +1V.

4.19 ADC Reset Mode

ADC Reset mode (also called Soft Reset mode) can only be entered through setting the RESET<3:0> bits high in the Configuration register. This mode is defined as the condition where the converters are active, but their output is forced to `0`.

The Flash ADC output of the corresponding channel will be reset to its default value (`0011`) in the MOD register.

The ADCs can immediately output meaningful codes after leaving Reset mode (and after the sinc filter settling time). This mode is both entered and exited through bit settings in the Configuration register.

Each converter can be placed in Soft Reset mode independently. The Configuration registers are not modified by the Soft Reset mode. A data ready pulse will not be generated by an ADC channel in Reset mode.

When an ADC exits ADC Reset mode, any phase delay present before Reset was entered will still be present. If one ADC was not in Reset, the ADC leaving Reset mode will automatically resynchronize the phase delay relative to the other ADC channel per the phase delay register block, and give data ready pulses accordingly.

If an ADC is placed in Reset mode while others are converting, it does not shut down the internal clock. When coming out of reset, it will be automatically resynchronized with the clock, which did not stop during Reset.

If all ADCs are in Soft Reset mode, the clock is no longer distributed to the digital core for low-power operation. Once any of the ADCs are back to normal operation, the clock is automatically distributed again.

However, when the four channels are in Soft Reset mode, the input structure is still clocking if MCLK is applied in order to properly bias the inputs so that no leakage current is observed. If MCLK is not applied, large analog input leakage currents can be observed for highly negative input voltages (typically below -0.6V referred to A_{GND}).

4.20 Hard Reset Mode ($\overline{\text{RESET}}$ = `0`)

This mode is only available during a POR or when the $\overline{\text{RESET}}$ pin is pulled logic low. The $\overline{\text{RESET}}$ pin logic-low state places the device in Hard Reset mode. In this mode, all internal registers are reset to their default state.

The DC biases for the analog blocks are still active, i.e., the MCP3912 is ready to convert. However, this pin clears all conversion data in the ADCs. The comparators' outputs of all ADCs are forced to their Reset state (`0011`). The SINC filters are all reset, as well as their double output buffers. The Hard Reset mode requires a minimum pulse low time (see **Section 1.0 "Electrical Characteristics"**). During a Hard Reset, no communication with the part is possible. The digital interface is maintained in a Reset state.

During this state, the clock MCLK can be applied to the part in order to properly bias the input structures of all channels. If not applied, large analog input leakage currents can be observed for highly negative input signals and, after removing the Hard Reset state, a certain start-up time is necessary to bias the input structure properly. During this delay, the ADC conversions can be inaccurate.

4.21 ADC Shutdown Mode

ADC Shutdown mode is defined as a state where the converters and their biases are off, consuming only leakage current. When one of the SHUTDOWN<3:0> bits is reset to '`0`', the analog biases of the corresponding channel will be enabled, as well as the clock and the digital circuitry. The ADC of the corresponding channel will give a data ready after the SINC filter settling time has occurred. However, since the analog biases are not completely settled at the beginning of the conversion, the sampling may not be accurate during about 1 ms (corresponding to the settling time of the biasing in worst-case conditions). In order to ensure accuracy, the data ready pulse within the delay of 1 ms + settling time of the SINC filter should be discarded.

Each converter can be placed in Shutdown mode independently. The configuration registers are not modified by the Shutdown mode. This mode is only available through programming the SHUTDOWN<3:0> bits of the CONFIG1 register.

The output data is flushed to all zeros while in ADC Shutdown mode. No data ready pulses are generated by any ADC while in ADC Shutdown mode.

When an ADC exits ADC Shutdown mode, any phase delay present before shutdown was entered will still be present. If one ADC was not in Shutdown, the ADC leaving Shutdown mode will automatically resynchronize the phase delay relative to the other ADC channel per the phase delay register block and give data ready pulses accordingly.

If an ADC is placed in Shutdown mode while others are converting, it does not shut down the internal clock. When coming back out of Shutdown mode, it will automatically be resynchronized with the clock that did not stop during reset.

If all ADCs are in ADC Shutdown mode, the clock is not distributed to the input structure or to the digital core for low-power operation. This can potentially cause high analog input leakage currents at the analog inputs if the input voltage is highly negative (typically below -0.6V referred to A_{GND}). Once either of the ADCs is back to normal operation, the clock is automatically distributed again.

4.22 Full Shutdown Mode

The lowest power consumption can be achieved when SHUTDOWN<3:0> = 1111,
VREFEXT = CLKEXT = 1. This mode is called Full Shutdown mode, and no analog circuitry is enabled. In this mode, both AV_{DD} and DV_{DD} POR monitoring are also disabled and no clock is propagated throughout the chip. All ADCs are in Shutdown mode, and the internal voltage reference is disabled. This mode does not reset the writable part of the register map to its default values.

The clock is no longer distributed to the input structure as well. This can potentially cause high analog input leakage currents at the analog inputs if the input voltage is highly negative (typically below -0.6V referred to A_{GND}).

The only circuit that remains active is the SPI interface, but this circuit does not induce any static power consumption. If SCK is idle, the only current consumption comes from the leakage currents induced by the transistors.

This mode can be used to power-down the chip completely and avoid power consumption when there is no data to convert at the analog inputs. Any SCK or MCLK edge occurring while in this mode will induce dynamic power consumption.

Once any of the SHUTDOWN<3:0>, CLKEXT and VREFEXT bits return to ‘0’, the two POR monitoring blocks are operational and AV_{DD} and DV_{DD} monitoring can take place.

4.23 Measurement Error

The measurement error specification is typically used in power meter applications. This specification is a measurement of the linearity of the active energy of a given power meter across its dynamic range.

For this measurement, the goal is to measure the active energy of one phase when the voltage Root Mean Square (RMS) value is fixed and the current RMS value is sweeping across the dynamic range specified by the meter. The measurement error is the nonlinearity error of the energy power across the current dynamic range. It is expressed as a percentage. Equation 4-13 shows the formula that calculates the measurement error:

EQUATION 4-13:

$$Measurement\ Error(I_{RMS}) = \frac{Measured\ Active\ Energy - Active\ Energy\ present\ at\ inputs}{Active\ Energy\ present\ at\ inputs} \times 100\%$$

In the present device, the calculation of the active energy is done externally as a post-processing step that typically happens in the microcontroller, considering, for example, the even channels as current channels and the odd channels as voltage channels. The odd channels (voltages) are fed with a full-scale sine wave at 600 mV peak, and are configured with GAIN = 1 and DITHER = Maximum. To obtain the active energy measurement error graphs, the even channels are fed with sine waves with amplitudes that vary from 600 mV peak to 60 µV peak, representing a 10000:1 dynamic range. The offset is removed on both current and voltage channels, and the channels are multiplied together to give instantaneous power. The active energy is calculated by multiplying the current and voltage channel, and averaging the results of this power during 20 seconds to extract the active energy. The sampling frequency is chosen as a multiple integer of line frequency (coherent sampling). Therefore, the calculation does not take into account any residue coming from bad synchronization.

The measurement error is a function of I_{RMS} and varies with the OSR, averaging time and MCLK frequency, and is tightly coupled with the noise and linearity specifications. The measurement error is a function of the linearity and THD of the ADCs, while the standard deviation of the measurement error is a function of the noise specification of the ADCs. Overall, the low THD specification enables low measurement error on a very large dynamic range (e.g. 10,000:1). A low noise and high SNR specification enables the decreasing of the measurement time and, therefore, the calibration time, to obtain a reliable measurement error specification.

Figure 2-5 shows the typical measurement error curves obtained with the samples acquired by the MCP3912, using the default settings with a 1-point and 2-point calibration. These calibrations are detailed in **Section 7.0 “Basic Application Recommendations”**.

NOTES:

5.0 DEVICE OVERVIEW

5.1 Analog Inputs (CHn+/-)

The MCP3912 analog inputs can be connected directly to current and voltage transducers (such as shunts, current transformers, or Rogowski coils). Each input pin is protected by specialized ESD structures that allow bipolar ±2V continuous voltage, with respect to A_{GND}, to be present at their inputs without the risk of permanent damage.

All channels have fully differential voltage inputs for better noise performance. The absolute voltage at each pin relative to A_{GND} should be maintained in the ±1V range during operation in order to ensure the specified ADC accuracy. The common-mode signals should be adapted to respect both the previous conditions and the differential input voltage range. For best performance, the common-mode signals should be maintained to A_{GND}.

Note: If the analog inputs are held to a potential of -0.6 to -1V for extended periods of time, MCLK must be present inside the device in order to avoid large leakage currents at the analog inputs. This is true even during Hard Reset mode or the Soft Reset of all ADCs. However, during the Shutdown mode of all the ADCs or POR state, the clock is not distributed inside the circuit. During these states, it is recommended to keep the analog input voltages above -0.6V referred to A_{GND} to avoid high analog input leakage currents.

5.2 Programmable Gain Amplifiers (PGA)

The four Programmable Gain Amplifiers (PGAs) reside at the front end of each delta-sigma ADC. They have two functions: translate the common-mode voltage of the input from A_{GND} to an internal level between A_{GND} and AV_{DD} and amplify the input differential signal. The translation of the common-mode voltage does not change the differential signal, but recenters the common-mode so that the input signal can be properly amplified.

The PGA block can be used to amplify very low signals, but the differential input range of the delta-sigma modulator must not be exceeded. The PGA on each channel is independent and is controlled by the PGA_CHn<2:0> bits in the GAIN register. Table 5-1 displays the gain settings for the PGA.

TABLE 5-1: PGA CONFIGURATION SETTING

Gain PGA_CHn<2:0>			Gain (V/V)	Gain (dB)	V_{IN} = (CHn+) – (CHn-) Differential Input Range (V)
0	0	0	1	0	±0.6
0	0	1	2	6	±0.3
0	1	0	4	12	±0.15
0	1	1	8	18	±0.075
1	0	0	16	24	±0.0375
1	0	1	32	30	±0.01875

Note: The two undefined settings are G = 1. This table is defined with V_{REF} = 1.2V.

5.3 Delta-Sigma Modulator

5.3.1 ARCHITECTURE

All ADCs are identical in the MCP3912, and they include a proprietary second-order modulator with a multi-bit 5-level DAC architecture (see Figure 5-1). The quantizer is a Flash ADC composed of four comparators with equally spaced thresholds and a thermometer output coding. The proprietary 5-level architecture ensures minimum quantization noise at the outputs of the modulators without disturbing linearity or inducing additional distortion. The sampling frequency is DMCLK (typically 1 MHz with MCLK = 4 MHz) so the modulators are refreshed at a DMCLK rate.

Figure 5-1 represents a simplified block diagram of the delta-sigma ADC present on MCP3912.

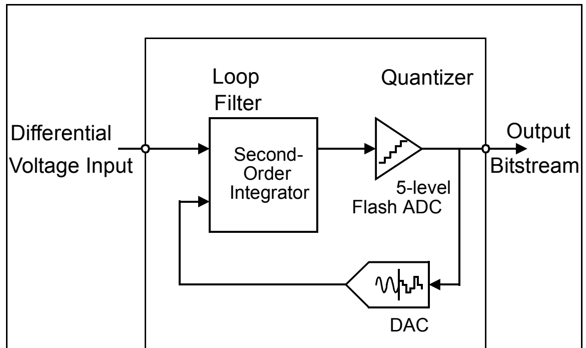


FIGURE 5-1: Simplified Delta-Sigma ADC Block Diagram.

5.3.2 MODULATOR INPUT RANGE AND SATURATION POINT

For a specified voltage reference value of 1.2V, the specified differential input range is ±600 mV. The input range is proportional to V_{REF} and scales according to the V_{REF} voltage. This range ensures the stability of the modulator over amplitude and frequency. Outside of this range, the modulator is still functional; however, its stability is no longer ensured and therefore it is not recommended to exceed this limit. The saturation point for the modulator is $V_{REF}/1.5$, since the transfer function of the ADC includes a gain of 1.5 by default (independent from the PGA setting). See **Section 5.5 "ADC Output Coding"**).

5.3.3 BOOST SETTINGS

The delta-sigma modulators include a programmable biasing circuit in order to further adjust the power consumption to the sampling speed applied through the MCLK. This can be programmed through the BOOST<1:0> bits, which are applied to all channels simultaneously.

The maximum achievable analog master clock speed (AMCLK), the maximum sampling frequency (DMCLK) and the maximum achievable data rate (DRCLK), highly depend on BOOST<1:0> and PGA_CHn<2:0> settings. Table 5-2 specifies the maximum AMCLK possible to keep optimal accuracy in the function of BOOST<1:0> and PGA_CHn<2:0> settings.

TABLE 5-2: MAXIMUM AMCLK LIMITS AS A FUNCTION OF BOOST AND PGA GAIN

Conditions		V_{DD} = 3.0V to 3.6V, T_A from -40°C to +125°C		V_{DD} = 2.7V to 3.6V, T_A from -40°C to +125°C	
Boost	**Gain**	**Maximum AMCLK (MHz) (SINAD within -3 dB from its maximum)**	**Maximum AMCLK (MHz) (SINAD within -5 dB from its maximum)**	**Maximum AMCLK (MHz) (SINAD within -3 dB from its maximum)**	**Maximum AMCLK (MHz) (SINAD within -5 dB from its maximum)**
0.5x	1	4	4	4	4
0.66x	1	6.4	7.3	6.4	7.3
1x	1	11.4	11.4	10.6	10.6
2x	1	16	16	16	16
0.5x	2	4	4	4	4
0.66x	2	6.4	7.3	6.4	7.3
1x	2	11.4	11.4	10.6	10.6
2x	2	16	16	13.3	14.5
0.5x	4	2.9	2.9	2.9	2.9
0.66x	4	6.4	6.4	6.4	6.4
1x	4	10.7	10.7	9.4	10.7
2x	4	16	16	16	16
0.5x	8	2.9	4	2.9	4
0.66x	8	7.3	8	6.4	7.3
1x	8	11.4	12.3	8	8.9
2x	8	16	16	10	11.4
0.5x	16	2.9	2.9	2.9	2.9
0.66x	16	6.4	7.3	6.4	7.3
1x	16	11.4	11.4	9.4	10.6
2x	16	13.3	16	8.9	11.4
0.5x	32	2.9	2.9	2.9	2.9
0.66x	32	7.3	7.3	7.3	7.3
1x	32	10.6	12.3	9.4	10,6
2x	32	13.3	16	10	11.4

5.3.4 DITHER SETTINGS

All modulators include a dithering algorithm that can be enabled through the DITHER<1:0> bits in the Configuration register. This dithering process improves THD and SFDR (for high OSR settings), while slightly increasing the noise floor of the ADCs. For power metering applications and applications that are distortion sensitive, it is recommended to keep DITHER at maximum settings for best THD and SFDR performance. In the case of power metering applications, THD and SFDR are critical specifications. Optimizing SNR (noise floor) is not problematic due to the large averaging factor at the output of the ADCs. Therefore, even for low OSR settings, the dithering algorithm will show a positive impact on the performance of the application.

5.4 $SINC^3$ + $SINC^1$ Filter

The decimation filter present in all channels of the MCP3912 is a cascade of two sinc filters ($sinc^3$+$sinc^1$): a third-order sinc filter with a decimation ratio of OSR_3, followed by a first-order sinc filter with a decimation ratio of OSR_1 (moving average of OSR_1 values). Figure 5-2 represents the decimation filter architecture.

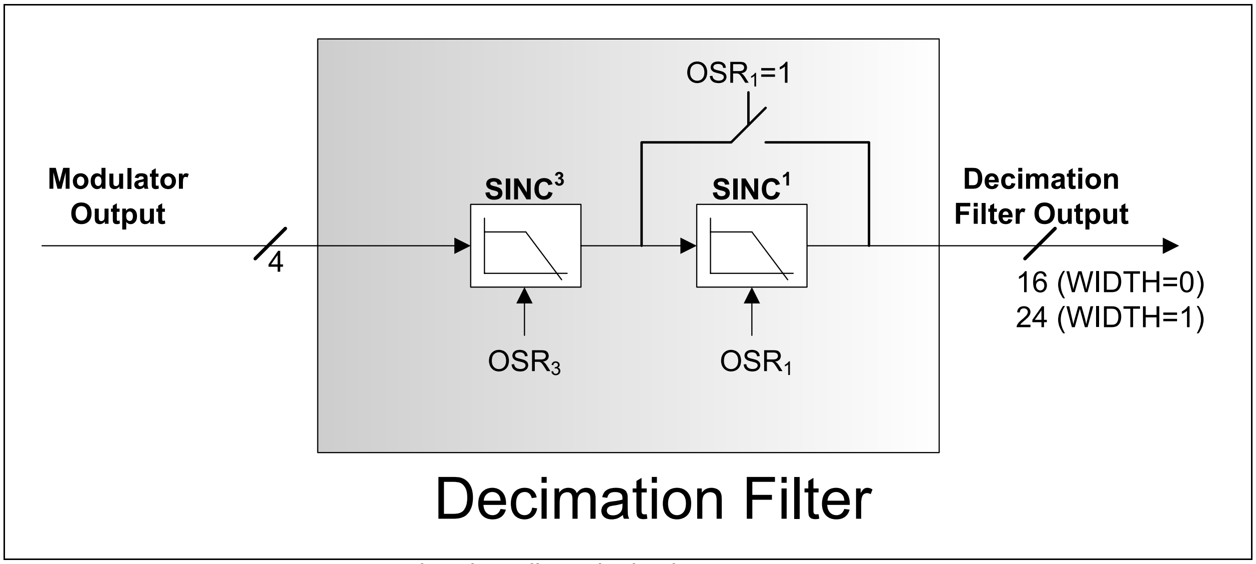


FIGURE 5-2: *MCP3912 Decimation Filter Block Diagram.*

Equation 5-1 calculates the filter z-domain transfer function.

EQUATION 5-1: SINC FILTER TRANSFER FUNCTION

$$H(z) = \frac{\left(1 - z^{-OSR_3}\right)^3}{\left(OSR_3(1 - z^{-1})\right)^3} \times \frac{\left(1 - z^{-OSR_1 \times OSR_3}\right)}{OSR_1 \times \left(1 - z^{-OSR_3}\right)}$$

$$Where\ z = EXP((2\pi \cdot j \cdot f_{in}) / (DMCLK))$$

Equation 5-2 calculates the settling time of the ADC as a function of DMCLK periods.

EQUATION 5-2:

$$SettlingTime(DMCLKperiods) = 3 \times OSR_3 + (OSR_1 - 1) \times OSR_3$$

The $SINC^1$ filter following the $SINC^3$ filter is only enabled for the high OSR settings (OSR > 512). This $SINC^1$ filter provides additional rejection at a low cost with little modification to the -3 dB bandwidth. The resolution (number of possible output codes expressed in powers of two or in bits) of the digital filter is 24-bit maximum for any OSR and data format choice. The resolution depends only on the OSR<2:0> settings in the CONFIG0 register per the Table 5-3. Once the OSR is chosen, the resolution is fixed and the output code respects the data format defined by the WIDTH_DATA<1:0> setting in the STATUSCOM register (see **Section 5.5 "ADC Output Coding"**).

The gain of the transfer function of this filter is one at each multiple of DMCLK (typically 1 MHz), so a proper anti-aliasing filter must be placed at the inputs. This will attenuate the frequency content around DMCLK and keep the desired accuracy over the baseband of the converter. This anti-aliasing filter can be a simple, first-order RC network, with a sufficiently low time constant to generate high rejection at the DMCLK frequency.

Any unsettled data is automatically discarded to avoid data corruption. Each data ready pulse corresponds to fully settled data at the output of the decimation filter. The first data available at the output of the decimation filter is present after the complete settling time of the filter (see Table 5-3). After the first data has been processed, the delay between two data ready pulses coming from the same ADC channel is one DRCLK period. The data stream from input to output is delayed by an amount equal to the settling time of the filter (which is the group delay of the filter).

The achievable resolution, the -3 dB bandwidth and the settling time at the output of the decimation filter (the output of the ADC), is dependent on the OSR of each sinc filter and is summarized in Table 5-3.

TABLE 5-3: OVERSAMPLING RATIO AND SINC FILTER SETTLING TIME

OSR<2:0>			OSR_3	OSR_1	Total OSR	Resolution in Bits (No Missing Code)	Settling Time	-3 dB Bandwidth
0	0	0	32	1	32	17	96/DMCLK	0.26*DRCLK
0	0	1	64	1	64	20	192/DMCLK	0.26*DRCLK
0	1	0	128	1	128	23	384/DMCLK	0.26*DRCLK
0	1	1	256	1	256	24	768/DMCLK	0.26*DRCLK
1	0	0	512	1	512	24	1536/DMCLK	0.26*DRCLK
1	0	1	512	2	1024	24	2048/DMCLK	0.37*DRCLK
1	1	0	512	4	2048	24	3072/DMCLK	0.42*DRCLK
1	1	1	512	8	4096	24	5120/DMCLK	0.43*DRCLK

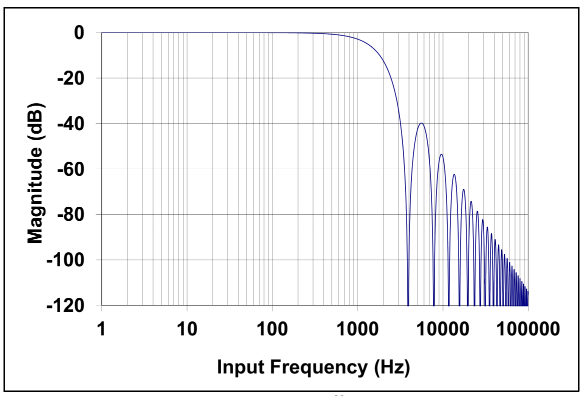


FIGURE 5-3: *SINC Filter Frequency Response, OSR = 256, MCLK = 4 MHz, PRE<1:0> = `00`.*

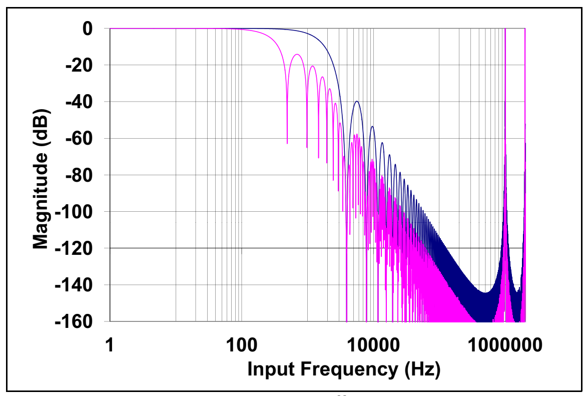


FIGURE 5-4: *SINC Filter Frequency Response, OSR = 4096 (in pink), OSR = 512 (in blue), MCLK = 4 MHz, PRE<1:0> = `00`.*

5.5 ADC Output Coding

The second-order modulator, $SINC^3+SINC^1$ filter, PGA, V_{REF} and the analog input structure all work together to produce the device transfer function for the analog-to-digital conversion (see Equation 5-3).

Channel data is calculated on 24-bit (23-bit plus sign) and coded in two's complement format, MSB first. The output format can then be modified by the WIDTH_DATA<1:0> settings in the STATUSCOM register to allow 16-/24-/32-bit format compatibility (see **Section 8.5 "STATUSCOM Register – Status and Communication Register"** for more information).

In case of positive saturation (CHn+ – CHn- > V_{REF}/1.5), the output is locked to 7FFFFF for 24-bit mode. In case of negative saturation (CHn+ - CHn- < -V_{REF}/1.5), the output code is locked to 800000 for 24-bit mode.

Equation 5-3 is only true for DC inputs. For AC inputs, this transfer function needs to be multiplied by the transfer function of the $SINC^3+SINC^1$ filter (see Equation 5-1 and Equation 5-3).

EQUATION 5-3:

$$DATA\_CHn = \left(\frac{(CH_{n+} - CH_{n-})}{V_{REF+} - V_{REF-}}\right) \times 8{,}388{,}608 \times G \times 1.5$$

For 24-bit Mode, WIDTH_Data<1:0> = 01(Default)

For other than the default 24-bit data formats, Equation 5-3 should be multiplied by a scaling factor depending on the data format used (defined by WIDTH_DATA<1:0>). The data format and associated scaling factors are given in Figure 5-5.

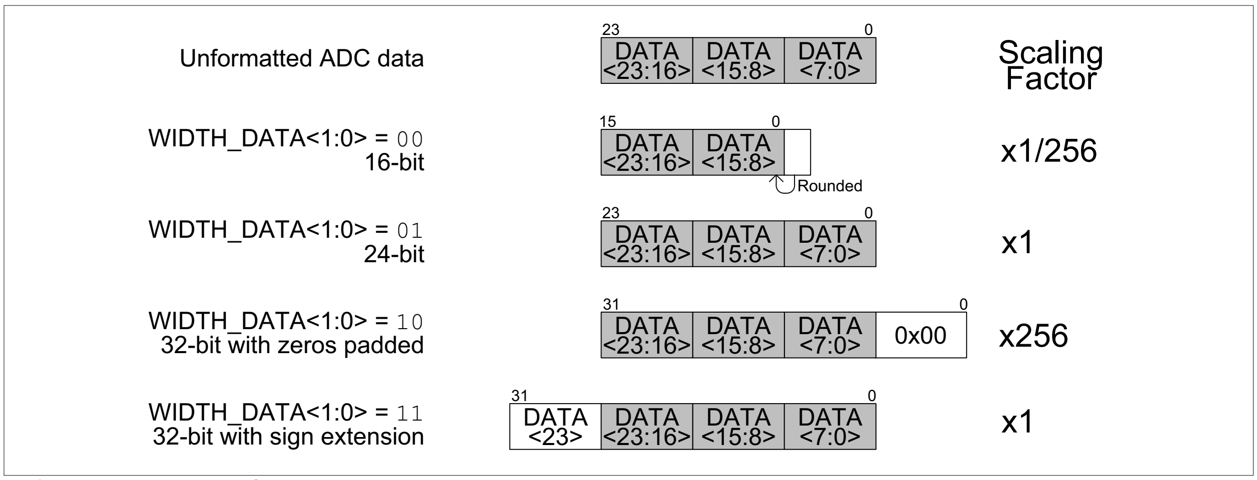


FIGURE 5-5: *Output Data Formats.*

The ADC resolution is a function of the OSR (**Section 5.4 "SINC3 + SINC1 Filter"**). The resolution is the same for all channels. No matter what the resolution is, the ADC output data is always calculated in 24-bit words, with added zeros at the end if the OSR is not large enough to produce 24-bit resolution (left justification).

TABLE 5-4: OSR = 256 (AND HIGHER) OUTPUT CODE EXAMPLES

ADC Output Code (MSB First)	Hexadecimal	Decimal, 24-bit Resolution
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0x7FFFFF	+ 8,388,607
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	0x7FFFFE	+ 8,388,606
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x000000	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0xFFFFFF	-1
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	0x800001	- 8,388,607
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x800000	- 8,388,608

TABLE 5-5: OSR = 128 OUTPUT CODE EXAMPLES

ADC Output Code (MSB First)	Hexadecimal	Decimal, 23-bit Resolution
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	0x7FFFFE	+ 4,194,303
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 0 0	0x7FFFFC	+ 4,194,302
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x000000	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	0xFFFFFE	-1
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	0x800002	- 4,194,303
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x800000	- 4,194,304

TABLE 5-6: OSR = 64 OUTPUT CODE EXAMPLES

ADC Output code (MSB First)	Hexadecimal	Decimal, 20-bit resolution
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0	0x7FFFF0	+ 524, 287
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0	0x7FFFE0	+ 524, 286
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x000000	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0	0xFFFFF0	-1
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0	0x800010	- 524,287
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x800000	- 524, 288

TABLE 5-7: OSR = 32 OUTPUT CODE EXAMPLES

ADC Output code (MSB First)	Hexadecimal	Decimal, 17-bit resolution
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0	0x7FFF80	+ 65, 535
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0	0x7FFF00	+ 65, 534
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x000000	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0	0xFFFF80	-1
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0	0x800080	- 65,535
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x800000	- 65, 536

5.6 Voltage Reference

5.6.1 INTERNAL VOLTAGE REFERENCE

The MCP3912 contains an internal voltage reference source specially designed to minimize drift over temperature. In order to enable the internal voltage reference, the VREFEXT bit in the Configuration register must be set to '0' (default mode). This internal V_{REF} supplies reference voltage to all channels. The typical value of this voltage reference is 1.2V ±2%. The internal reference has a very low typical temperature coefficient of ±9 ppm/°C, allowing the output to have minimal variation with respect to temperature, since they are proportional to ($1/V_{REF}$).

The noise of the internal voltage reference is low enough not to significantly degrade the SNR of the ADC, if compared to a precision external low-noise voltage reference. The output pin for the internal voltage reference is REFIN+/OUT.

If the voltage reference is only used as an internal V_{REF}, adding bypass capacitance on REFIN+/OUT is not necessary for keeping ADC accuracy, but a minimal 0.1 µF ceramic capacitance can be connected to avoid EMI/EMC susceptibility issues due to the antenna created by the REFIN+/OUT pin, if left floating.

The bypass capacitors also help applications where the voltage reference output is connected to other circuits. In this case, additional buffering may be needed since the output drive capability of this output is low.

Adding too much capacitance on the REFIN+/OUT pin may slightly degrade the THD performance of the ADCs.

5.6.2 DIFFERENTIAL EXTERNAL VOLTAGE INPUTS

When the VREFEXT bit is set to '1', the two reference pins (REFIN+/OUT, REFIN-) become a differential voltage reference input. The voltage at the REFIN+/OUT is noted $V_{REF}+$, and the voltage at the REFIN- pin is noted $V_{REF}-$. The differential voltage input value is shown in Equation 5-4.

EQUATION 5-4:

$$V_{REF} = V_{REF}+ - V_{REF}-$$

The specified V_{REF} range is from 1.1V to 1.3V. The REFIN- pin voltage ($V_{REF}-$) should be limited to ±0.1V, with respect to A_{GND}. Typically, for single-ended reference applications, the REFIN- pin should be directly connected to A_{GND}, with its own separate track to avoid any spike due to switching noise.

These buffers are injecting a certain quantity of 1/f noise into the system. This noise can be modulated with the incoming input signals and can limit the SNR at very high OSR (OSR>256). To overcome this limitation, these buffers include an auto-zeroing algorithm that greatly diminishes their 1/f noise as well as their offset, so that the SNR of the system is not limited by this noise component, even at maximum OSR. This auto-zeroing algorithm is performed synchronously with the MCLK coming to the device.

5.6.3 TEMPERATURE COMPENSATION (VREFCAL<7:0>)

The internal voltage reference consists of a proprietary circuit and algorithm to compensate first-order and second-order temperature coefficients (tempco). The compensation enables very low temperature coefficients (typically 9 ppm/°C) on the entire range of temperatures, from -40°C to +125°C. This temperature coefficient varies from part to part.

This temperature coefficient can be adjusted on each part through the VREFCAL<7:0> bits present in the CONFIG0 register (bits 7 to 0). These register settings are only for advanced users. VREFCAL<7:0> should not be modified unless the user wants to calibrate the temperature coefficient of the whole system or application. The default value of this register is set to 0x50. The default value (0x50) was chosen to optimize the standard deviation of the tempco across process variation. The value can be slightly improved to around 7 ppm/°C if the VREFCAL<7:0> is written at 0x42, but this setting degrades the standard deviation of the V_{REF} tempco.The typical variation of the temperature coefficient of the internal voltage reference with respect to the VREFCAL register code is shown in Figure 5-6. Modifying the value stored in the VREFCAL<7:0> bits may also vary the voltage reference in addition to the temperature coefficient.

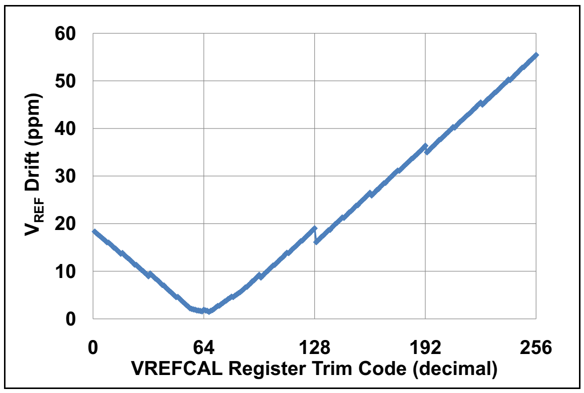


FIGURE 5-6: V_{REF} Tempco vs. V_{REFCAL} Trim Code Chart.

5.6.4 VOLTAGE REFERENCE BUFFERS

Each channel includes a voltage reference buffer tied to the REFIN+/OUT pin, which allows the internal capacitors to properly charge with the voltage reference signals, even in the case of an external voltage reference connection with weak load regulation specifications. This ensures the correct amount of current is sourced to each channel to guarantee their accuracy specifications, and diminishes the constraints on the voltage reference load regulation.

5.7 Power-on Reset

The MCP3912 contains an internal POR circuit that monitors both analog and digital supply voltages during operation. The typical threshold for a power-up event detection is 2.0V ±10% and a typical start-up time (t_{POR}) of 50 µs. The POR circuit has a built-in hysteresis for improved transient spike immunity that has a typical value of 200 mV. Proper decoupling capacitors (0.1 µF in parallel with 10 µF) should be mounted as close as possible to the AV_{DD} and DV_{DD} pins, providing additional transient immunity.

Figure 5-7 illustrates the different conditions at a power-up and a power-down event in typical conditions. All internal DC biases are not settled until at least 1 ms in worst case conditions after system POR. Any data-ready pulse occurring within 1 ms plus the SINC filter settling time after system reset should be ignored to ensure proper accuracy. After POR, data ready pulses are present at the pin with all the default conditions in the Configuration registers.

Both AV_{DD} and DV_{DD} are monitored, so either power supply can sequence first.

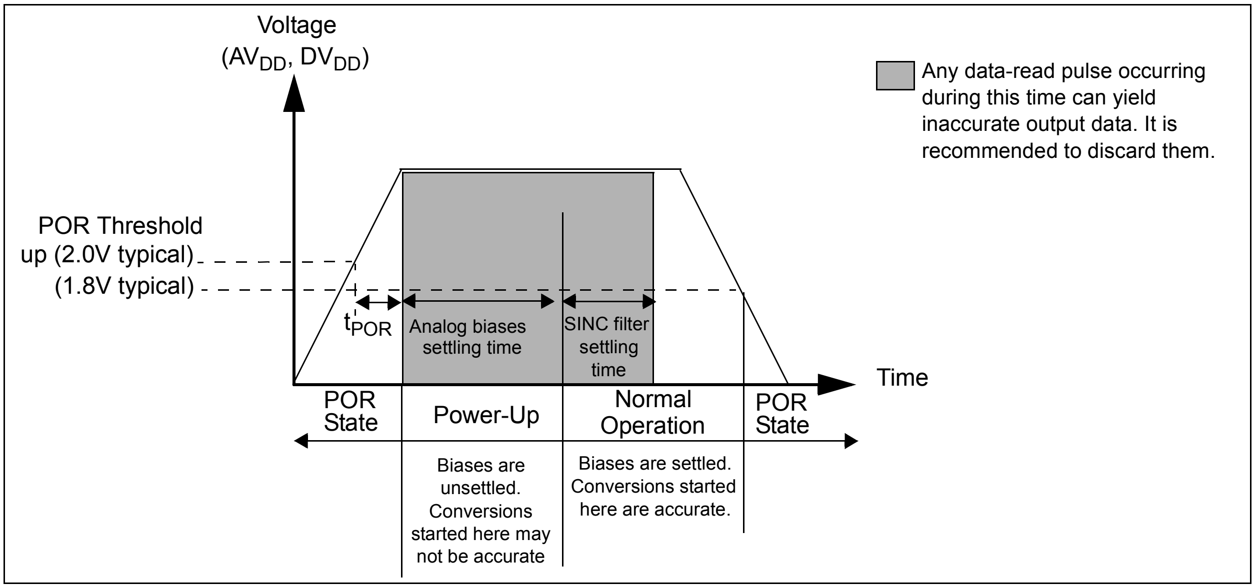


FIGURE 5-7: Power-On Reset Operation.

5.8 Hard Reset Effect On Delta-Sigma Modulator/SINC Filter

When the $\overline{RESET}$ pin is logic low, all ADCs will be in Reset and output code 0x000000h. The $\overline{RESET}$ pin performs a hard reset (DC biases are still on, the part is ready to convert) and clears all charges contained in the delta-sigma modulators. The comparator's output is '`0011`' for each ADC.

The SINC filters are all reset, as well as their double output buffers. This pin is independent of the serial interface. It brings all the registers to the default state. When $\overline{RESET}$ is logic low, any write with the SPI interface will be disabled and will have no effect. All output pins (SDO, $\overline{DR}$) are high-impedance.

If an external clock (MCLK) is applied, the input structure is enabled and is properly biasing the substrate of the input transistors. In this case, the leakage current on the analog inputs is low if the analog input voltages are kept between -1V and +1V.

If MCLK is not applied when in Reset mode, the leakage can be high if the analog inputs are below -0.6V, as referred to A_{GND}.

5.9 Phase Delay Block

The MCP3912 incorporates a phase delay generator which ensures that each pair of ADCs (CH0/1, CH2/3) are converting the inputs with a fixed delay between them. The four ADCs are synchronously sampling, but the averaging of modulator outputs is delayed so that the SINC filter outputs (thus the ADC outputs) show a fixed phase delay as determined by the PHASE register setting. The odd channels (CH1,3) are the reference channels for the phase delays of each pair, and set the time reference. Typically, these channels can be the voltage channels for a polyphase energy metering application. These odd channels are synchronous at all times, so they become ready and output a data ready pulse at the same time. The even channels (CH0/2) are delayed, compared to the time reference (CH1/3), by a fixed amount of time defined for each pair channel in the PHASE register.

The PHASE register is split into two 12-bit banks that represent the delay between each pair of channels. The equivalence is defined in Table 5-8. Each phase value (PHASEA/B) represents the delay of the even channel with respect to the associated odd channel with an 11-bit plus sign, MSB-first two's complement code. This code indicates how many DMCLK periods there are between each channel in the pair. (see Equation 5-5). Since the odd channels are the time reference, when PHASEX<11:0> is positive, the even channel of the pair is lagging and the odd channel is leading. When PHASEX<11:0> is negative, the even channel of the pair is leading and the odd channel is lagging.

TABLE 5-8: PHASE DELAYS EQUIVALENCE

Pair of channels	Phase Bank	Register Map Position
CH1/CH0	PHASEA<11:0>	PHASE<11:0>
CH3/CH2	PHASEB<11:0>	PHASE<23:12>

EQUATION 5-5:

$$Total\ Delay = \frac{PHASEX\langle 11:0 \rangle\ Decimal\ Code}{DMCLK}$$

where: X = A/B

The timing resolution of the phase delay is 1/DMCLK or 1 µs in the default configuration with MCLK = 4 MHz.

Given the definition of DMCLK, the phase delay is affected by a change in the prescaler settings (PRE<1:0>) and the MCLK frequency.

The data ready signals are affected by the phase delay settings. Typically, the time difference between the data ready pulses of odd and even channels is equal to the associated phase delay setting.

Each ADC conversion start and, therefore, each data ready pulse is delayed by a timing of OSR/2 x DMCLK periods (equal to half a DRCLK period). This timing allows for the odd channel's data ready signals to be located at a fixed time reference (OSR/2 x DMCLK periods from the reset) while the even channel can be leading or lagging around this time reference with the corresponding PHASEX<11:0> delay value.

> **Note:** For a detailed explanation of the Data Ready pin ($\overline{DR}$) with phase delay, see **Section 5.11 "Data Ready Status Bits"**.

5.9.1 PHASE DELAY LIMITS

The limits of the phase delays are determined by the OSR settings: the phase delays can only go from -OSR/2 to +OSR/2-1 DMCLK periods.

If larger delays between the two channels are needed, they can be implemented externally to the chip with an MCU. A FIFO in the MCU can save incoming data from the leading channel for a number N of DRCLK clocks. In this case, DRCLK would represent the coarse timing resolution, and DMCLK the fine timing resolution. The total delay will then be equal to:

EQUATION 5-6:

$$Total\ Delay = N/DRCLK + PHASE/DMCLK$$

> **Note:** Rewriting the PHASE registers with the same value automatically resets and restarts all ADCs.

The Phase delay registers can be programmed once with the OSR = 4096 setting, and will adjust the OSR automatically afterwards without the need to change the value of the phase registers.

- **OSR = 4096**: The delay can go from -2048 to +2047. PHASEX<11> is the sign bit. PHASEX<10> is the MSB and PHASEX<0> the LSB.
- **OSR = 2048**: The delay can go from -1024 to +1023. PHASEX<10> is the sign bit. PHASEX<9> is the MSB and PHASEX<0> the LSB.
- **OSR = 1024**: The delay can go from -512 to +511. PHASEX<9> is the sign bit. PHASEX<8> is the MSB and PHASEX<0> the LSB.
- **OSR = 512**: The delay can go from -256 to +255 PHASEX<8> is the sign bit. PHASEX<7> is the MSB and PHASEX<0> the LSB.
- **OSR = 256**: The delay can go from -128 to +127. PHASEX<7> is the sign bit. PHASEX<6> is the MSB and PHASEX<0> the LSB.
- **OSR = 128:** The delay can go from -64 to +63. PHASEX<6> is the sign bit. PHASEX<5> is the MSB and PHASEX<0> the LSB.
- **OSR = 64:** The delay can go from -32 to +31. PHASEX<5> is the sign bit. PHASEX<4> is the MSB and PHASEX<0> the LSB.
- **OSR = 32:** The delay can go from -16 to +15. PHASEX<4> is the sign bit. PHASEX<3> is the MSB and PHASEX<0> the LSB.

TABLE 5-9: PHASE VALUES WITH MCLK = 4 MHZ, OSR = 4096, PRE<1:0> = 00

PHASEX<11:0> for the Channel Pair CH<n/n+1>												Hex	Delay (CH<n> relative to CH<n+1>)
0	1	1	1	1	1	1	1	1	1	1	1	0x7FF	+ 2047 µs
0	1	1	1	1	1	1	1	1	1	1	0	0x7FE	+ 2046 µs
0	0	0	0	0	0	0	0	0	0	0	1	0x001	+ 1 µs
0	0	0	0	0	0	0	0	0	0	0	0	0x000	0 µs
1	1	1	1	1	1	1	1	1	1	1	1	0xFFF	- 1 µs
1	0	0	0	0	0	0	0	0	0	0	1	0x801	- 2047 µs
1	0	0	0	0	0	0	0	0	0	0	0	0x800	-2048 µs

5.10 Data Ready Link

There are two modes defined with the DR_LINK bit in the STATUSCOM register that control the data ready pulses. The position of the data ready pulses varies with respect to this mode, to the OSR<2:0> and to the PHASE register settings. **Section 5.11 "Data Ready Status Bits"** represents the behavior of the Data Ready pin with the two DR_LINK configurations

- DR_LINK = 0: Data ready pulses from all enabled channels are output on the $\overline{DR}$ pin.
- DR_LINK = 1 (Recommended and Default mode): Only the data ready pulses from the most lagging ADC between all the active ADCs are present on the $\overline{DR}$ pin.

The lagging ADC data ready position depends on the PHASE register, the PRE<1:0> and the OSR<2:0> settings. In this mode, the active ADCs are linked together, so their data is latched together when the lagging ADC output is ready. For power metering applications, DR_LINK = 1 is recommended (Default mode); it allows the host MCU to gather all channels synchronously within a unique interrupt pulse, and it ensures that all channels have been latched at the same time so that no data corruption is happening.

5.11 Data Ready Status Bits

In addition to the data ready pin indicator, the MCP3912 device includes a separate data ready status bit for each channel. Each ADC channel CHn is associated to the corresponding DRSTATUS<n> that can be read at all times in the STATUSCOM register. These status bits can be used to synchronize the data retrieval in case the $\overline{DR}$ pin is not connected (see **Section 6.8 "ADC Channels Latching and Synchronization"**).

The DRSTATUS<3:0> bits are not writable; writing on them has no effect. They have a default value of '1', which indicates that the data of the corresponding ADC is not ready. This means that the ADC output register has not been updated since the last reading (or since the last reset). The DRSTATUS bits take the '0' state, once the ADC channel register is updated (which happens at a DRCLK rate). A simple read of the STATUSCOM register clears all the DRSTATUS bits to their default value ('1').

In the case of DR_LINK = 1, the DRSTATUS<3:0> bits are all updated synchronously with the most lagging channel at the same time the $\overline{DR}$ pulse is generated. In case of DR_LINK = 0, each DRSTATUS bit is updated independently and synchronously with its corresponding channel.

5.12 Crystal Oscillator

The MCP3912 includes a Pierce-type crystal oscillator with very high stability and ensures very low tempco and jitter for the clock generation. This oscillator can handle crystal frequencies up to 20 MHz, provided proper load capacitances and quartz quality factors are used. The crystal oscillator is enabled when CLKEXT = 0 in the CONFIG1 register.

For a proper start-up, the load capacitors of the crystal should be connected between OSC1 and D_{GND} and between OSC2 and D_{GND}. They should also respect Equation 5-7.

EQUATION 5-7:

$$R_M < 1.6 \times 10^6 \times \left(\frac{1}{f \bullet C_{LOAD}}\right)^2$$

Where:

f = crystal frequency in MHz

C_{LOAD} = load capacitance in pF including parasitics from the PCB

R_M = motional resistance in ohms of the quartz

When CLKEXT = 1, the crystal oscillator is bypassed by a digital buffer to allow direct clock input for an external clock (see Figure 4-1). In this case, the OSC2 pin is pulled down internally to D_{GND} and should be connected to D_{GND} externally for better EMI/EMC immunity.

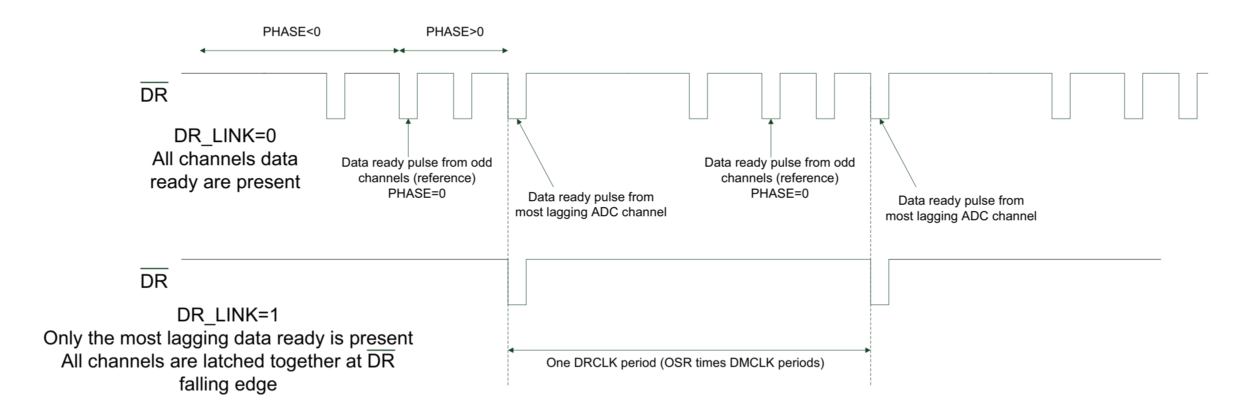


FIGURE 5-8: *DR_LINK Configurations.*

The external clock should not be higher than 20 MHz before prescaling (MCLK < 20 MHz) for proper operation.

Note:	In addition to the conditions defining the maximum MCLK input frequency range, the AMCLK frequency should be maintained inferior to the maximum limits defined in Table 5-2 to ensure the accuracy of the ADCs. If these limits are exceeded, it is recommended to choose either a larger OSR or a larger prescaler value so that AMCLK can respect these limits.

5.13 Digital System Offset and Gain Calibration Registers

The MCP3912 incorporates two sets of additional registers per channel to perform system digital offset and gain error calibration. Each channel has its own set of associated registers that will modify the output result of the channel, if calibration is enabled. The gain and offset calibrations can be enabled or disabled through two CONFIG0 bits (EN_OFFCAL and EN_GAINCAL). These two bits enable or disable system calibration on all channels at the same time. When both calibrations are enabled, the output of the ADC is modified per Equation 5.13.1.

5.13.1 DIGITAL OFFSET ERROR CALIBRATION

The OFFCAL_CHn registers are 23-bit plus two's complement registers, and whose LSB value is the same as the Channel ADC Data. These registers are added bit by bit to the ADC output codes if the EN_OFFCAL bit is enabled. Enabling the EN_OFFCAL bit does not create a pipeline delay; the offset addition is instantaneous. For low OSR values, only the significant digits are added to the output (up to the resolution of the ADC; for example, at OSR = 32, only the 17 first bits are added).

The offset is not added when the corresponding channel is in Reset or Shutdown mode. The corresponding input voltage offset value added by each LSB in these 24-bit registers is:

EQUATION 5-8:

$$OFFSET(1LSB) = V_{REF}/(PGA\_CHn \times 1.5 \times 8388608)$$

These registers are a "Don't Care" if EN_OFFCAL = 0 (offset calibration disabled), but their value is not cleared by the EN_OFFCAL bit.

5.13.2 DIGITAL GAIN ERROR CALIBRATION

These registers are signed 24-bit MSB – first registers coded with a range of -1x to $+(1 - 2^{-23})$x (from 0x800000 to 0x7FFFFF). The gain calibration adds 1x to this register and multiplies it to the output code of the channel bit by bit after offset calibration. The range of the gain calibration is thus from 0x to 1.9999999x (from 0x800000 to 0x7FFFFF). The LSB corresponds to a 2^{-23} increment in the multiplier.

Enabling EN_GAINCAL creates a pipeline delay of 24 DMCLK periods on all channels. All data ready pulses are delayed by 24 DMCLK periods, starting from the data ready following the command enabling EN_GAINCAL bit. The gain calibration is effective on the next data ready following the command enabling EN_GAINCAL bit.

The digital gain calibration does not function when the corresponding channel is in Reset or Shutdown mode. The gain multiplier value for an LSB in these 24-bit registers is:

$$GAIN\ (1LSB) = 1/8388608$$

This register is a "Don't Care" if EN_GAINCAL = 0 (offset calibration disabled), but its value is not cleared by the EN_GAINCAL bit.

The output data on each channel is kept to either 7FFF or 8000 (16-bit mode) or 7FFFFF or 800000 (24-bit mode) if the output results are out of bounds after all calibrations are performed.

EQUATION 5-9: DIGITAL OFFSET AND GAIN ERROR CALIBRATION REGISTERS CALCULATIONS

$$DATA\_CHn(post-cal) = (DATA\_CHn(pre-cal) + OFFCAL\_CHn) \times (1 + GAINCAL\_CHn)$$

6.0 SPI SERIAL INTERFACE DESCRIPTION

6.1 Overview

The MCP3912 device includes a four-wire ($\overline{\text{CS}}$, SCK, SDI, SDO) digital serial interface that is compatible with SPI Modes 0,0 and 1,1. Data is clocked out of the MCP3912 on the falling edge of SCK, and data is clocked into the MCP3912 on the rising edge of SCK. In these modes, the SCK clock can idle either high (1,1) or low (0,0). The digital interface is asynchronous with the MCLK clock that controls the ADC sampling and digital filtering. All the digital input pins are Schmitt-triggered to avoid system noise perturbations on the communications.

Each SPI communication starts with a $\overline{\text{CS}}$ falling edge and stops with the $\overline{\text{CS}}$ rising edge. Each SPI communication is independent. When $\overline{\text{CS}}$ is logic high, SDO is in high-impedance and transitions on SCK and SDI have no effect. Changing from an SPI Mode 1,1 to an SPI Mode 0,0 and vice versa is possible, and can be done while the $\overline{\text{CS}}$ pin is logic high. Any $\overline{\text{CS}}$ rising edge clears the communication and resets the SPI digital interface.

Additional control pins ($\overline{\text{RESET}}$, $\overline{\text{DR}}$) are also provided on separate pins for advanced communication features. The Data Ready pin ($\overline{\text{DR}}$) outputs pulses when a new ADC channel data is available for reading, which can be used as an interrupt for an MCU. The Master Reset pin ($\overline{\text{RESET}}$) acts like a hard reset and can reset the part to its default power-up configuration (equivalent to a POR state).

The MCP3912 interface has a simple command structure. Every command is either a read command from a register, or a write command to a register. The MCP3912 device includes 32 registers defined in the Table 8-1 register map. The first byte (8-bit wide) transmitted is always the CONTROL byte that defines the address of the register and the type of command (read or write). It is followed by the register itself, which can be in a 16-, 24- or 32-bit format, depending on the multiple format settings defined in the STATUSCOM register. The MCP3912 is compatible with multiple formats that help reduce overhead in the data handling for most MCUs and processors available on the market (8-/16- or 32-bit MCUs) and improve MCU-code compaction and efficiency.

The MCP3912 digital interface is capable of handling various continuous read and write modes, which allows it to perform ADC data streaming or full register map writing within only one communication (and therefore with only one unique control byte). The internal registers can be grouped together with various configurations through the READ<1:0> and WRITE bits. The internal address counter of the serial interface can be automatically incremented, with no additional control byte needed, in order to loop through the various groups of registers within the register map. The groups are defined in Table 8-2.

The MCP3912 device also includes advanced security features to secure each communication, in order to avoid unwanted write commands being processed to change the desired configuration and to alert the user in case of a change in the desired configuration.

Each SPI read communication can be secured through a selectable CRC-16 checksum provided on the SDO pin at the end of every communication sequence. This CRC-16 computation is compatible with the DMA CRC hardware of the PIC24 and PIC32 MCUs, resulting in no additional overhead for the added security.

For securing the entire configuration of the device, the MCP3912 includes an 8-bit lock code (LOCK<7:0>), which blocks all write commands to the full register map if the value of the LOCK<7:0> is not equal to a defined password (0xA5). The user can protect its configuration by changing the LOCK<7:0> value to 0x00 after the full programming, so that any unwanted write command will not result in a change to the configuration (because LOCK<7:0> is different than the password 0xA5).

An additional CRC-16 calculation is also running continuously in the background to ensure the integrity of the full register map. All writable registers of the register map (except the MOD register) are processed through a CRC-16 calculation engine and give a CRC-16 checksum that depends on the configuration. This checksum is readable on the LOCK/CRC register and updated at all times. If a change in this checksum happens, a selectable interrupt can give a flag on the $\overline{\text{DR}}$ pin ($\overline{\text{DR}}$ pin becomes logic low) to warn the user that the configuration is corrupted.

6.2 Control Byte

The control byte of the MCP3912 contains two device Address bits (A<6:5>), five register Address bits (A<4:0>) and a Read/Write bit (R/$\overline{\text{W}}$). The first byte transmitted to the MCP3912 in any communication is always the control byte. During the control byte transfer, the SDO pin is always in a high-impedance state. The MCP3912 interface is device addressable (through A<6:5>) so that multiple chips can be present on the same SPI bus with no data bus contention. Even if they use the same $\overline{\text{CS}}$ pin, they use a provided half-duplex SPI interface with a different address identifier. This functionality enables, for example, a Serial EEPROM like 24AAXXX/24LCXXX or 24FCXXX and the MCP3912 to share all the SPI pins and consume less I/O pins in the application processor, since all these Serial EEPROM circuits use A<6:5> = `00`.

A<6>	A<5>	A<4>	A<3>	A<2>	A<1>	A<0>	R/$\overline{\text{W}}$
Device Address		Register Address					Read/ Write

FIGURE 6-1: Control Byte.

The default device address bits are A<6:5> = `01` (contact the Microchip factory for other available device address bits). For more information, see the **Product Identification System** section. The register map is defined in Table 8-1.

6.3 Reading from the Device

The first register read on the SDO pin is the one defined by the address (A<4:0>) given in the CONTROL byte. After this first register is fully transmitted, if the $\overline{CS}$ pin is maintained logic low, the communication continues without an additional control byte and the SDO pin transmits another register with the address automatically incremented or not, depending on the READ<1:0> bit settings.

Four different Read mode configurations can be defined through the READ<1:0> bits in the STATUSCOM register for the address increment (see **Section 6.5, Continuous Communications, Looping on Register Sets** and Table 8-2). The data on SDO is clocked out of the MCP3912 on the falling edge of SCK. The reading format for each register is defined on **Section 6.5 "Continuous Communications, Looping on Register Sets"**.

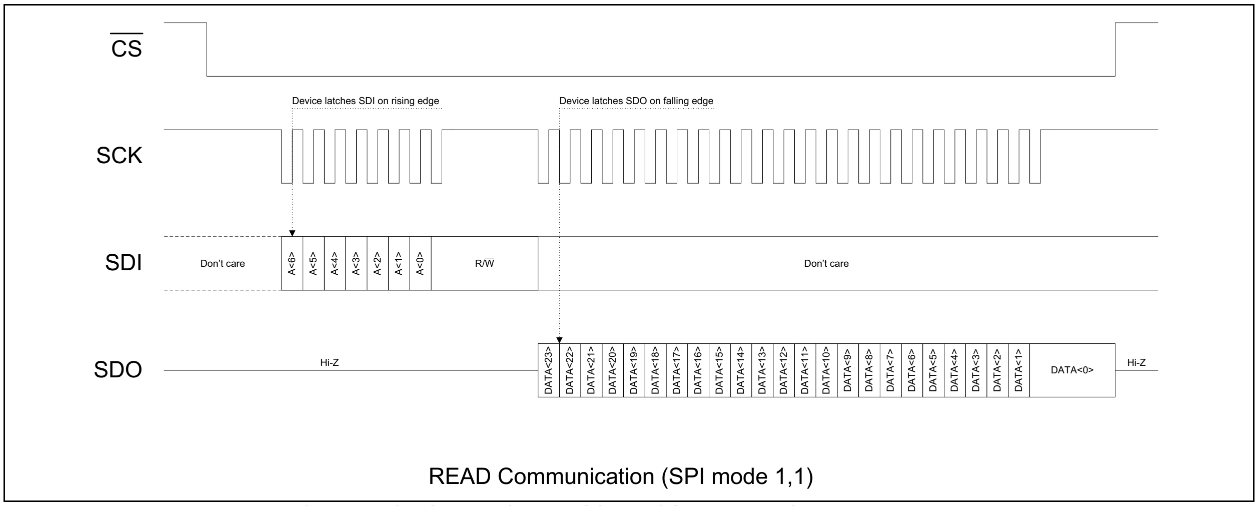


FIGURE 6-2: *Read on a Single Register with 24-bit Format (WIDTH_DATA<1:0> = `01`, SPI Mode 1,1).*

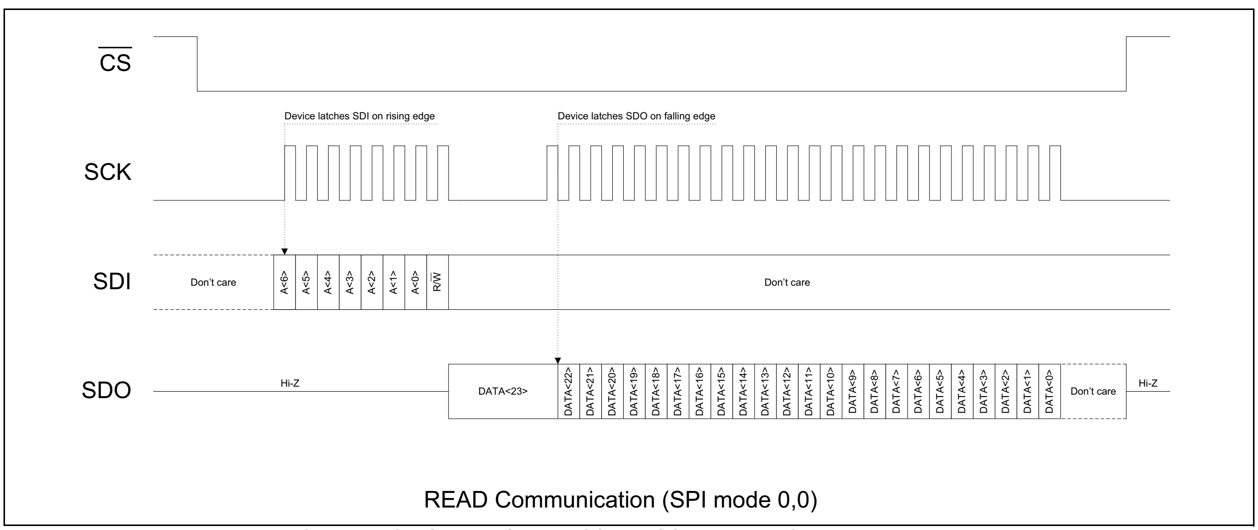
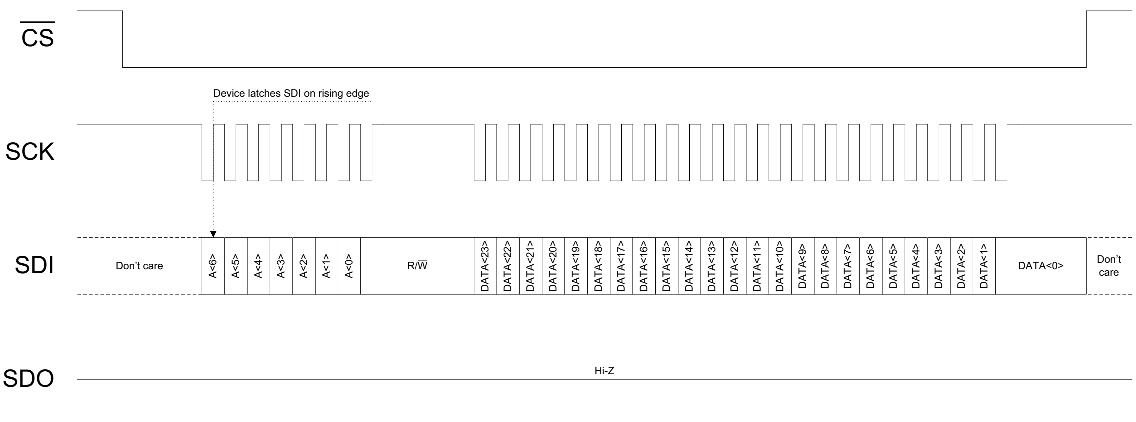


FIGURE 6-3: *Read on a Single Register with 24-bit Format (WIDTH_DATA<1:0> = `01`, SPI Mode 0,0).*

6.4 Writing to the Device

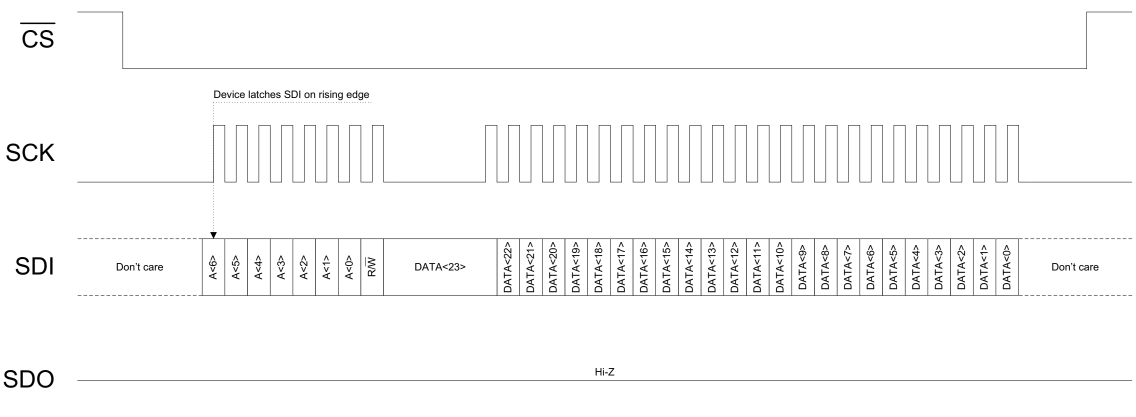
The first register written from the SDI pin to the device is the one defined by the address (A<4:0>) given in the CONTROL byte. After this first register is fully transmitted, if the $\overline{CS}$ pin is maintained logic low, the communication continues without an additional control byte and the SDI pin transmits another register with the address automatically incremented or not, depending on the WRITE bit setting.

Two different Write mode configurations for the address increment can be defined through the WRITE bit in the STATUSCOM register (see **Section 6.5, Continuous Communications, Looping on Register Sets** and Table 8-2). The SDO pin stays in a high-impedance state during a write communication. The data on SDI is clocked into the MCP3912 on the rising edge of SCK. The writing format for each register is defined in **Section 6.5, Continuous Communications, Looping on Register Sets**. A write on an undefined or nonwritable address, such as the ADC channel's register addresses, will have no effect and also will not increment the address counter.



WRITE Communication (SPI mode 1,1)

FIGURE 6-4: *Write to a Single Register with 24-bit Format (SPI Mode 1,1).*



WRITE Communication (SPI mode 0,0)

FIGURE 6-5: *Write to a Single Register with 24-bit Format (SPI Mode 0,0).*

6.5 Continuous Communications, Looping on Register Sets

The MCP3912 digital interface can process communications in Continuous mode without having to enter an SPI command between each read or write to a register. This feature allows the user to reduce communication overhead to the strict minimum, which diminishes EMI emissions and reduces switching noise in the system.

The registers can be grouped into multiple sets for continuous communications. The grouping of the registers in the different sets is defined by the READ<1:0> and WRITE bits that control the internal SPI communication address pointer. For a graphical representation of the register map sets in function of the READ<1:0> and WRITE bits, please see Table 8-2.

In the case of a continuous communication, there is only one control byte on SDI to start the communication after a $\overline{CS}$ pin falling edge. The part stays within the same communication loop until the $\overline{CS}$ pin returns logic high. The SPI internal register address pointer starts by transmitting/receiving the address defined in the control byte. After this first transmission/reception, the SPI internal register address pointer automatically increments to the next available address in the register set for each transmission/reception. When it reaches the last address of the set, the communication sequence is finished. The address pointer automatically loops back to the first address of the defined set and restarts a new sequence with auto-increment (see Table 6-6). This internal address pointer automatic selection allows the following functionality:

- Read one ADC channel data, pairs of ADC channels or all ADC channels continuously
- Continuously read the entire register map
- Continuously read or write each separate register
- Continuously read or write all configuration registers

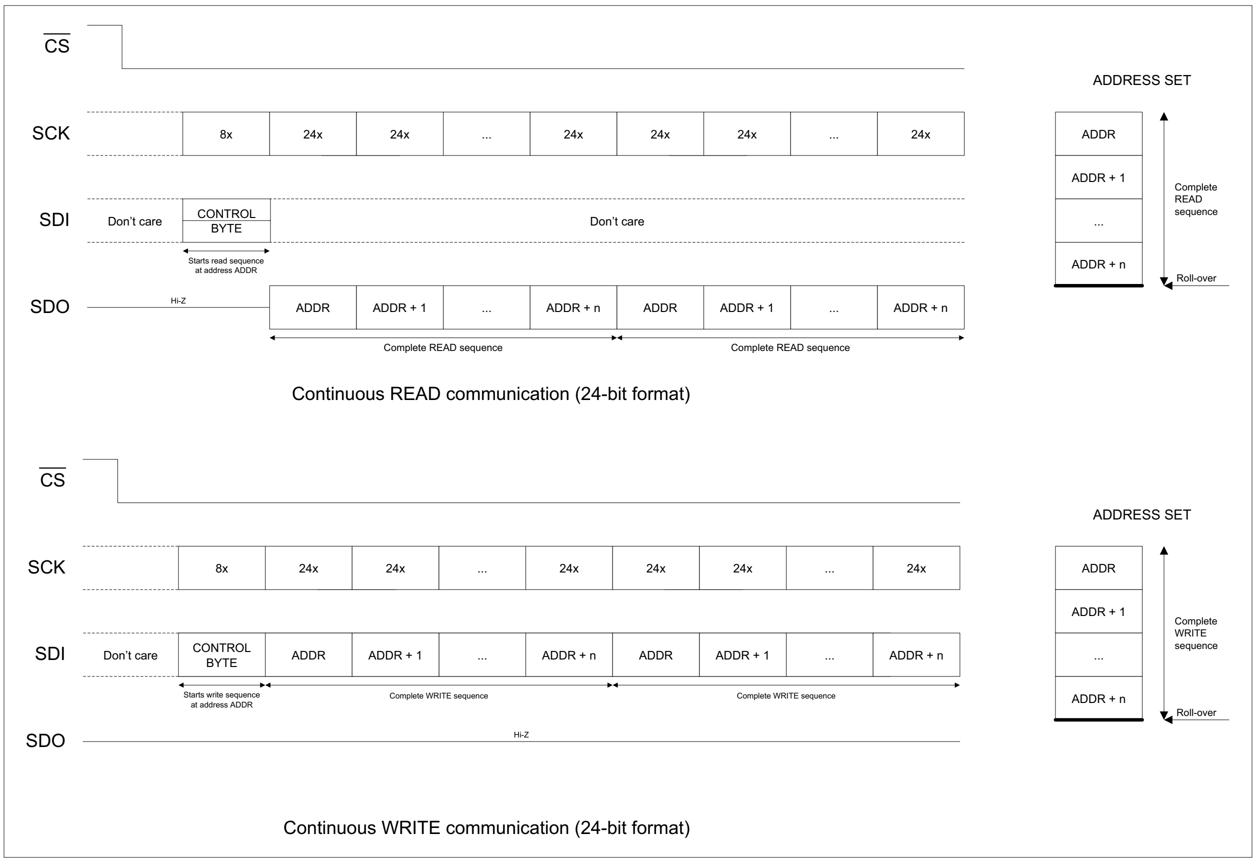


FIGURE 6-6: *Continuous Communication Sequences.*

6.5.1 CONTINUOUS READ

The STATUSCOM register contains the read communication loop settings for the internal register address pointer (READ<1:0> bits). For Continuous Read modes, the address selection can take the following four values:

TABLE 6-1: ADDRESS SELECTION IN CONTINUOUS READ

READ<1:0>	Register Address Set Grouping for Continuous Read Communications
`00`	Static (no incrementation)
`01`	Groups
`10`	Types (default)
`11`	Full Register Map

Any SDI data coming after the control byte is not considered during a continuous read communication. The following figures represent a typical continuous read communication on all four ADC channels in TYPES mode with the default settings (DR_LINK = `1`, READ<1:0> = `10`, WIDTH_DATA<1:0> = `01`) in case of the SPI Mode 0,0 (Figure 6-7) and SPI Mode 1,1 (Figure 6-8).

> **Note:** For continuous reading of ADC data in SPI Mode 0,0 (see Figure 6-7), once the data has been completely read after a data ready, the SDO pin will take the MSB value of the previous data at the end of the reading (falling edge of the last SCK clock). If SCK stays idle at logic low (by definition of Mode 0,0), the SDO pin will be updated at the falling edge of the next data ready pulse (synchronously with the DR pin falling edge with an output timing of t_{DODR}) with the new MSB of the data corresponding to the data ready pulse. This mechanism allows the MCP3912 to continuously read ADC data outputs seamlessly, even in SPI Mode (0,0).

In SPI Mode (1,1), the SDO pin stays in the last state (LSB of previous data) after a complete reading which also allows seamless continuous Read mode (see Figure 6-8).

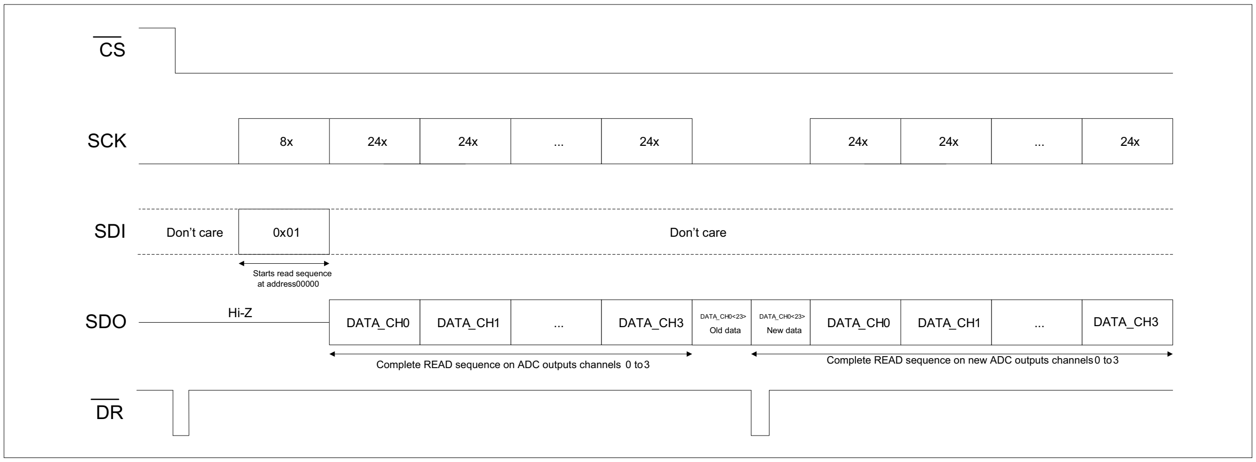


FIGURE 6-7: *Typical Continuous Read Communication (WIDTH_DATA<1:0> = `01`, SPI Mode 0,0).*

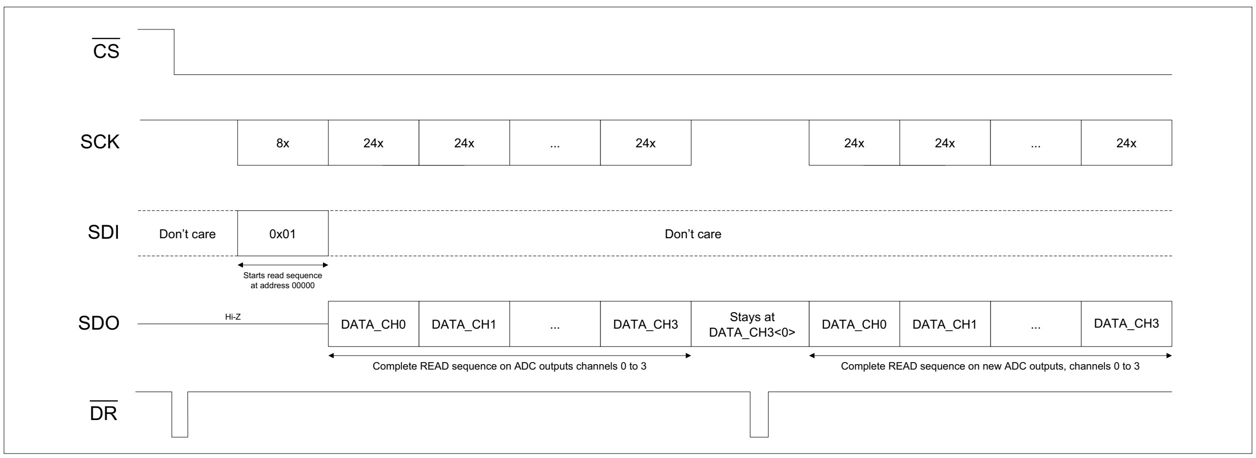


FIGURE 6-8: *Typical Continuous Read Communication (WIDTH_DATA<1:0> = `01`, SPI Mode 1,1).*

6.5.2 CONTINUOUS WRITE

The STATUSCOM register contains the write loop settings for the internal register address pointer (WRITE). For a continuous write, the address selection can take the following two values:

TABLE 6-2: ADDRESS SELECTION IN CONTINUOUS WRITE

WRITE	Register Address Set Grouping for Continuous Read Communications
`0`	Static (no incrementation)
`1`	Types (default)

SDO is always in a high-impedance state during a continuous write communication. Writing to a non-writable address (such as addresses 0x00 to 0x07) has no effect and does not increment the address pointer. In this case, the user needs to stop the communication and restart a communication with a control byte pointing to a writable address (0x08 to 0x1F).

> **Note:** When LOCK<7:0> is different than 0xA5, all the addresses, except 0x1F, become nonwritable (see **Section 4.13 "MCP3912 Delta-Sigma Architecture"**)

6.6 Situations that Reset and Restart Active ADCs

Immediately after the following actions, the active ADCs (the ones not in Soft Reset or Shutdown modes) are reset and automatically restarted in order to provide proper operation:

1. Change in PHASE register.
2. Overwrite of the same PHASE register value.
3. Change in the OSR<2:0> settings.
4. Change in the PRE<1:0> settings.
5. Change in the CLKEXT setting.
6. Change in the VREFEXT setting.

After these temporary resets, the ADCs go back to Normal operation, with no need for an additional command. Each ADC data output register is cleared during this process. The PHASE register can be used to serially soft reset the ADCs, without using the RESET<3:0> bits in the Configuration register, if the same value is written in the PHASE register.

6.7 Data Ready Pin ($\overline{\text{DR}}$)

To communicate when channel data is ready for transmission, the data ready signal is available on the Data Ready pin ($\overline{\text{DR}}$) at the end of a channel conversion. The Data Ready pin outputs an active-low pulse with a pulse width equal to half a DMCLK clock period. After a data ready pulse falling edge has occurred, the ADC output data is updated within the t_{DODR} timing and can then be read through SPI communication.

The first data ready pulse after a Hard or a Soft Reset is located after the settling time of the sinc filter (see Table 5-3) plus the phase delay of the corresponding channel (see **Section 5.9 "Phase Delay Block"**). Each subsequent pulse is then periodic, and the period is equal to a DRCLK clock period (see Equation 4-3 and Figure 1-3). The data ready pulse is always synchronous with the internal DRCLK clock.

The $\overline{\text{DR}}$ pin can be used as an interrupt pin when connected to an MCU or DSP, which will synchronize the readings of the ADC data outputs. When not active-low, this pin can either be in high-impedance (when DR_HIZ = `0`) or in a defined logic high state (when DR_HIZ = `1`). This is controlled through the STATUSCOM register. This allows multiple devices to share the same Data Ready pin (with a pull-up resistor connected between $\overline{\text{DR}}$ and DV_{DD}). If only the MCP3912 device is connected on the interrupt bus, the $\overline{\text{DR}}$ pin does not require a pull-up resistor, and therefore it is recommended to use DR_HIZ = `1` configuration for such applications.

The $\overline{\text{CS}}$ pin has no effect over the $\overline{\text{DR}}$ pin, which means even if the $\overline{\text{CS}}$ pin is logic high, the data ready pulses coming from the active ADC channels will still be provided; the $\overline{\text{DR}}$ pin behavior is independent from the SPI interface. While the $\overline{\text{RESET}}$ pin is logic low, the $\overline{\text{DR}}$ pin is not active. The $\overline{\text{DR}}$ pin is latched in the logic low state when the interrupt flag on the CRCREG is present to signal that the desired registers configuration has been corrupted (see **Section 6.11 "Detecting Configuration Change Through CRC-16 Checksum On Register Map and its Associated Interrupt Flag"**).

6.8 ADC Channels Latching and Synchronization

The ADC channel's data output registers (addresses 0x00 to 0x03) have a double buffer output structure. The two sets of latches in series are triggered by the data ready signal and an internal signal indicating the beginning of a read communication sequence (read start).

The first set of latches holds each ADC channel data output register when the data is ready, and latches all active outputs together when DR_LINK = 1. This behavior is synchronous with the DMCLK clock.

The second set of latches ensures that when reading starts on an ADC output, the corresponding data is latched so that no data corruption can occur within a read. This behavior is synchronous with the SCK clock. If an ADC read has started, in order to read the following ADC output, the current reading needs to be fully completed (all bits must be read on the SDO pin from the ADC output data registers).

Since the double output buffer structure is triggered with two events that depend on two asynchronous clocks (data ready with DMCLK and read start with SCK), implement one of the three following methods on the MCU or processor in order to synchronize the reading of the channels:

1. **Use the Data Ready pin pulses as an interrupt**: once a falling edge occurs on the $\overline{\text{DR}}$ pin, the data is available for reading on the ADC output registers after the t_{DODR} timing. If this timing is not respected, data corruption can occur.
2. **Use a timer clocked with MCLK as a synchronization event:** since the Data Ready is synchronous with DMCLK, the user can calculate the position of the Data Ready depending on the PHASE, the OSR<2:0> and the PRE<1:0> settings for each channel. Again, the t_{DODR} timing needs to be added to this calculation, to avoid data corruption.
3. **Poll the DRSTATUS<3:0> bits in the STATUSCOM register:** this method consists of continuously reading the STATUSCOM register and waiting for the DRSTATUS bits to be equal to '0'. When this event happens, the user can start a new communication to read the desired ADC data. In this case, no additional timing is required.

The first method is the preferred one, as it can be used without adding additional MCU code space, but requires connecting the $\overline{\text{DR}}$ pin to an I/O pin of the MCU. The last two methods require more MCU code space and execution time, but they allow synchronized reading of the channels without connecting the $\overline{\text{DR}}$ pin, which saves one I/O pin on the MCU.

6.9 Securing Read Communications Through CRC-16 Checksum

Since power/energy metering systems can generate or receive large EMI/EMC interferences and large transient spikes, it is helpful to secure SPI communications as much as possible to maintain data integrity and desired configurations during the lifetime of the application.

The communication data on the SDO pin can be secured through the insertion of a Cyclic Redundancy Check (CRC) checksum at the end of each continuous reading sequence. The CRC checksum on communications can be enabled or disabled through the EN_CRCCOM bit in the STATUSCOM register. The CRC message ensures the integrity of the read sequence bits transmitted on the SDO pin, and the CRC checksum is inserted in between each read sequence (see Figure 6-9).

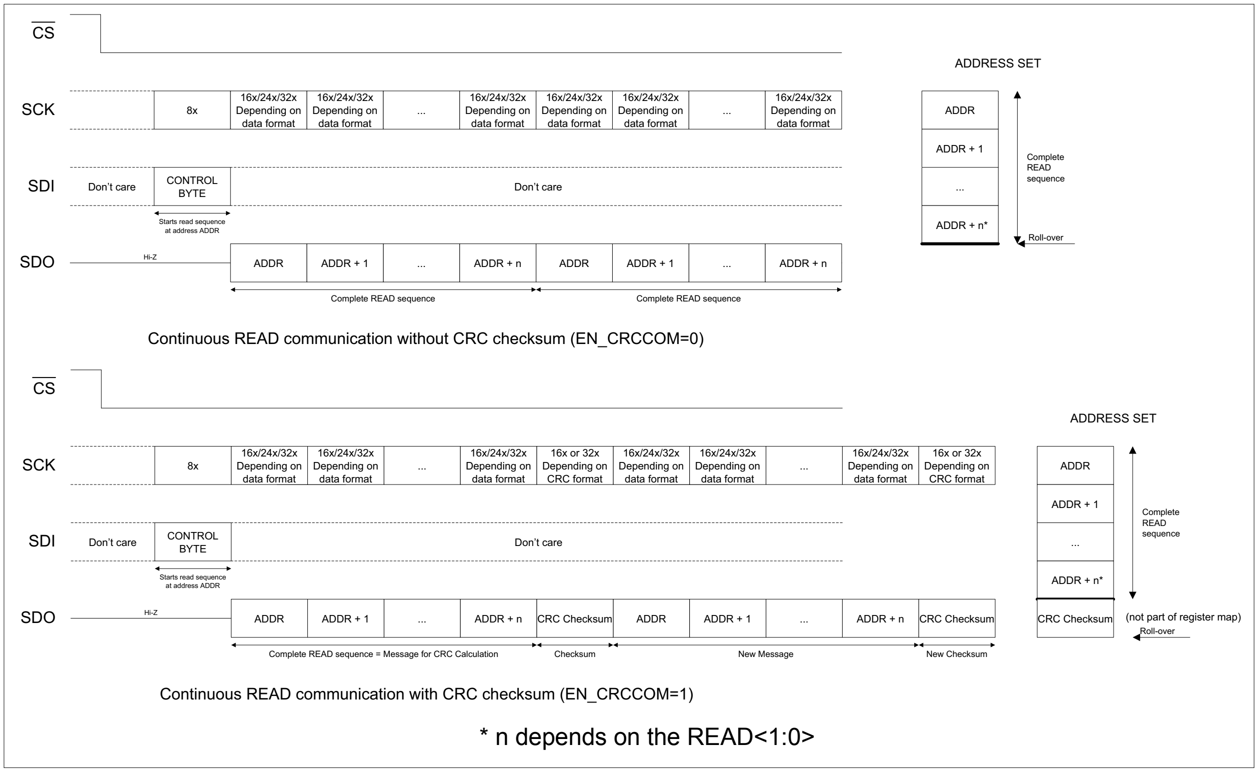


FIGURE 6-9: *Continuous Read Sequences With and Without CRC Checksum Enabled.*

The CRC checksum in the MCP3912 device uses the 16-bit CRC-16 ANSI polynomial as defined in the IEEE 802.3 standard: $x^{16} + x^{15} + x^2 + 1$. This polynomial can also be noted as 0x8005. CRC-16 detects all single and double-bit errors, all errors with an odd number of bits, all burst errors of length 16 or less, and most errors for longer bursts. This allows an excellent coverage of the SPI communication errors that can happen in the system and heavily reduces the risk of a miscommunication, even under noisy environments.

The CRC-16 format displayed on the SDO pin depends on the WIDTH_CRC bit in the STATUSCOM register (see Figure 6-10). It can be either 16-bit or 32-bit format, to be compatible with both 16-bit and 32-bit MCUs. The CRCCOM<15:0> bits calculated by the MCP3912 device are not dependent on the format (the device always calculates only a 16-bit CRC checksum). If a 32-bit MCU is used in the application, it is recommended to use 32-bit formats (WIDTH_CRC = 1) only.

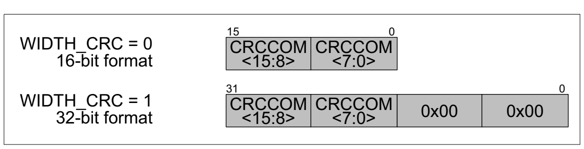


FIGURE 6-10: *CRC Checksum Format.*

The CRC calculation computed by the MCP3912 device is fully compatible with CRC hardware contained in the Direct Memory Access (DMA) of the PIC24 and PIC32 MCU product lines. The CRC message that should be considered in the PIC® device DMA is the concatenation of the read sequence and its associated checksum. When the DMA CRC hardware computes this extended message, the resulted checksum should be 0x0000. Any other result indicates that a miscommunication has happened and that the current communication sequence should be stopped and restarted.

Note:	The CRC will be generated only at the end of the selected address set, before the rollover of the address pointer occurs (see Figure 6-9).

6.10 Locking/Unlocking Register Map Write Access

The MCP3912 digital interface includes an advanced security feature that permits locking or unlocking the register map write access. This feature prevents the miscommunications that can corrupt the desired configuration of the device, especially an SPI read becoming an SPI write because of the noisy environment.

The last register address of the register map (0x1F: LOCK/CRC) contains the LOCK<7:0> bits. If these bits are equal to the password value (which is equal to the default value of 0xA5), the register map write access is not locked. Any write can take place and the communications are not protected.

When the LOCK<7:0> bits are different than 0xA5, the register map write access is locked. The register map, and therefore the full device configuration, is write-protected. Any write to an address other than 0x1F will yield no result. All the register addresses, except the address 0x1F, become read-only. In this case, if the user wants to change the configuration, the LOCK<7:0> bits have to be reprogrammed back to 0xA5 before sending the desired write command.

The LOCK<7:0> bits are located in the last register, so the user can program the whole register map, starting from 0x09 to 0x1E within one continuous write sequence, and then lock the configuration at the end of the sequence by writing all zeros, in the address 0x1F for example.

6.11 Detecting Configuration Change Through CRC-16 Checksum On Register Map and its Associated Interrupt Flag

In order to prevent internal corruption of the register and to provide additional security on the register map configuration, the MCP3912 device includes an automatic and continuous CRC checksum calculation on the full register map configuration bits. This calculation is not the same as the communication CRC checksum described in **Section 6.9 “Securing Read Communications Through CRC-16 Checksum”**. This calculation takes the full register map as the CRC message and outputs a checksum on the CRCREG<15:0> bits located in the LOCK/CRC register (address 0x1F).

Since this feature is intended for protecting the configuration of the device, this calculation is run continuously only when the register map is locked (LOCK<7:0> different than 0xA5, see **Section 6.10, Locking/Unlocking Register Map Write Access**). If the register map is unlocked, the CRCREG<15:0> bits are cleared and no CRC is calculated.

The calculation is fully completed in 16 DMCLK periods and refreshed every 16 DMCLK periods continuously. The CRCREG<15:0> bits are reset when a POR or a hard reset occurs. All the bits contained in the registers from addresses 0x09 — 0x1F are processed by the CRC engine to give the CRCREG<15:0>. The DRSTATUS<3:0> bits are set to '1' (default) and the CRCREG<15:0> bits are set to '0' (default) for this calculation engine, as they could vary during the calculation.

An interrupt flag can be enabled through the EN_INT bit in the STATUSCOM register and provided on the $\overline{\text{DR}}$ pin when the configuration has changed without a write command being processed. This interrupt is a logic low state. This interrupt is cleared when the register map is unlocked (since the CRC calculation is not processed).

At power-up, the interrupt is not present and the register map is unlocked. As soon as the user finishes writing its configuration, the user needs to lock the register map (writing 0x00 for example in the LOCK bits) to be able to use the interrupt flag. The CRCREG<15:0> bits will be calculated for the first time in 16 DMCLK periods. This first value will then be the reference checksum value and will be latched internally until a hard reset, a POR or an unlocking of the register map happens. The CRCREG<15:0> will then be calculated continuously and checked against the reference checksum. If the CRCREG<15:0> is different than the reference, the interrupt sends a flag by setting the $\overline{\text{DR}}$ pin to a logic low state until it is cleared.

NOTES:

7.0 BASIC APPLICATION RECOMMENDATIONS

7.1 Typical Application Examples

The application schematic referenced in Figure 7-1 can be used as a starting point for MCP3912 applications.The most common solution is to use one channel for voltage measurement and the rest of the channels for current measurement. Since all current lines are at the same potential, shunts can be used as current sensors, even if they do not provide any galvanic isolation.

Since all channels are identical in the MCP3912, any channel can be chosen as the voltage channel (preferably CH0 or CH3 since they are on the edges and can lead to a cleaner layout).

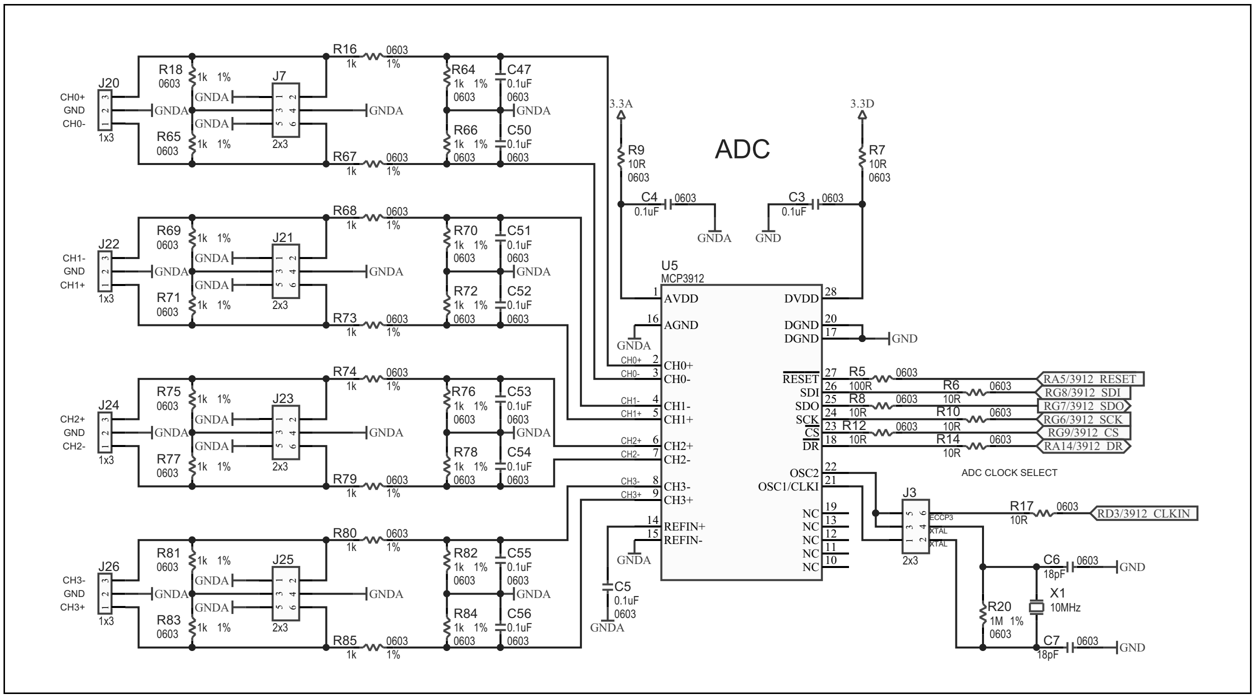


FIGURE 7-1: *MCP3912 Application Example Schematic.*

7.2 Power Supply Design and Bypassing

The MCP3912 device was designed to measure positive and negative voltages that might be generated by a current sensing device. This current sensing device, with a common mode voltage close to 0V, is referred to as A_{GND}, which is a shunt or current transformer (CT) with burden resistors attached to ground. The high performance and good flexibility that characterize this ADC enables them to be used in other applications, as long as the absolute voltage on each pin, referred to A_{GND}, stays in the -1V to +1V interval.

In any system, the analog ICs (such as references or operational amplifiers) are always connected to the analog ground plane. The MCP3912 should also be considered as a sensitive analog component, and connected to the analog ground plane. The ADC features two pairs of pins: A_{GND}, AV_{DD}, D_{GND} and DV_{DD}. For best performance, it is recommended to keep the two pairs connected to two different networks (Figure 7-2). This way, the design will feature two ground traces and two power supplies (Figure 7-3).

This means the analog circuitry (including MCP3912) and the digital circuitry (MCU) should have separate power supplies and return paths to the external ground reference, as described in Figure 7-2. An example of a typical power supply circuit, with different lines for analog and digital power, is shown in Figure 7-3. A possible split example is shown in Figure 7-4, where the ground star connection can be done at the bottom of the device with the exposed pad. The split here between analog and digital can be done under the device, and AV_{DD} and DV_{DD} can be connected together with lines coming under the ground plane.

Another possibility, sometimes easier to implement in terms of PCB layout, is to consider the MCP3912 as an analog component and, therefore, connect both AV_{DD} and DV_{DD} together, and A_{GND} and D_{GND} together with a star connection. In this scheme, the decoupling capacitors may be larger due to the ripple on the digital power supply (caused by the digital filters and the SPI interface of the MCP3912) now causing glitches on the analog power supply.

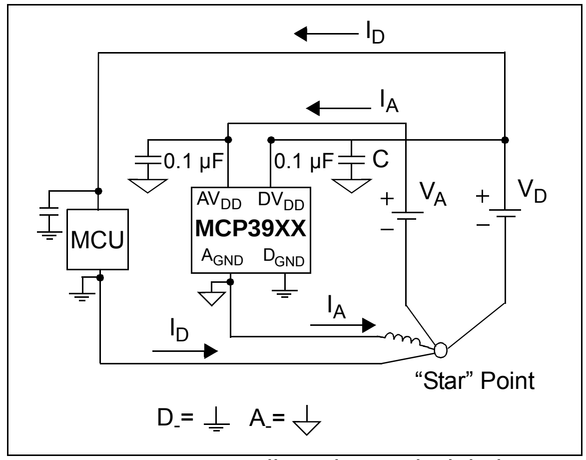


FIGURE 7-2: All Analog and Digital Return Paths Need to Stay Separate with Proper Bypass Capacitors.

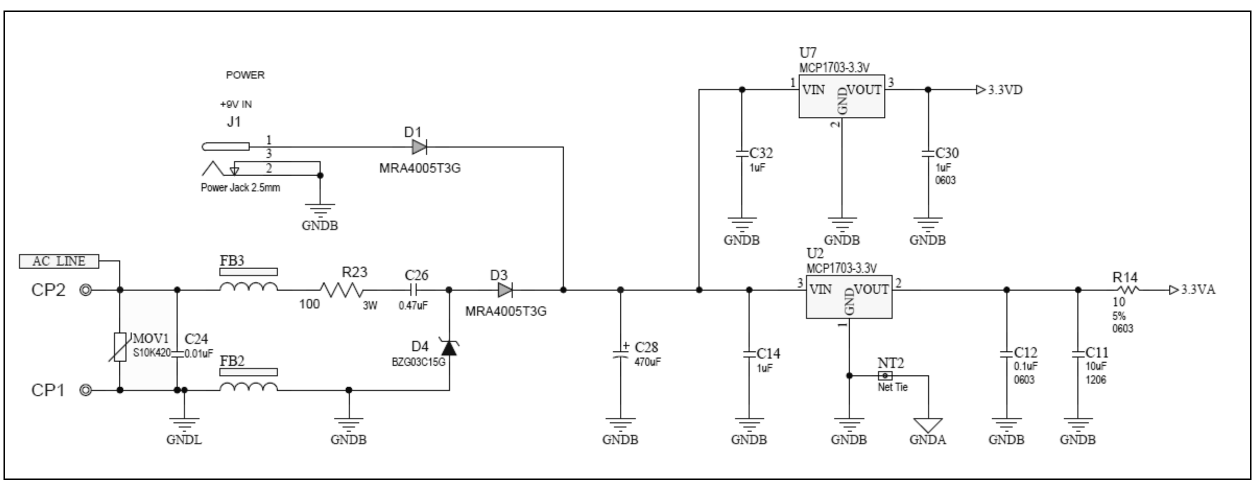


FIGURE 7-3: Power Supply with Separate Lines for Analog and Digital Sections. Note the "Net Tie" Object NT2 that Represents the Start Ground Connection.

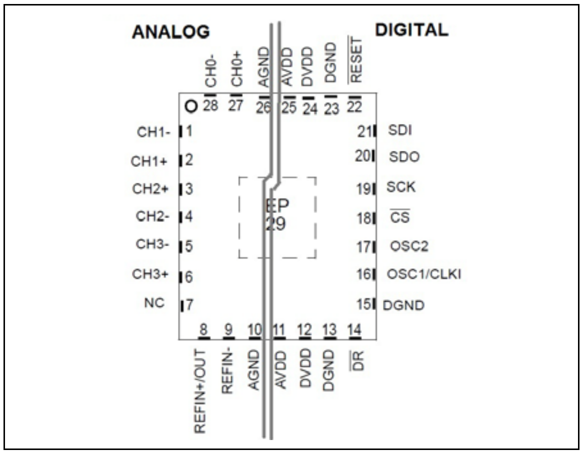


FIGURE 7-4: Separation of Analog and Digital Circuits on Layout.

Figure 7-5 shows a more detailed example with a direct connection to a high-voltage line (e.g., a two-wire 120V or 220V system). A current-sensing shunt is used for current measurement on the high side/line side that also supplies the ground for the system. This is necessary as the shunt is directly connected to the channel input pins of the MCP3912. To reduce sensitivity to external influences such as EMI, these two wires should form a twisted pair, as noted in Figure 7-5. The power supply and MCU are separated on the right side of the PCB, surrounded by the digital ground plane. The MCP3912 is kept on the left side, surrounded by the analog ground plane. There are two separate power supplies going to the digital section of the system and the analog section, including the MCP3912. With this placement, there are two separate current supply paths and current return paths, I_A and I_D.

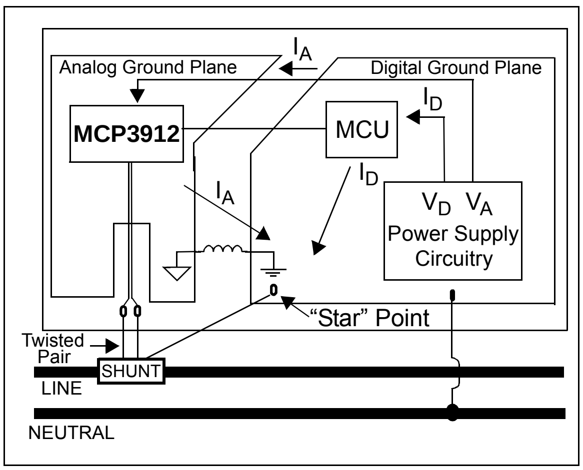


FIGURE 7-5: Connection Diagram.

The ferrite bead between the digital and analog ground planes helps keep high-frequency noise from entering the device. This ferrite bead is recommended to be low resistance; most often it is a THT component. Ferrite beads are typically placed on the shunt inputs and into the power supply circuit for additional protection.

7.3 SPI Interface Digital Crosstalk

The MCP3912 incorporates a high-speed 20 MHz SPI digital interface. This interface can induce a crosstalk, especially with the outer channels (CH0, for example), if it is running at its full speed without any precautions. The crosstalk is caused by the switching noise created by the digital SPI signals (also called ground bouncing). This crosstalk would negatively impact the SNR in this case. The noise is attenuated if a proper separation between the analog and digital power supplies is put in place (see **Section 7.2 "Power Supply Design and Bypassing"**).

In order to further remove the influence of the SPI communication on measurement accuracy, it is recommended to add series resistors on the SPI lines to reduce the current spikes caused by the digital switching noise (see Figure 7-5 where these resistors have been implemented). The resistors also help to keep the level of electromagnetic emissions low.

The measurement graphs provided in this MCP3912 data sheet have been performed with 100Ω series resistors connected on each SPI I/O pin. Measurement accuracy disturbances have not been observed even at the full speed of 20 MHz interfacing.

The crosstalk performance is dependent on the package choice due to the difference in the pin arrangement (dual in-line or quad), and is improved in the QFN-28 package.

7.4 Sampling Speed and Bandwidth

If ADC power consumption is not a concern in the design, the boost settings can be increased for best performance so that the OSR is always kept at the maximum settings to improve the SINAD performance (see Table 7-1). If the MCU cannot generate a clock fast enough, it is possible to tap the OSC1/OSC2 pins of the MCP3912 crystal oscillator directly to the crystal of the microcontroller. When the sampling frequency is enlarged, the phase resolution is improved, and with the OSR increased, the phase compensation range can be kept in the same range as the default settings.

TABLE 7-1: SAMPLING SPEED VS. MCLK AND OSR, ADC PRESCALE 1:1

MCLK (MHz)	Boost<1:0>	OSR	Sampling Speed (ksps)
16	11	1024	3.91
14	11	1024	3.42
12	11	1024	2.93

TABLE 7-1: SAMPLING SPEED VS. MCLK AND OSR, ADC PRESCALE 1:1

MCLK (MHz)	Boost<1:0>	OSR	Sampling Speed (ksps)
10	10	1024	2.44
8	10	512	3.91
6	01	512	2.93
4	01	256	3.91

7.5 Differential Inputs Anti-Aliasing Filter

Due to the nature of the ADCs used in the MCP3912 (oversampling converters), each differential input of the ADC channels requires an anti-aliasing filter so that the oversampling frequency (DMCLK) is largely attenuated and does not generate any disturbances on the ADC accuracy. This anti-aliasing filter also needs to have a gain close to one in the signal bandwidth of interest.

Typically for 50/60 Hz measurement and default settings (DMCLK = 1 MHz), a simple RC filter with 1 kΩ and 100 nF can be used. The anti-aliasing filter used for the measurement graphs is a first-order RC filter with 1 kΩ and 15 nF. The typical schematic for connecting a current transformer to the ADC is shown in Figure 7-6. If wires are involved, twisting them is also recommended.

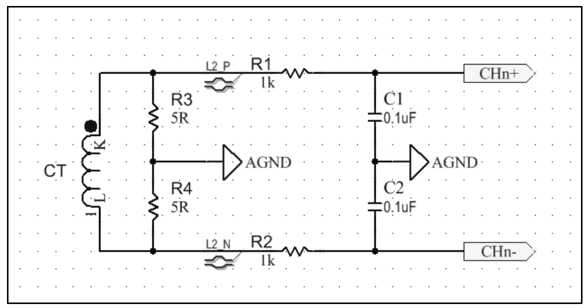


FIGURE 7-6: *First-Order Anti-Aliasing Filter for CT-Based Designs.*

The di/dt current sensors, such as Rogowski coils, can be an alternative to current transformers. Since these sensing elements are highly sensitive to high-frequency electromagnetic fields, using a second order anti-aliasing filter is recommended to increase the attenuation of potential perturbing RF signals.

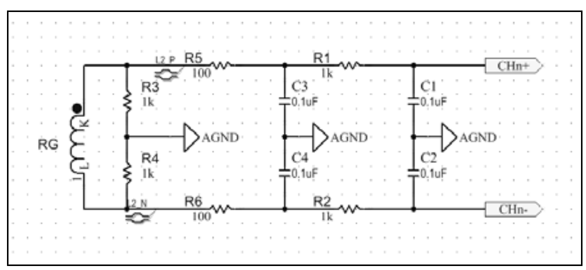


FIGURE 7-7: *Second-Order Anti-Aliasing Filter for Rogowski Coil-Based Designs.*

The MCP3912 is highly recommended in applications using di/dt as current sensors because of the extremely low noise floor at low frequencies. In such applications, a low-pass filter (LPF) with a cut-off frequency much lower than the signal frequency (50-60 Hz for metering) is used to compensate for the 90 degree shift and for the 20 db/decade attenuation induced by the di/dt sensor. Because of this filter, the SNR will be decreased, since the signal will attenuate by a few orders of magnitude while the low-frequency noise will not be attenuated. Usually, a high-order high-pass filter (HPF) is used to attenuate the low-frequency noise in order to prevent a dramatic degradation of the SNR, which can be very important in other parts. A high-order filter will also consume a significant portion of the computation power of the MCU. When using the MCP3912, such a high-order HPF is not required since this part has a low noise floor at low frequencies. A first-order HPF is enough to achieve very good accuracy.

7.6 Energy Measurement Error Considerations

The measurement error is a typical representation of the nonlinearity of a pair of ADCs (see **Section 4.0 "Terminology And Formulas"** for the definition of measurement error). The measurement error is dependent on the THD and on the noise floor of the ADCs.

Improving the measurement error specification on the MCP3912 can be realized by increasing the OSR (to get a better SINAD and THD performance) and, to some extent, the BOOST settings (if the bandwidth of the measurements is too limited by the bandwidth of the amplifiers in the sigma-delta ADCs). In most of the energy metering AC applications, high-pass filters are used to cancel the offset on each ADC channel (current and voltage channels), and therefore a single-point calibration is necessary to calibrate the system for active energy measurement. This calibration is a system gain calibration, and the user can utilize the EN_GAINCAL bit and the GAINCAL_CHn registers to perform this digital calibration. After such calibration, typical measurement error curves like Figure 2-7 can be generated by sweeping the current channel amplitude and measuring the energy at the outputs (the energy calculations here are being realized off-chip). The error is measured using a gain of 1x, as it is commonly used in most CT-based applications.

At low signal amplitude values (typically 1000:1 dynamic range and higher), the crosstalk between channels, mainly caused by the PCB, becomes a significant part of the perturbation as the measurement error increases. The 1-point measurement error curves in Figure 2-5 have been performed with a full-scale sine wave on all the inputs that are not measured, which means that these channels induce a maximum amount of crosstalk on the measurement error curve. In order to avoid such behavior, a 2-point calibration can be put in place in the calculation section.

This 2-point calibration can be a simple linear interpolation between two calibration points (one at high amplitudes, one at low amplitudes at each end of the dynamic range) and helps to significantly lower the effect of crosstalk between channels. A 2-point calibration is very effective in maintaining the measurement error close to zero on the whole dynamic range, since the nonlinearity and distortion of the MCP3912 is very low. Figure 2-6 shows the measurement error curves obtained with the same ADC data taken for Figure 2-5, but where a 2-point calibration has been applied. The difference is significant only at the low end of the dynamic range, where all the perturbing factors are a bigger part of the ADC output signals. These curves show extremely tight measurement error across the full dynamic range (here, typically 10,000:1), which is required in high-accuracy class meters.

NOTES:

8.0 MCP3912 INTERNAL REGISTERS

The addresses associated with the internal registers are listed in Table 8-1. This section also describes the registers in detail. All registers are 24-bit long registers, which can be addressed and read separately.

The format of the data registers (0x00 to 0x03) can be changed with WIDTH_DATA<1:0> bits in the STATUSCOM register. The READ<1:0> and WRITE bits define the groups and types of registers for continuous read/write communication or looping on address sets, as shown in Table 8-2.

TABLE 8-1: MCP3912 REGISTER MAP

Address	Name	Bits	R/W	Description
0x00	CHANNEL0	24	R	Channel 0 ADC Data <23:0>, MSB first
0x01	CHANNEL1	24	R	Channel 1 ADC Data <23:0>, MSB first
0x02	CHANNEL2	24	R	Channel 2 ADC Data <23:0>, MSB first
0x03	CHANNEL3	24	R	Channel 3 ADC Data <23:0>, MSB first
0x04	Unused	24	U	Unused
0x05	Unused	24	U	Unused
0x06	Unused	24	U	Unused
0x07	Unused	24	U	Unused
0x08	MOD	24	R/W	Delta-Sigma Modulators Output Value
0x09	Unused	24	R/W	Unused
0x0A	PHASE	24	R/W	Phase Delay Configuration Register - Channel pairs 0/1 and 2/3
0x0B	GAIN	24	R/W	Gain Configuration Register
0x0C	STATUSCOM	24	R/W	Status and Communication Register
0x0D	CONFIG0	24	R/W	Configuration Register
0x0E	CONFIG1	24	R/W	Configuration Register
0x0F	OFFCAL_CH0	24	R/W	Offset Correction Register - Channel 0
0x10	GAINCAL_CH0	24	R/W	Gain Correction Register - Channel 0
0x11	OFFCAL_CH1	24	R/W	Offset Correction Register - Channel 1
0x12	GAINCAL_CH1	24	R/W	Gain Correction Register - Channel 1
0x13	OFFCAL_CH2	24	R/W	Offset Correction Register - Channel 2
0x14	GAINCAL_CH2	24	R/W	Gain Correction Register - Channel 2
0x15	OFFCAL_CH3	24	R/W	Offset Correction Register - Channel 3
0x16	GAINCAL_CH3	24	R/W	Gain Correction Register - Channel 3
0x17	Unused	24	U	Unused
0x18	Unused	24	U	Unused
0x19	Unused	24	U	Unused
0x1A	Unused	24	U	Unused
0x1B	Unused	24	U	Unused
0x1C	Unused	24	U	Unused
0x1D	Unused	24	U	Unused
0x1E	Unused	24	U	Unused
0x1F	LOCK/CRC	24	R/W	Security Register (Password and CRC-16 on Register Map)

TABLE 8-2: REGISTER MAP GROUPING FOR ALL CONTINUOUS READ/WRITE MODES

Function	Address	READ<1:0>				WRITE	
		= “11”	= “10”	= “01”	= “00”	= “1”	= “0”
CHANNEL 0	0x00	LOOP ENTIRE REGISTER MAP	TYPE	GROUP	Static	Not Writable (Address undefined for Write access)	Not Writable (Address undefined for Write access)
CHANNEL 1	0x01				Static		
CHANNEL 2	0x02			GROUP	Static		
CHANNEL 3	0x03				Static		
MOD	0x08		TYPE	GROUP	Static	LOOP ONLY ON WRITABLE REGISTERS	Static
PHASE	0x0A				Static		Static
GAIN	0x0B				Static		Static
STATUSCOM	0x0C			GROUP	Static		Static
CONFIG0	0x0D				Static		Static
CONFIG1	0x0E				Static		Static
OFFCAL_CH0	0x0F			GROUP	Static		Static
GAINCAL_CH0	0x10				Static		Static
OFFCAL_CH1	0x11			GROUP	Static		Static
GAINCAL_CH1	0x12				Static		Static
OFFCAL_CH2	0x13			GROUP	Static		Static
GAINCAL_CH2	0x14				Static		Static
OFFCAL_CH3	0x15			GROUP	Static		Static
GAINCAL_CH3	0x16				Static		Static
LOCK/CRC	0x1F			GROUP	Static		Static

8.1 CHANNEL Registers - ADC Channel Data Output Registers

Name	Bits	Address	Cof.
CHANNEL0	24	0x00	R
CHANNEL1	24	0x01	R
CHANNEL2	24	0x02	R
CHANNEL3	24	0x03	R

The ADC Channel Data Output registers always contain the most recent A/D conversion data for each channel. These registers are read-only. They can be accessed independently or linked together (with READ<1:0> bits). These registers are latched when an ADC read communication occurs. When a data ready event occurs during a read communication, the most current ADC data is also latched to avoid data corruption issues. These registers are updated and latched together if DR_LINK = 1 synchronously with the data ready pulse (toggling on the most lagging ADC channel data ready event).

REGISTER 8-1: MCP3912 CHANNEL REGISTERS

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DATA_CHn <23> (MSB)	DATA_CHn <22>	DATA_CHn <21>	DATA_CHn <20>	DATA_CHn <19>	DATA_CHn <18>	DATA_CHn <17>	DATA_CHn <16>
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DATA_CHn <15>	DATA_CHn <14>	DATA_CHn <13>	DATA_CHn <12>	DATA_CHn <11>	DATA_CHn <10>	DATA_CHn <9>	DATA_CHn <8>
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DATA_CHn <7>	DATA_CHn <6>	DATA_CHn <5>	DATA_CHn <4>	DATA_CHn <3>	DATA_CHn <2>	DATA_CHn <1>	DATA_CHn <0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-0 **DATA_CHn:** Output code from ADC Channel n. This data is post-calibration if the EN_OFFCAL or EN_GAINCAL bits are enabled. This data can be formatted in 16-/24-/32-bit modes, depending on the WIDTH_DATA<1:0> settings. (see **Section 5.5 “ADC Output Coding”**)

8.2 MOD Register – Modulators Output Register

Name	Bits	Address	Cof.
MOD	24	0x08	R/W

The MOD register contains the most recent modulator data output and is updated at a DMCLK rate. The default value corresponds to an equivalent input of 0V on all ADCs. Each bit in this register corresponds to one comparator output on one of the channels. Do not write to this register to ensure the accuracy of each ADC.

REGISTER 8-2: MOD REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1
COMP3_CH3	COMP2_CH3	COMP1_CH3	COMP0_CH3	COMP3_CH2	COMP2_CH2	COMP1_CH2	COMP0_CH2
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1
COMP3_CH1	COMP2_CH1	COMP1_CH1	COMP0_CH1	COMP3_CH0	COMP2_CH0	COMP1_CH0	COMP0_CH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented**: read as 0

bit 15-12 **COMPn_CH3**: Comparator Outputs from ADC Channel 3

bit 11-8 **COMPn_CH2**: Comparator Outputs from ADC Channel 2

bit 7-4 **COMPn_CH1**: Comparator Outputs from ADC Channel 1

bit 3-0 **COMPn_CH0**: Comparator Outputs from ADC Channel 0

8.3 PHASE Register – Phase Configuration Register for Channel Pairs 2/3 and 0/1

Name	Bits	Address	Cof.
PHASE	24	0x0A	R/W

Any write to this register automatically resets and restarts all active ADCs.

REGISTER 8-3: PHASE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEB<11>	PHASEB<10>	PHASEB<9>	PHASEB<8>	PHASEB<7>	PHASEB<6>	PHASEB<5>	PHASEB<4>
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEB<3>	PHASEB<2>	PHASEB<1>	PHASEB<0>	PHASEA<11>	PHASEA<10>	PHASEA<9>	PHASEA<8>
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEA<7>	PHASEA<6>	PHASEA<5>	PHASEA<4>	PHASEA<3>	PHASEA<2>	PHASEA<1>	PHASEA<0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-12	**PHASEB<11:0>** Phase delay between channels CH2 and CH3 (reference). Delay = PHASEB<11:0> decimal code/DMCLK
bit 11-0	**PHASEA<11:0>** Phase delay between channels CH0 and CH1(reference). Delay = PHASEA<11:0> decimal code/DMCLK

8.4 GAIN Register – PGA Gain Configuration Register

Name	Bits	Address	Cof.
GAIN	24	0x0B	R/W

REGISTER 8-4: GAIN REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	PGA_CH3<2>	PGA_CH3<1>	PGA_CH3<0>	PGA_CH2<2>
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PGA_CH2<1>	PGA_CH2<0>	PGA_CH1<2>	PGA_CH1<1>	PGA_CH1<0>	PGA_CH0<2>	PGA_CH0<1>	PGA_CH0<0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-12 **Unimplemented:** Read as 0

bit 11-0 **PGA_CHn<2:0>:** PGA Setting for Channel n
- `111` = Reserved (Gain = 1)
- `110` = Reserved (Gain = 1)
- `101` = Gain is 32
- `100` = Gain is 16
- `011` = Gain is 8
- `010` = Gain is 4
- `001` = Gain is 2
- `000` = Gain is 1 (DEFAULT)

8.5 STATUSCOM Register – Status and Communication Register

Name	Bits	Address	Cof.
STATUSCOM	24	0x0C	R/W

REGISTER 8-5: STATUSCOM REGISTER

R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1
READ<1>	READ<0>	WRITE	$\overline{\text{DR\_HIZ}}$	DR_LINK	WIDTH_ CRC	WIDTH_ DATA<1>	WIDTH_ DATA<0>
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
EN_CRCCOM	EN_INT	Reserved	Reserved	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-1	R-1	R-1	R-1
—	—	—	—	DRSTATUS<3>	DRSTATUS<2>	DRSTATUS<1>	DRSTATUS<0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-22 **READ<1:0>:** Address counter increment setting for Read Communication
- `11` = Address counter auto-increments, and loops on the entire register map
- `10` = Address counter auto-increments, and loops on register TYPES (DEFAULT)
- `01` = Address counter auto-increments, and loops on register GROUPS
- `00` = Address is not incremented, and continually reads the same single-register address

bit 21 **WRITE:** Address counter increment setting for Write Communication
- `1` = Address counter auto-increments and loops on writable part of the register map (DEFAULT)
- `0` = Address is not incremented, and continually writes to the same single register address

bit 20 **$\overline{\text{DR\_HIZ}}$:** Data Ready Pin Inactive State Control
- `1` = The $\overline{\text{DR}}$ pin state is a logic high when data is NOT ready
- `0` = The $\overline{\text{DR}}$ pin state is high-impedance when data is NOT ready (DEFAULT)

bit 19 **DR_LINK** Data Ready Link Control
- `1` = Data Ready link enabled. Only one pulse is generated on the $\overline{\text{DR}}$ pin for all ADC channels, corresponding to the data ready pulse of the most lagging ADC. (DEFAULT)
- `0` = Data Ready link disabled. Each ADC produces its own data ready pulse on the $\overline{\text{DR}}$ pin.

bit 18 **WIDTH_CRC** Format for CRC-16 on communications
- `1` = 32-bit (CRC-16 code is followed by zeros). This coding is compatible with CRC implementation in most 32-bit MCUs (including PIC32 MCUs).
- `0` = 16 bit (default)

bit 17-16 **WIDTH_DATA<1:0>:** ADC Data Format Settings for all ADCs (see **Section 5.5 “ADC Output Coding”**)
- `11` = 32-bit with sign extension
- `10` = 32-bit with zeros padding
- `01` = 24-bit (default)
- `00` = 16-bit (with rounding)

bit 15 **EN_CRCCOM:** Enable CRC CRC-16 Checksum on Serial communications
- `1` = CRC-16 Checksum is provided at the end of each communication sequence (therefore each communication is longer). The CRC-16 Message is the complete communication sequence (see section **Section 6.9 “Securing Read Communications Through CRC-16 Checksum”** for more details).
- `0` = Disabled **(Default)**

REGISTER 8-5: STATUSCOM REGISTER (CONTINUED)

bit 14	**EN_INT:** Enable for the CRCREG interrupt function 1 = The interrupt flag for the CRCREG checksum verification is enabled. The Data Ready pin ($\overline{DR}$) will become logic low and stays logic low if a CRCREG checksum error happens. This interrupt is cleared if the LOCK<7:0> value is made equal to the PASSWORD value (0xA5). 0 = The interrupt flag for the CRCREG checksum verification is disabled. The CRCREG<15:0> bits are still calculated properly and can still be read in this mode. No interrupt is generated even when a CRCREG checksum error happens. (Default)
bit 13-12	**Reserved:** Should be kept equal to 0 at all times
bit 11-4	**Unimplemented:** Read as 0
bit 3-0	**DRSTATUS<3:0>:** Data ready status bit for each individual ADC channel DRSTATUS<n> = 1 - Channel CHn data is not ready (DEFAULT) DRSTATUS<n> = 0 - Channel CHn data is ready. The status bit is set back to '1' after reading the STATUSCOM register. The status bit is not set back to '1' by the read of the corresponding channel ADC data.

8.6 CONFIG0 Register – Configuration Register 0

Name	Bits	Address	Cof.
CONFIG0	24	0x0D	R/W

REGISTER 8-6: CONFIG0 REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
EN_OFFCAL	EN_GAINCAL	DITHER<1>	DITHER<0>	BOOST<1>	BOOST<0>	PRE<1>	PRE<0>
bit 23							bit 16

R/W-0	R/W-1	R/W-1	U-0	U-0	U-0	U-0	U-0
OSR<2>	OSR<1>	OSR<0>	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
VREFCAL<7>	VREFCAL<6>	VREFCAL<5>	VREFCAL<4>	VREFCAL<3>	VREFCAL<2>	VREFCAL<1>	VREFCAL<0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23 **EN_OFFCAL:** Enables the 24-bit digital offset error calibration on all channels
1 = Enabled. This mode does not add any group delay to the ADC data.
0 = Disabled (DEFAULT)

bit 22 **EN_GAINCAL:** Enables or disables the 24-bit digital gain error calibration on all channels
1 = Enabled. This mode adds a group delay on all channels of 24 DMCLK periods. All data ready pulses are delayed by 24 DMCLK clock periods, compared to the mode with EN_GAINCAL = 0.
0 = Disabled (DEFAULT)

bit 21-20 **DITHER<1:0>:** Control for dithering circuit for idle tone’s cancellation and improved THD on all channels
11 = Dithering ON, Strength = Maximum (DEFAULT)
10 = Dithering ON, Strength = Medium
01 = Dithering ON, Strength = Minimum
00 = Dithering turned OFF

bit 19-18 **BOOST<1:0>:** Bias Current Selection for all ADCs (impacts achievable maximum sampling speed, see Table 5-2)
11 = All channels have current x 2
10 = All channels have current x 1 (Default)
01 = All channels have current x 0.66
00 = All channels have current x 0.5

bit 17-16 **PRE<1:0>** Analog Master Clock (AMCLK) Prescaler Value
11 = AMCLK = MCLK/8
10 = AMCLK = MCLK/4
01 = AMCLK = MCLK/2
00 = AMCLK = MCLK (Default)

REGISTER 8-6: CONFIG0 REGISTER (CONTINUED)

bit 15-13	**OSR<2:0>** Oversampling Ratio for delta sigma A/D Conversion (ALL CHANNELS, f_d / f_S) `111` = 4096 (f_d = 244 sps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz) `110` = 2048 (f_d = 488 sps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz) `101` = 1024 (f_d = 976 sps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz) `100` = 512 (f_d = 1.953 ksps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz) `011` = 256 (f_d = 3.90625 ksps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz) (Default) `010` = 128 (f_d = 7.8125 ksps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz) `001` = 64 (f_d = 15.625 ksps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz) `000` = 32 (f_d = 31.25 ksps for MCLK = 4 MHz, f_s = AMCLK = 1 MHz)
bit 12-8	**Unimplemented:** Read as 0
bit 7-0	**VREFCAL<7:0>:** Internal Voltage Temperature coefficient VREFCAL<7:0> value. (See **Section 5.6.3 "Temperature compensation (VREFCAL<7:0>)"** for complete description).

8.7 CONFIG1 Register – Configuration Register 1

Name	Bits	Address	Cof.
CONFIG1	24	0x0E	R/W

REGISTER 8-7: CONFIG1 REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	RESET<3>	RESET<2>	RESET<1>	RESET<0>
bit 23							bit 16

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	SHUTDOWN<3>	SHUTDOWN<2>	SHUTDOWN<1>	SHUTDOWN<0>
bit 15							bit 8

R/W-0	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0
VREFEXT	CLKEXT	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-20 **Unimplemented:** Read as 0

bit 19-16 **RESET<3:0>:** Soft Reset mode setting for each individual ADC
RESET<n> = `1`: Channel CHn in soft reset mode
RESET<n> = `0`: Channel CHn not in soft reset mode

bit 15-12 **Unimplemented:** Read as 0

bit 11-8 **SHUTDOWN<3:0>:** Shutdown Mode setting for each individual ADC
SHUTDOWN<n> = `1`: ADC Channel CHn in Shutdown
SHUTDOWN<n> = `0`: ADC Channel CHn not in Shutdown

bit 7 **VREFEXT:** Internal Voltage Reference selection bit
`1` = Internal Voltage Reference Disabled. An external reference voltage needs to be applied across the REFIN+/- pins. The analog power consumption (AI_{DD}) is slightly diminished in this mode since the internal voltage reference is placed into Shutdown mode.
`0` = Internal Reference enabled. For optimal accuracy, the REFIN+/OUT pin needs proper decoupling capacitors. REFIN- pin should be connected to A_{GND}, when in this mode.

bit 6 **CLKEXT:** Internal Clock selection bit
`1` = MCLK is generated externally and should be provided on the OSC1 pin. The crystal oscillator is disabled and consumes no current (Default)
`0` = Crystal oscillator enabled. A crystal must be placed between OSC1 and OSC2 with proper decoupling capacitors. The digital power consumption (DI_{DD}) is increased in this mode due to the oscillator.

bit 5-0 **Unimplemented:** Read as 0

8.8 OFFCAL_CHn and GAINCAL_CHn Registers – Digital Offset and Gain Error Calibration Registers

Name	Bits	Address	Cof.
OFFCAL_CH0	24	0x0F	R/W
GAINCAL_CH0	24	0x10	R/W
OFFCAL_CH1	24	0x11	R/W
GAINCAL_CH1	24	0x12	R/W
OFFCAL_CH2	24	0x13	R/W
GAINCAL_CH2	24	0x14	R/W
OFFCAL_CH3	24	0x15	R/W
GAINCAL_CH3	24	0x16	R/W

REGISTER 8-8: OFFCAL_CHN REGISTERS

R/W-0	
OFFCAL_CHn<23:0>	
bit 23	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-0 **OFFCAL_CHn:** Digital Offset calibration value for the corresponding channel CHn. This register is simply added to the output code of the channel bit-by-bit. This register is 24-bit two's complement MSB first coding. CHn Output Code = OFFCAL_CHn + ADC CHn Output Code. This register is a Don't Care if EN_OFFCAL = 0 (Offset calibration disabled), but its value is not cleared by the EN_OFFCAL bit.

REGISTER 8-9: GAINCAL_CHN REGISTERS

R/W-0	
GAINCAL_CHn<23:0>	
bit 23	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-0 **GAINCAL_CHn:** Digital gain error calibration value for the corresponding channel CHn. This register is 24-bit signed MSB first coding with a range of -1x to +0.9999999x (from 0x800000 to 0x7FFFFF). The gain calibration adds 1x to this register and multiplies it to the output code of the channel bit-by-bit, after offset calibration. The range of the gain calibration is thus from 0x to 1.9999999x (from 0x800000 to 0x7FFFFF). The LSB corresponds to a 2^{-23} increment in the multiplier. CHn Output Code = (GAINCAL_CHn+1)*ADC CHn Output Code. This register is a Don't Care if EN_GAINCAL = 0 (Gain calibration disabled) but its value is not cleared by the EN_GAINCAL bit.

8.9 SECURITY Register – Password and CRC-16 On Register Map

Name	Bits	Address	Cof.
LOCK/CRC	24	0x1F	R/W

REGISTER 8-10: LOCK/CRC REGISTER

R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
LOCK<7>	LOCK<6>	LOCK<5>	LOCK<4>	LOCK<3>	LOCK<2>	LOCK<1>	LOCK<0>
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CRCREG<15>	CRCREG<14>	CRCREG<13>	CRCREG<12>	CRCREG<11>	CRCREG<10>	CRCREG<9>	CRCREG<8>
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CRCREG<7>	CRCREG<6>	CRCREG<5>	CRCREG<4>	CRCREG<3>	CRCREG<2>	CRCREG<1>	CRCREG<0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-16 **LOCK<7:0>:** Lock Code for the writable part of the register map

LOCK<7:0> = PASSWORD =0xA5 (Default value): The entire register map is writable. The CRCREG<15:0> bits and the CRC Interrupt are cleared. No CRC-16 checksum on register map is calculated.

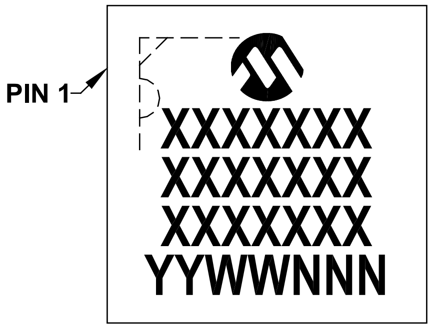
LOCK<7:0> are different than 0xA5: The only writable register is the LOCK/CRC register. All other registers will appear as undefined while in this mode. The CRCREG checksum is calculated continuously and can generate interrupts if the CRC Interrupt EN_INT bit has been enabled. If a write to a register needs to be performed, the user needs to unlock the register map beforehand by writing 0xA5 to the LOCK<7:0> bits.

bit 15-0 **CRCREG<15:0>:** CRC-16 Checksum that is calculated with the writable part of the register map as a message. This is a read-only 16-bit code. This checksum is continuously recalculated and updated every 16 DMCLK periods. It is reset to its default value (0x0000) when LOCK<7:0> = 0xA5.

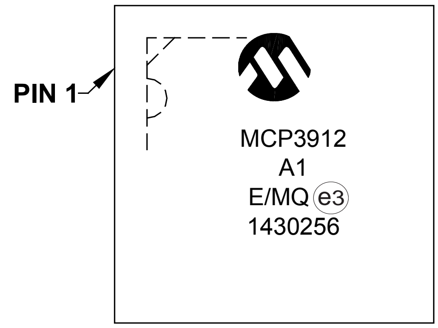
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

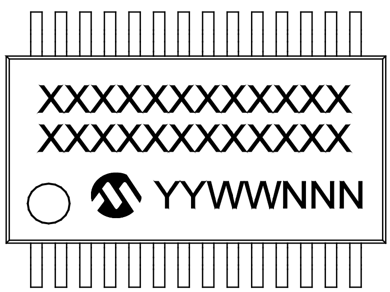
28-Lead QFN (5x5x0.9 mm)



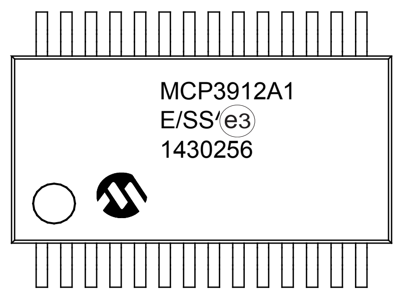
Example



28-Lead SSOP (5.30 mm)



Example

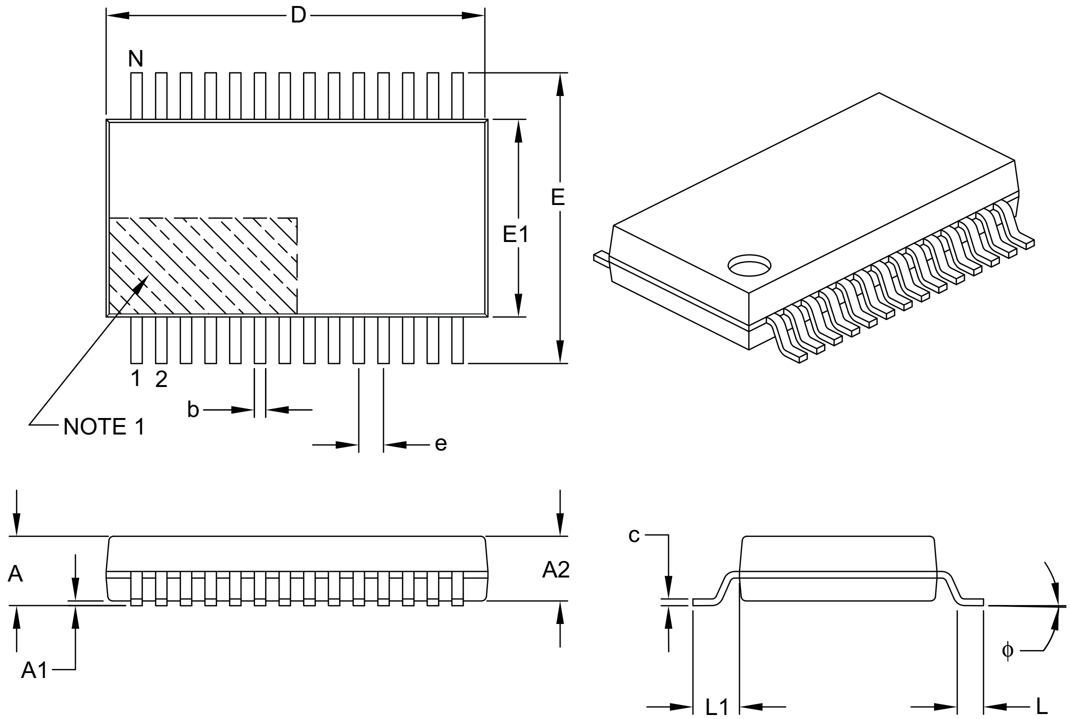


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

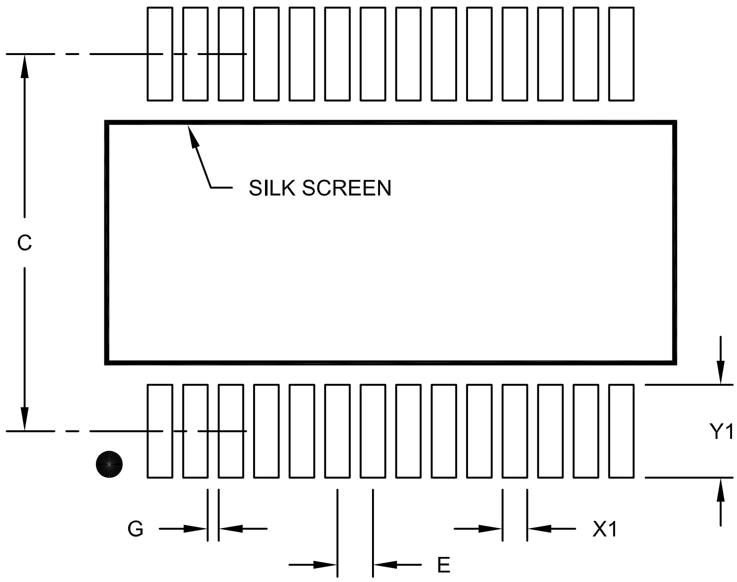
Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

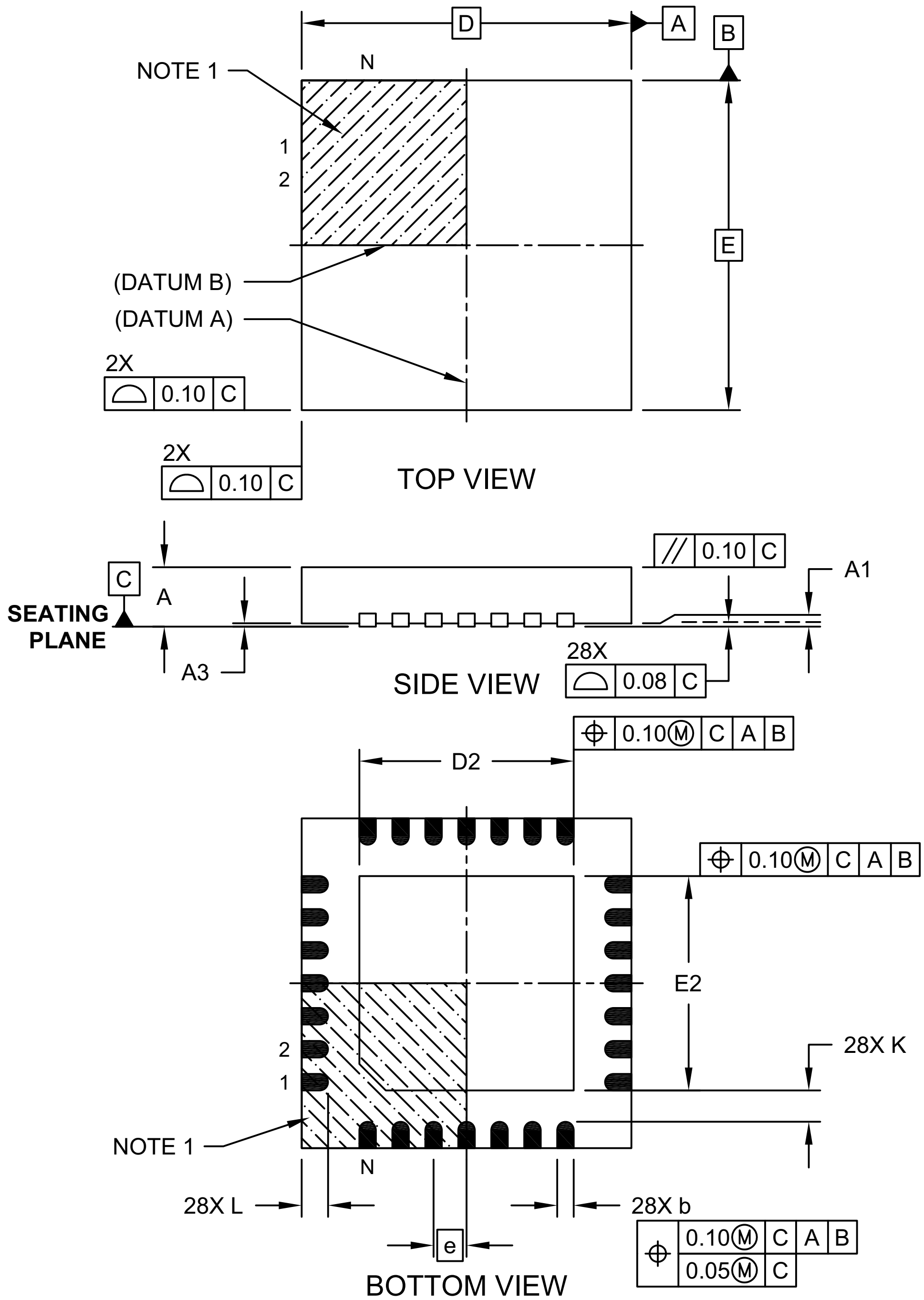
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN or VQFN]

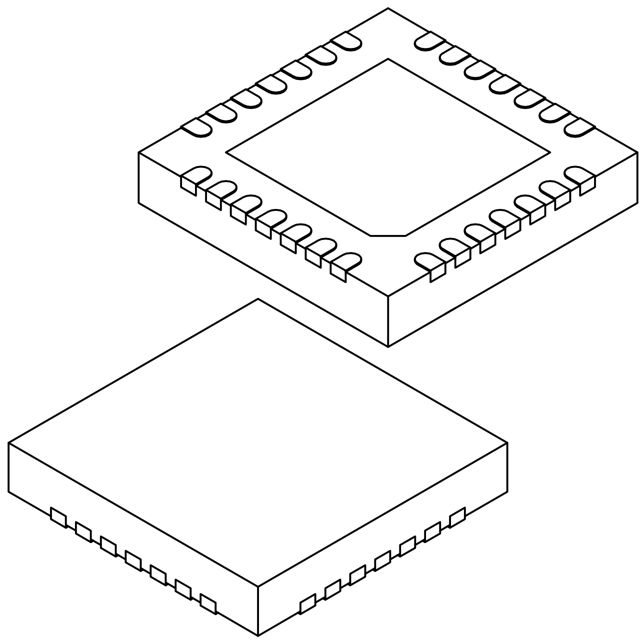
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-140C Sheet 1 of 2

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN or VQFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.15	3.25	3.35
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.15	3.25	3.35
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.35	0.40	0.45
Contact-to-Exposed Pad	K	0.20	-	-

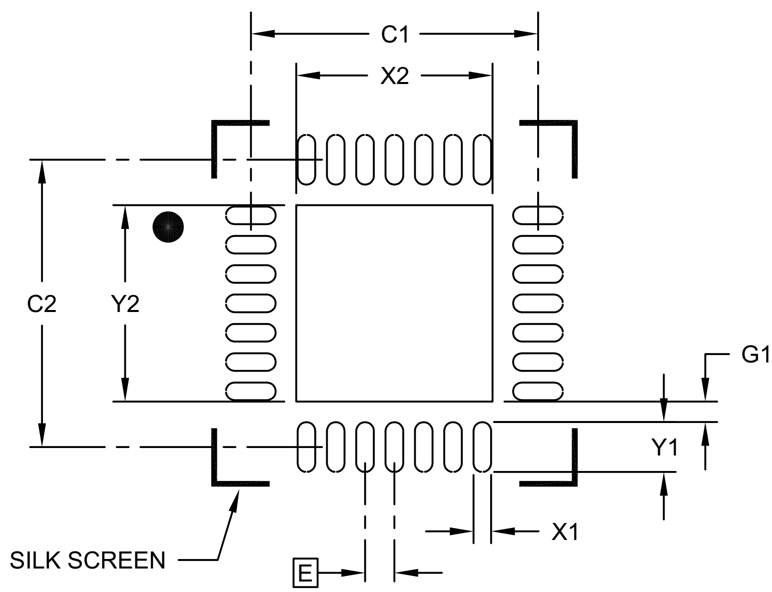
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-140C Sheet 2 of 2

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN or VQFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			3.35
Optional Center Pad Length	T2			3.35
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			0.85
Contact Pad Length (X28)	G1	0.35		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2140A

APPENDIX A: REVISION HISTORY

Revision A (September 2014)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	[X][(1)]	X	/XX
Device	Address Option	Tape and Reel	Temperature Range	Package

Device: MCP3912: Four-Channel Analog Front-End Converter

Address Options:

XX		A6	A5
A0	=	0	0
A1*	=	0	1
A2	=	1	0
A3	=	1	1

* Default option. Contact Microchip factory for other address options.

Tape and Reel Option:
- Blank = Standard packaging (tube or tray)
- T = Tape and Reel[(1)]

Temperature Range: E = -40°C to +125°C

Package:
- MQ = Plastic Quad Flat, No Lead package (QFN)
- SS = Plastic Shrink Small Outline, 5.30 mm body (SSOP)

Examples:

a) MCP3912A1-E/SS: Address Option A1, Extended Temperature, 28LD SSOP package

b) MCP3912A1T-E/SS: Address Option A1, Tape and Reel, Extended Temperature, 28LD SSOP package

c) MCP3912A1-E/MQ: Address Option A1, Extended Temperature, 28LD QFN package

d) MCP3912A1T-E/MQ: Address Option A1, Tape and Reel, Extended Temperature, 28LD QFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip sales office for package availability for the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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Korea - Seoul
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